MP2388

1A, 21V, 2MHz, High-Efficiency, Synchronous, Step-Down Converter in Ultra-Thin QFN Package

The Future of Analog IC Technology

DESCRIPTION

The MP2388 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in, internal power MOSFETs. It offers a very compact solution that achieves 1A of continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MP2388 requires a minimum number of readily available, standard, external components and is available in a space-saving QFN-8 (1.5mmx2.5mm) package.

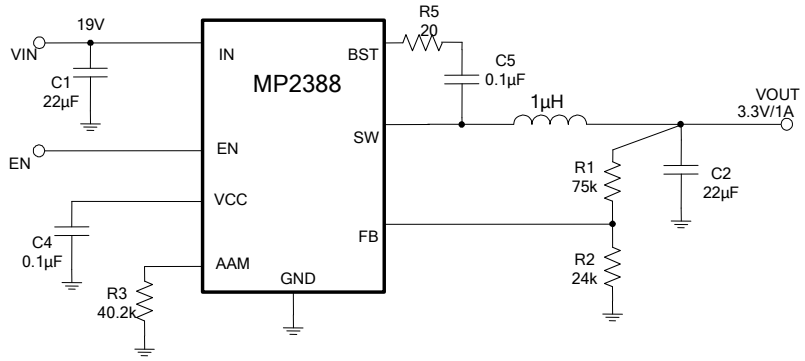
FEATURES

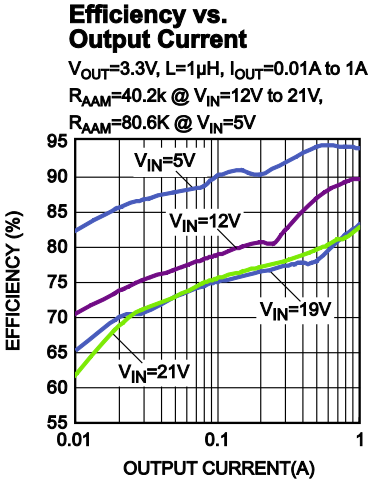
- Wide 4.5V to 21V Operating Input Range
- 1A Load Current
- 110mΩ/50mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Low Quiescent Current
- High-Efficiency Synchronous Mode Operation
- Fixed 2MHz Switching Frequency
- AAM Power Save Mode
- Internal Soft Start
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a QFN-8 (1.5mmx2.5mm) Package

APPLICATIONS

- Notebook Systems and I/O Power
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2388GQEU	QFN-8 (1.5mmx2.5mm)	*See Below*

For Tape & Reel, add suffix –Z (e.g. MP2388GQEU-Z)

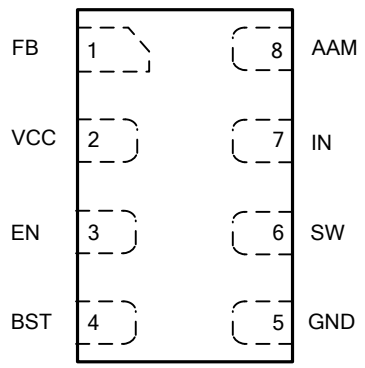
TOP MARKING

$\overline{\text{EL}}$
YW
LL

EL: Product code of MP2388GQEU
Y: Year code
W: Week code
LL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-8 (1.5mmx2.5mm)

ABSOLUTE MAXIMUM RATINGS(1)

V_{IN} ..... -0.3V to +28V
V_{SW} .... -0.3V (-5V < 10ns) to +28V (30V < 10ns)
V_{BST} ..... V_{SW} + 6V
All other pins(2) ..... -0.3V to +6V
Continuous power dissipation (T_A = +25°C)(3) 1.25W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions(4)

Supply voltage (V_{IN}) ..... 4.5 to 21V
Output voltage (V_{OUT}) ..... 0.8V to V_{IN}*D_{MAX}
Operating junction temp (T_J). ... -40°C to +125°C

Thermal Resistance(5) θ_{JA} θ_{JC}

QFN-8 (1.5mmx2.5mm).....	100…..	20..... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) For details of EN's ABS MAX rating, please refer to the EN control section on page 11.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			1	μA
Supply current (quiescent)	I_q	V_{EN} = 2V, V_{FB} = 1V, AAM = 0.5V		0.2		mA
		V_{EN} = 2V, V_{FB} = 1V, AAM = 5V		0.7		
HS switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 5V		110		mΩ
LS switch on resistance	LS_{RDS-ON}	V_{CC} = 5V		50		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V			1	μA
Current limit	I_{LIMIT}	Duty cycle = 40%	2.4	3		A
Oscillator frequency	f_{SW}	V_{FB} = 750mV	1700	2000	2400	kHz
Foldback frequency	f_{FB}	V_{FB} < 400mV		0.3		f_{SW}
Maximum duty cycle	D_{MAX}	V_{FB} = 700mV	78	83		%
Minimum on time (6)	T_{ON_MIN}			35		ns
Feedback voltage	V_{FB}	T_A = 25°C	786	798	810	mV
Feedback current	I_{FB}	V_{FB} = 820mV		10	50	nA
EN rising threshold	V_{EN_RISING}		1.2	1.4	1.6	V
EN hysteresis	V_{EN_HYS}		80	150	220	mV
EN input current	I_{EN}	V_{EN} = 2V		2		μA
		V_{EN} = 0		0		nA
VIN under-voltage lockout threshold rising	$INUV_{Vth}$		3.7	3.9	4.1	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			620		mV
VCC regulator	V_{CC}			4.9		V
VCC load regulation		I_{CC} = 5mA		1.5		%
Soft-start period	T_{SS}	V_{OUT} from 10% to 90%	0.8	1.5	2.2	ms
Thermal shutdown(6)				150		°C
Thermal hysteresis(6)				20		°C
AAM source current	I_{AAM}		5.6	6.2	6.8	μA

NOTE:

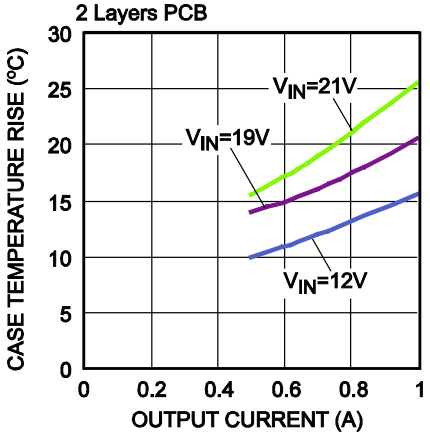
6) Guaranteed by design

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 19V, V_{OUT} = 3.3V, L = 1µH, T_A = 25°C, unless otherwise noted.

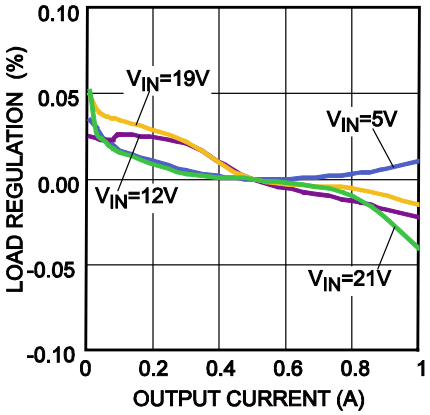
Case Temperature Rise vs. Output Current

V_{OUT}=3.3V, I_{OUT}=0.5A to 1A, 2 Layers PCB



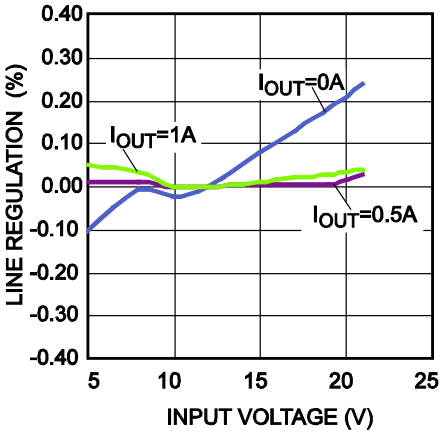
Load Regulation

V_{IN}=5V to 21V, I_{OUT}=0.1A to 1A

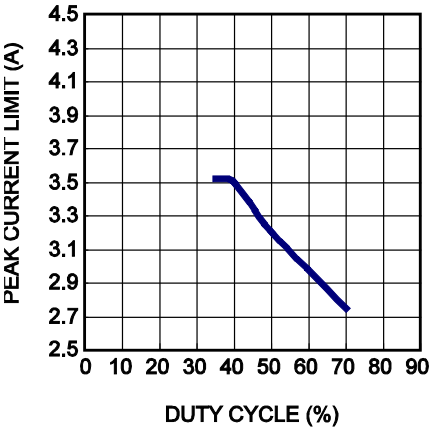


Line Regulation

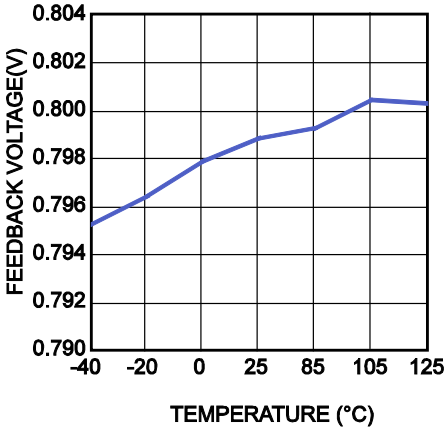
V_{IN}=5V to 21V, I_{OUT}=0A to 1A



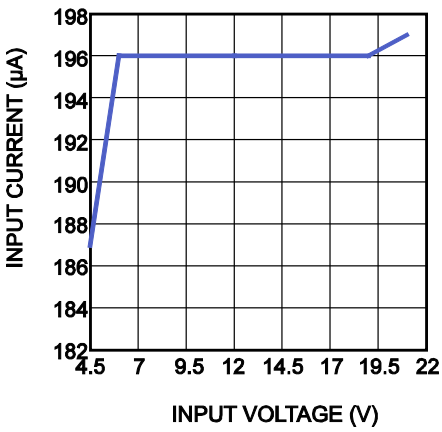
Peak Current Limit vs. Duty Cycle



Feedback Voltage vs. Temperature



Enabled Supply Current vs. Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

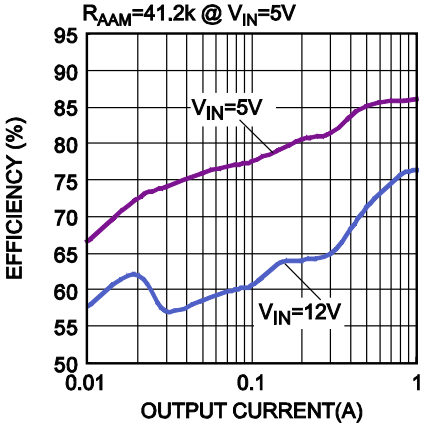
V_{IN} = 19V, V_{OUT} = 3.3V, L = 1µH, T_A = 25°C, unless otherwise noted.

Efficiency vs. Output Current

V_{OUT}=1.2V, L=0.68µH, I_{OUT}=0.01A to 1A

R_{AAM}=19.1k @ V_{IN}=12V,

R_{AAM}=41.2k @ V_{IN}=5V

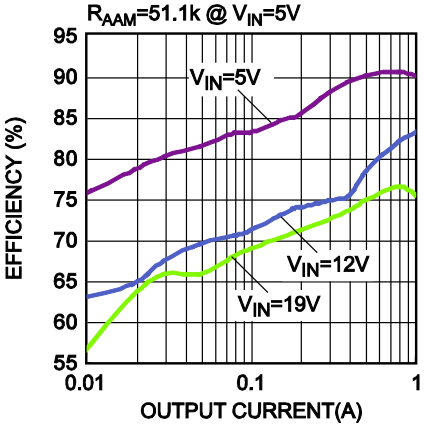


Efficiency vs. Output Current

V_{OUT}=1.8V, L=0.82µH, I_{OUT}=0.01A to 1A

R_{AAM}=32.4k @ Vin=12V to 19V

R_{AAM}=51.1k @ V_{IN}=5V

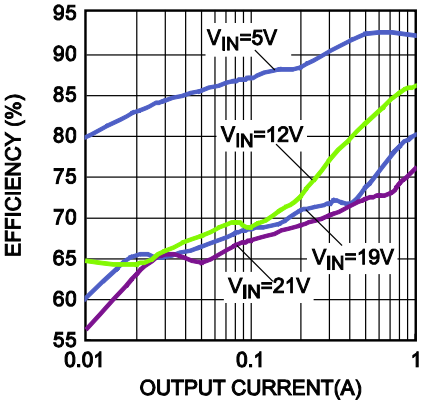


Efficiency vs. Output Current

V_{OUT}=2.5V, L=0.82µH, I_{OUT}=0.01A to 1A

R_{AAM}=28.7k @ V_{IN}=12V to 21V,

R_{AAM}=63.4k @ V_{IN}=5V

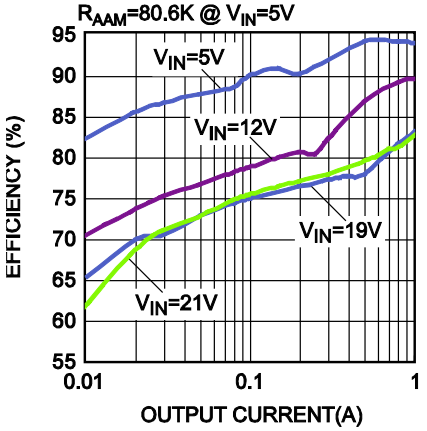


Efficiency vs. Output Current

V_{OUT}=3.3V, L=1µH, I_{OUT}=0.01A to 1A

R_{AAM}=40.2k @ V_{IN}=12V to 21V,

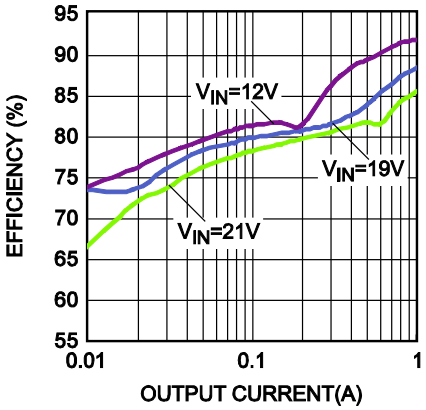
R_{AAM}=80.6K @ V_{IN}=5V



Efficiency vs. Output Current

V_{OUT}=5V, L=1.5µH, I_{OUT}=0.01A to 1A

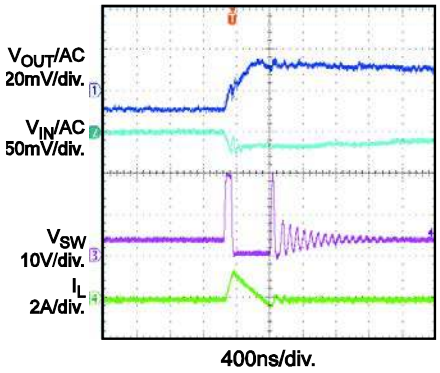
R_{AAM}=54.9k @ V_{IN}=12V to 21V



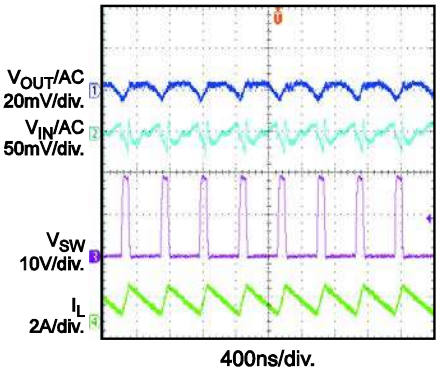
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 1µH, T_A = 25°C, unless otherwise noted.

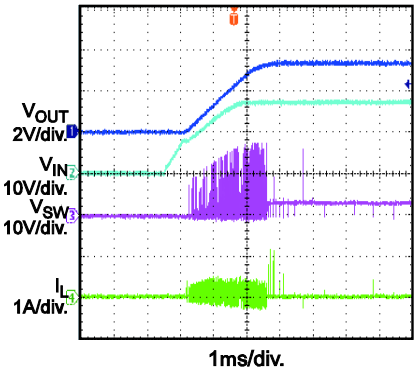
Input/Output Ripple
I_{OUT} = 0A



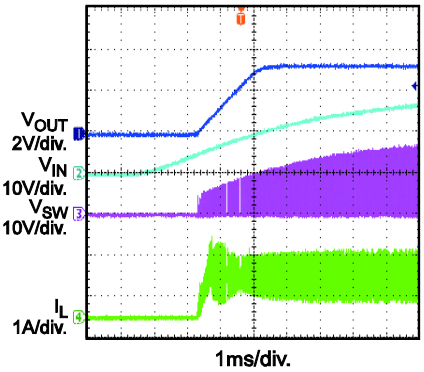
Input/Output Ripple
I_{OUT} = 1A



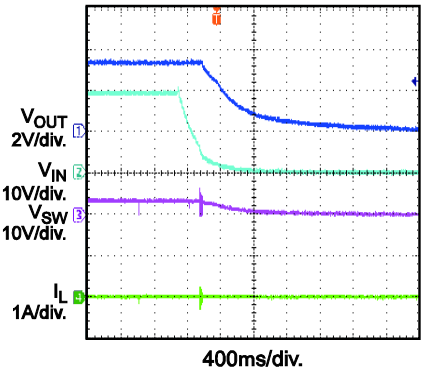
Start-Up through Input Voltage
I_{OUT} = 0A



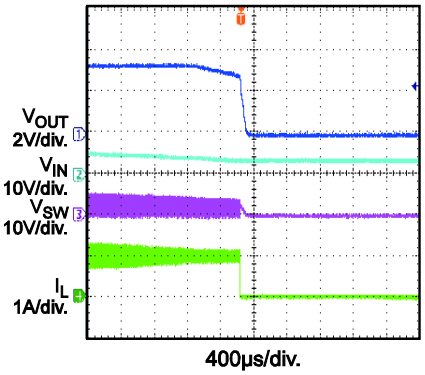
Start-Up through Input Voltage
I_{OUT} = 1A



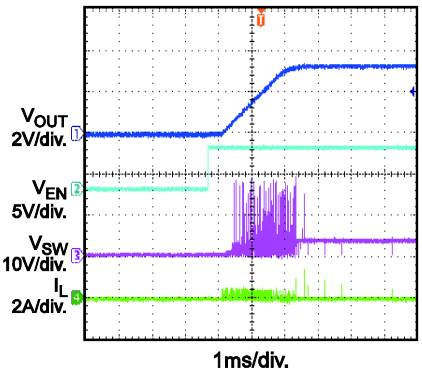
Shutdown through Input Voltage
I_{OUT} = 0A



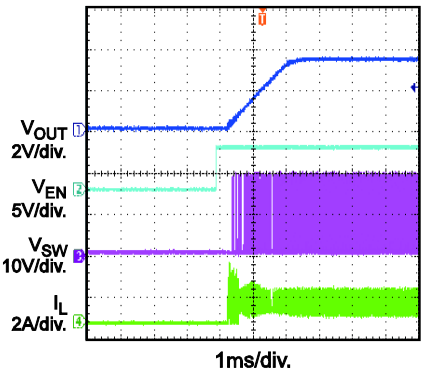
Shutdown through Input Voltage
I_{OUT} = 1A



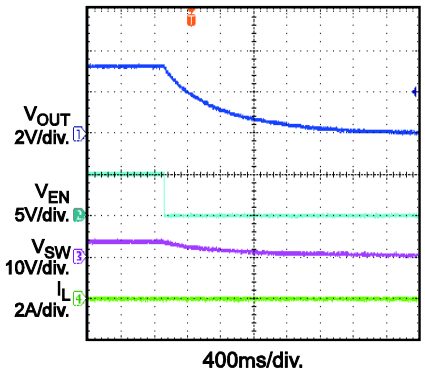
Start-Up through Enable
I_{OUT} = 0A



Start-Up through Enable
I_{OUT} = 1A



Shutdown through Enable
I_{OUT} = 0A

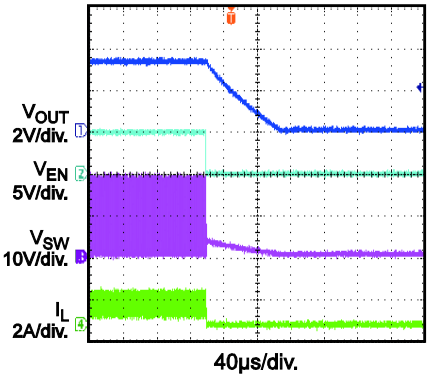


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 19V, V_{OUT} = 3.3V, L = 1µH, T_A = 25°C, unless otherwise noted.

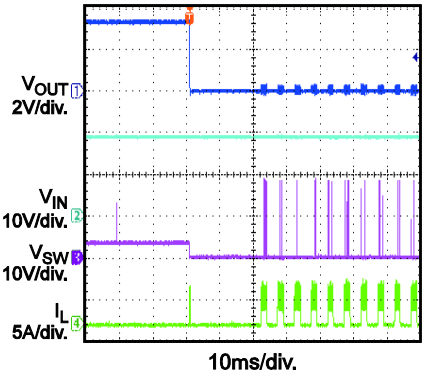
Shutdown through Enable

I_{OUT} = 1A



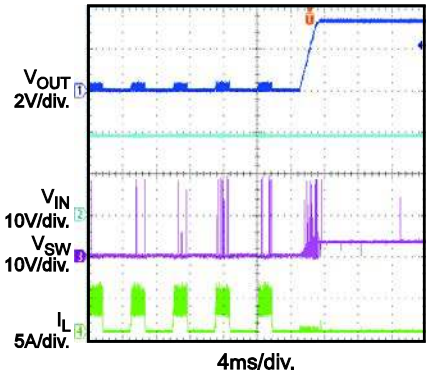
Short-Circuit Entry

I_{OUT} = 0A



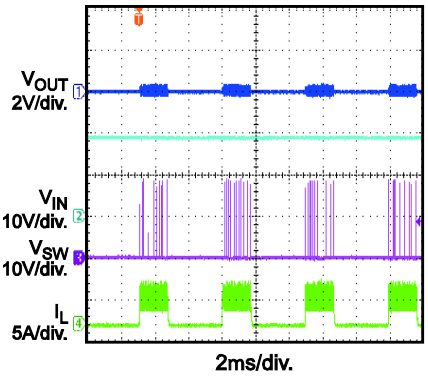
Short-Circuit Recovery

I_{OUT} = 0A



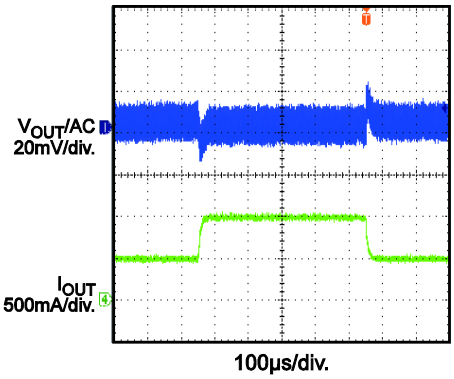
Short-Circuit Steady

I_{OUT} = 0A



Load Transient

I_{OUT} = 0.5A to 1A, 2.5A/µs



PIN FUNCTIONS

Package Pin #	Name	Description
1	FB	**Feedback.** An external resistor divider from the output to GND tapped to FB sets the output voltage. To prevent current limit runaway during a short-circuit fault condition, the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400mV.
2	VCC	**Bias supply.** Decouple VCC with a 0.1μF - 0.22μF capacitor. The capacitance should be no more than 0.22μF.
3	EN	**Enable.** Set EN to 1 to enable the MP2388.
4	BST	**Bootstrap.** A capacitor and a 20Ω resistor connected between SW and BST are required to form a floating supply across the high-side switch driver.
5	GND	**System ground.** GND is the reference ground of the regulated output voltage and requires careful consideration during PCB layout. Connect GND with coppers and vias.
6	SW	**Switch output.** Use wide PCB traces to make the connection.
7	IN	**Supply voltage.** The MP2388 operates on a 4.5V-to-21V input rail. C1 is needed to decouple the input rail. Use wide PCB traces to make the connection.
8	AAM	**Advanced asynchronous modulation.** A resistor connected from AAM to ground sets an AAM voltage to force the MP2388 into non-synchronous mode when the load is small. Drive AAM high when connected to VCC or float AAM to force the MP2388 into continuous conduction mode (CCM).

BLOCK DIAGRAM

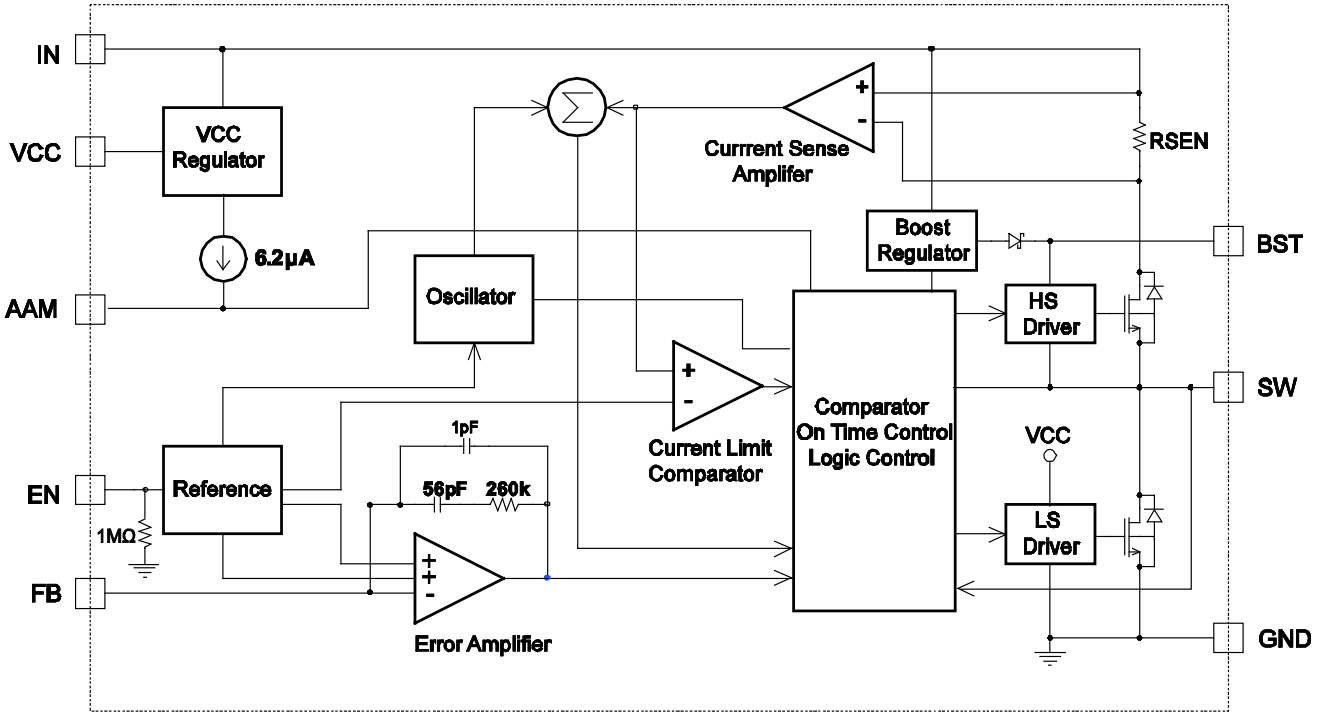


Figure 1: Functional Block Diagram

OPERATION

The MP2388 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in, internal power MOSFETs. It offers a very compact solution that achieves 1A of continuous output current over a wide input supply range with excellent load and line regulation.

The MP2388 operates with fixed-frequency, peak-current-control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET (HS-FET) is turned on and remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle starts. If the current in the power MOSFET does not reach the COMP-set current value within 83% of one PWM period, the power MOSFET is forced off.

Internal Regulator

Most of the internal circuitries are powered by the 5V internal regulator. After EN pulls high, this regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} is greater than 5.0V, the output of the regulator is in full regulation. When V_{IN} is lower than 5.0V, the output decreases. A 0.1µF ceramic capacitor is required for decoupling.

Error Amplifier (EA)

The error amplifier compares the FB voltage with the internal 0.798V reference (REF) and outputs a COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

AAM Operation

The MP2388 uses advanced asynchronous modulation (AAM) power-save mode for light-load conditions (see Figure 2). Connect a resistor from AAM to GND to set the AAM voltage (V_{AAM}). Under heavy-load conditions, V_{COMP} is higher than V_{AAM}. When the clock goes low, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}. The internal clock resets whenever V_{COMP} is higher than V_{AAM}.

Under light-load conditions, the value of V_{COMP} is low. When V_{COMP} is less than V_{AAM} and V_{FB} is less than V_{REF}, V_{COMP} ramps up until it exceeds V_{AAM}. During this time, the internal clock is blocked, so the MP2388 skips some pulses for pulse frequency modulation (PFM) mode and achieves light-load power save.

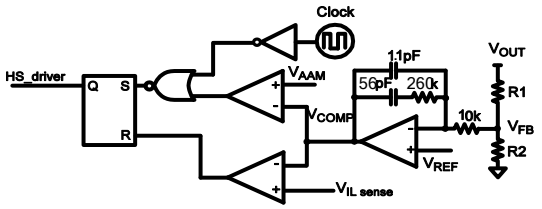


Figure 2: Simplified AAM Control Logic

Enable (EN) Control

Enable (EN) is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. There is an internal 1MΩ resistor from EN to GND, so EN can be floated to shut down the chip. The EN voltage is clamped at around 6.5V by an internal Zener diode. Connect a pull-up resistor between V_{IN} and EN that is large enough to limit the EN input current below 100µA. Typically, a resistor around 100k is sufficient for all applications.

For example, with 12V connected to V_{IN}, $R_{PULLUP} \geq (12V - 6.5V) \div 100\mu A = 55k\Omega$.

Connecting EN to a voltage source directly without a pull-up resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode (see Figure 3).

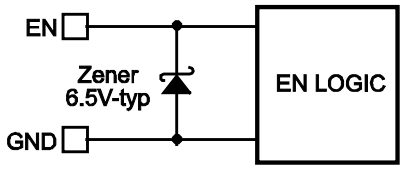


Figure 3: 6.5V Zener Diode Connection

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating with an insufficient supply voltage. The MP2388 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 3.9V, while its falling threshold is a consistent 3.25V.

Internal Soft Start (SS)

A soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage that ramps up from 0V. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage (0.798V). At this point, the reference voltage takes over. The soft-start time is internally set to around 1.5ms.

Over-Current Protection (OCP) and Hiccup

The MP2388 uses a cycle-by-cycle over-current limit when the inductor current peak value exceeds the set current-limit threshold. Meanwhile, the output voltage drops until FB is below the under-voltage (UV) threshold, typically 50% below the reference. Once UV is triggered, the MP2388 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the regulator. The MP2388 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, the entire chip shuts down. When the temperature is below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. The UVLO rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, R5, C5, L1, and C2 (see Figure 4). If V_{IN} - V_{SW} is more than 5V, U1 regulates M1 to maintain a 5V BST voltage across C5.

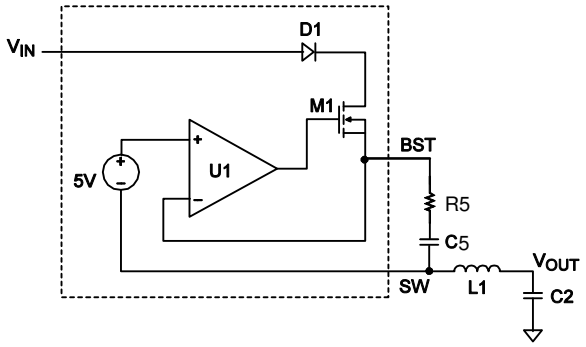


Figure 4: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to prevent any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see the Typical Application on page 1). R2 can then be calculated with Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.798V} - 1} \quad (1)$$

The feedback network is shown in Figure 5.

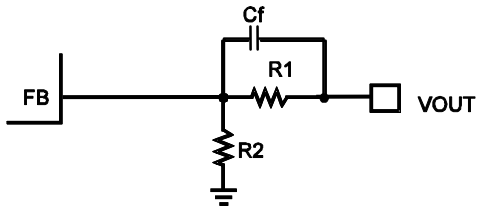


Figure 5: Feedback Network

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.05	191	604
1.2	191	383
1.8	102	82
2.5	102	47.5
3.3	75	24
5	100	19.1

Selecting the Inductor

A 0.47µH-to-4.7µH inductor with a DC current rating at least 25% percent higher than the maximum load current is recommended for most applications. For the highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Under light-load conditions below 100mA, a larger inductance is recommended for improved efficiency.

Setting the AAM Voltage

The AAM voltage is used to set the transition point from AAM to PWM. It should be chosen to provide the best combination of efficiency, stability, ripple, and transient.

If the AAM voltage is set lower, then stability and ripple improve, but efficiency during AAM mode and transient degrade. Likewise, if the AAM voltage is set higher, then the efficiency during AAM and transient improve, but stability and ripple degrade.

Adjust the AAM threshold by connecting a resistor from AAM to ground (see Figure 6). An internal 6.2µA current source charges the external resistor.

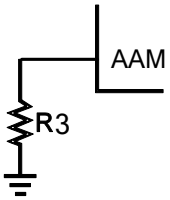


Figure 6: AAM Network

Generally, R3 is can be calculated with Equation (4):

$$V_{AAM} = R3 \times 6.2\mu A \quad (4)$$

The optimized AAM is shown in Figure 7.

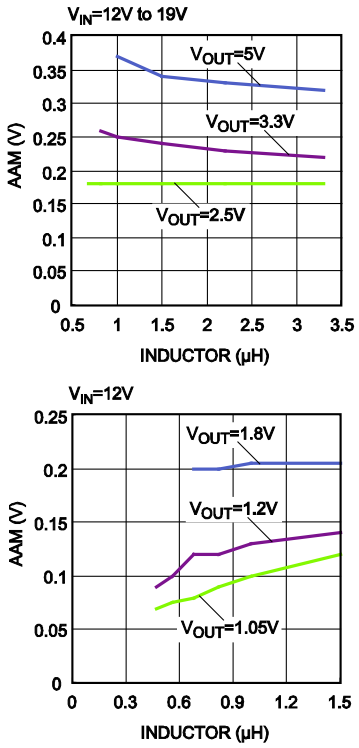


Figure 7: AAM Selection for Common Output Voltages

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (i.e.: 0.1µF) should be placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (8)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2388 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator. The applicable conditions of the external BST diode are:

- V_{OUT} is 5V or 3.3V
- Duty cycle is high: $D=\frac{V_{OUT}}{V_{IN}} > 65\%$

In these cases, an external BST diode is recommended from VCC to BST (see Figure 8).

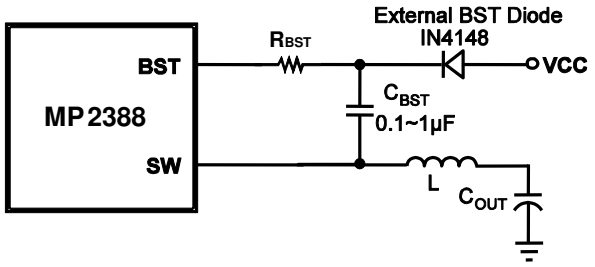


Figure 8: Optional External Bootstrap Diode Added to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST cap is 0.1 - 1μF.

PCB Layout Guidelines[7]

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 9 and follow the guidelines below.

1. Keep the connection of the input ground and GND as short and wide as possible.
2. Keep the connection of the input capacitor and IN as short and wide as possible.
3. Ensure that all feedback connections are short and direct.
4. Place the feedback resistors and compensation components as close to the chip as possible.
5. Route SW away from sensitive analog areas, such as FB.

NOTE:

7) The recommended layout is based on the Typical Application Circuit on page 16.

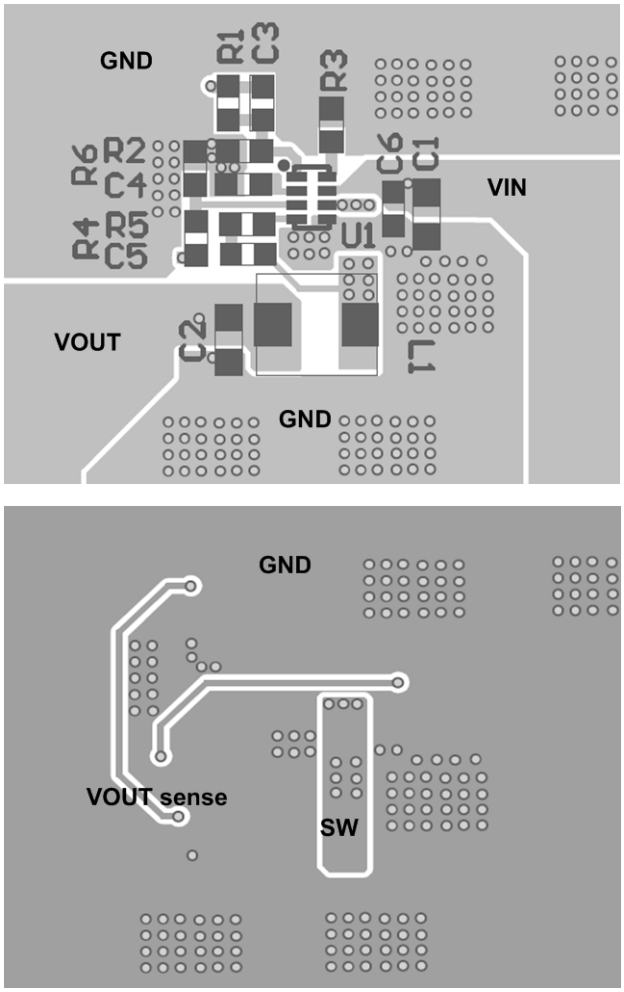


Figure 9: Sample Board Layout

Design Example

Table 2 is a design example following the application guidelines for the specifications below:

Table 2: Design Example

V_{IN}	19V
V_{OUT}	3.3V
I_O	1A

The detailed application schematics are shown in Figure 10 through Figure 15. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS (8)

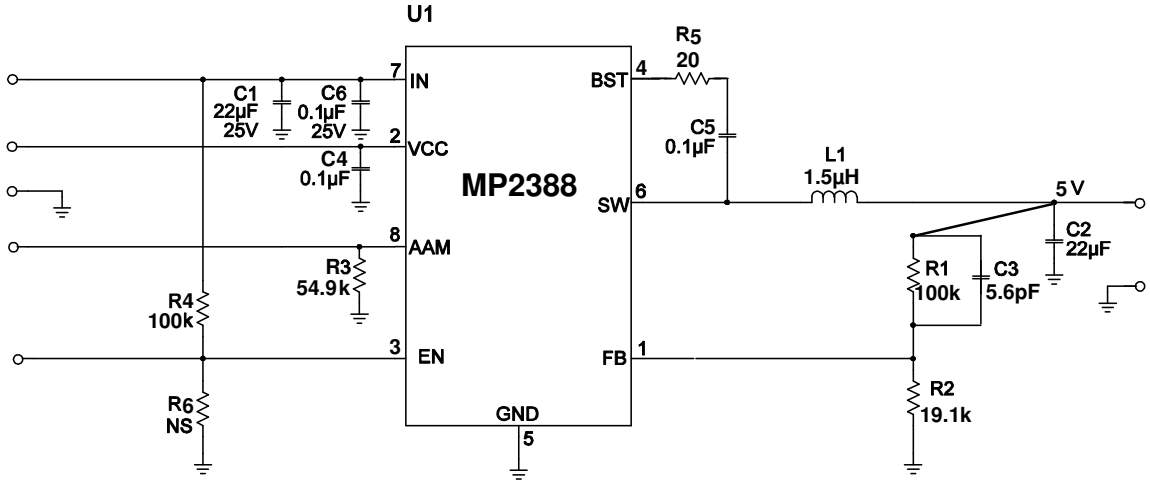


Figure 10: V_{IN} = 19V, Vo = 5V, Io = 1A

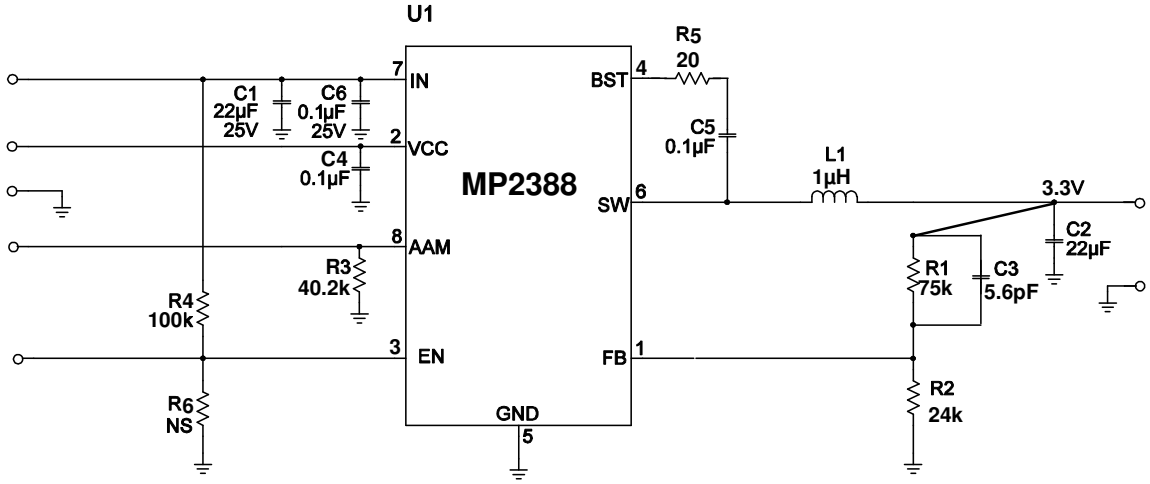


Figure 11: V_{IN} = 19V, Vo = 3.3V, Io = 1A

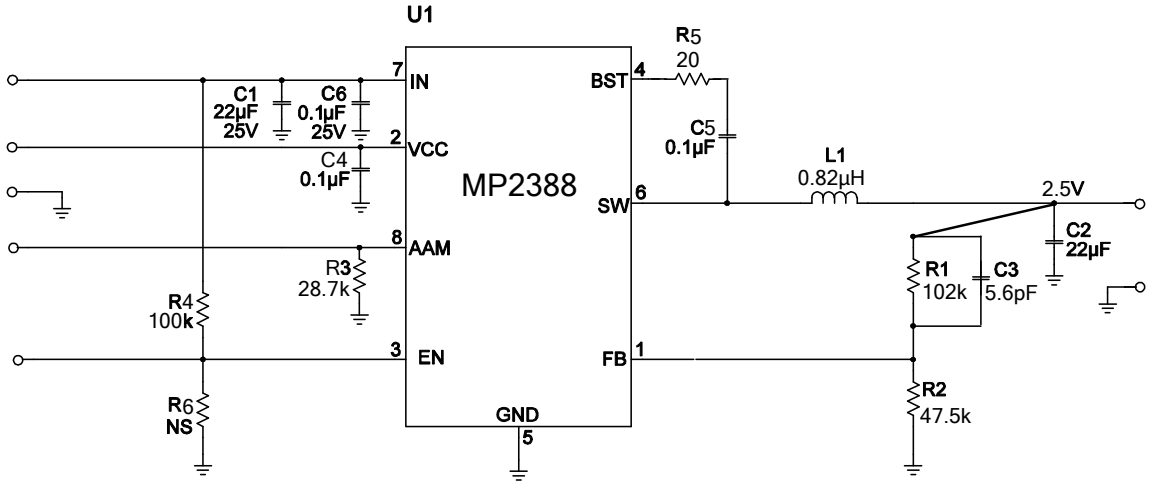


Figure 12: V_{IN} = 19V, Vo = 2.5V, Io = 1A

TYPICAL APPLICATION CIRCUITS (*continued*)

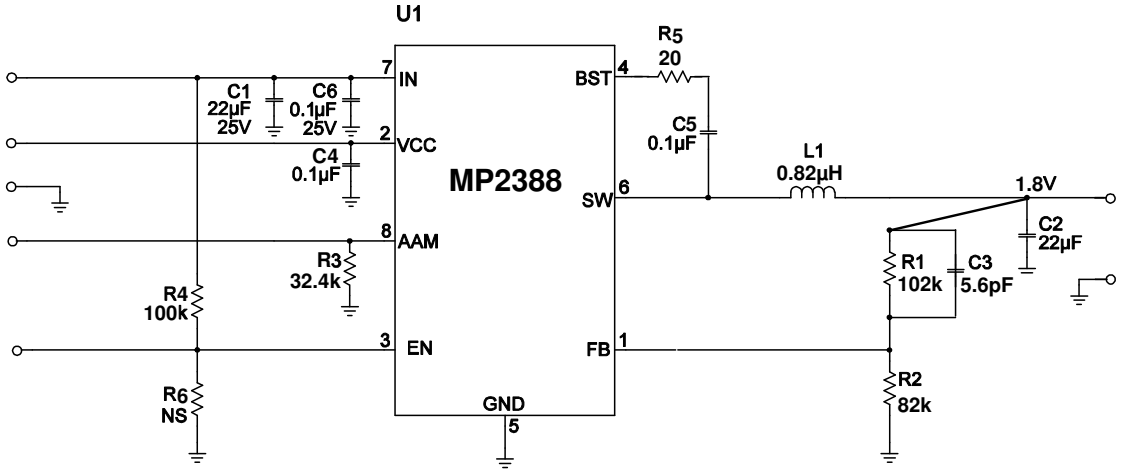


Figure 13: V_{IN} = 12V, Vo = 1.8V, Io = 1A

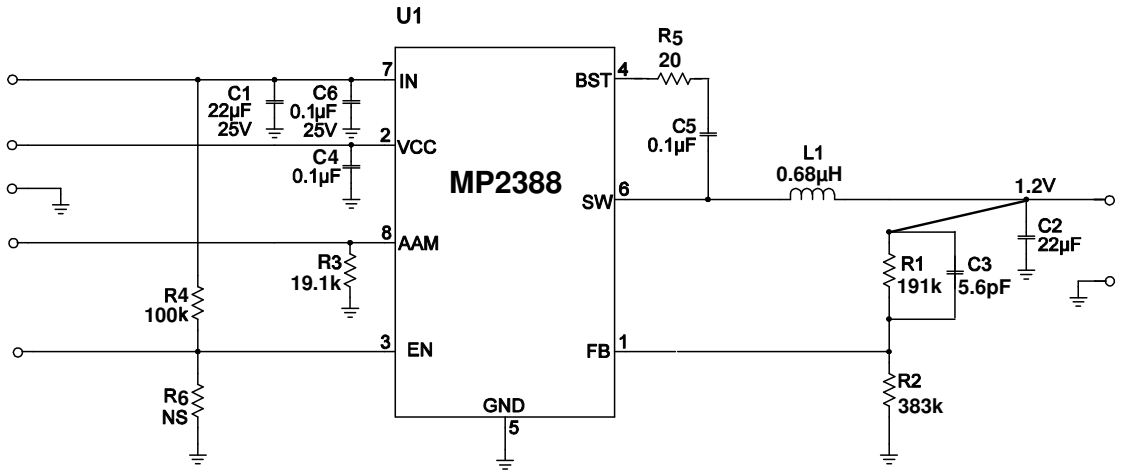


Figure 14: V_{IN} = 12V, Vo = 1.2V, Io = 1A

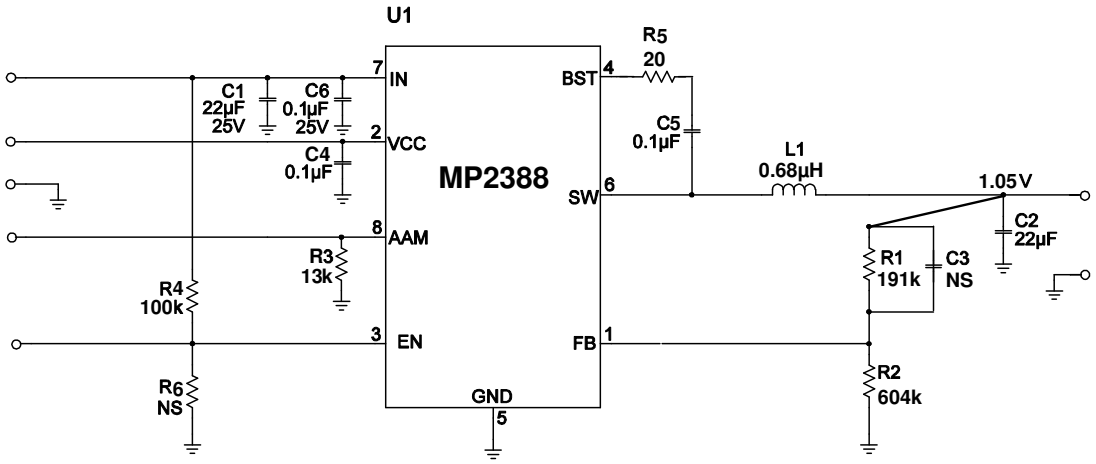


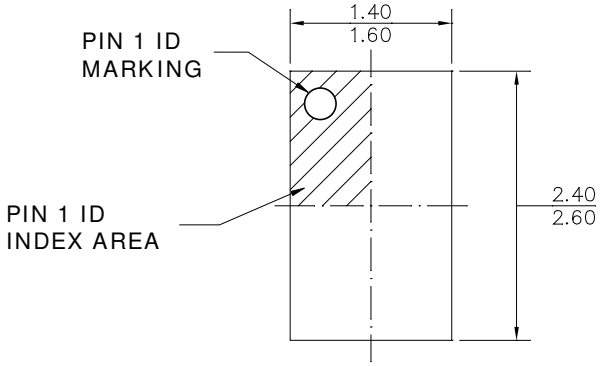
Figure 15: VIN = 12V, Vo = 1.05V, Io = 1A

NOTE:

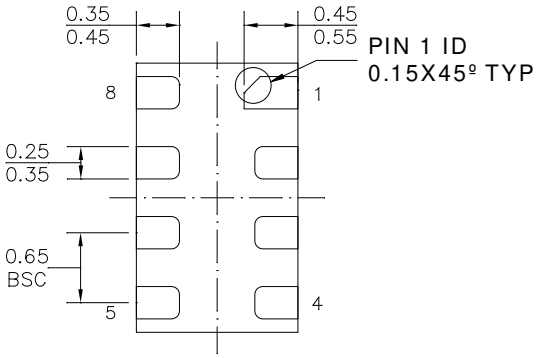
8) In $12V_{IN}$ to $1.05V_{OUT}$ applications, the HS-FET's on time is close to the minimum on time. Although the SW may have a little jitter, the output voltage ripple is smaller than 15mV in PWM mode.

PACKAGE INFORMATION

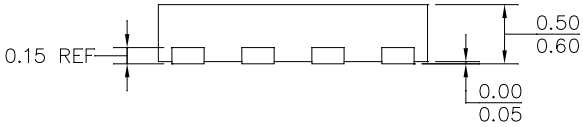
QFN-8 (1.5mmx2.5mm)



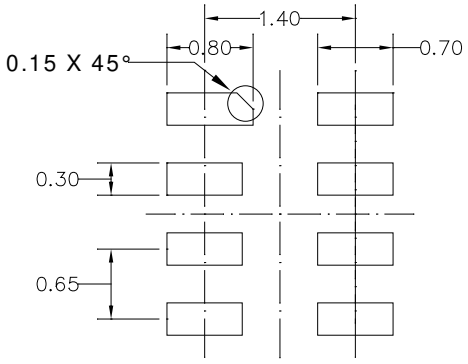
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.