Phase-Locked Loop Clock Driver

Product Features

- High-Performance Phase-Locked-Loop Clock Distribution for Networking, ATM, 100/134 MHz Registered DIMM Synchronous DRAM modules for server/workstation/PC applications
- Zero Input-to-Output delay
- Low jitter: Cycle-to-Cycle jitter ± 100ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V_{CC}
- Packaged in Plastic 8-pin SOIC Package (W)
  Pb-free and Green Available
- Wide range of Clock Frequencies

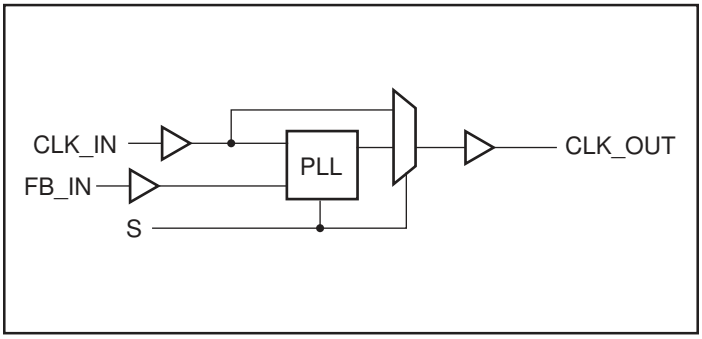
Product Description

The PI6C2401 features a low-skew, low-jitter, phase-locked loop (PLL) clock driver. By connecting the feedback CLK_OUT output to the feedback FB_IN input, the propagation delay from the CLK_IN input to any clock output will be nearly zero.

Application

If the system designer needs more than 16 outputs with the features just described, using two or more zero-delay buffers such as PI6C2509Q, and PI6C2510Q, is likely to be impractical. The device-to-device skew introduced can significantly reduce the performance. Pericom recommends the use of a zero-delay buffer and an eighteen output non-zero-delay buffer . As shown in Figure 1, this combination produces a zero-delay buffer with all the signal characteristics of the original zero-delay buffer, but with as many outputs as the non-zero-delay buffer part. For example, when combined with an eighteen output non-zero delay buffer, a system designer can create a seventeen-output zero-delay buffer.

Logic Block Diagram



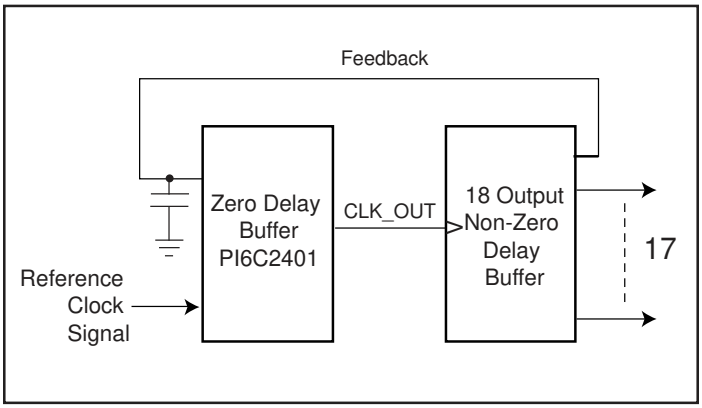
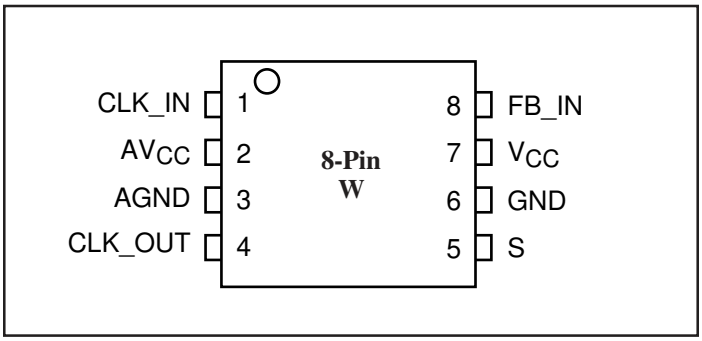


Figure 1. This Combination Provides Zero-Delay Between the Reference Clocks Signal and 17 Outputs

Product Pin Configuration



Control Input

S	Output Source	PLL Shutdown
1	PLL	N
0	CLK_IN	Y

Pin Functions

Pin Name	Pin Number	Type	Description
CLK_IN	1	I	Reference Clock input. CLK_IN allows spread spectrum clock input.
AV_{CC}	2	Power	Analog power supply.
AGND	3	Ground	Analog ground.
CLK_OUT	4	O	Clock outputs. The output provides low-skew copies of CLK_IN and has an embedded series-damping resistor.
S	5	I	Control Input S. S is used to bypass the PLL for test purposes. When S is strapped to ground, PLL is bypassed and CLK_IN is buffered directly to the device outputs.
GND	6	Ground	Ground.
V_{CC}	7	Power	Power supply.
FB_IN	8	I	Feedback input. FB_{IN} provides the feedback signal to the internal PLL.

DC Specifications (Absolute maximum ratings over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
V_I	Input voltage range	–0.5	V_{CC} + 0.5	V
V_O	Output voltage range			
VI_DC	DC input voltage		+5.0	
IO_DC	DC output current		100	mA
Power	Maximum power dissipation at T_A= 55°C in still air		1.0	W
T_{STG}	Storage temperature	-65	150	°C

Note: Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

Parameter	Test Conditions	V_{CC}	Min.	Typ.	Max.	Units
I_{CC}	V_I = V_{CC} or GND; I_O = 0(1)	3.6V			10	µA
C_I	V_I = V_{CC} or GND	3.3V		4		pF
C_O	V_O = V_{CC} or GND			6		

Note:
1. Continuous output current

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply voltage	3.0	3.6	V
V_{IH}	High level input voltage	2.0		
V_{IL}	Low level input voltage		0.8	
V_I	Input voltage	0	V_{CC}	
T_A	Operating free-air temperature	0	70	ºC

Electrical Characteristics

(Over recommended operating free-air temperature range Pull Up/Down Currents, V_{CC} = 3.0V)

Symbol	Parameter	Condition	Min.	Max.	Units
I_{OH}	Pull-up current	V_{OUT} = 2.4V		−12	mA
		V_{OUT} = 2.0V		−18	
I_{OL}	Pull-down current	V_{OUT} = 0.8V	18		
		V_{OUT} = 0.55V	12		

AC Specifications Timing Requirements

(Over recommended ranges of supply voltage and operating free-air temperature)

Symbol	Parameter	Min.	Max.	Units
F_{CLOCK}	Clock frequency	25	134	MHz
D_{CYI}	Input clock duty cycle	40	60	%
	Stabilization Time after power up		1	ms

Switching Characteristics

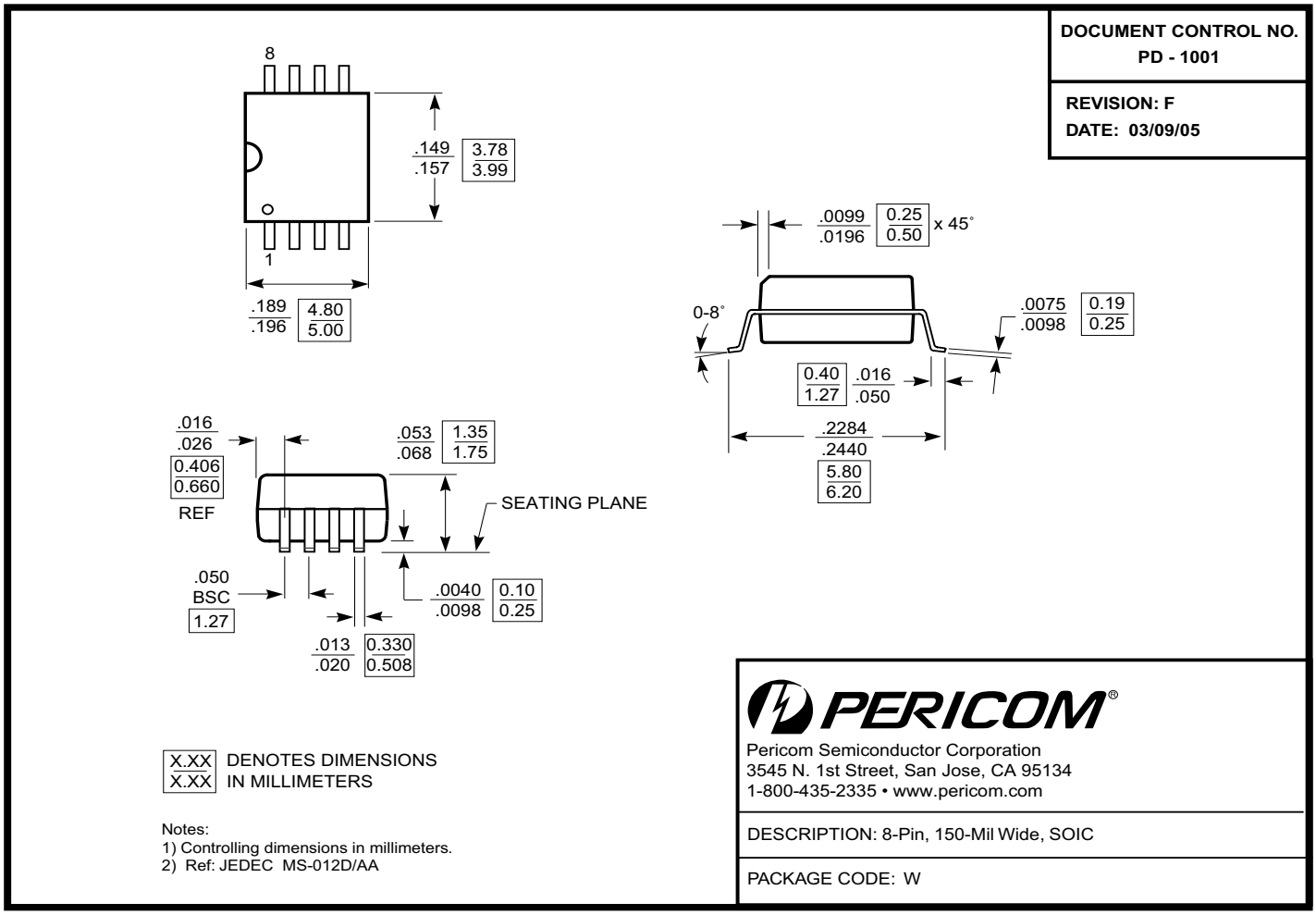
(Over recommended ranges of supply voltage and operating free-air temperature, C_L=30pF)

Parameter	From	To	V_{CC}= 3.3V ± 0.3V, 0-70 °C			Units
			Min.	Typ.	Max.	
tphase error without jitter	CLK_IN ↑ at 100 MHz and 66 MHz	FB_IN↑			+175	ps
Jitter, cycle-to-cycle	At 100 MHz and 66 MHz	CLK_OUT	−150		+150	
Duty cycle		CLK_OUT	35		65	%
tr, rise-time, 0.4V to 2.0V				1.0		ns
tf, fall-time, 2.0V to 0.4V				1.1		

Note: These switching parameters are guaranteed by design.

Package Mechanical Information

Plastic 8-pin SOIC Package



Ordering Information

Ordering Code	Package Code	Package Type	Operating Range
PI6C2401WE	W	Pb-free and Green 8-pin 150-mil SOIC	Commercial

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. X = Tape/Reel
3. E = Pb-free & Green