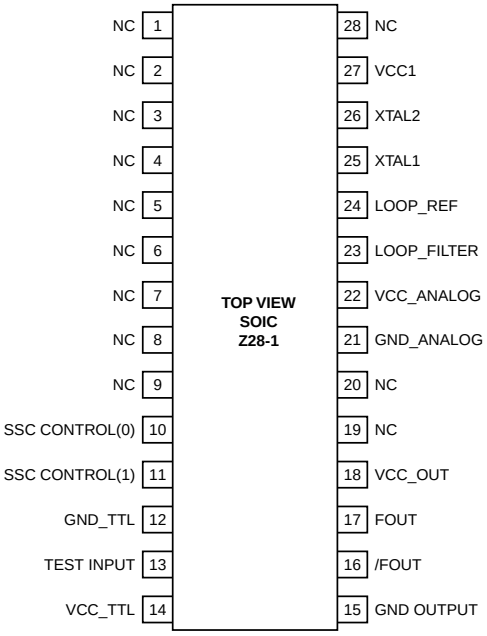
- **Low voltage, 3.3V power supply operation**
- **200MHz precision LVPECL output from a low cost 16.66MHz crystal**
- **0.5% spread-spectrum modulation control**
- **> 7dB reduction in EMI with spread-spectrum modulation**
- **LVTTL/LVCMOS compatible control inputs**
- **interfaces directly to a crystal**
- **Precision PLL architecture ensures < 30ps peak-to-peak, cycle-to-cycle output jitter**
- **48%-to-52% precision duty cycle is ideal for double-data-rate clocking applications**
- **Available in low cost 32-pin TQFP and 28-pin SOIC packages**

The SY89529L is a high-speed, precision PLL-based LVPECL clock synthesizer with spread-spectrum modulation control. With an external 16.66MHz crystal providing a reference frequency to the internal PLL, the differential PECL output frequency will be 200MHz with < 30ps (20ps typ.) peak-to-peak, cycle-to-cycle output jitter. The SY89529L spread-spectrum mode operates with a 30kHz triangle modulation with 0.5% down-spread (+0.0%/–0.5%). When spread-spectrum is activated, the output signal is modulated which spreads the peak amplitudes and, thus, decreases EMI (Electro-Magnetic Interference).

APPLICATIONS

- **High-speed synchronous systems**
- **CPU clock**
- **Multi-processor workstations and servers**
- **Networking**

PACKAGE/ORDERING INFORMATION



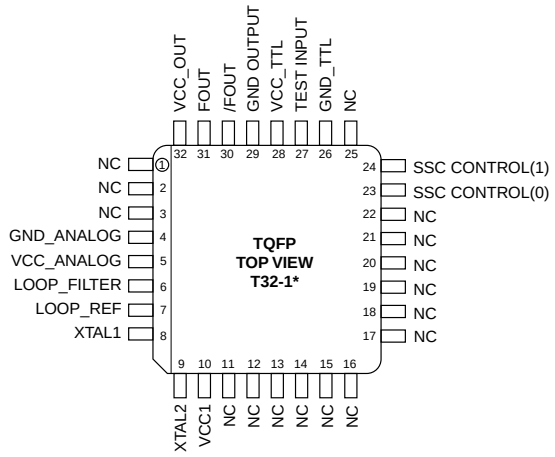
28-Pin SOIC (Z28-1)

Ordering Information(1)

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89529LZC	Z28-1	Commercial	SY89529LZC	Sn-Pb
SY89529LZCTR(2)	Z28-1	Commercial	SY89529LZC	Sn-Pb
SY89529LTC	T32-1	Commercial	SY89529LTC	Sn-Pb
SY89529LTCTR(2)	T32-1	Commercial	SY89529LTC	Sn-Pb
SY89529LZH(3)	Z28-1	Commercial	SY89529LZH with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY89529LZHTR(2, 3)	Z28-1	Commercial	SY89529LZH with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY89529LTH(3)	T32-1	Commercial	SY89529LTH with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY89529LTHTR(2, 3)	T32-1	Commercial	SY89529LTH with Pb-Free bar-line indicator	Pb-Free NiPdAu

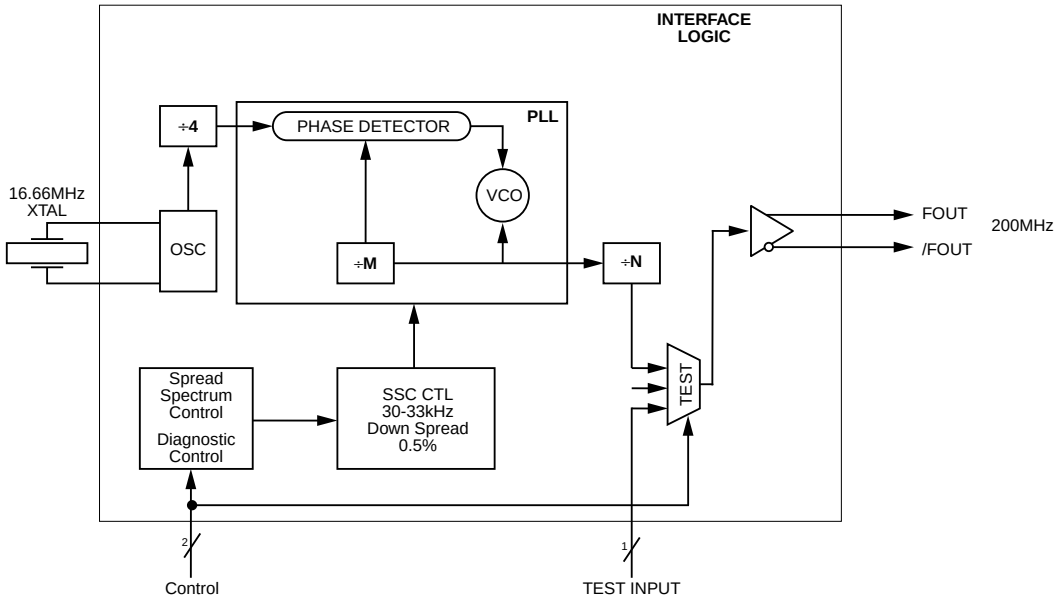
Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.



32-Pin TQFP (T32-1)

BLOCK DIAGRAM



Commands				Operational Modes
SSC_CTL (1:0)	VCO	SSC	FOUT, /FOUT	
0 0	—	—	—	Reserved (Supplier Internal Test Mode)
0 1	Run	Run	200MHz	Default SSC; Modulation Factor = 0.5%
1 0	Stop	Stop	TEST_I/O	Diagnostic Mode; (1MHz ≤ TEST INPUT ≤ 200MHz)
1 1	Run	Stop	200MHz	No Spread-Spectrum

Table 1. SY89529L Control/Operational Modes

PIN DESCRIPTIONS

Input/Output Pins

Pin Number SOIC	Pin Number TQFP	Pin Name	I/O	Pin Function
25,26	8, 9	XTAL1, XTAL2	Analog Inputs	These pins form an oscillator when connected to an external crystal. Either series or parallel-resonant crystals are acceptable. Connect directly to the device.
10, 11	23, 24	SSC Control (0:1)	LVTTL Inputs	LVTTL-compatible spread-spectrum control pins. Data on control pins maintain device control. For spread-spectrum operation, leave SSC_0 and SSC_1 pins floating (default is spread ON). To reconfigure the device, simply change the SSC and the device will respond dynamically. SSC_0 = 24kΩ pullup. SSC_1 = 24kΩ pulldown
16, 17	30, 31	FOUT, /FOUT	Differential	Differential, LVPECL clock outputs. These outputs must be terminated to V_{CC} –2V. (see Figure 6)
23	6	LOOP_FILTER	Analog I/O	Used for the R//C PLL loop filter. (see Figure 2.)
24	7	LOOP_REF	Analog I/O	Provides the reference voltage for the PLL. (see Figure 2).
13	27	TEST INPUT	LVTTL Inputs	Pin is used for test and debug purposes. Is intended to be left floating in production environment. Programmed as input in PLL-bypass mode. Pin includes an internal 24kΩ pullup resistor.

Power Supply Pins

Pin Number SOIC	Pin Number TQFP	Pin Name	I/O	Pin Function
14, 27	10, 28	V_{CC1}, V_{CC_TTL}	Logic Power	3.3V LVTTL core logic power-supply pins. Connect each pin directly to the logic-supply plane and use proper bypassing at each pin as close to the pin as possible; Ferrite bead in parallel with 1µF//0.01µF capacitors. (see Figure 5 for typical bypass circuit.)
22	5	ANALOG_ V_{CC} Power	PLL	3.3V PLL core supply pin. Must be a noise free supply. Bypass as close to the pin as possible; ferrite bead in parallel with 1µF//0.01µF capacitors. (see Figure 5 for typical bypass circuit.)
18	32	V_{CC_OUT}	Output Power	This is the positive power supply reference for the LVPECL outputs (FOUT and /FOUT). See Figure 5 for typical bypass circuit.
12	26	GND_TTL	Logic	This is the ground pin for for the TTL control logic. Normally connected to the logic ground.
21	4	GND_ANALOG	Analog GND	This is the ground pin for the PLL Core. Normally connected to a quiet, noise-free ground plane for low jitter perfomance.
15	29	GND_OUTPUT	Output GND	Ground for differential outputs. Normally connected to the logic ground plane.

No Connect Pins

Pin Number SOIC	Pin Number TQFP	Pin Name	I/O	Pin Function
1, 2, 3, 4, 5 6, 7, 8, 9, 19 20, 28	1, 2, 3, 11, 12, 13 14, 15, 16, 17, 18 19, 20, 21, 22, 25	NC	No Connect	Pins are high-impedance, low leakage and are not used by internal circuits of the device. These pins are intended to be left floating in production.

FUNCTIONAL DESCRIPTION AND TEST MODES

Introduction

The SY89529L supports three operational modes, as shown in Table 1, page 2. The three modes are spread-spectrum clocking (SSC), non-spread-spectrum clock, and a test mode dynamically controlled with the SSC_Control pins. Unlike other synthesizers, the SY89529L can change spread-spectrum operation on the fly.

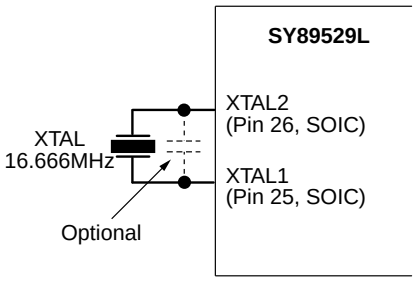
In SSC mode, the output clock is modulated (30KHz, triangle waveform) in order to achieve a reduction in EMI. In the PLL-bypass test mode, the PLL is disconnected as the source to the differential output, thus allowing an external source to be connected to the TEST INPUT pin. This is useful for in-circuit testing by enabling the differential output to be driven at a lower frequency.

Crystal Input and Oscillator Interface

The SY89529L features a fully integrated on-board oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design, and thus, a series-resonant crystal is preferred, but not required.

A parallel-resonant crystal can be used with the SY89529L with only a minor error in the desired frequency. A parallel-resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to KHz inaccuracies. In a general computer application this level of inaccuracy is immaterial.

As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the SY89529L as possible to avoid any board level parasitics. In addition, trace lengths should be matched. Figure 1 shows how to interface with a crystal. Table 2 illustrates the crystal specifications. If a start-up problem occurs, consider adding a 10pf capacitor across XTAL1 and XTAL2.



Quartz Crystal Selection:
(1) Raltron Series Resonant: AS-16.666-S-SMD-T-MI
(2) Raltron Parallel Resonant: AS-16.666-18-SMD-T-MI

Figure 1. Crystal Interface

Loop Filter Design

The filter for any Phase Locked Loop (PLL) based device deserves special attention. SY89529L provides filter pins for an external filter. A simple three-component passive filter is required for achieving ultra low jitter. Figure 2 shows the recommended three-components. Due to the differential design, the filter is connected between LOOP_FILTER and LOOP_REF pins. With this configuration, extremely high supply noise rejection is achieved. It is important that the filter circuit and filter pins be isolated from any non-common mode coupling plane.

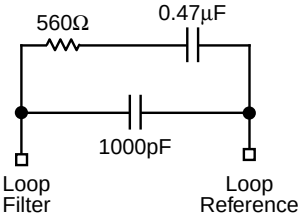


Figure 2. External Loop Filter Connection

Output Frequency: 16.666MHz				
Mode of Oscillation: Fundamental				
	Min.	**Typ.**	**Max.**	**Unit**
Frequency Tolerance @25°C	—	±30	±50	ppm
Frequency Stability over 0°C to 70°C	—	±50	±100	ppm
Operating Temperature Range	–20	—	+70	°C
Storage Temperature Range	–55	—	+125	°C
Aging (per yr/1st 3yrs)	—	—	±5	ppm
Load Capacitance	—	18 (or series)	—	pF
Equivalent Series Resistance (ESR)	—	—	50	Ω
Drive Level	—	100	—	µW

Table 2. Quartz Crystal Oscillator Specifications

Spread Spectrum

Spread-spectrum clocking is a frequency modulation technique for EMI reduction. When spread-spectrum is enabled, a 30kHz triangle waveform is used with 0.5% down-spread (+0.0%/–0.5%) from the nominal 200MHz clock frequency. An example of a triangle frequency modulation profile is shown in the figure 3 below. The ramp profile can be expressed as:

- Fnom = Nominal Clock Frequency in Spread OFF mode (200MHz with 16.66MHz IN)
- Fm = Nominal Modulation Frequency (30kHz)
- δ = Modulation Factor (0.5% down spread)

$$(1-\delta)\,fnom + 2\,fm \times \delta \times fnom \times t \quad when \quad 0 < t < \frac{1}{2\,fm},$$

$$(1+\delta)\,fnom - 2\,fm \times \delta \times fnom \times t \quad when \quad \frac{1}{2\,fm} < t < \frac{1}{fm}$$

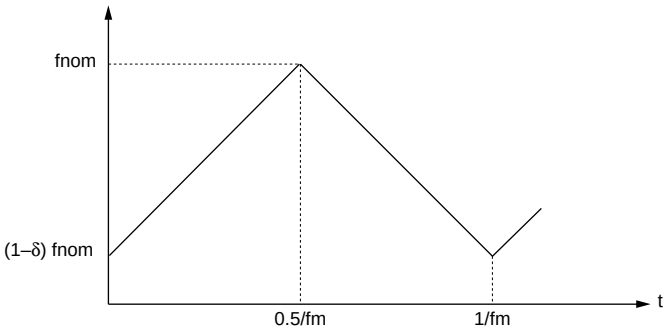


Figure 3. Triangle Frequency Modulation

The SY89529L triangle modulation frequency deviation (δ) will not exceed 0.6% down-spread from the nominal clock frequency (+0.0%/–0.5%). An example of the amount of down spread relative to the nominal clock frequency can be seen in the frequency domain, as shown in Figure 4. The ratio of this width to the fundamental frequency is typically 0.5%, and will not exceed 0.6%. The resulting spectral reduction will be greater than 7dB, as shown in Figure 5. It is important to note the SY89529L 7dB minimum spectral reduction is the component-specific EMI reduction, and will not necessarily be the same as the system EMI reduction.

200MHz Clock Output in Frequency Domain
(A) Spread-Spectrum OFF
(B) Spread-Spectrum ON

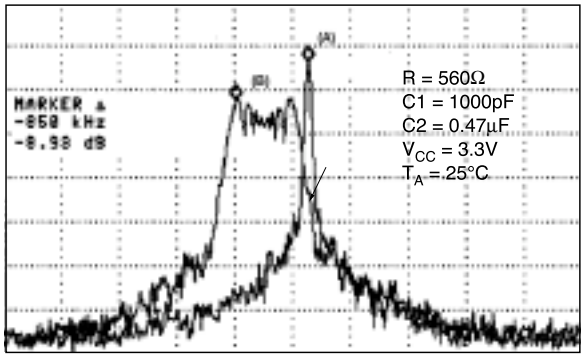


Figure 5. 200MHz Clock Output in Frequency Domain

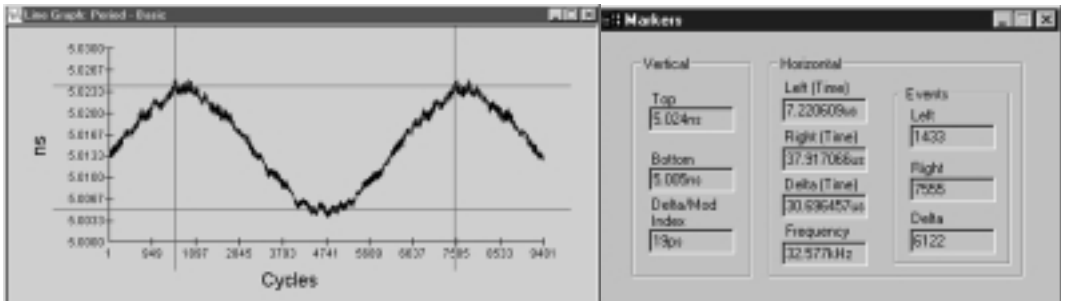
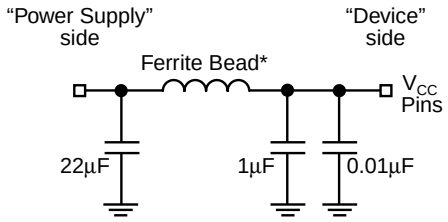


Figure 4. 0.38% Modulation,
32.7KHz Modulation Frequency

Power Supply Filtering Techniques

As in any high speed integrated circuits, power supply filtering is very important. V_{CC1}, $V_{CC_}$Analog, V_{CC_TTL} and V_{CC_OUT} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, better power-supply isolation is required. In this case a ferrite bead along with a 1µF and a 0.01µF bypass capacitor should be connected to each power supply pin. Figure 6 illustrates power-supply filtering using ferrite beads and bypass capacitors.



*For $V_{CC_}$Analog, V_{CC_TTL}, V_{CC1}, use ferrite bead = 200mA, 0.45Ω DC, Murata P/N BLM21A1025

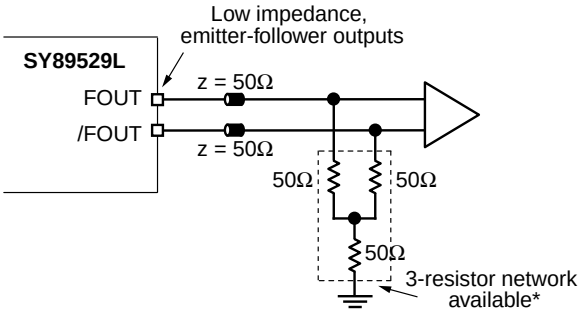
*For V_{CC_OUT} use ferrite bead = 3A, 0.025Ω DC, Murata, P/N BLM31P005

*Componet sizs: 0805

Figure 5. Power Supply Filtering

Termination for PECL Outputs

The differential PECL outputs, FOUT and /FOUT, are low-impedance emitter-follower outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. There are a few simple termination schemes. Figure 7 shows a common 3-resistor termination scheme. For more termination examples, see Micrel's Application Note 9 online at www.micrel.com.



*3-resistor network = Thin-film Technologies, P/N TFT-RN1632-AN1DNC

Figure7. LVPECL Output Termination

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	V
V_{IN}	Input Voltage	–0.5 to +7.0	V
I_{OUT}	Output Source –Continuous –Surge	50 100	mA
T_{LEAD}	Lead Temperature (soldering, 20sec.)	260	°C
T_{store}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	–0 to +75	°C

NOTE:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.

LVPECL DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC_}$Analog $= V_{CC\_TTL} = V_{CC\_OUT} = +3.3V \pm 10\%$; $T_A = 0°C$ to $+85°C$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	V_{CC_OUT} –1.075	—	V_{CC_OUT} –0.830	V	50Ω to V_{CC_OUT} –2V
V_{OL}	Output LOW Voltage	V_{CC_OUT} –1.860	—	V_{CC_OUT} –1.570	V	50Ω to V_{CC_OUT} –2V
V_{CMR}	Common Mode Range	600	700	800	mV	

LVTTL DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC_}$Analog $= V_{CC\_TTL} = V_{CC\_OUT} = +3.3V \pm 10\%$; $T_A = 0°C$ to $+85°C$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
	Power Supply Voltage ($V_{CC_}$Analog, V_{CC1}, V_{CC_OUT}, V_{CC_TTL})	3.135	3.3	3.465	V	
V_{IH}	Input HIGH Voltage SSC TEST INPUT	2.0 $V_{CC}/2$ +0.3	— —	V_{CC} +0.3 —	V V	Note 1
V_{IL}	Input LOW Voltage SSC TEST INPUT	–0.3 —	— —	0.80 $V_{CC}/2$ –0.3	V V	Note 1
V_{IK}	Input Clamp Voltage	—	—	–1.2	V	I_{IN} = –12mA
I_{IH}	Input HIGH Current SSC TEST INPUT	— —	— —	50 50	µA µA	Note 2
I_{IL}	Input LOW Current SSC TEST INPUT	— —	— —	0.60 0.60	mA mA	Note 2
I_{CC}	Total Supply Current Typcial % of I_{CC} V_{CC1} V_{CC_OUT} $V_{CC_}$Analog V_{CC_TTL}	— — — — —	110 14% 5% 5% 76%	145 — — — —	mA	No output load

NOTES:

1. For TEST INPUT, input threshold is $V_{CC}/2$.
2. Posituve and negative-going input threshold is set internally to track $V_{CC}/2$.

AC ELECTRICAL CHARACTERISTICS

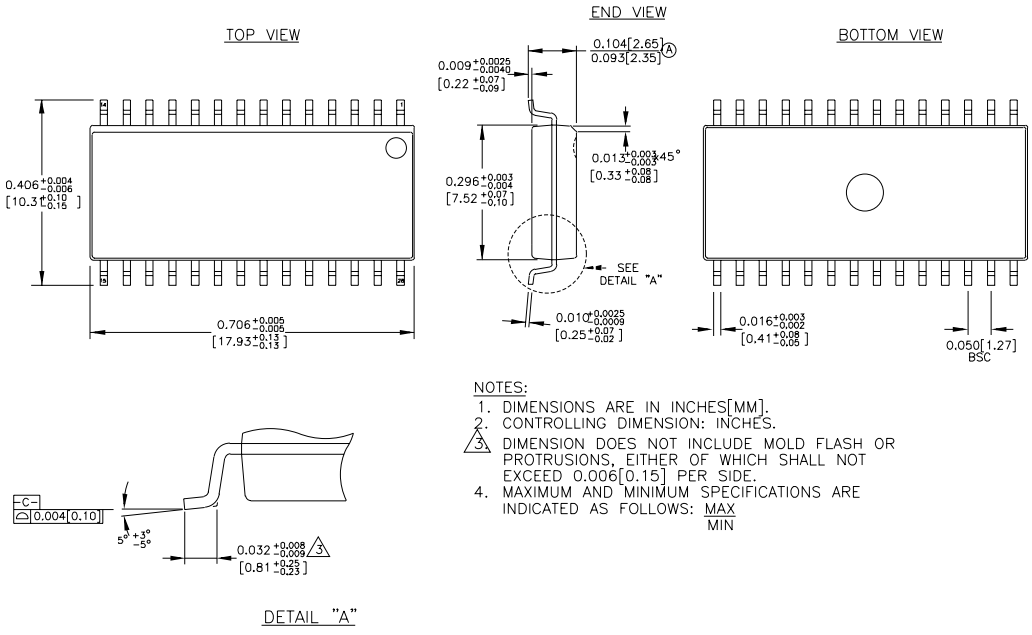
V_{CC1} = $V_{CC_}$Analog = V_{CC_TTL} = V_{CC_OUT} = +3.3V ±10%; T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
F_M	SSC Modulation Frequency	30	—	33.33	KHz	
F_{MF}	SSC Modulation Factor	—	0.5	0.6	%	
$S_{RED'N}$	Spectral Reduction	7	9	—	dB	FOUT = 200MHz(2)
F_{XTAL}	Crystal Input Range	14	16.66	18	MHz	
t_{DC}	Output Duty Cycle(1)	48	—	52	%	FOUT = 200MHz
t_{JIT}	Peak-to-Peak, Cycle-to-Cycle Jitter(1)	—	20	30	ps	FOUT = 200MHz
t_{PERIOD}	Output Period(1)	4995	—	5005	ps	FOUT = 200MHz
t_{STABLE}	Power-Up to Stable Clock Output	—	—	10	ms	
t_r t_f	Output Rise/Fall Times (20% to 80%)	300	—	800	ps	FOUT, /FOUT

NOTES:

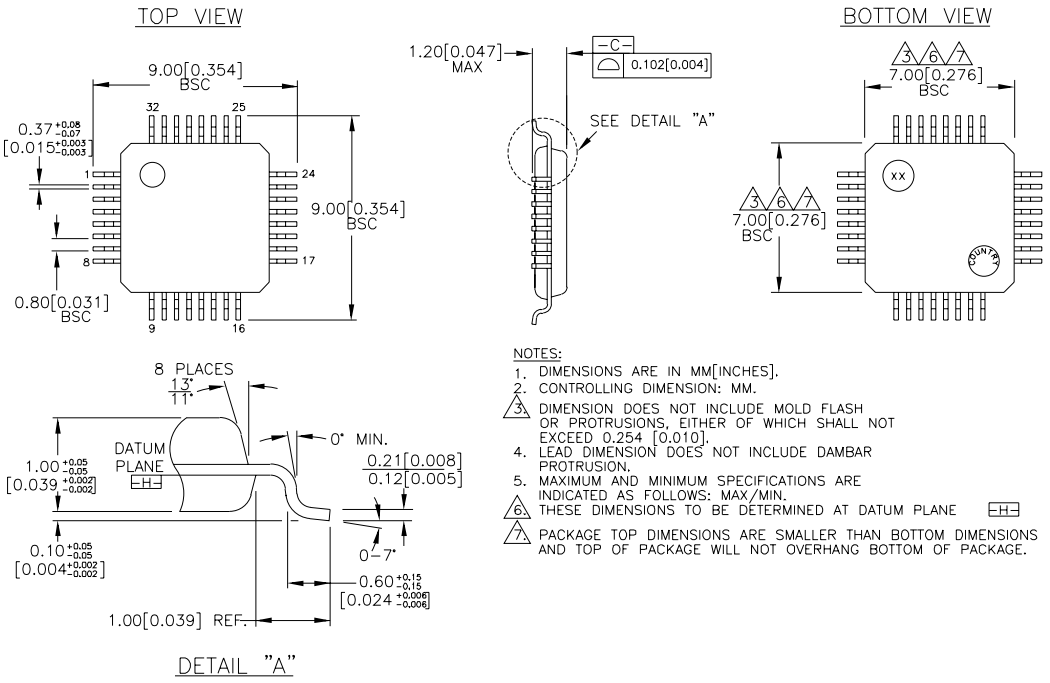
1. Spread-spectrum clocking enabled.
2. SY89529L spectral reduction is the component-specific indication of EMI reduction. The SY89529L's spectral peak reduction is not necessarily the same as the system EMI reduction.

28-PIN SOIC .300" WIDE (Z28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.
4. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN

32-PIN TQFP (T32-1)



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.

Rev. 01

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com