



1 M x 32 CMOS STATIC RAM MODULE

IDT7MP4120

FEATURES

- High-density 4MB Static RAM module
- Low profile 72-pin ZIP (Zig-zag In-line vertical Package) or 72-pin SIMM (Single In-line Memory Module)
- Fast access time: 15ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V ($\pm 10\%$) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

PIN CONFIGURATION⁽¹⁾

NC	2	1	NC	PD ₀ - GND
PD ₃	4	3	PD ₂	PD ₁ - NC
PD ₀	6	5	GND	PD ₂ - GND
I/O ₀	8	7	PD ₁	PD ₃ - NC
I/O ₁	10	9	I/O ₈	
I/O ₂	12	11	I/O ₉	
I/O ₃	14	13	I/O ₁₀	
V _{CC}	16	15	I/O ₁₁	
A ₇	18	17	A ₀	
A ₈	20	19	A ₁	
A ₉	22	21	A ₂	
I/O ₄	24	23	I/O ₁₂	
I/O ₅	26	25	I/O ₁₃	
I/O ₆	28	27	I/O ₁₄	
I/O ₇	30	29	I/O ₁₅	
WE	32	31	GND	
A ₁₄	34	33	A ₁₅	
\overline{CS}_1	36	35	\overline{CS}_2	
\overline{CS}_3	38	37	\overline{CS}_4	
A ₁₆	40	39	A ₁₇	
GND	42	41	\overline{OE}	
I/O ₁₆	44	43	I/O ₂₄	
I/O ₁₇	46	45	I/O ₂₅	
I/O ₁₈	48	47	I/O ₂₆	
I/O ₁₉	50	49	I/O ₂₇	
A ₁₀	52	51	A ₃	
A ₁₁	54	53	A ₄	
A ₁₂	56	55	A ₅	
A ₁₃	58	57	V _{CC}	
I/O ₂₀	60	59	A ₆	
I/O ₂₁	62	61	I/O ₂₈	
I/O ₂₂	64	63	I/O ₂₉	
I/O ₂₃	66	65	I/O ₃₀	
GND	68	67	I/O ₃₁	
A ₁₉	70	69	A ₁₈	
NC	72	71	NC	

ZIP, SIMM
TOP VIEW

3019 drw 01

NOTE:

1. Pins 6, 7, 3 and 4 (PD₀, PD₁, PD₂ and PD₃ respectively) are read by the user to determine the density of the module. If PD₀ reads GND, PD₁ reads NC, PD₂ reads GND and PD₃ reads NC, then the module has a 1M depth.

DESCRIPTION

The IDT7MP4120 is a 1M x 32 Static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 1M x 4 Static RAMs in plastic packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. The IDT7MP4120 is available with access time as fast as 15ns with minimal power consumption.

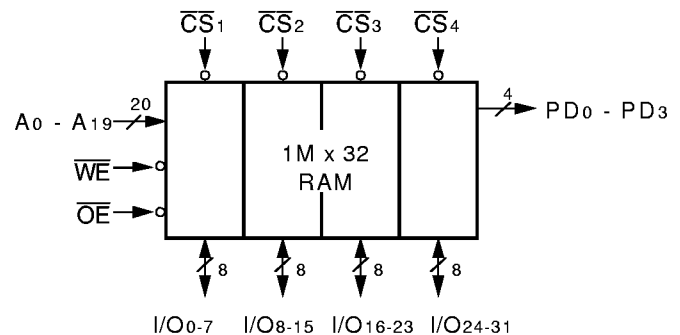
The IDT7MP4120 is packaged in a 72-pin FR-4 ZIP (Zig-zag In-line vertical Package) or a 72-pin SIMM (Single In-line Memory Module). The ZIP configuration allows 72 pins to be placed on a package 4.05" long and 0.365" wide. At only 0.60" high, this low-profile package is ideal for systems with minimum board spacing while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4120 are TTL-compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Four identification pins (PD₀, PD₁, PD₂ and PD₃) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD₀, PD₁, PD₂ and PD₃ to determine a 1M depth.

The SIMM contact pins are plated with 100 micro-inches of nickel covered by 30 micro-inches minimum of selective gold.

FUNCTIONAL BLOCK DIAGRAM



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PIN NAMES

I/O ₀ -I/O ₃₁	Data Inputs/Outputs
A ₀ -A ₁₉	Addresses
\overline{CS}_1 - \overline{CS}_4	Chip Selects
WE	Write Enable
\overline{OE}	Output Enable
PD ₀ -PD ₃	Depth Identification
V _{CC}	Power
GND	Ground
NC	No Connect

3019 tbl 01

MARCH 1999

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{I/O}	Data I/O Capacitance	V _(IN) = 0V	15	pF
C _{IN1}	Input Capacitance (Address)	V _(IN) = 0V	60	pF
C _{IN2}	Input Capacitance (WE, OE)	V _(IN) = 0V	75	pF
C _{IN3}	Input Capacitance (\overline{CS})	V _(IN) = 0V	20	pF

NOTE: 3019 tbl 02
 1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	V _{CC} +0.5	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE: 3019 tbl 03
 1. V_{IL} (min) = -1.5V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V _{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

3019 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
II _{L1}	Input Leakage (Address and Control)	V _{CC} = Max.; V _{IN} = GND to V _{CC}	—	80	μA
II _{L2}	Input Leakage (Data)	V _{CC} = Max.; V _{IN} = GND to V _{CC}	—	10	μA
II _{LO1}	Output Leakage	V _{CC} = Max.; \overline{CS} = V _{IH} , V _{OUT} = GND to V _{CC}	—	10	μA
V _{OL}	Output LOW	V _{CC} = Min., I _{OL} = 8mA	—	0.4	V
V _{OH}	Output HIGH	V _{CC} = Min., I _{OH} = -4mA	2.4	—	V

3019 tbl 07

Symbol	Parameter	Test Conditions	-15	-20/25	Unit
			Max.	Max.	
I _{CC}	Dynamic Operating Current	f = f _{MAX} ; \overline{CS} = V _{IL} V _{CC} = Max.; Output Open	1480	1280	mA
I _{SB}	Standby Supply Current	$\overline{CS} \geq V_{IH}$, V _{CC} = Max. Outputs Open, f = f _{MAX}	480	480	mA
I _{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC} - 0.2V$; f = 0 V _{IN} > V _{CC} - 0.2V or < 0.2V	240	120	mA

3019 tbl 08

TRUTH TABLE

Mode	\overline{CS}	\overline{OE}	WE	I/O	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DATA _{OUT}	Active
Write	L	X	L	DATA _{IN}	Active
Output Disable	L	H	H	High-Z	Active

3019 tbl 05

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	°C
T _{BIAS}	Temperature Under Bias	-10 to +85	°C
T _{STG}	Storage Temperature	-55 to +125	°C
I _{OUT}	DC Output Current	50	mA

NOTE: 3019 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2769 tbl 09

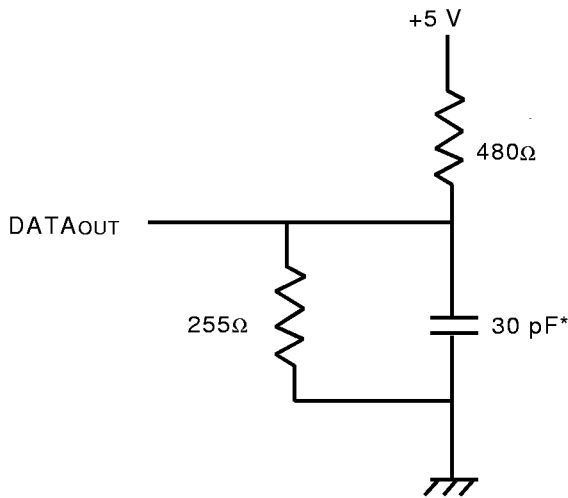


Figure 1. Output Load

3019 drw 03

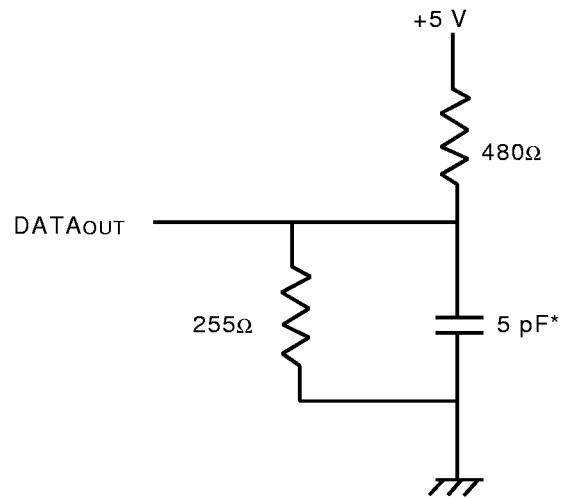


Figure 2. Output Load
(for tOLZ, tOHZ, tCHZ, tCLZ, tWHZ, tOW)

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*Includes scope and jig.

AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ±10%, TA = 0°C to +70°C)

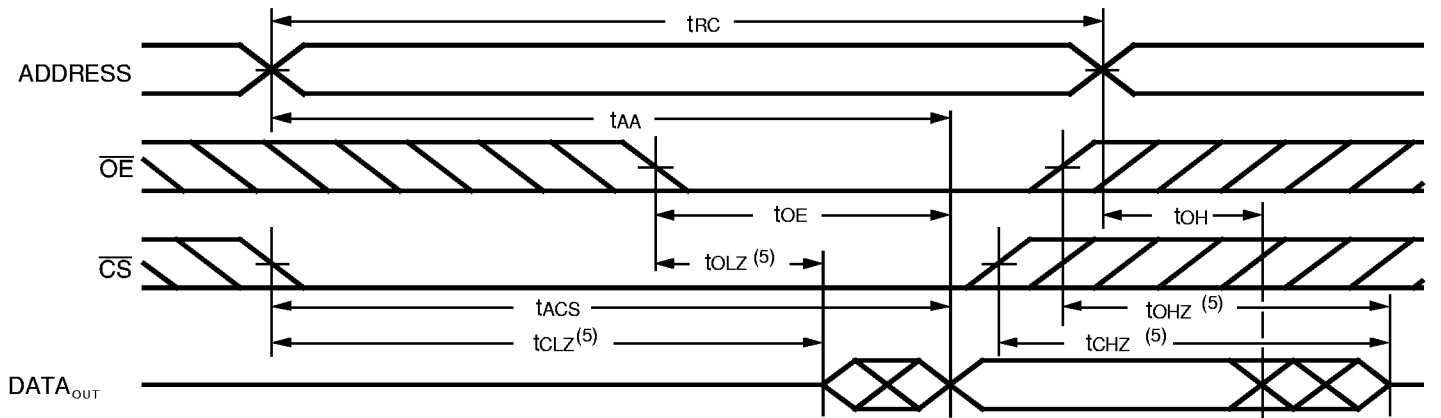
Symbol	Parameter	7MP4120SxxZ/M						Unit
		-15		-20		-25		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	15	—	20	—	25	—	ns
tAA	Address Access Time	—	15	—	20	—	25	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low-Z	3	—	3	—	3	—	ns
tOE	Output Enable to Output Valid	—	10	—	12	—	15	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
tCHZ ⁽¹⁾	Chip Deselect to Output in High-Z	—	8	—	10	—	12	ns
tOHZ ⁽¹⁾	Output Disable to Output in High-Z	—	8	—	10	—	12	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tPU ⁽¹⁾	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
tPD ⁽¹⁾	Chip Deselect to Power-Down Time	—	15	—	20	—	25	ns
Write Cycle								
tWC	Write Cycle Time	15	—	20	—	25	—	ns
tCW	Chip Select to End-of-Write	12	—	17	—	20	—	ns
tAW	Address Valid to End-of-Write	12	—	17	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	3	—	3	—	ns
tWHZ ⁽¹⁾	Write Enable to Output in High-Z	—	8	—	10	—	15	ns
tdW	Data to Write Time Overlap	8	—	12	—	15	—	ns
tdH	Data Hold from Write Time	0	—	0	—	0	—	ns
tOW ⁽¹⁾	Output Active from End-of-Write	0	—	0	—	0	—	ns

NOTE:

1. This parameter is guaranteed by design, but not tested.

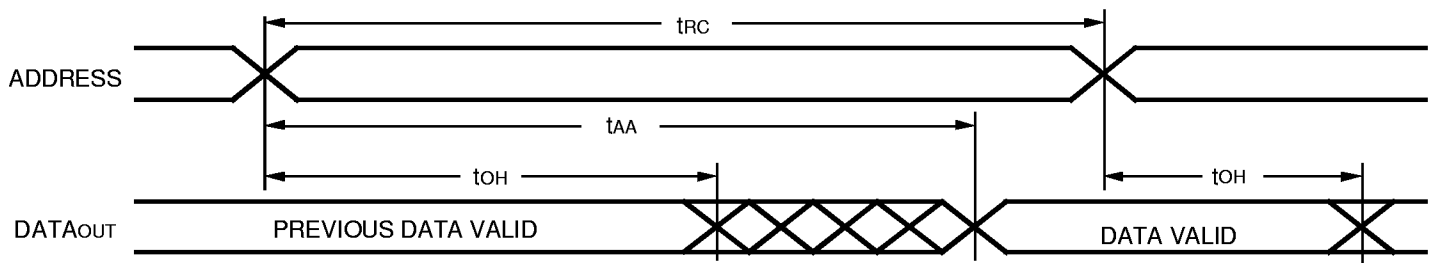
3019 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



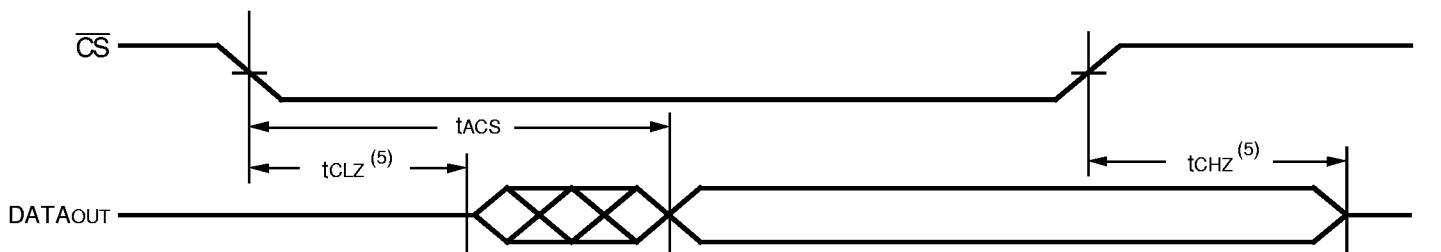
3019 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



3019 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)

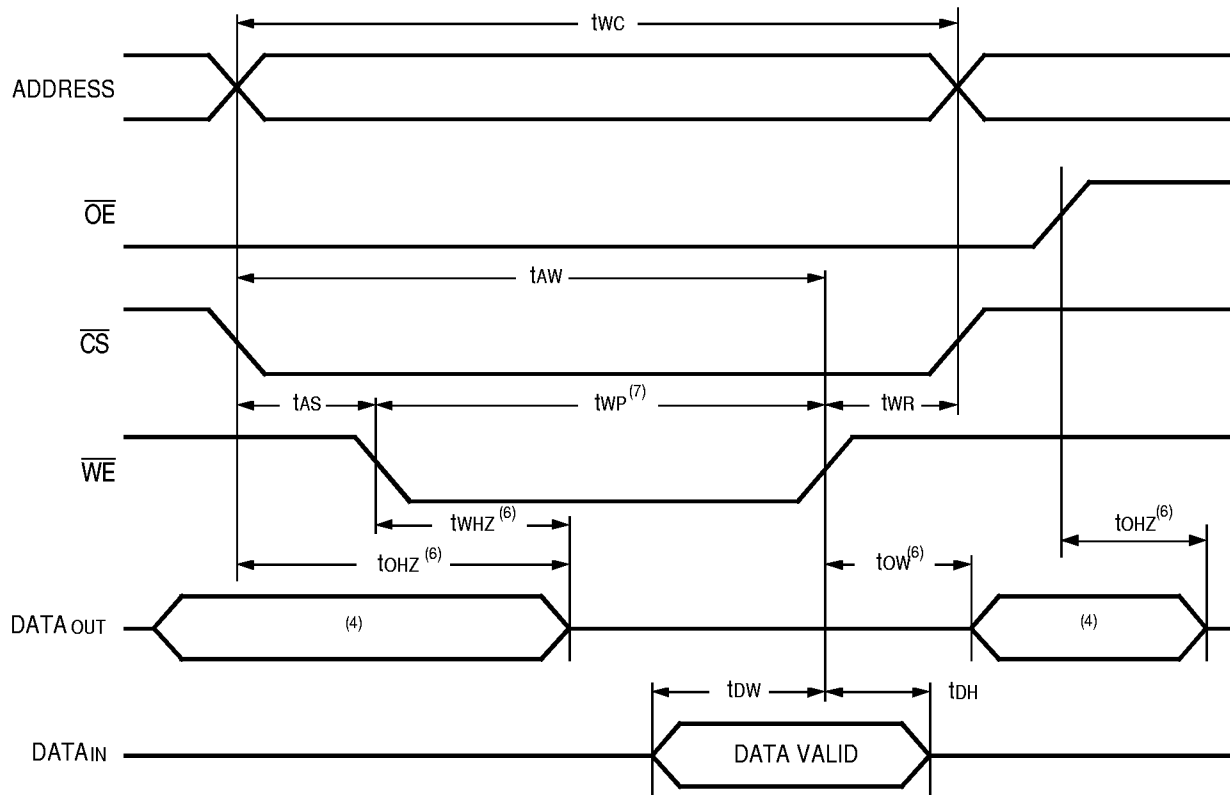


3019 drw 07

NOTES:

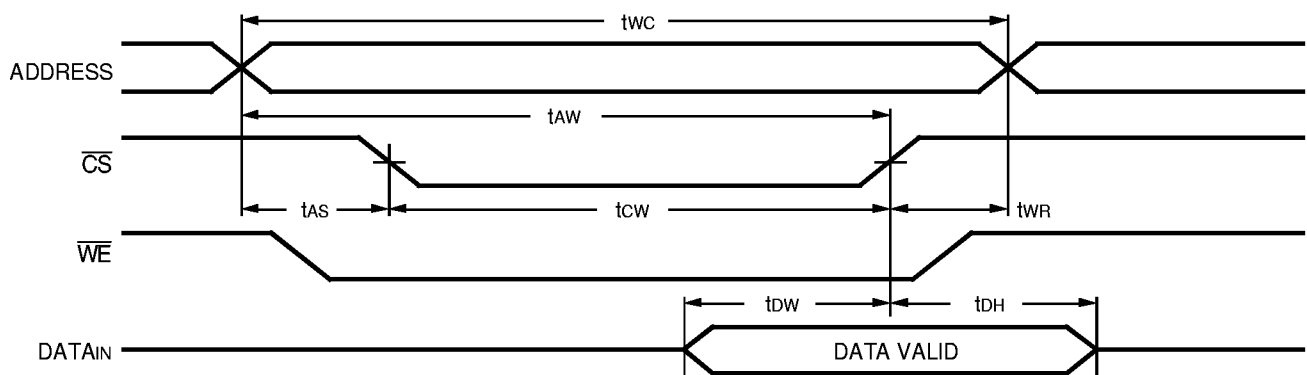
1. \overline{WE} is HIGH for Read Cycle.
2. Device is continuously selected. $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with \overline{CS} transition LOW.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 200mV$ from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED) (1, 2, 3, 7)



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TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} CONTROLLED) (1, 2, 3, 5)



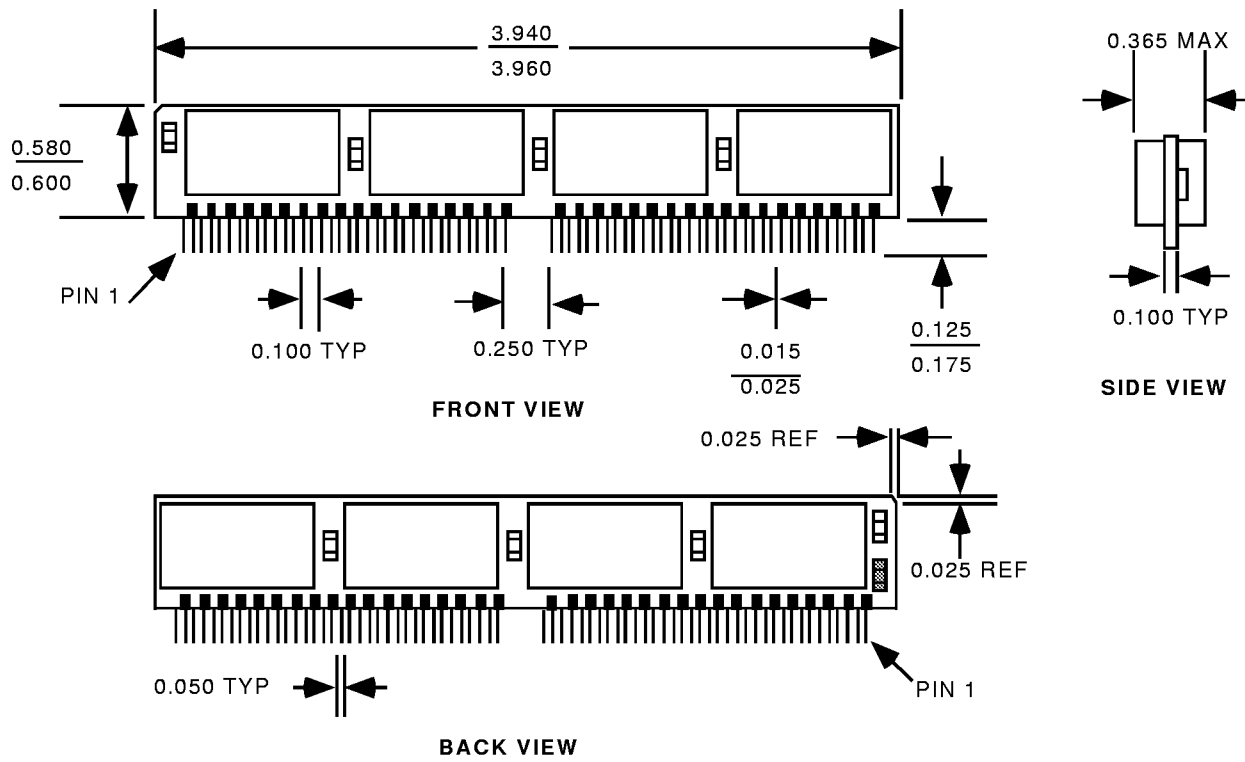
3019 drw 09

NOTES:

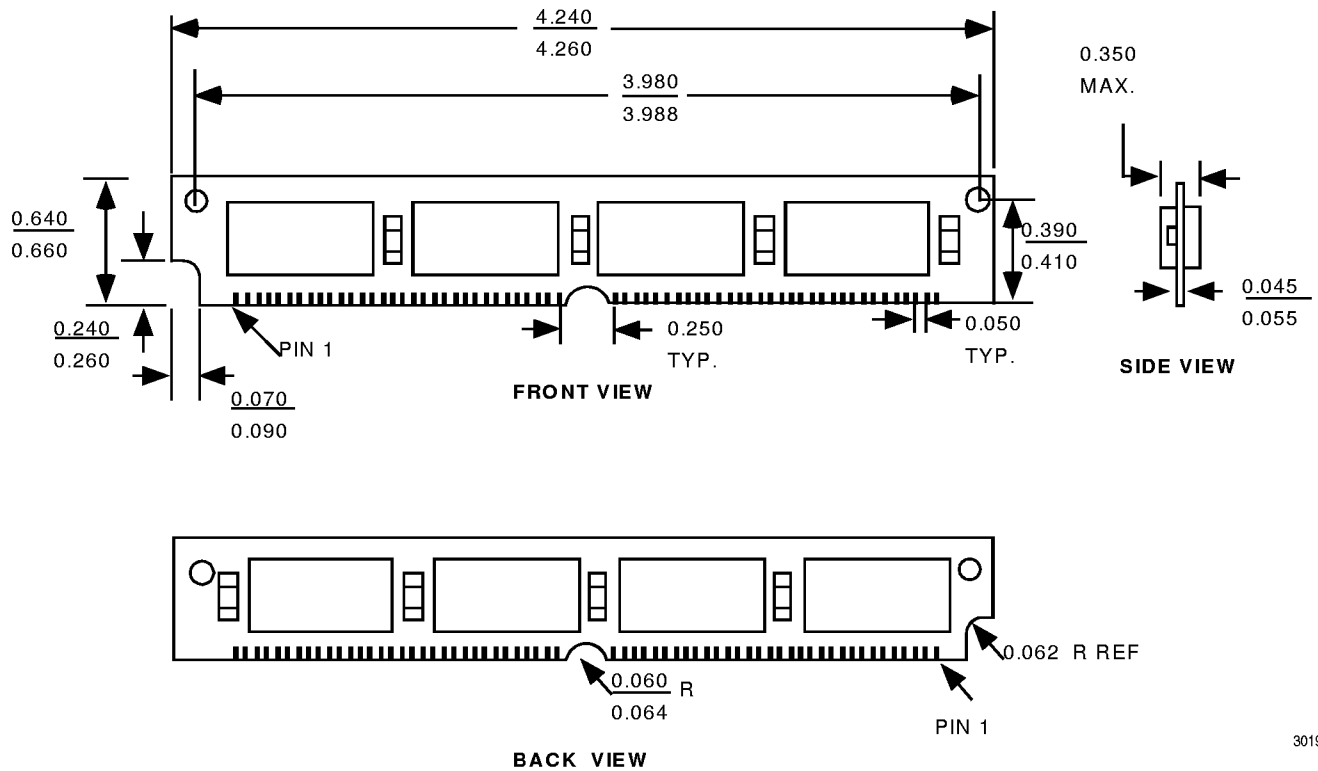
1. \overline{WE} or \overline{CS} must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW \overline{CS} and a LOW \overline{WE} .
3. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CS} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured $\pm 200mV$ from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If \overline{OE} is LOW during a \overline{WE} controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WHZ} + t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

PACKAGE DIMENSIONS

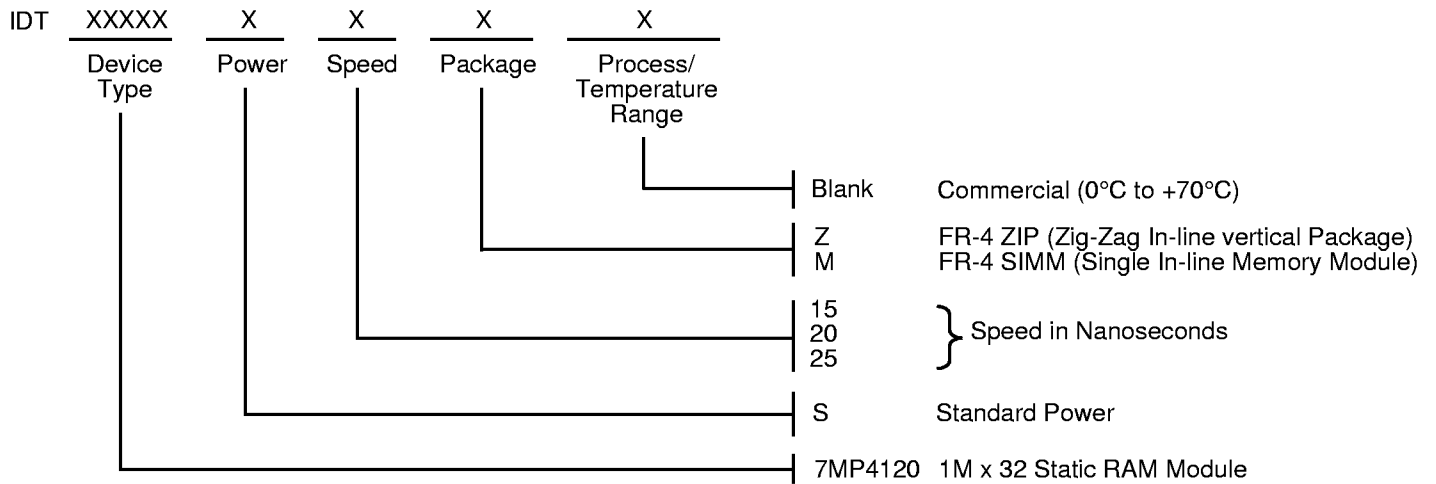
ZIP VERSION



SIMM VERSION



ORDERING INFORMATION



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