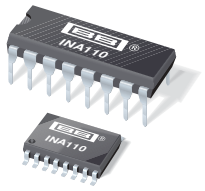
INA110



SBOS147A – SEPTEMBER 1986 – JULY 2005

Fast-Settling FET-Input INSTRUMENTATION AMPLIFIER

FEATURES

- LOW BIAS CURRENT: 50pA max
- FAST SETTLING: 4μs to 0.01%
- HIGH CMR: 106dB min; 90dB at 10kHz
- INTERNAL GAINS: 1, 10, 100, 200, 500
- VERY LOW GAIN DRIFT: 10 to 50ppm/°C
- LOW OFFSET DRIFT: 2μV/°C
- LOW COST
- PINOUT SIMILAR TO AD524 AND AD624

APPLICATIONS

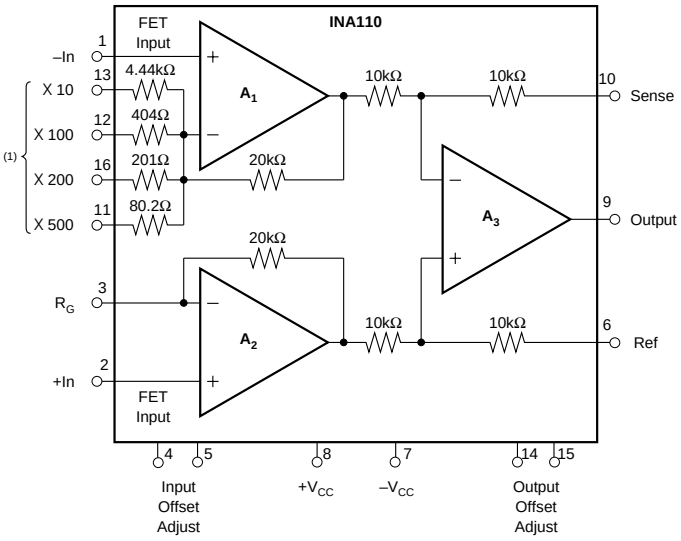
- MULTIPLEXED INPUT DATA ACQUISITION SYSTEM
- FAST DIFFERENTIAL PULSE AMPLIFIER
- HIGH SPEED GAIN BLOCK
- AMPLIFICATION OF HIGH IMPEDANCE SOURCES

DESCRIPTION

The INA110 is a versatile monolithic FET-input instrumentation amplifier. Its current-feedback circuit topology and laser trimmed input stage provide excellent dynamic performance and accuracy. The INA110 settles in 4μs to 0.01%, making it ideal for high speed or multiplexed-input data acquisition systems.

Internal gain-set resistors are provided for gains of 1, 10, 100, 200, and 500V/V. Inputs are protected for differential and common-mode voltages up to $\pm V_{CC}$. Its very high input impedance and low input bias current make the INA110 ideal for applications requiring input filters or input protection circuitry.

The INA110 is available in 16-pin plastic and ceramic DIPs, and in the SOL-16 surface-mount package. Military, industrial and commercial temperature range grades are available.



NOTE: (1) Connect to R_G for desired gain.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Input Voltage Range	$\pm V_{CC}$
Operating Temperature Range: G	–55°C to +125°C
P, U	–25°C to +85°C
Storage Temperature Range: G	–65°C to +150°C
P, U	–40°C to +85°C
Lead Temperature (soldering, 10s): G, P	+300°C
(soldering, 3s): U	+260°C
Output Short Circuit Duration	Continuous to Common

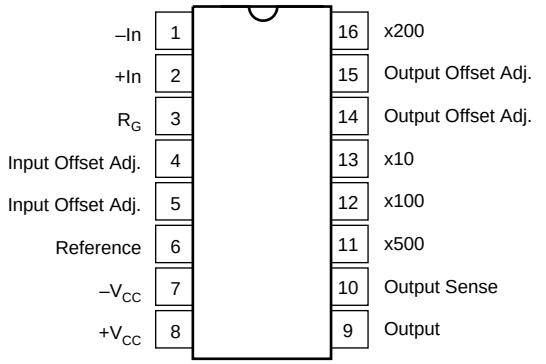
NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN CONFIGURATION

Top View **DIP/SOIC**



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

At +25°C, $\pm V_{CC}$ = 15VDC, and R_L = 2kΩ, unless otherwise specified.

PARAMETER	CONDITIONS	INA110AG			INA110BG, SG			INA110KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Range of Gain		1		800	*		*	*		*	V/V
Gain Equation[1]			*			G = 1 + [40k/(R_G + 50Ω)]			*		V/V
Gain Error, DC: G = 1			0.002	0.04		*	0.02		*	*	%
G = 10			0.01	0.1		0.005	0.05		*	*	%
G = 100			0.02	0.2		0.01	0.1		*	*	%
G = 200			0.04	0.4		0.02	0.2		*	*	%
G = 500			0.1	1		0.05	0.5		*	*	%
Gain Temp. Coefficient: G = 1			±3	±20		*	±10		*		ppm/°C
G = 10			±4	±20		±2	±10		*		ppm/°C
G = 100			±6	±40		±3	±20		*		ppm/°C
G = 200			±10	±60		±5	±30		*		ppm/°C
G = 500			±25	±100		±10	±50		*		ppm/°C
Nonlinearity, DC: G = 1			±0.001	±0.01		±0.0005	±0.005		*	*	% of FS
G = 10			±0.002	±0.01		±0.001	±0.005		*	*	% of FS
G = 100			±0.004	±0.02		±0.002	±0.01		*	*	% of FS
G = 200			±0.006	±0.02		±0.003	±0.01		*	*	% of FS
G = 500			±0.01	±0.04		±0.005	±0.02		*	*	% of FS
OUTPUT											
Voltage, R_L = 2kΩ	Over Temperature	±10	±12.7		*	*		*	*		V
Current	Over Temperature	±5	±25		*	*		*	*		mA
Short-Circuit Current			±25			*			*		mA
Capacitive Load	Stability		5000			*			*		pF
INPUT OFFSET VOLTAGE[2]											
Initial Offset: G, P			±(100 + 1000/G)	±(500 + 5000/G)		±(50 + 600/G)	±(250 + 3000/G)		*	*	µV
U									±(200 + 2000/G)	±(1000 + 5000/G)	µV
vs Temperature			±(2 + 20/G)	±(5 + 100/G)		±(1 + 10/G)	±(2 + 50/G)		*		µV/°C
vs Supply	V_{CC} = ±6V to ±18V		±(4 + 60/G)	±(30 + 300/G)		±(2 + 30/G)	±(10 + 180/G)		*	*	µV/V
BIAS CURRENT											
Initial Bias Current	Each Input		20	100		10	50		*	*	pA
Initial Offset Current			2	50		1	25		*	*	pA
Impedance: Differential			$5x10^{12}$||6			*			*		Ω || pF
Common-Mode			$2x10^{12}$||1			*			*		Ω || pF
VOLTAGE RANGE	V_{IN} Diff. = 0V[3]										
Range, Linear Response		±10	±12					*	*		V
CMR with 1kΩ Source Imbalance:											
G = 1	DC	70	90		80	100		*	*		dB
G = 10	DC	87	104		96	112		*	*		dB
G = 100	DC	100	110		106	116		*	*		dB
G = 200	DC	100	110		106	116		*	*		dB
G = 500	DC	100	110		106	116		*	*		dB
INPUT NOISE[4]											
Voltage, f_O = 10kHz			10			*			*		$nV/\sqrt{Hz}$
f_B = 0.1Hz to 10Hz			1			*			*		μV_{PP}
Current, f_O = 10kHz			1.8			*			*		$fA/\sqrt{Hz}$
OUTPUT NOISE[4]											
Voltage, f_O = 10kHz			65			*			*		$nV/\sqrt{Hz}$
f_B = 0.1Hz to 10Hz			8			*			*		μV_{PP}
DYNAMIC RESPONSE											
Small Signal: G = 1	–3dB		2.5			*			*		MHz
G = 10			2.5			*			*		MHz
G = 100			470			*			*		kHz
G = 200			240			*			*		kHz
G = 500			100			*			*		kHz
Full Power	V_{OUT} = ±10V,										
	G = 2 to 100	190	270		*	*			*	*	kHz
Slew Rate	G = 2 to 100	12	17		*	*			*	*	V/µs
Settling Time:											
0.1%, G = 1	V_O = 20V Step		4			*			*		µs
G = 10			2			*			*		µs
G = 100			3			*			*		µs
G = 200			5			*			*		µs
G = 500			11			*			*		µs

ELECTRICAL CHARACTERISTICS (Cont)

At +25°C, $\pm V_{CC}$ 15VDC, and R_L = 2KΩ, unless otherwise specified.

PARAMETER	CONDITIONS	INA110AG			INA110BG, SG			INA110KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC RESPONSE (CONT)											
Settling Time:											
0.01%,G = 1	V_O = 20V Step		5	12.5		*	*		*		µs
G = 10			3	7.5		*	*		*		µs
G = 100			4	7.5		*	*		*		µs
G = 200			7	12.5		*	*		*		µs
G = 500			16	25		*	*		*		µs
Recovery[5]	50% Overdrive		1			*			*		µs
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±6		±18	*		*	*		*	V
Quiescent Current	V_O = 0V		±3	±4.5		*	*		*	*	mA
TEMPERATURE RANGE											
Specification: P, U		–25		+85	*		*	0		+70	°C
G					–55		+125				°C
Operation		–55		+125	*		*	–25		+85	°C
Storage		–65		+150	*		*	–40		+85	°C
θ_{JA}			100			*			*		°C/W

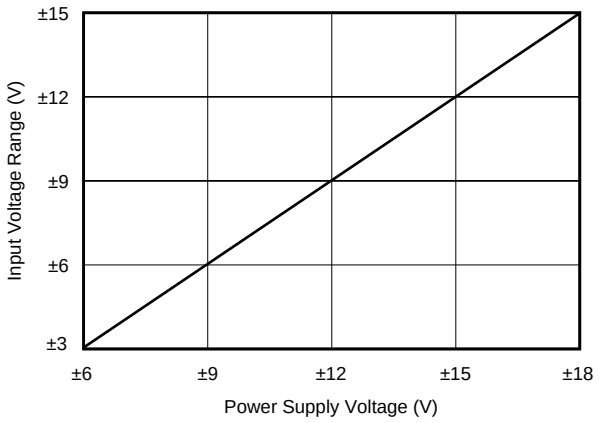
* Same as INA110AG.

NOTES: (1) Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, R_G, between pin 3 and pins 11, 12 and 16. Gain accuracy is a function of R_G and the internal resistors which have a ±20% tolerance with 20ppm/°C drift. (2) Adjustable to zero. (3) For differential input voltage other than zero, see Typical Characteristics. (4) $V_{NOISE\,RTI} = \sqrt{V_{N\,INPUT}^2 + (V_{N\,OUTPUT}/Gain)^2}$. (5) Time required for output to return from saturation to linear operation following the removal of an input overdrive voltage.

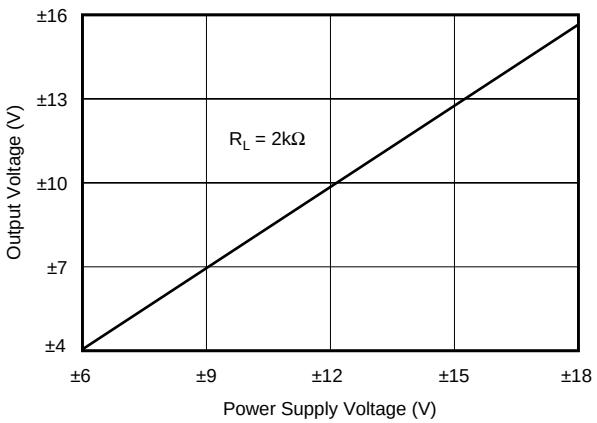
TYPICAL CHARACTERISTICS

At T_A = +25°C and $\pm V_{CC}$ = 15VDC, unless otherwise noted.

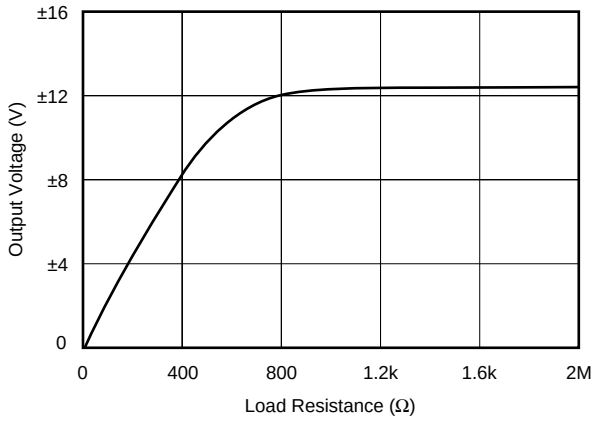
INPUT VOLTAGE RANGE vs SUPPLY



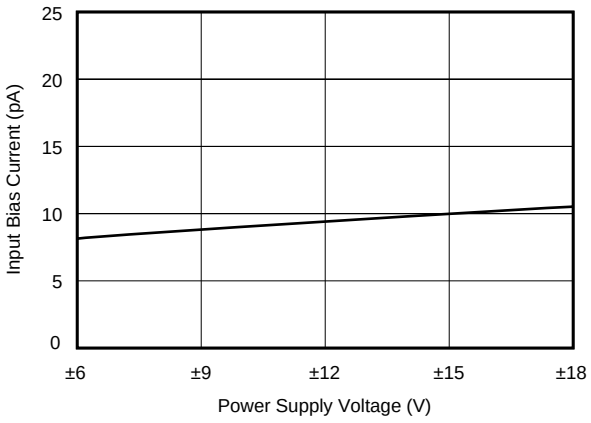
OUTPUT SWING vs SUPPLY



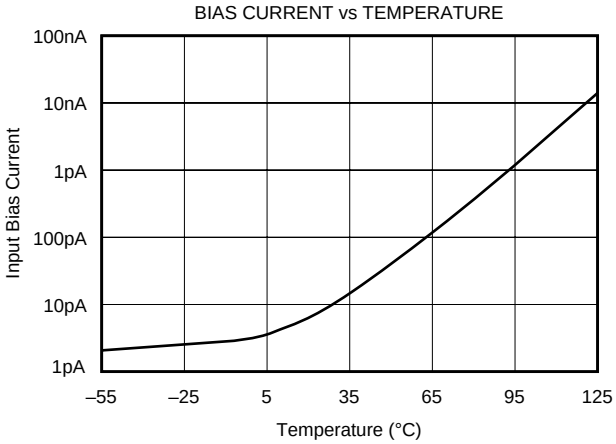
OUTPUT SWING vs LOAD RESISTANCE



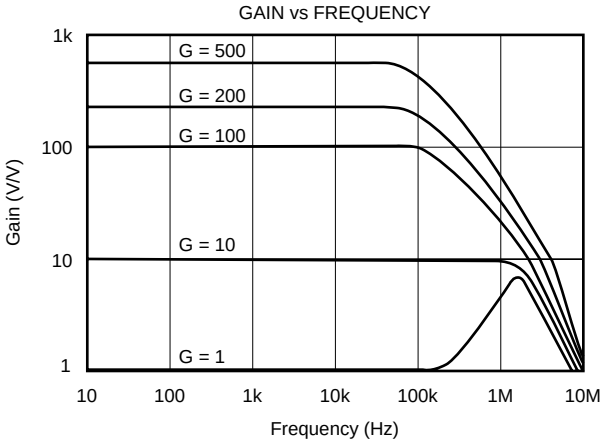
BIAS CURRENT vs SUPPLY



BIAS CURRENT vs TEMPERATURE



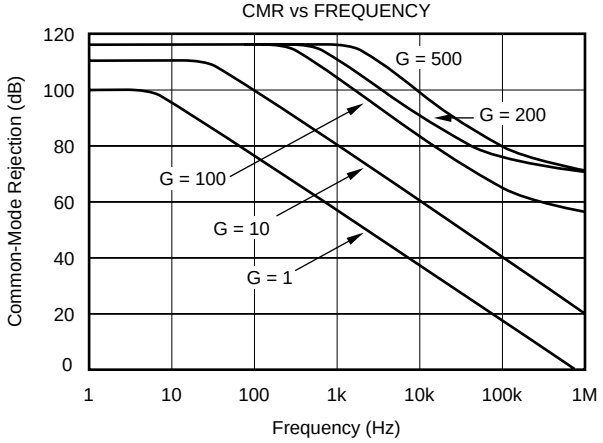
GAIN vs FREQUENCY



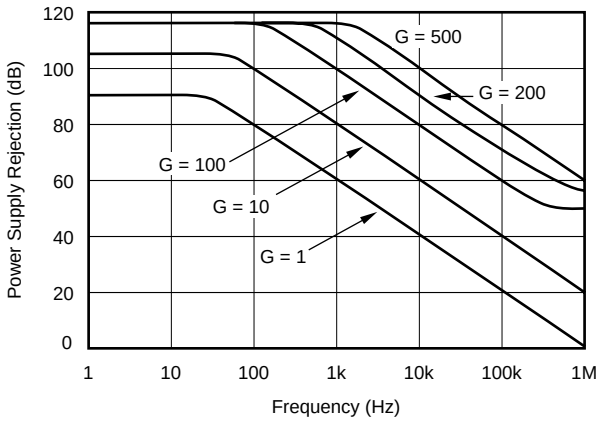
TYPICAL CHARACTERISTICS (Cont)

At T_A = +25°C and $\pm V_{CC}$ = 15VDC, unless otherwise noted.

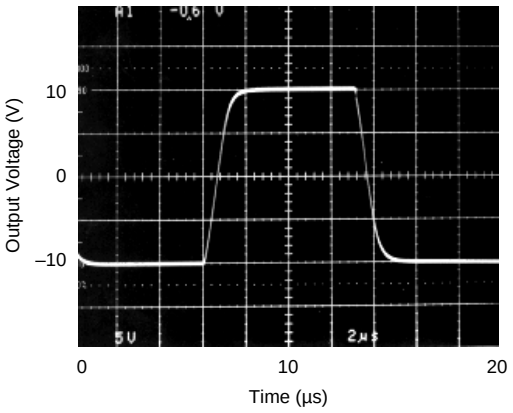
CMR vs FREQUENCY



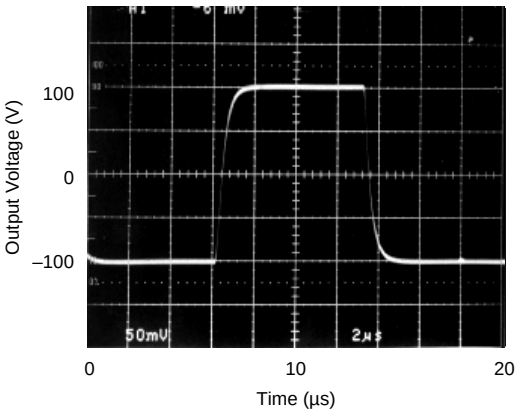
POWER SUPPLY REJECTION vs FREQUENCY



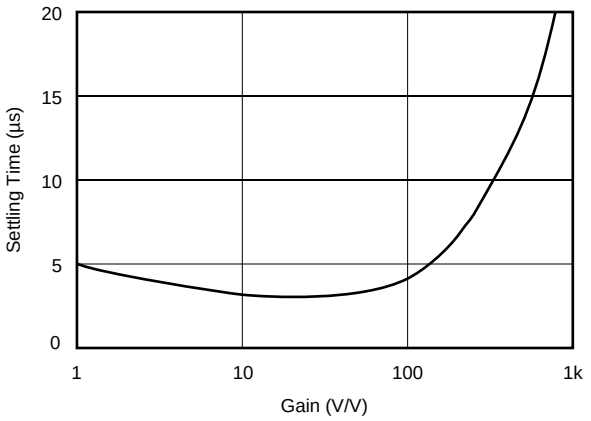
LARGE SIGNAL TRANSIENT RESPONSE
(G = 100)



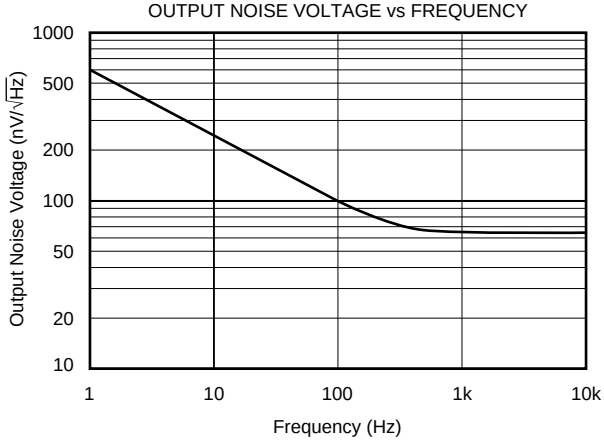
SMALL SIGNAL TRANSIENT RESPONSE
(G = 100)



SETTLING TIME vs GAIN
(0.01%, 20V Step)



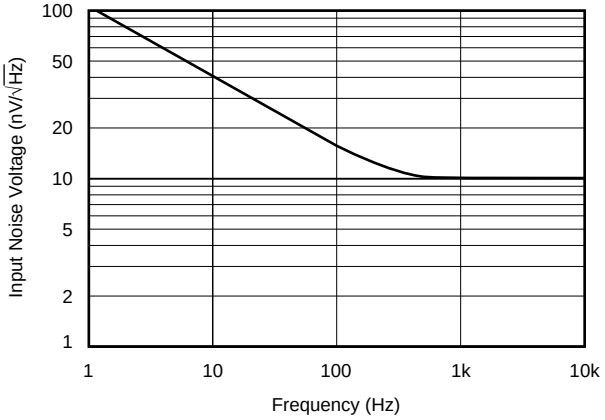
OUTPUT NOISE VOLTAGE vs FREQUENCY



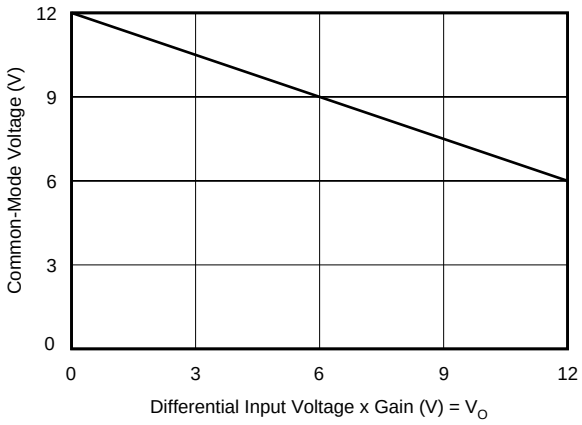
TYPICAL CHARACTERISTICS (Cont)

At T_A = +25°C and $\pm V_{CC}$ = 15VDC, unless otherwise noted.

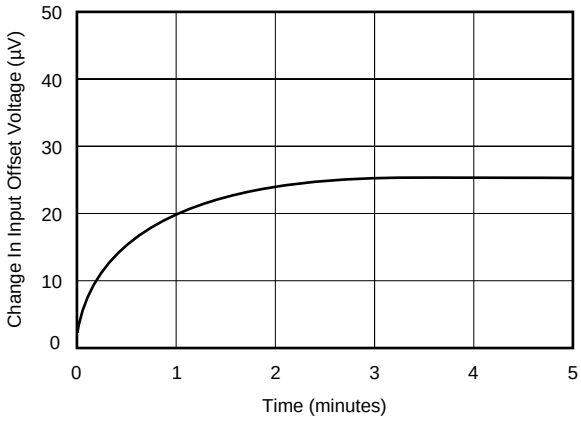
INPUT NOISE VOLTAGE vs FREQUENCY



COMMON-MODE VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE



WARM-UP DRIFT vs TIME



DISCUSSION OF PERFORMANCE

A simplified diagram of the INA110 is shown on the first page. The design consists of the classical three operational amplifier configuration using current-feedback type op amps with precision FET buffers on the input. The result is an instrumentation amplifier with premium performance not normally found in integrated circuits.

The input section (A_1 and A_2) incorporates high performance, low bias current, and low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide high input impedance ($10^{12}\Omega$). Laser-trimming is used to achieve low offset voltage. Input cascoding assures low bias current and high CMR. Thin-film resistors on the integrated circuit provide excellent gain accuracy and temperature stability.

The output section (A_3) is connected in a unity-gain difference amplifier configuration. Precision matching of the four 10kΩ resistors, especially over temperature and time, assures high common-mode rejection.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Supplies should be decoupled with 1µF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. Resistance in series with the reference (pin 6) will degrade CMR. To maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins.

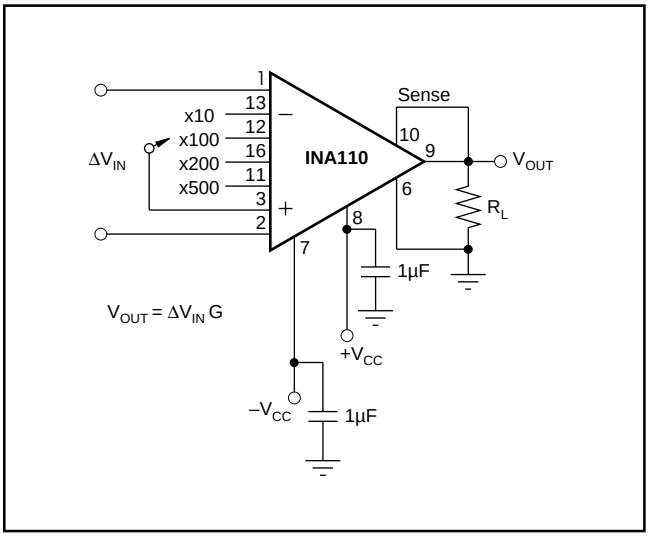


FIGURE 1. Basic Circuit Connection.

OFFSET ADJUSTMENT

Figure 2 shows the offset adjustment circuit for the INA110. Both the offset of the input stage and output stage can be adjusted separately. Notice that the offset referred to the INA110's input (RTI) is the offset of the input stage plus the offset of the output stage divided by the gain of the input stage. This allows specification of offset independent of gain.

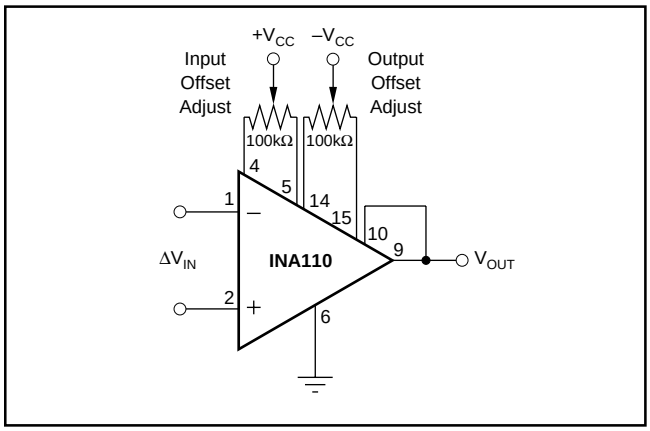


FIGURE 2. Offset Adjustment Circuit.

For systems using computer autozeroing techniques, neither offset nor offset drift are of concern. In many other applications, the factory-trimmed offset gives excellent results. When greater accuracy is desired, one adjustment is usually sufficient. In high gains (>100) adjust only the input offset, and in low gains the output offset. For higher precision in all gains, both can be adjusted by first selecting high gain and adjusting input offset and then low gain and adjusting output offset. The offset adjustment will, however, add to the drift by approximately 0.33µV/°C per 100µV of input offset voltage that is adjusted. Therefore, care should be taken when considering use of adjustment.

Output offsetting can be accomplished as shown in Figure 3 by applying a voltage to the reference (pin 6) through a buffer. This limits the resistance in series with pin 6 to minimize CMR error. Be certain to keep this resistance low. Note that the offset error can be adjusted at this reference point with no appreciable degradation in offset drift.

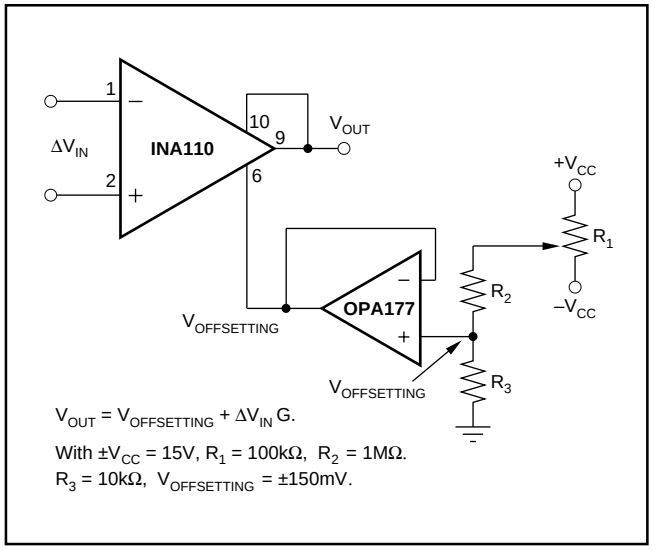


FIGURE 3. Output Offsetting.

GAIN SELECTION

Gain selection is accomplished by connecting the appropriate pins together on the INA110. Table I shows possible gains from the internal resistors. Keep the connections as short as possible to maintain accuracy.

GAIN	CONNECT PIN 3 TO PIN	GAIN ACCURACY (%)	GAIN DRIFT (ppm/°C)
The following gains have assured accuracy:			
1	none	0.02	10
10	13	0.05	10
100	12	0.1	20
200	16	0.2	30
500	11	0.5	50
The following gains have typical accuracy as shown:			
300	12, 16	0.25	10
600	11, 12	0.25	40
700	11, 16	2	40
800	11, 12, 16	2	80

TABLE I. Internal Gain Connections.

Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, R_G, between pin 3 and pins 12, 16, and 11. Gain accuracy is a function of R_G and the internal resistors which have a ±20% tolerance with 20ppm/°C drift. The equation for choosing R_G is shown below.

$$R_G = \frac{40k\Omega}{G - 1} - 50\Omega$$

Gain can also be changed in the output stage by adding resistance to the feedback loop shown in Figure 4. This is useful for increasing the total gain or reducing the input stage gain to prevent saturation of input amplifiers.

The output gain can be changed as shown in Table II. Matching of R_1 and R_3 is required to maintain high CMR. R_2 sets the gain with no effect on CMR.

OUTPUT STAGE GAIN	R_1 AND R_3	R_2
2	1.2kΩ	2.74kΩ
5	1kΩ	511Ω
10	1.5kΩ	340Ω

TABLE II. Output Stage Gain Control.

COMMON-MODE INPUT RANGE

It is important not to exceed the input amplifiers' dynamic range (see Typical Characteristics). The differential input signal and its associated common-mode voltage should not cause the output of A_1 and A_2 (input amplifiers) to exceed approximately ±10V with ±15V supplies or nonlinear operation will result. Such large common-mode voltages, when the INA110 is in high gain, can cause saturation of the input stage even though the differential input is very small. This can be avoided by reducing the input stage gain and increasing the output stage gain with an H pad attenuator (see Figure 4).

OUTPUT SENSE

An output sense has been provided to allow greater accuracy in connecting the load. By attaching this feedback point to the load at the load site, IR drops due to load currents that are eliminated since they are inside the feedback loop. Proper connection is shown in Figure 1. When more current is to be supplied, a power booster can be placed within the feedback loop as shown in Figure 5. Buffer errors are minimized by the loop gain of the output amplifier.

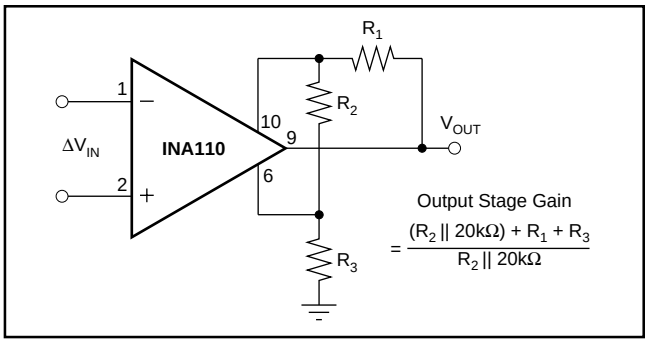


FIGURE 4. Gain Adjustment of Output Stage Using H Pad Attenuator.

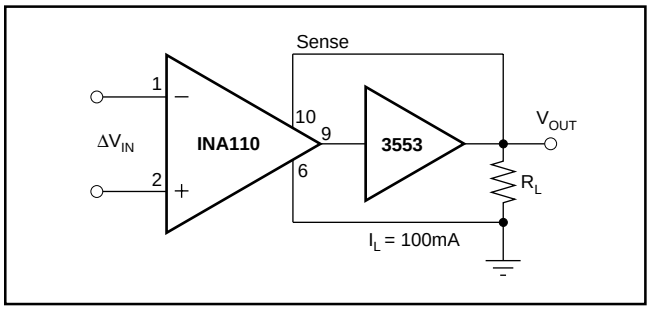


FIGURE 5. Current Boosting the Output.

LOW BIAS CURRENT OF FET INPUT ELIMINATES DC ERRORS

Because the INA110 has FET inputs, bias currents drawn through input source resistors have a negligible effect on DC accuracy. The picoamp levels produce no more than microvolts through megohm sources. Thus, input filtering and input series protection are readily achievable.

A return path for the input bias currents must always be provided to prevent charging of stray capacitance. Otherwise, the output can wander and saturate. A 1MΩ to 10MΩ resistor from the input to common will return floating sources such as transformers, thermocouples, and AC-coupled inputs (see Applications section).

DYNAMIC PERFORMANCE

The INA110 is a fast-settling FET input instrumentation amplifier. Therefore, careful attention to minimize stray capacitance is necessary to achieve specified performance. High source resistance will interact with input capacitance to reduce the overall bandwidth. Also, to maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins.

Applications with balanced-source impedance will provide the best performance. In some applications, mismatched source impedances may be required. If the impedance in the

negative input exceeds that in the positive input, stray capacitance from the output will create a net negative feedback and improve the circuit stability. If the impedance in the positive input is greater, the feedback due to stray capacitance will be positive and instability may result. The degree of positive feedback depends upon source impedance imbalance, operating gain, and board layout. The addition of a small bypass capacitor of 5pF to 50pF directly between the inputs of the IA will generally eliminate any positive feedback. CMR errors due to the input impedance mismatch will also be reduced by the capacitor.

The INA110 is designed for fast settling with easy gain selection. It has especially excellent settling in high gain. It can also be used in fast-settling unity-gain applications. As with all such amplifiers, the INA110 does exhibit significant gain peaking when set to a gain of 1. It is, however, unconditionally stable. The gain peaking can be cancelled by band-limiting the negative input to 400kHz with a simple external RC circuit for applications requiring flat response. CMR is not affected by the addition of the 400kHz RC in a gain of 1.

Another distinct advantage of the INA110 is the high frequency CMR response. High frequency noise and sharp common-mode transients will be rejected. To preserve AC CMR, be sure to minimize stray capacitance on the input lines. Matching the RCs in the two inputs will help to maintain high AC CMR.

APPLICATIONS

In addition to general purpose uses, the INA110 is designed to accurately handle two important and demanding applications: (1) inputs with high source impedances such as capacitance/crystal/photodetector sensors and low-pass filters and series-input protection devices, and (2) rapid-scanning data acquisition systems requiring fast settling time. Because the user has access to the output sense, current sources can also be constructed using a minimum of external components. Figures 6 through 19 show application circuits.

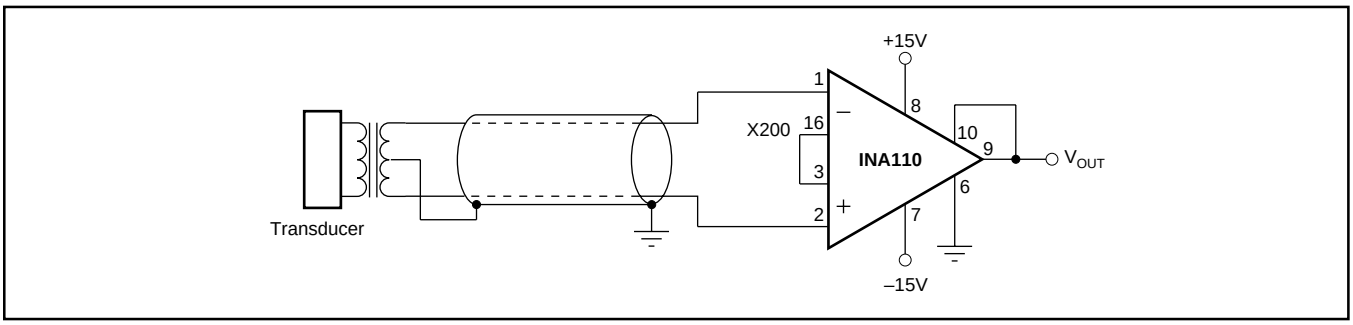


FIGURE 6. Transformer-Coupled Amplifier.

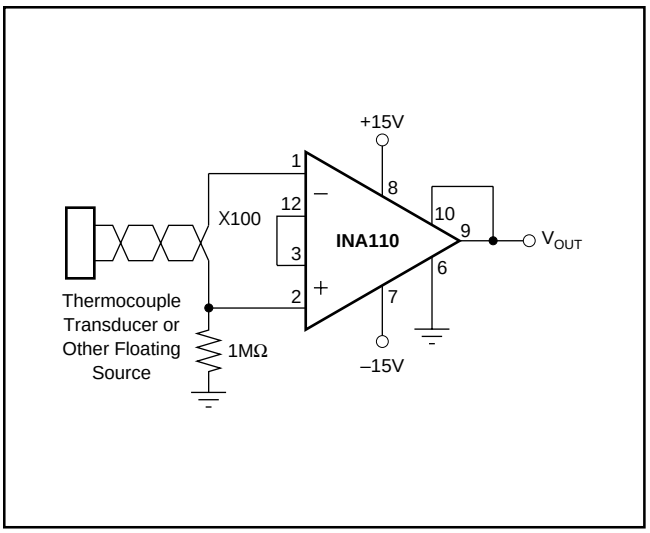


FIGURE 7. Floating Source Instrumentation Amplifier.

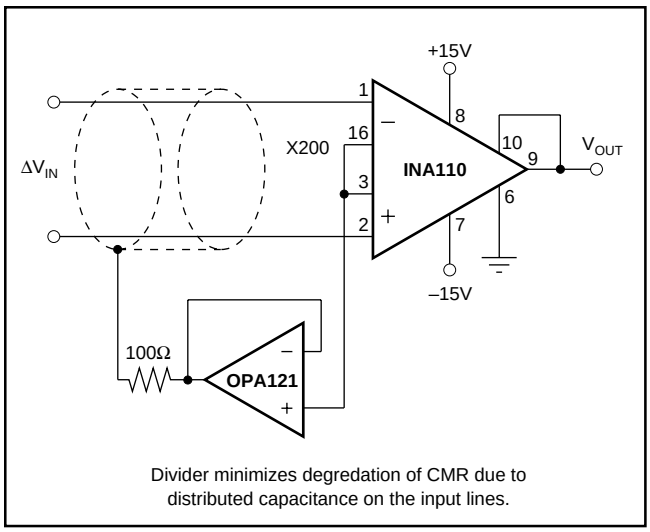


FIGURE 8. Instrumentation Amplifier with Shield Driver.

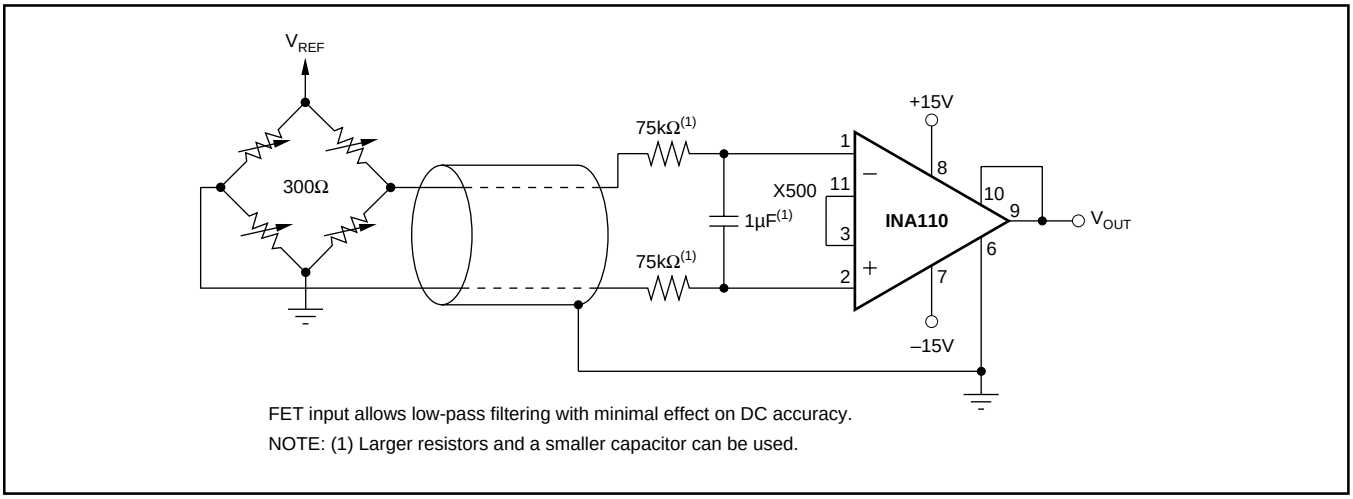


FIGURE 9. Bridge Amplifier with 1Hz Low-Pass Input Filter.

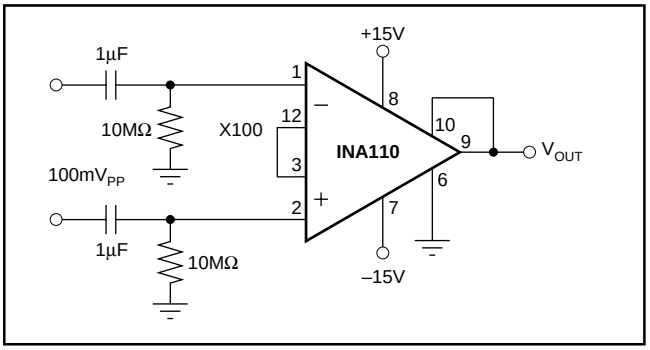


FIGURE 10. AC-Coupled Differential Amplifier for Frequencies Greater Than 0.016Hz.

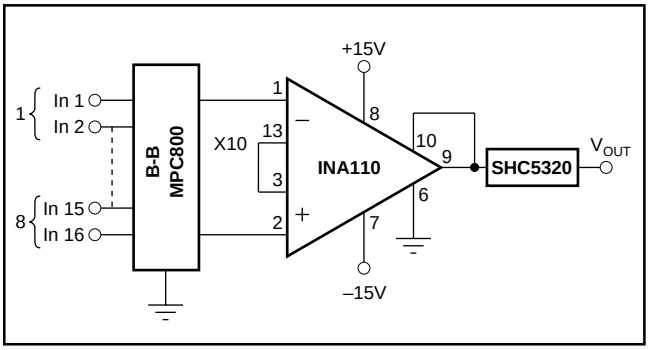


FIGURE 12. Rapid-Scanning-Rate Data Acquisition Channel with 5μs Settling to 0.01%.

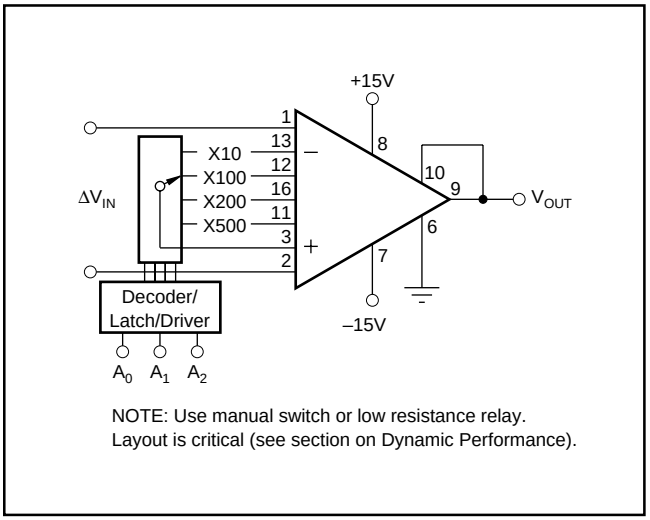


FIGURE 11. Programmable-Gain Instrumentation Amplifier (Precision Noninverting or Inverting Buffer with Gain).

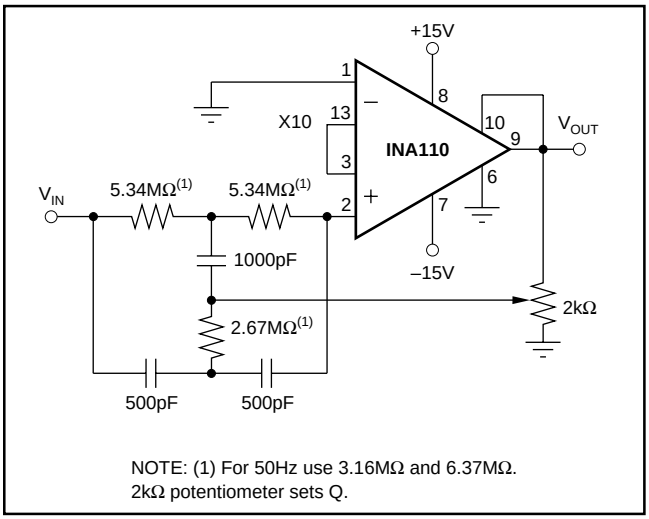


FIGURE 13. 60Hz Input Notch Filter.

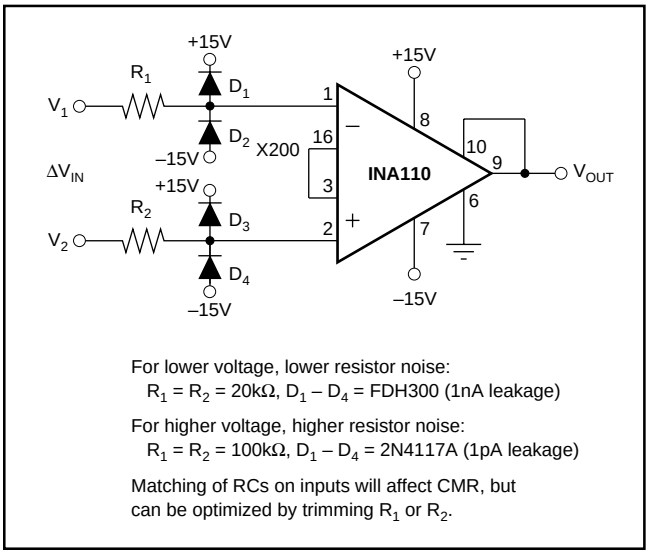


FIGURE 14. Input-Protected Instrumentation Amplifier.

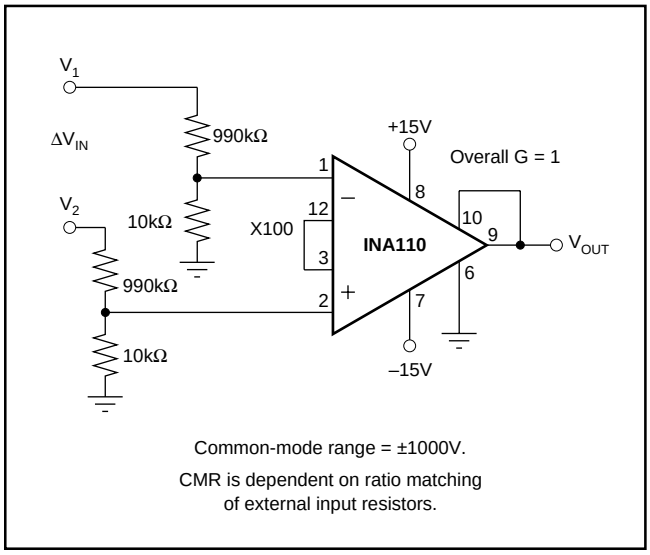
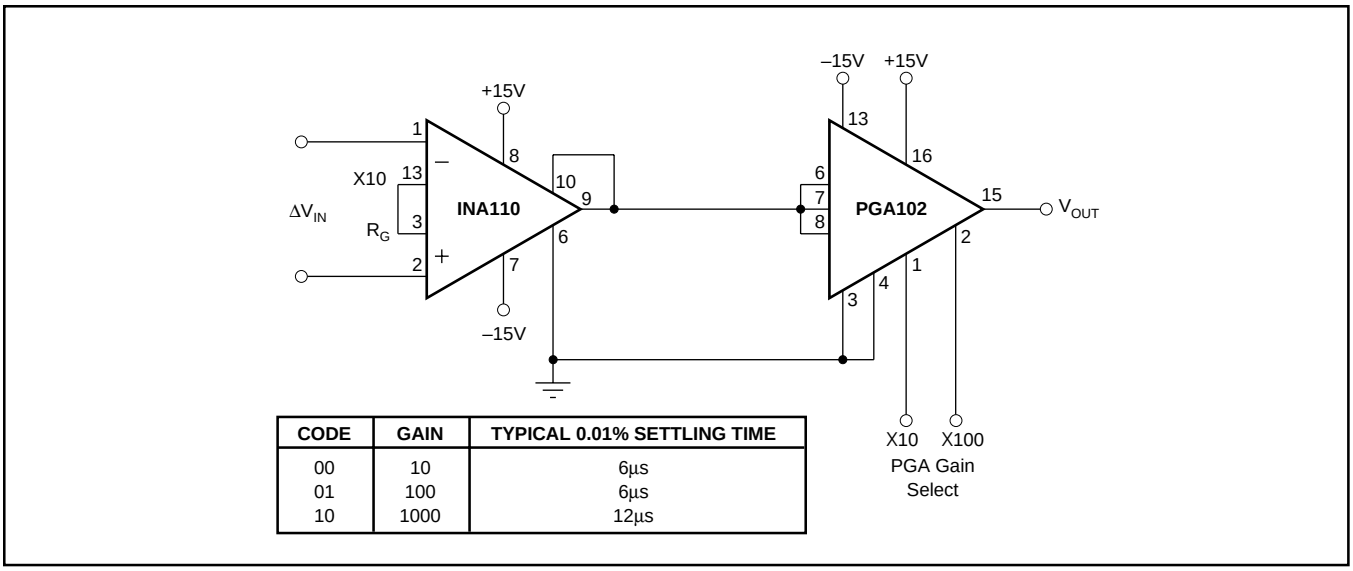


FIGURE 15. High Common-Mode Voltage Differential Amplifier.



CODE	GAIN	TYPICAL 0.01% SETTLING TIME
00	10	6µs
01	100	6µs
10	1000	12µs

FIGURE 16. Digitally-Controlled Fast-Settling Programmable Gain Instrumentation Amplifier.

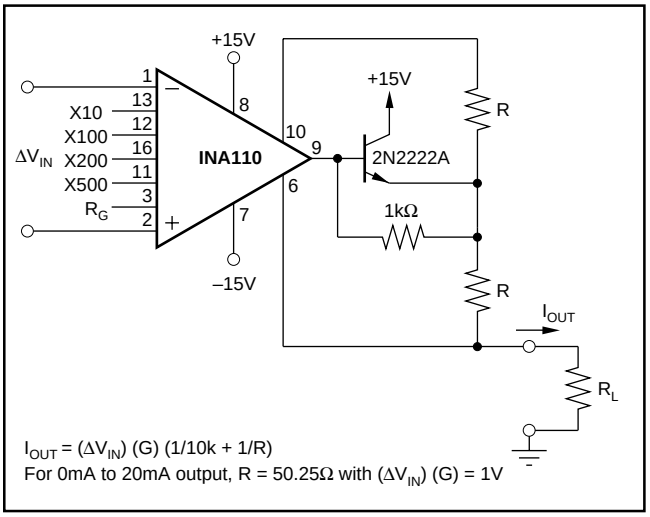


FIGURE 17. Differential Input FET Buffered Current Source.

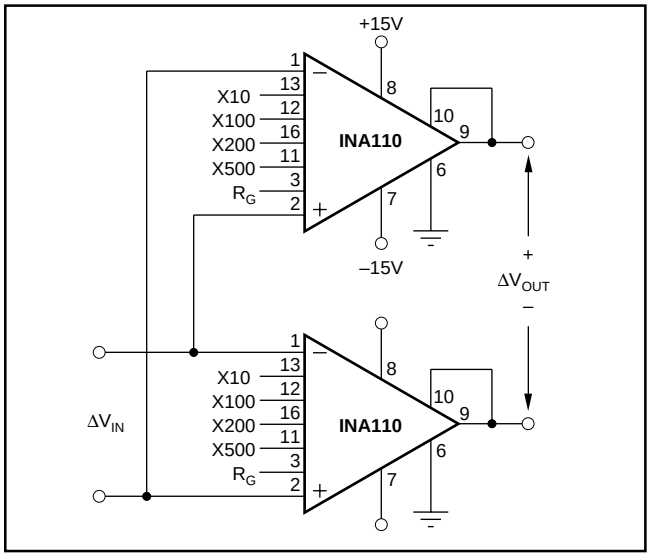


FIGURE 18. Differential Input/Differential Output Amplifier.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA110KP	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	INA110KP	Samples
INA110KU	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR		INA110KU	Samples
INA110KUG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR		INA110KU	Samples
INA110SG	NRND	CDIP SB	JD	16	1	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type		INA110SG	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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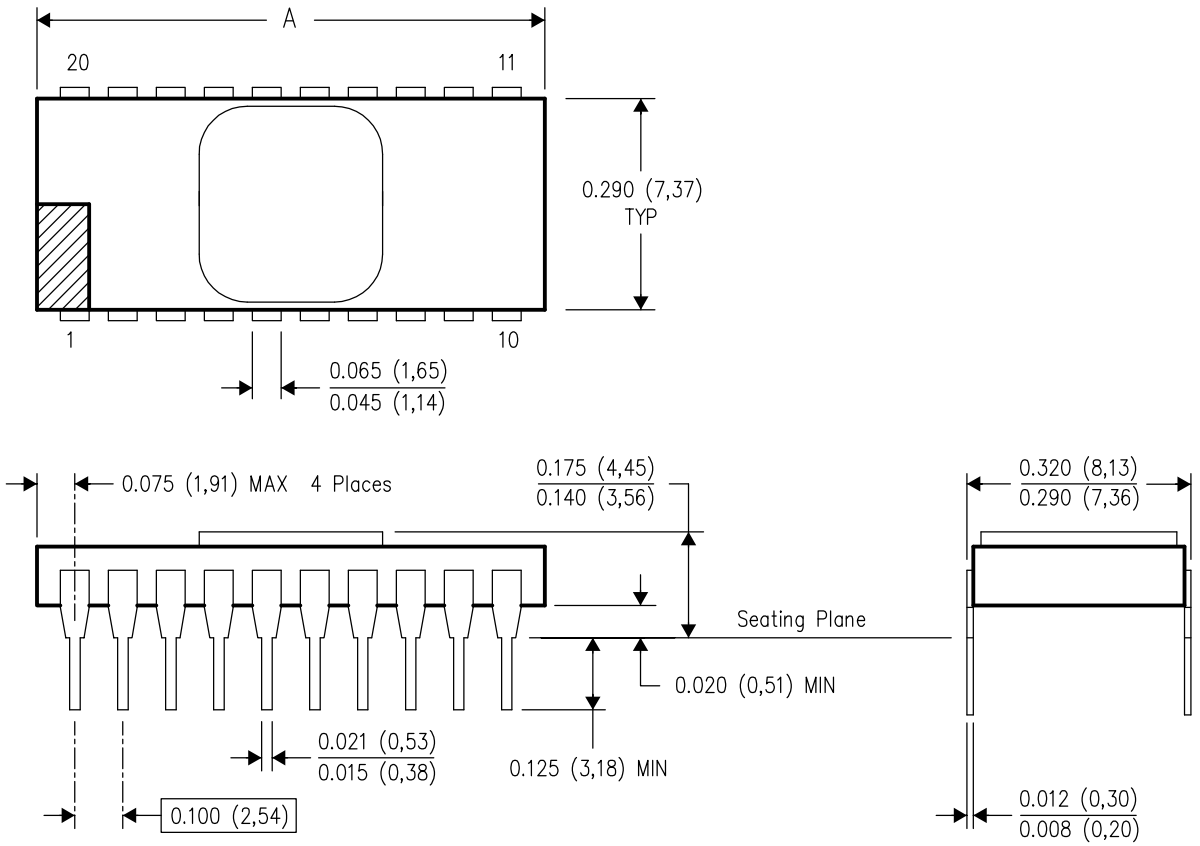
JD (R–CDIP–T**) CERAMIC SIDE–BRAZE DUAL–IN–LINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	8	14	16	18	20	24
A MAX	0.405 (10,29)	0.757 (19,23)	0.810 (20,57)	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

4040086–2/F 07/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

GENERIC PACKAGE VIEW

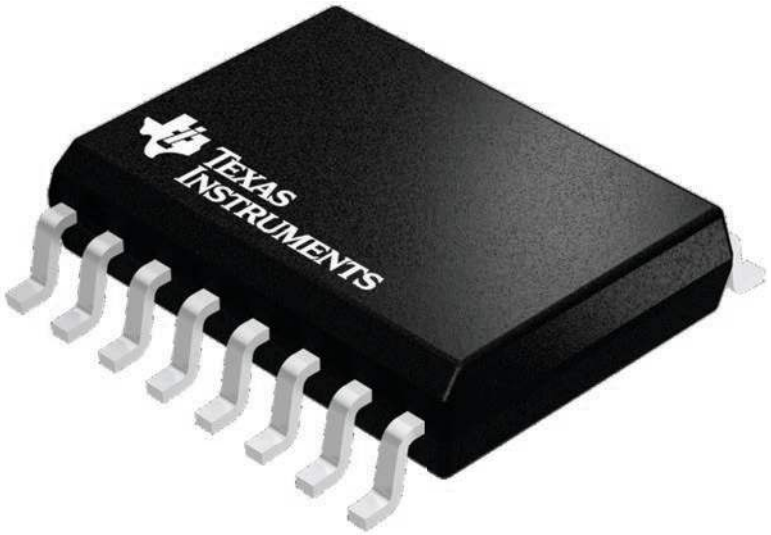
DW 16

SOIC - 2.65 mm max height

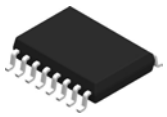
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

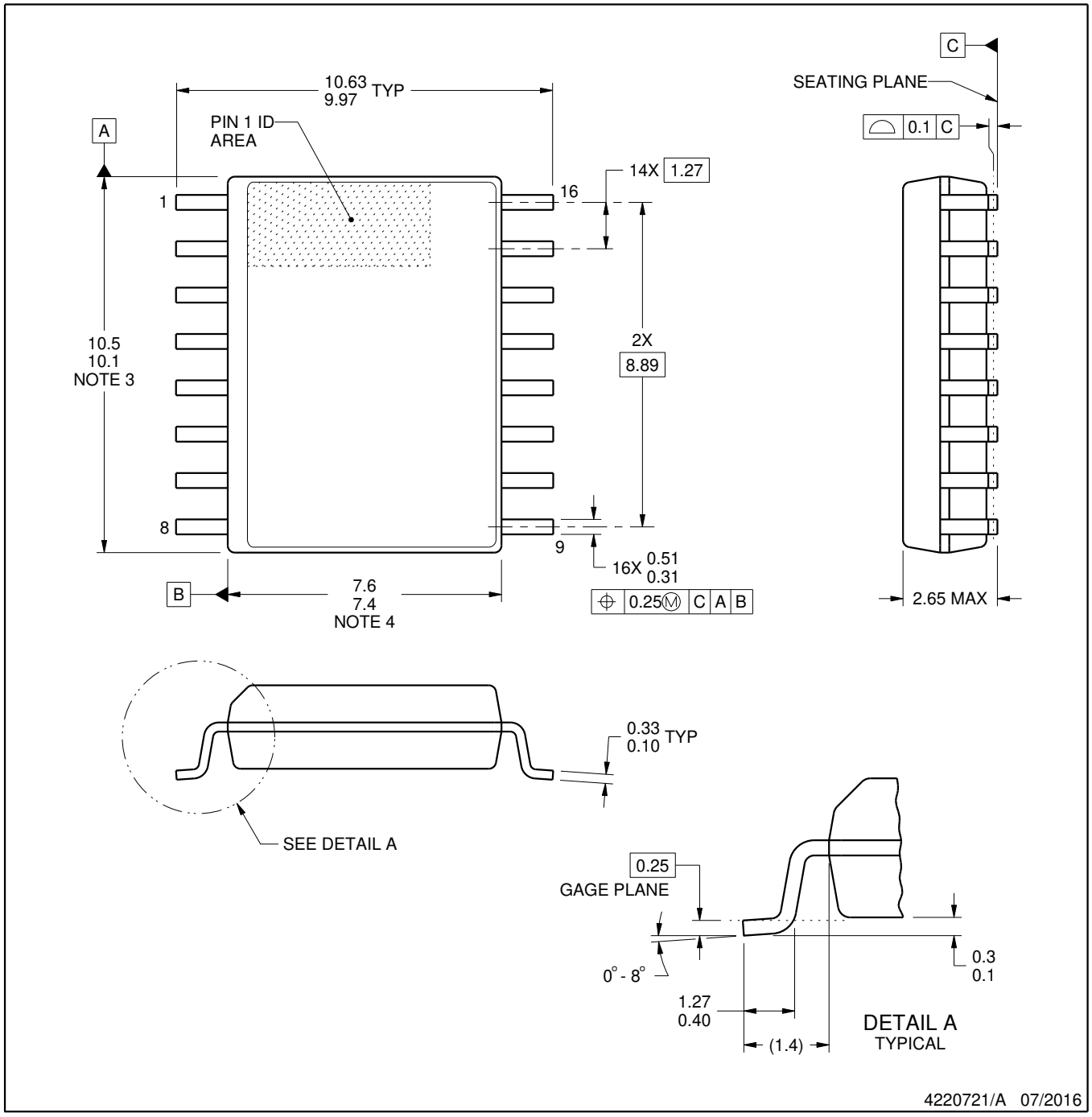


PACKAGE OUTLINE

DW0016A

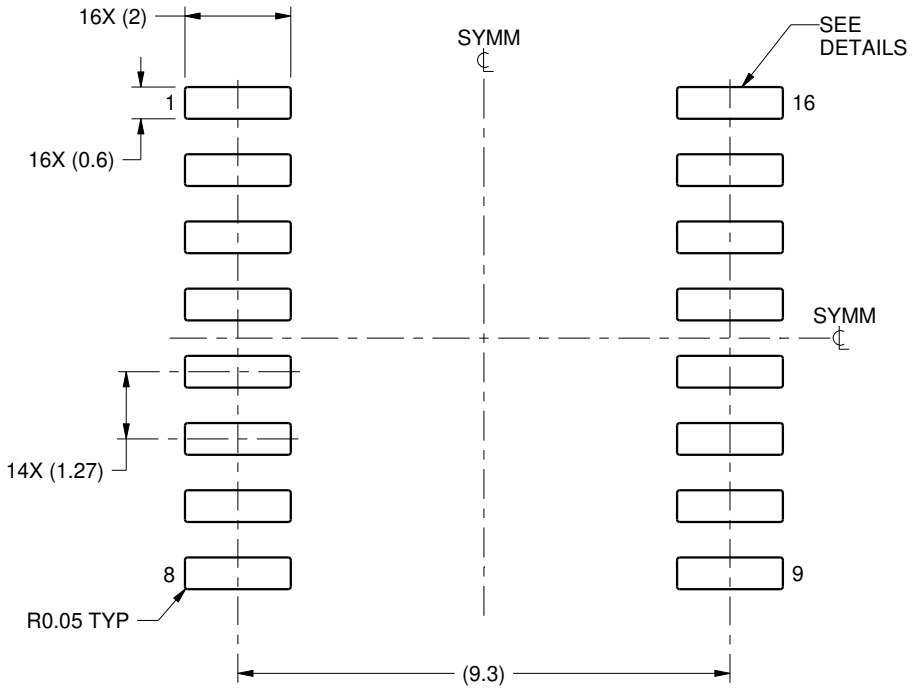
SOIC - 2.65 mm max height

SOIC

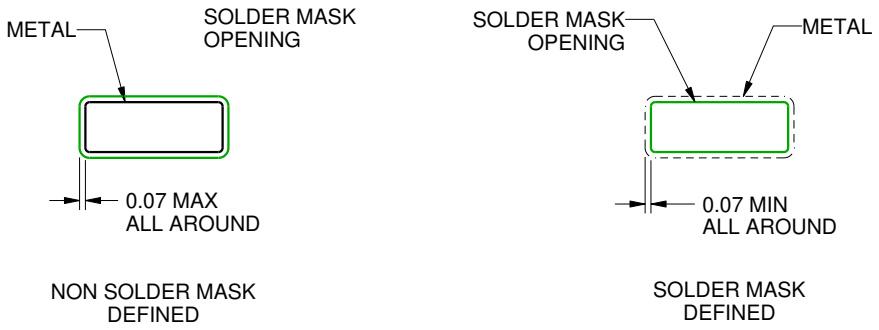


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

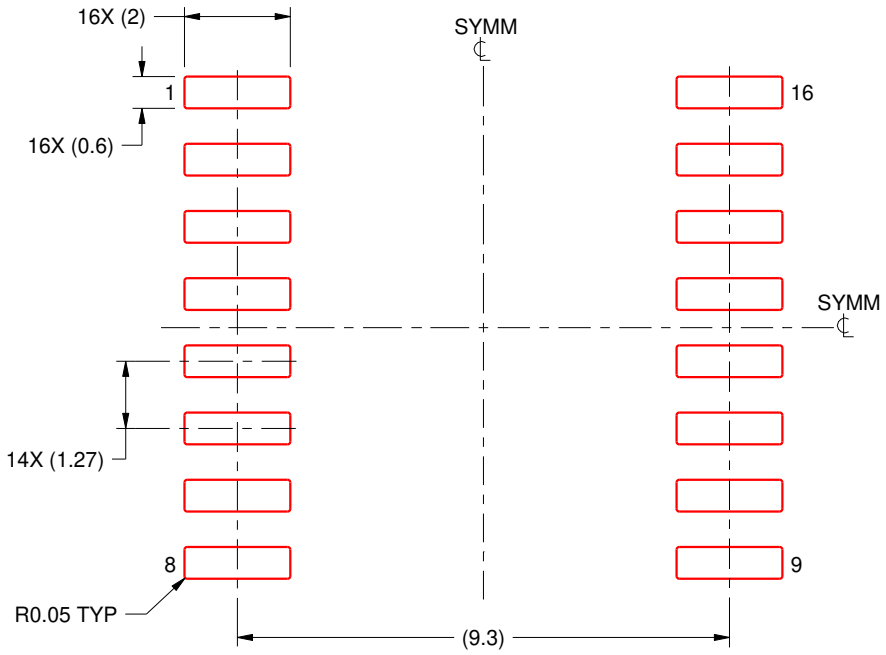


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

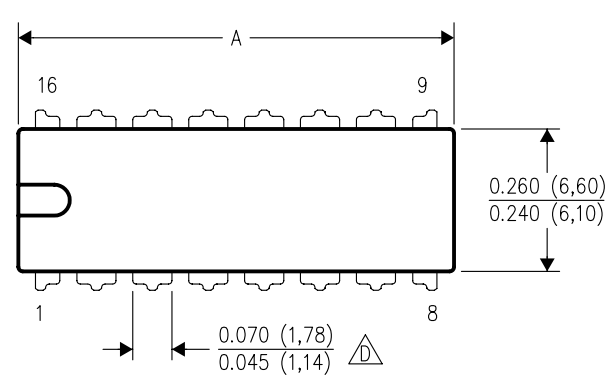
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

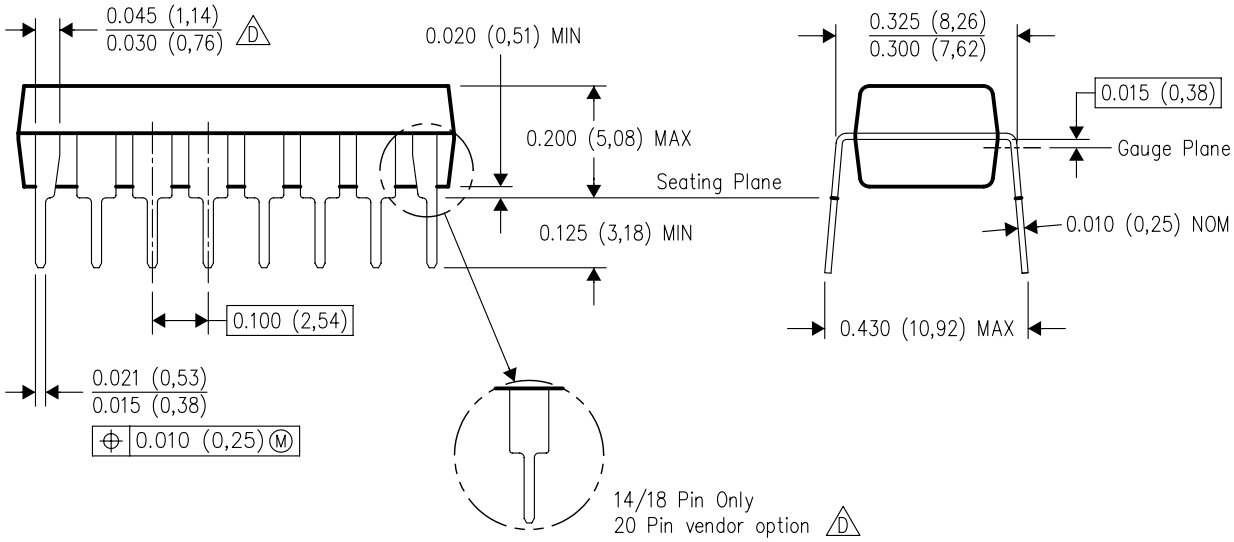
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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