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		30A3702D - 3L1	
•	Qualified for Automotive Applications Operates From 1.65 V to 3.6 V		V PACKAGE P VIEW)
•	Inputs Accept Voltages to 5.5 V	1G 🛛 1	
•	Max t _{pd} of 6.2 ns	1A 🛛 2	15 2 2 G
•	Typical V _{OLP} (Output Ground Bounce) <0.8 V at V _{CC} = 3.3 V, T _A = 25°C	1B [] 3 1Y0 [] 4	14] 2A 13] 2B
•	Typical V _{OHV} (Output V _{OH} Undershoot) >2 V at V _{CC} = 3.3 V, T _A = 25°C	1Y1 []5 1Y2 []6	12 2Y0 11 2Y1
•	Latch-Up Performance Exceeds 250 mA Per JESD 17	1Y3 [7 GND [8	10 2Y2 9 2Y3
•	ESD Protection Level Per AEC-Q100		

- Classification
 - 2000-V (H2) Human-Body Model
 - 200-V (M3) Machine Model
 - 1000-V (C5) Charged-Device Model

description/ordering information

This dual 2-line to 4-line decoder/demultiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

The device comprises two individual 2-line to 4-line decoders in a single package. The active-low enable (\overline{G}) input can be used as a data line in demultiplexing applications. This decoder/demultiplexer features fully buffered inputs, each of which represents only one normalized load to its driving circuit.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION[†]

T _A	PACK	AGE‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Reel of 2500	SN74LVC139AQDRQ1	LVC139AQ
-40 C to 125°C	TSSOP – PW	Reel of 2000	SN74LVC139AQPWRQ1	LC139AQ

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

FUNCTION TABLE

[‡] Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

	(each decoder/demultiplexer)												
	INPUTS		OUTPUTS										
G	SEL	ECT		001	-015								
G	в	Α	Y3	Y2	Y1	Y0							
L	LL		Н	Н	Н	L							
L	L	н	Н	н	L	Н							
L	н	L	н	L	Н	н							
L	н н		L	Н	н	Н							
н	х			Н	Н	Н							



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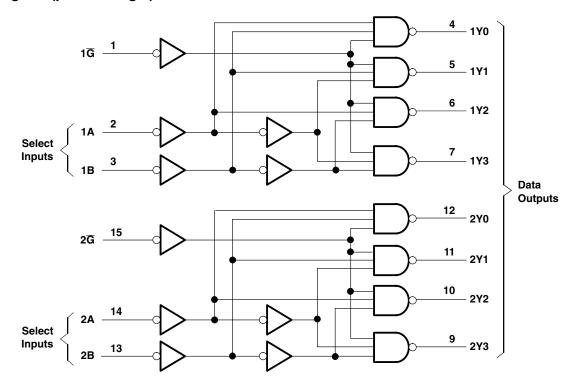
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	–0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V _O (see Notes 1 and 2)	\dots –0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, I _O	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
(see Note 3): PW package	108°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The value of V_{CC} is provided in the recommended operating conditions table.

3. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 4)

			MIN	МАХ	UNIT
.,		Operating	1.65	3.6	
V _{CC}	Supply voltage	Data retention only	1.5		V
		V _{CC} = 1.65 V to 1.95 V	$0.65 imes V_{CC}$		
ViH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
V _{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-4	
		$V_{CC} = 2.3 V$		-8	
I _{ОН}	High-level output current	$V_{CC} = 2.7 V$		-12	mA
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ $V_{CC} = 2.3 \text{ V}$ $V_{CC} = 2.3 \text{ V}$ $V_{CC} = 2.3 \text{ V}$ $V_{CC} = 2.7 \text{ V}$ $V_{CC} = 3 \text{ V}$ $V_{CC} = 1.65 \text{ V}$ $V_{CC} = 2.7 \text{ V}$ $V_{CC} = 3 \text{ V}$ $V_{CC} = 2.3 \text{ V}$		-24	
		V _{CC} = 1.65 V		4	
	Level events a summer t	$V_{CC} = 2.3 V$		8	
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12	mA
		$V_{CC} = 3 V$		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	125	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				$T_{A} = -40^{\circ}$	°C TO 12	5°C	T _A = -40	°C TO 8	5°C		
PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	MIN	TYP†	MAX	UNIT	
		I _{OH} = −100 μA	1.65 V to 3.6 V	V _{CC} – 0.2			V _{CC} – 0.2				
		I _{OH} = -4 mA	1.65 V	1.2			1.2				
		I _{OH} = -8 mA	2.3 V	1.7			1.7				
V _{OH}		1 10 A	2.7 V	2.1			2.2			V	
		I _{OH} = -12 mA	3 V	2.3			2.4				
		I _{OH} = -24 mA	3 V	2.1			2.2				
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2			0.2	0.2	
		I _{OL} = 4 mA	1.65 V			0.45			0.45		
VOL		I _{OL} = 8 mA	2.3 V			0.7			0.7	V	
		I _{OL} = 12 mA	2.7 V			0.4			0.4		
		I _{OL} = 24 mA	3 V			0.55			0.55		
l _l	All inputs	V _I = 5.5 V or GND	3.6 V			±5			±5	μA	
I _{CC}		$V_{I} = V_{CC} \text{ or GND}, I_{O} = 0$	3.6 V			10			10	μA	
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.7 V to 3.6 V			500			500	μA	
Ci		V _I = V _{CC} or GND	3.3 V		5			5		pF	

 † All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} =	2.7 V	V _{CC} = ± 0.3	UNIT	
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	
	A or B	X	1	8.8	1	7.7	
t _{pd}	G	Y	1	6.7	1	6.2	ns
t _{sk(o)}						1	ns

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST	V _{CC} = 1.8 V	V_{CC} = 2.5 V	V _{CC} = 3.3 V	LINUT	
		CONDITIONS	ТҮР	TYP	ТҮР	UNIT	
Cp	Power dissipation capacitance	f = 10 MHz	28.5	29.5	30.5	pF	



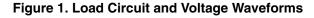
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O VLOAD **S1** RL O Open From Output TEST S1 **Under Test** O GND Open t_{PLH}/t_{PHL} CL ≶ \mathbf{R}_{L} t_{PLZ}/t_{PZL} V_{LOAD} (see Note A) GND t_{PHZ}/t_{PZH} LOAD CIRCUIT INPUTS RL \mathbf{V}_{Δ} Vcc Vм VLOAD C_L ٧ı t_r/t_f 2.7 V 2.7 V ≤2.5 ns 1.5 V 6 V 50 pF **500** Ω 0.3 V 3.3 V \pm 0.3 V 2.7 V ≤2.5 ns 1.5 V 6 V 50 pF **500** Ω 0.3 V VI **Timing Input** Vм 0 V t_{su} t_h V ٧ı Vм V_M Input Data Input Vм Vм 0 V 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PULSE DURATION SETUP AND HOLD TIMES VI Vı Output Vм Vм Input Vм Vм Control 0 V 0 V t_{PLH} t_{PHL} t_{PZL} t_{PLZ} Output VOH V_{LOAD}/2 Waveform 1 Vм Output Vм S1 at V_{LOAD} $V_{OL} + V_{\Delta}$ VoL (see Note B) VoL t_{PHL} t_{PLH} t_{р7н} t_{PHZ} Output V_{OH} VOH Waveform 2 Vм $V_{OH} - V_{\Delta}$ Vм Output Vм S1 at GND VOL ≈0 V (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES ENABLE AND DISABLE TIMES** INVERTING AND NONINVERTING OUTPUTS LOW- AND HIGH-LEVEL ENABLING

PARAMETER MEASUREMENT INFORMATION

NOTES: A. Cl includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.







10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLVC139AQPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC139AQ	Samples
SN74LVC139AQPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC139AQ	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

10-Dec-2020

OTHER QUALIFIED VERSIONS OF SN74LVC139A-Q1 :

• Catalog: SN74LVC139A

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

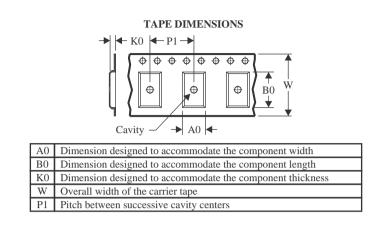


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STRUMENTS

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



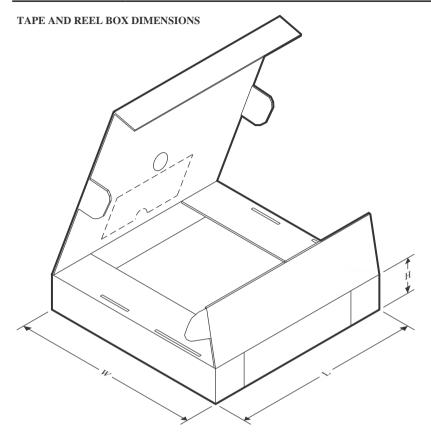
*All dimensions are nominal												
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVC139AQPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC139AQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



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PACKAGE MATERIALS INFORMATION

3-Jun-2022



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVC139AQPWRG4Q1	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LVC139AQPWRQ1	TSSOP	PW	16	2000	356.0	356.0	35.0

PW0016A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice. 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



PW0016A

EXAMPLE BOARD LAYOUT

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PW0016A

EXAMPLE STENCIL DESIGN

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

9. Board assembly site may have different recommendations for stencil design.



^{8.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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