HARRIS SEMICONDUCTOR

HI-300 thru HI-307

August 1997

CMOS Analog Switches

Features

- Analog Signal Range (±15V Supplies) ..... ±15V
- Low Leakage at 25°C (Typ) 40pA
- Low Leakage at 125°C (Typ) 1nA
- Low On Resistance at 25°C (Typ) 35Ω
- Break-Before-Make Delay (Typ) 60ns
- Charge Injection 30pC
- TTL, CMOS Compatible
- Symmetrical Switch Elements
- Low Operating Power (Typ for HI-300 - 303) . . . 1.0mW

Applications

- Sample and Hold (i.e., Low Leakage Switching)
- Op Amp Gain Switching (i.e., Low On Resistance)
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Description

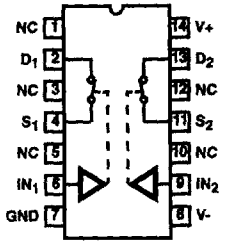
The HI-300 thru HI-307 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These switches feature break-before-make switching, (HI-301, HI-303, HI-305 and HI-307 only), low and nearly constant ON resistance over the full analog signal range, and low power dissipation, (a few mW for the HI-300 thru HI-303, a few hundred mW for the HI-304 thru HI-307).

The HI-300 thru HI-303 are TTL compatible and have a logic "0" condition with an input less than 0.8V and a logic "1" condition with an input greater than 4V. The HI-304 thru HI-307 switches are CMOS compatible and have a low state with an input less than 3.5V and a high state with an input greater than 11V. (See pinouts for switch conditions with a logic "1" input.)

Pinouts (Switch States are for a Logic "1" Input)

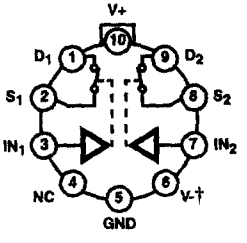
DUAL SPST HI-300 AND HI-304
TOP VIEWS

(CERDIP, PDIP, SOIC)



LOGIC	SWITCH
0	OFF
1	ON

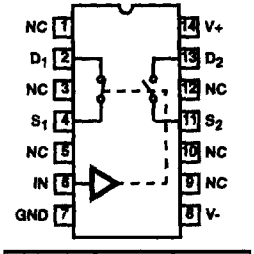
(METAL CAN)



† The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

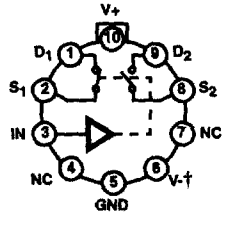
SPST HI-301 AND HI-305
TOP VIEWS

(CERDIP, PDIP, SOIC)



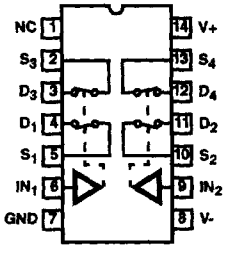
LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

(METAL CAN)



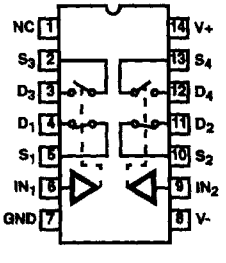
† The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-302 AND HI-306 (PDIP, CERDIP, SOIC)
TOP VIEW



LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT HI-303 AND HI-307 (PDIP, CERDIP, SOIC)
TOP VIEW



LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

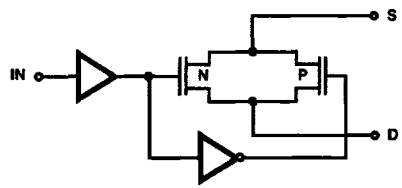
File Number **3125.1**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0300-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0300-5	0 to 75	14 Ld CERDIP	F14.3
HI2-0300-2	-55 to 125	10 Pin Metal Can (TO-100)	T10.B
HI2-0300-5	0 to 75	10 Pin Metal Can (TO-100)	T10.B
HI3-0300-5	0 to 75	14 Ld PDIP	E14.3
HI1-0301-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0301-5	0 to 75	14 Ld CERDIP	F14.3
HI2-0301-2	-55 to 125	10 Pin Metal Can (TO-100)	T10.B
HI2-0301-5	0 to 75	10 Pin Metal Can (TO-100)	T10.B
HI3-0301-5	0 to 75	14 Ld PDIP	E14.3
HI9P0301-5	0 to 75	14 Ld SOIC	M14.15
HI1-0302-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0302-5	0 to 75	14 Ld CERDIP	F14.3
HI3-0302-5	0 to 75	14 Ld PDIP	E14.3
HI9P0302-5	0 to 75	14 Ld SOIC	M14.15
HI1-0303-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0303-5	0 to 75	14 Ld CERDIP	F14.3
HI3-0303-5	0 to 75	14 Ld PDIP	E14.3
HI9P0303-5	0 to 75	14 Ld SOIC	M14.15
HI9P0303-9	-40 to 85	14 Ld SOIC	M14.15
HI1-0304-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0304-5	0 to 75	14 Ld CERDIP	F14.3
HI2-0304-2	-55 to 125	10 Pin Metal Can (TO-100)	T10.B
HI2-0304-5	0 to 75	10 Pin Metal Can (TO-100)	T10.B
HI3-0304-5	0 to 75	14 Ld PDIP	E14.3
HI1-0305-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0305-5	0 to 75	14 Ld CERDIP	F14.3
HI2-0305-2	-55 to 125	10 Pin Metal Can (TO-100)	T10.B
HI2-0305-5	0 to 75	10 Pin Metal Can (TO-100)	T10.B
HI3-0305-5	0 to 75	14 Ld PDIP	E14.3
HI9P0305-5	0 to 75	14 Ld SOIC	M14.15
HI1-0306-5	0 to 75	14 Ld CERDIP	F14.3
HI3-0306-5	0 to 75	14 Ld PDIP	E14.3
HI1-0307-2	-55 to 125	14 Ld CERDIP	F14.3
HI1-0307-5	0 to 75	14 Ld CERDIP	F14.3
HI3-0307-5	0 to 75	14 Ld PDIP	E14.3
HI9P0307-5	0 to 75	14 Ld SOIC	M14.15

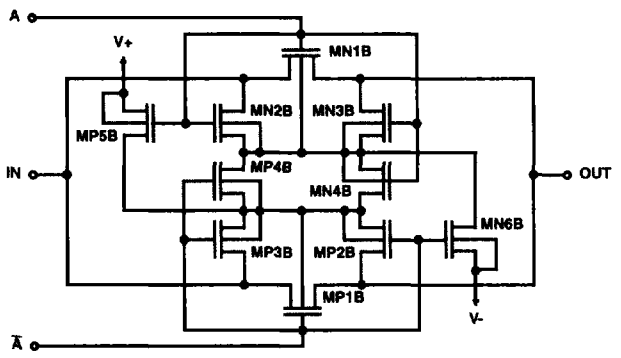
Functional Block Diagram

TYPICAL SWITCH HI-300 SERIES

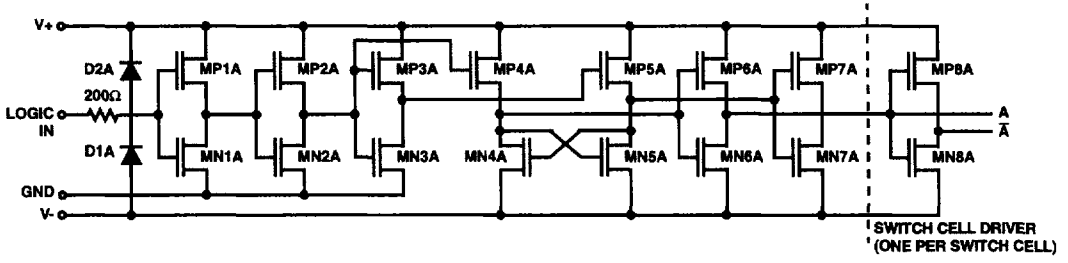


Schematic Diagrams

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Absolute Maximum Ratings

Voltage Between Supplies ..... 44V (±22V)
Digital Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage ..... $+V_{SUPPLY}$ +1.5V
$-V_{SUPPLY}$ -1.5V
Typical Derating Factor..... 1.5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Operating Conditions

Temperature Range
HI-3XX-2..... -55°C to 125°C
HI-3XX-5..... 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	95	40
PDIP Package	100	N/A
SOIC Package	120	N/A
10 Pin TO-100 Metal Can Package	160	75

Maximum Junction Temperature
CERDIP, TO-Can Packages ..... 175°C
PDIP, SOIC Packages ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s)..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{IN} = Logic Input. HI-300-303: V_{IN} - for Logic "1" = 4V, for Logic "0" = 0.8V. HI-304-307: V_{IN} - for Logic "1" = 11V, for Logic "0" = 3.5V, Unless Otherwise Specified

PARAMETER	TEMP (°C)	-55°C TO 125°C			0°C TO 75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS								
Break-Before-Make Delay, t_{OPEN} (Note 15)	25	-	60	-	-	60	-	ns
Switch On Time, t_{ON} (Note 13)	25	-	210	300	-	210	300	ns
Switch Off Time, t_{OFF} (Note 13)	25	-	160	250	-	160	250	ns
Switch Off Time, t_{ON} (Note 14)	25	-	160	250	-	160	250	ns
Switch Off Time, t_{OFF} (Note 14)	25	-	100	150	-	100	150	ns
"Off Isolation" (Note 6)	25	-	60	-	-	60	-	dB
Charge Injection (Note 7)	25	-	3	-	-	3	-	mV
Input Switch Capacitance, $C_{S(OFF)}$	25	-	16	-	-	16	-	pF
Output Switch Capacitance, $C_{D(OFF)}$	25	-	14	-	-	14	-	pF
Output Switch Capacitance, $C_{D(ON)}$	25	-	35	-	-	35	-	pF
(High) Digital Input Capacitance, C_{IN}	25	-	5	-	-	5	-	pF
(Low) Digital Input Capacitance, C_{IN}	25	-	5	-	-	5	-	pF
DIGITAL INPUT CHARACTERISTICS								
Input Low Level, V_{INL} (Note 13)	Full	-	-	0.8	-	-	0.8	V
Input High Level, V_{INH} (Note 13)	Full	4	-	-	4	-	-	V
Input Low Level, V_{INL} (Note 14)	Full	-	-	3.5	-	-	3.5	V
Input High Level, V_{INH} (Note 14)	Full	11	-	-	11	-	-	V
Input Leakage Current (Low), I_{INL} (Note 5)	Full	-	-	1	-	-	1	µA
Input Leakage Current (High), I_{INH} (Note 5)	Full	-	-	1	-	-	1	µA
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
On Resistance, r_{ON} (Note 2)	25	-	35	50	-	35	50	Ω
	Full	-	40	75	-	40	75	Ω
Off Input Leakage Current, $I_{S(OFF)}$ (Note 3)	25	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA

Electrical Specifications Supplies = +15V, -15V; V_{IN} = Logic Input. HI-300-303: V_{IN} - for Logic "1" = 4V, for Logic "0" = 0.8V. HI-304-307: V_{IN} - for Logic "1" = 11V, for Logic "0" = 3.5V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP (°C)	-55°C TO 125°C			0°C TO 75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Off Output Leakage Current, $I_{D(OFF)}$ (Note 3)	25	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA
On Leakage Current, $I_{D(ON)}$ (Note 4)	25	-	0.03	1	-	0.03	5	nA
	Full	-	0.5	100	-	0.2	100	nA
POWER SUPPLY CHARACTERISTICS								
Current, I+ (Notes 8, 13)	25	-	0.09	0.5	-	0.09	0.5	mA
	Full	-	-	1	-	-	1	mA
Current, I- (Notes 8, 13)	25	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I+ (Notes 9, 13)	25	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I- (Notes 9, 13)	25	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I+ (Notes 10, 14)	25	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I- (Notes 10, 14)	25	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I+ (Notes 11, 14)	25	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I- (Notes 11, 14)	25	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA

NOTES:

1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.
2. $V_S = \pm 10V$, $I_{OUT} = \mp 10mA$. On resistance derived from the voltage measured across the switch under the above conditions.
3. $V_S = \pm 14V$, $V_D = \mp 14V$.
4. $V_S = V_D = \pm 14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1K.
7. V_S = 0V, C_L = 10,000pF, Logic Drive = 5V pulse. (HI-300 - 303) Switches are symmetrical; S and D may be interchanged. Logic Drive = 15V (HI-304 - 307).
8. V_{IN} = 4V (one input) (all other inputs = 0V).
9. V_{IN} = 0.8V (all inputs).
10. V_{IN} = 15V (all inputs).
11. V_{IN} = 0V (all inputs).
12. To drive from DTL/TTL circuits, pullup resistors to +5V supply are recommended.
13. HI-300 thru HI-303 only.
14. HI-304 thru HI-307 only.
15. HI-301, HI-303, HI-305, HI-307 only.

Typical Performance Curves

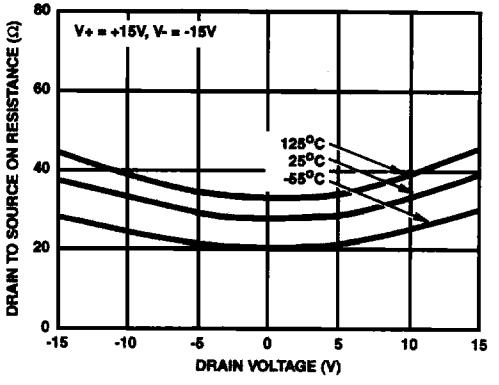


FIGURE 1. $R_{DS(ON)}$ vs V_D AND TEMPERATURE

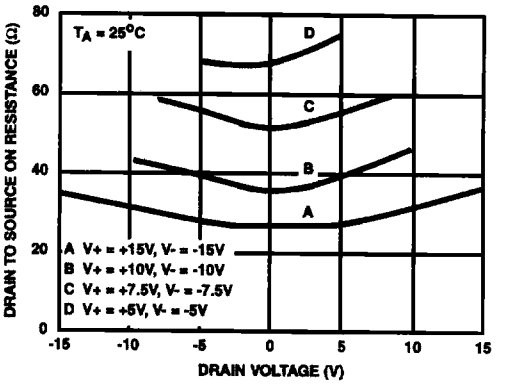


FIGURE 2. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

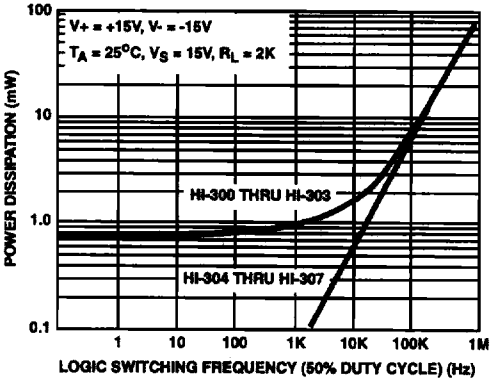


FIGURE 3. DEVICE POWER DISSIPATION vs SWITCHING FREQUENCY SINGLE LOGIC INPUT

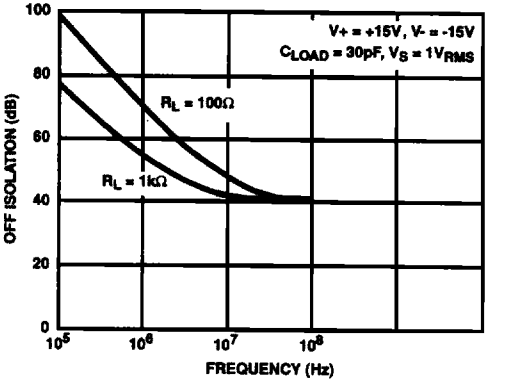


FIGURE 4. OFF ISOLATION vs FREQUENCY

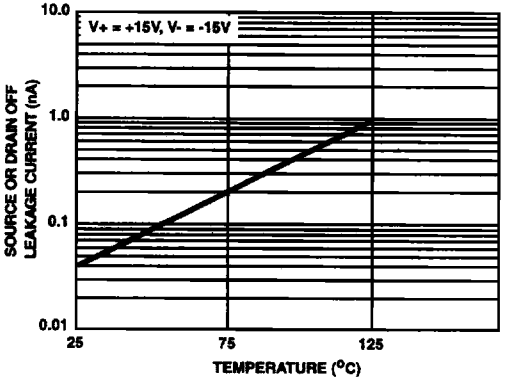


FIGURE 5. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE†

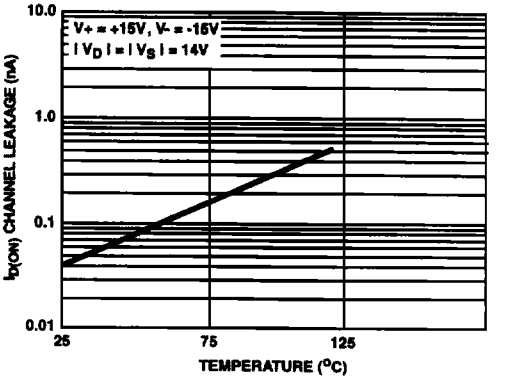


FIGURE 6. $I_{D(ON)}$ vs TEMPERATURE†

† The net leakage into the source or drain is the N-Channel leakage minus the P-Channel leakage. This difference can be positive, negative or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

Typical Performance Curves (Continued)

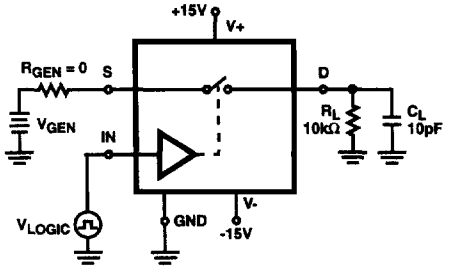


FIGURE 7A. TEST CIRCUIT

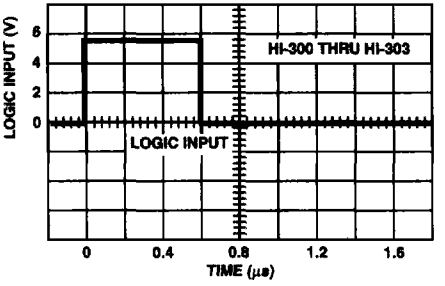


FIGURE 7B. $V_{IN(LOGIC)}$ vs TIME

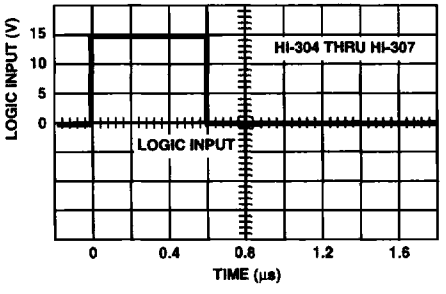


FIGURE 7C. $V_{IN(LOGIC)}$ vs TIME

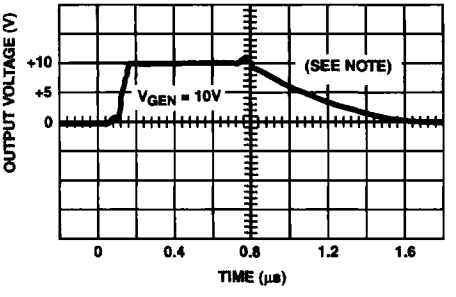


FIGURE 7D. V_{OUT} vs TIME

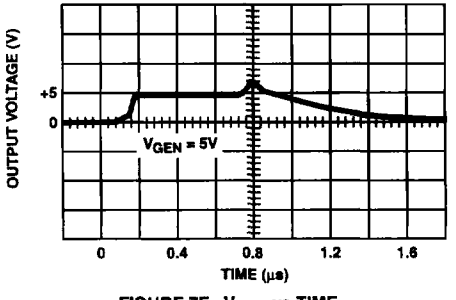


FIGURE 7E. V_{OUT} vs TIME

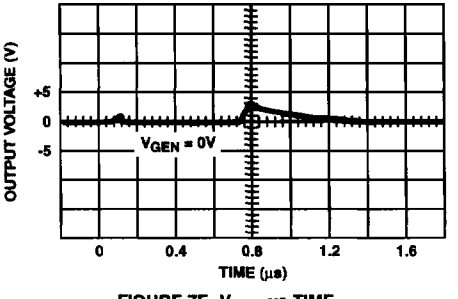


FIGURE 7F. V_{OUT} vs TIME

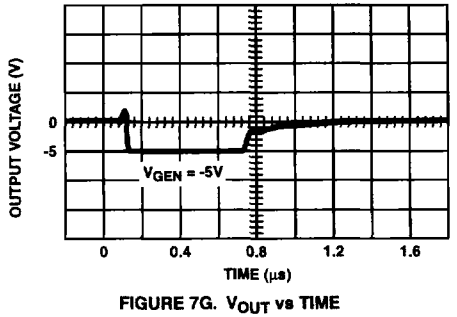


FIGURE 7G. V_{OUT} vs TIME

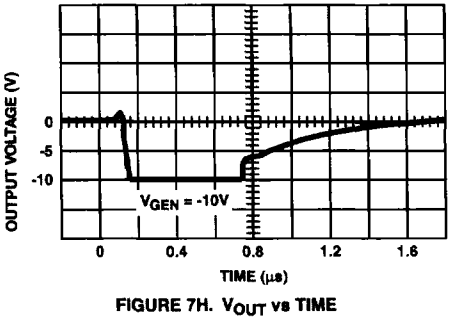


FIGURE 7H. V_{OUT} vs TIME

NOTE: If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

FIGURE 7. TYPICAL DELAY, RISE, FALL, SETTLING TIMES AND SWITCHING TRANSIENTS

Typical Performance Curves (Continued)

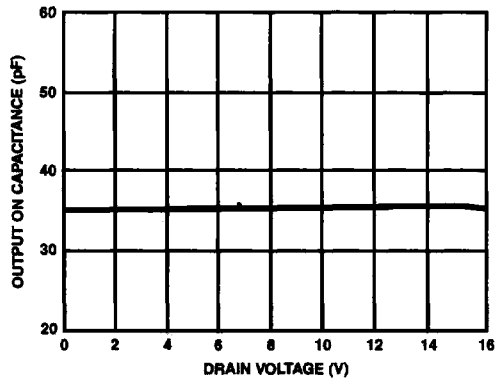


FIGURE 8. OUTPUT ON CAPACITANCE vs DRAIN VOLTAGE

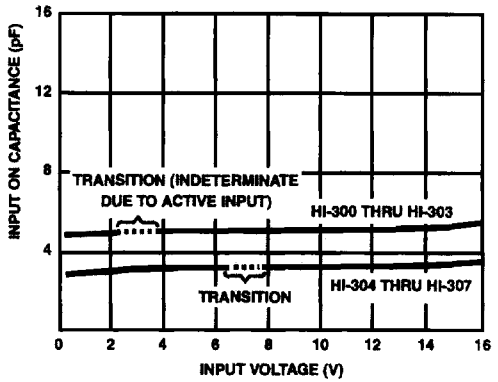


FIGURE 9. DIGITAL INPUT CAPACITANCE vs INPUT VOLTAGE

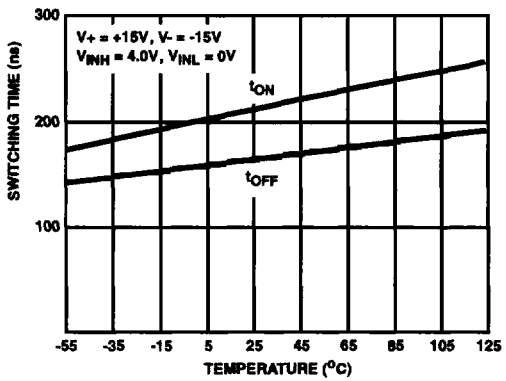


FIGURE 10. SWITCHING TIME vs TEMPERATURE, HI-300 THRU HI-303

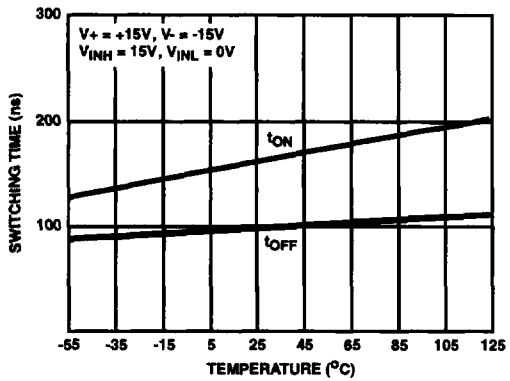


FIGURE 11. SWITCHING TIME vs TEMPERATURE, HI-304 THRU HI-307

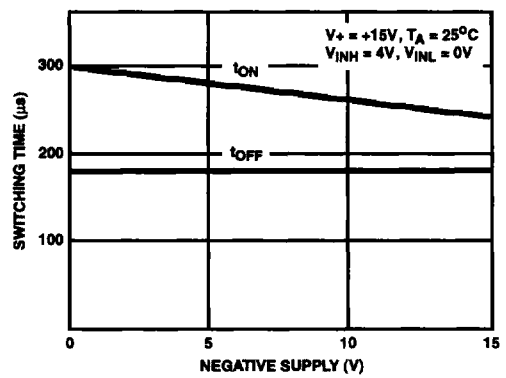


FIGURE 12. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE, HI-300 THRU HI-303

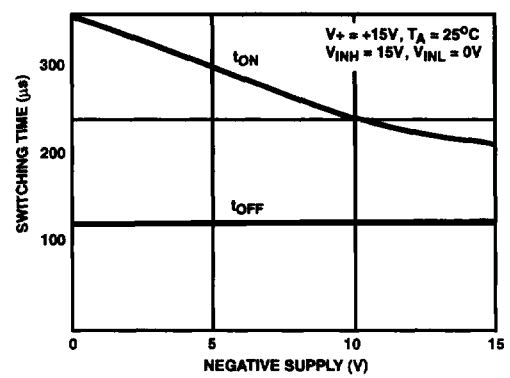


FIGURE 13. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE, HI-304 THRU HI-307

Typical Performance Curves (Continued)

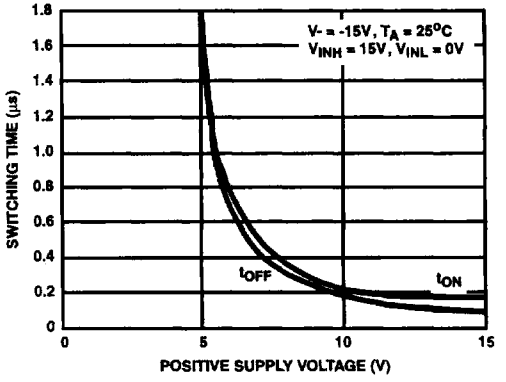


FIGURE 14. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE, HI-304 THRU HI-307

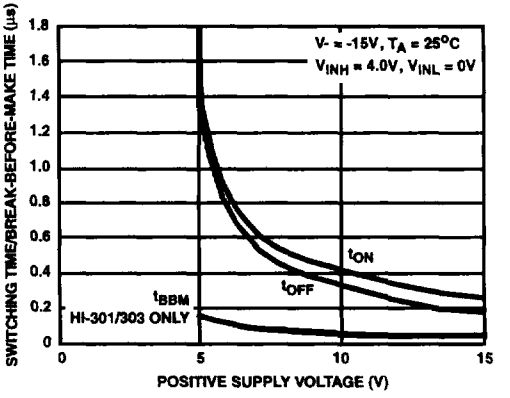


FIGURE 15. SWITCHING TIME AND BREAK-BEFORE-MAKE TIME vs POSITIVE SUPPLY VOLTAGE, HI-300 THRU HI-303

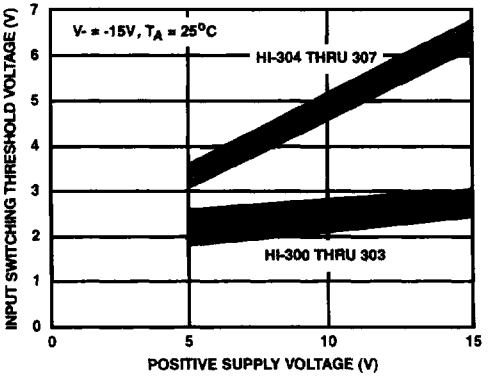
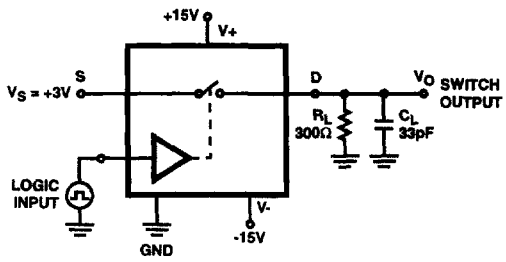


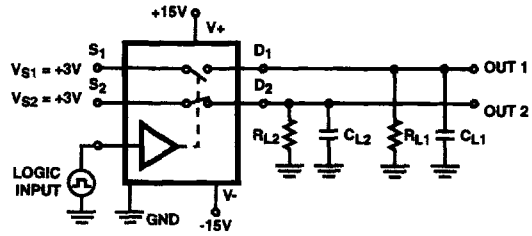
FIGURE 16. INPUT SWITCHING THRESHOLD vs POSITIVE SUPPLY VOLTAGE, HI-300 THRU HI-307

Test Circuits and Waveforms

SWITCH TYPE	V_{INH}
HI-300 thru HI-303	4V
HI-304 thru HI-307	15V

SWITCH TYPE	V_{INH}
HI-301, HI-303	5V
HI-305, HI-307	15V





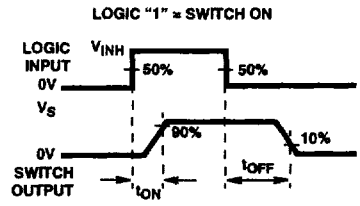


FIGURE 17. SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

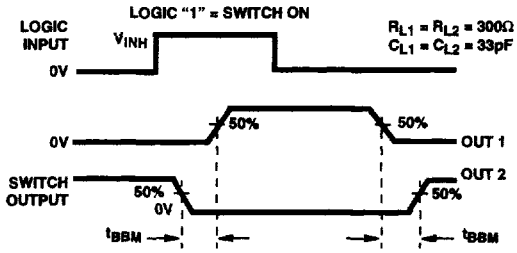


FIGURE 18. BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM}