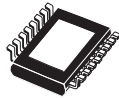


## 8-channel LED driver with direct switch control


 HTSSOP16  
(Exposed pad)

### Features

- 8 constant current output channels controlled by switch inputs
- Output enable input for global dimming
- Output current: from 5 mA to 100 mA
- Current programmable through external resistor
- Supply voltage: 3 V to 5.5 V
- Thermal shutdown
- 19 V current generators rated voltage
- Available in high thermal efficiency TSSOP exposed pad package
- ESD protection 2.0 kV HBM, 100 V MM

### Applications

- White and RGB lighting and Backlight
  - Appliance display and human interface
  - Industrial display and function indicator
  - Architectural Lighting

### Description

The **LED8102S** is a monolithic, low voltage, 8 low-side-channel LED driver. The **LED8102S** guarantees up to 19 V output driving capability allowing users to connect several LEDs in series. In the output stage, 8 regulated current sources provide from 5 mA to 100 mA constant current to drive the LEDs. Current is programmed through a single external resistor.

**LED8102S** is equipped with a thermal management that protects the device forcing it in shutdown (typically: power-off at 170 °C with 15 °C hysteresis to restart). The thermal protection switches OFF only the output channels.

The operative supply voltage range is between 3 V and 5.5 V. The output control is provided by four switch inputs, providing an on/off toggle action suitable also for local dimming. Moreover, on all active output LEDs brightness can be adjusted with a global PWM signal applied to the output enable pin ( $\overline{OE}$ ). Outputs can be connected in parallel, or left unconnected if not used, as required by the application.

#### Maturity status link

[LED8102S](#)

#### Device summary

<b>Order code</b>	LED8102SXTTR
<b>Package</b>	HTSSOP16
<b>Packing</b>	2500 parts per reel

# 1 Pin description

Figure 1. Pinout for HTSSOP16

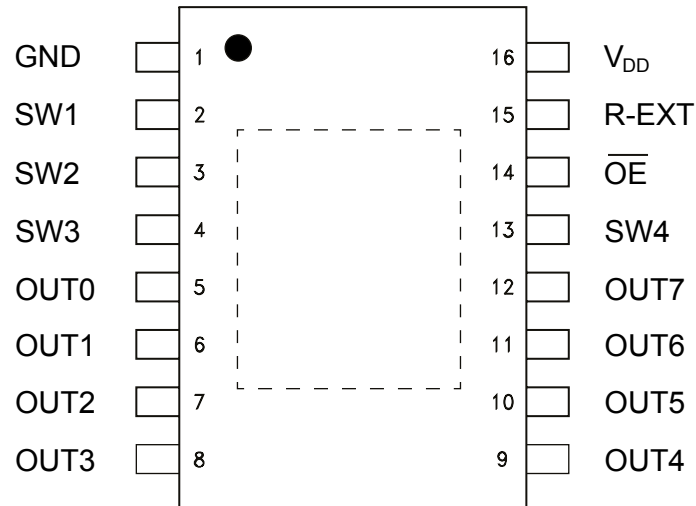
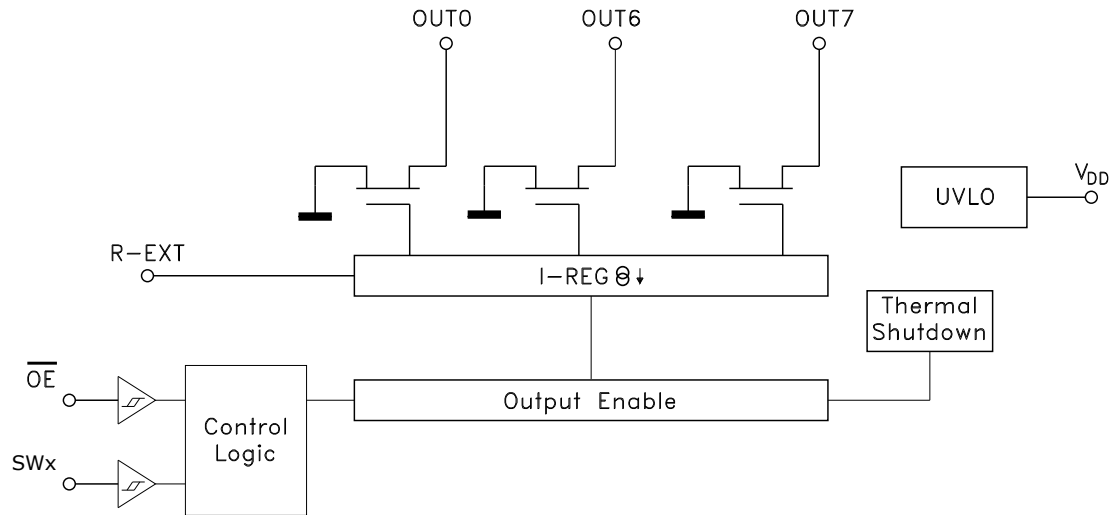


Table 1. Pin description

HTSSOP16	Symbol	Name and function
1	GND	Ground terminal
2	SW1	Switch input 1 to enable OUT0 and OUT1 simultaneously
3	SW2	Switch input 2 to enable OUT2 and OUT3 simultaneously
4	SW3	Switch input 3 to enable OUT4 and OUT5 simultaneously
5-12	OUT0-OUT7	Output terminals
13	SW4	Switch input 4 to enable OUT6 and OUT7 simultaneously
14	$\overline{OE}$	Global PWM brightness control input terminal (it must be connected to GND if not used)
15	R-EXT	Terminal for external resistor for constant current programming
16	V <sub>DD</sub>	Supply voltage terminal

## 2 Simplified internal block diagram

Figure 2. LED8102S simplified block diagram



### 3 Absolute maximum ratings

Stressing the device above the ratings listed in the table below may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply voltage	0 to 7	V
$V_{SW1}$ - $V_{SW4}$ , $V_{OE}$	Input pins voltage	- 0.4 to 5.5	V
$V_{OUT0}$ - $OUT7$	Output pins voltage	- 0.5 to 20	V
$I_{GND}$	GND terminal current	800	mA
ESD	Electrostatic discharge protection HBM human body model	± 2	kV
	Electrostatic discharge protection CDM machine model	500	V

#### 3.1 Thermal characteristics

**Table 3. Thermal characteristics**

Symbol	Parameter	Value	Unit
$T_J$	Operative junction temperature range	-40 to +150	°C
$T_{STG}$	Storage ambient temperature range	-55 to +150	
$R_{thj-amb}$	Thermal resistance junction-ambient (HTSSOP16) <sup>(1)</sup>	37.5	°C/W

1. The exposed pad should be soldered directly to the PCB to realize the thermal benefits

## 4 Electrical characteristics

$V_{DD} = 5\text{ V}$ ,  $T_j = 25\text{ °C}$ ,  $R_{EXT} = 980\ \Omega$ ,  $V_O = 0.85\text{ V}$  unless otherwise specified.

**Table 4. Electrical characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply voltage		3.0	-	5.5	V
$V_{UVLO}$	UVLO threshold (rising)			2.7	2.9	
	UVLO threshold (falling)		2.1	2.3		
$H_{YUVLO}$	UVLO hysteresis			0.4		
$V_O$	Output voltage <sup>(1) (2)</sup>	OUT0 – OUT7	0.85	-	19	
$V_{IH}$	SWx / $\overline{OE}$ input voltage		$0.8V_{DD}$	-	$V_{DD}$	
$V_{IL}$			GND	-	$0.2V_{DD}$	
$R_{UP}$	Pull-up resistor for $\overline{OE}$ pin		-	300	-	k $\Omega$
$R_{DW}$	Pull-down resistor for SWx pins		-	310	-	
$R_{EXT}$	External current set-up resistance		0.19	-	3.9	
$I_{DD(OFF1)}$	Supply current (OFF)	OUT0 to 7 = OFF	-	7	8	mA
$I_{DD(OFF2)}$		$R_{EXT} = 190\ \Omega$ OUT0 to 7 = OFF	-	14	16	
$I_{DD(ON)}$		$R_{EXT} = 190\ \Omega$ $V_O = 1.4\text{ V}$ OUT0 to 7 = ON	-	14	16	
%d $V_O$	Output current vs. output voltage regulation <sup>(1) (3)</sup>	$V_O$ from 1 V to 3 V;	-	0.1	-	%/V
%d $V_{DD}$	Output current vs. supply voltage regulation <sup>(1) (4)</sup>	$V_{DD}$ from 3 V to 5.5 V	-	1	-	
$\Delta I_{OL}$	Output current precision: device to device <sup>(1)</sup>	$V_O = 0.3\text{ V}$ ; $R_{EXT} = 3.9\text{ k}\Omega$	-	-	$\pm 6$	%
$\Delta I_{OL1}$	Output current precision: channel to channel <sup>(1) (5)</sup>	$V_O = 0.7\text{ V}$	-	$\pm 1.5$	$\pm 4$	%
$\Delta I_{OL2}$		$V_O = 1.4\text{ V}$ ; $R_{EXT} = 190\ \Omega$	-	$\pm 1.2$	$\pm 4$	
$I_{Oleak}$	Single output leakage current	$V_O = 19\text{ V}$ OUTn = OFF	-	0.5	2	$\mu\text{A}$
$T_{sd}$	Thermal shutdown <sup>(6)</sup>			170		$^{\circ}\text{C}$
$T_{sd\_hys}$	Thermal shutdown hysteresis <sup>(6)</sup>			15		$^{\circ}\text{C}$

1. Test with just one output ON.

2. Minimum regulation voltage @  $I_O = 50\text{ mA}$ .

$$3. \Delta\left(\frac{\%}{V}\right) = \frac{(I_{on@V_{on}3.0V}) - (I_{on@V_{on}1.0V})}{(I_{on@V_{on}1.0V})} \times \frac{100}{3-1}$$

$$4. \Delta\left(\frac{\%}{V}\right) = \frac{(I_{on@V_{DD}5.5V}) - (I_{on@V_{DD}3.0V})}{(I_{on@V_{DD}3.0V})} \times \frac{100}{5.5-3.0}$$

5.  $((I_{On} - I_{Oavg0-7}) / I_{Oavg0-7}) \times 100$ .

6. Not tested in production.

## 5 Switching characteristics

$V_{DD} = 5\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_O = 50\text{ mA}$ ,  $R_L = 60\text{ }\Omega$ ,  $C_L = 10\text{ pF}$ ,  $V_L = 5\text{ V}$ , unless otherwise specified.

**Table 5. Switching characteristics**

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
$t_{PLH1}$	SWx – OUTn ( $\overline{OE}$ just “0”)	Propagation delay time (“L” to “H”)	$V_{DD} = 3.3\text{ V}$	-	220	500	ns
			$V_{DD} = 5\text{ V}$	-	200	500	
$t_{PLH2}$	$\overline{OE}$ – OUTn (SWx just “1”)	Propagation delay time (“L” to “H”)	$V_{DD} = 3.3\text{ V}$	-	90	250	
			$V_{DD} = 5\text{ V}$	-	100	250	
$t_{PHL1}$	SWx – OUTn ( $\overline{OE}$ just “0”)	Propagation delay time (“H” to “L”)	$V_{DD} = 3.3\text{ V}$	-	100	250	
			$V_{DD} = 5\text{ V}$	-	100	250	
$t_{PHL2}$	$\overline{OE}$ – OUTn (SWx just “1”)	Propagation delay time (“H” to “L”)	$V_{DD} = 3.3\text{ V}$	-	220	500	
			$V_{DD} = 5\text{ V}$	-	220	500	
$t_{ON}$	OUTn Current rise time. Evaluated as OUTn falling time		$V_{DD} = 3.3\text{ V}$	-	430	600	
			$V_{DD} = 5\text{ V}$	-	400	600	
$t_{OFF}$	OUTn current fall time. Evaluated as OUTn rising time		$V_{DD} = 3.3\text{ V}$	-	430	600	
			$V_{DD} = 5\text{ V}$	-	400	600	

**Figure 3.  $t_{ON}$  -  $t_{OFF}$  time evaluation**

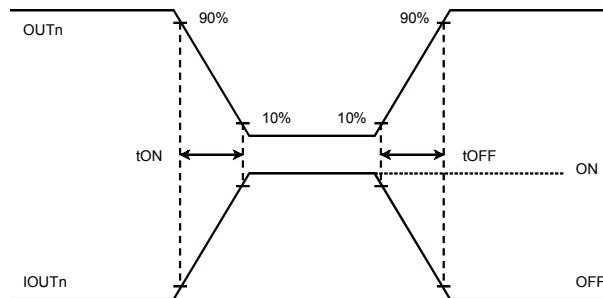
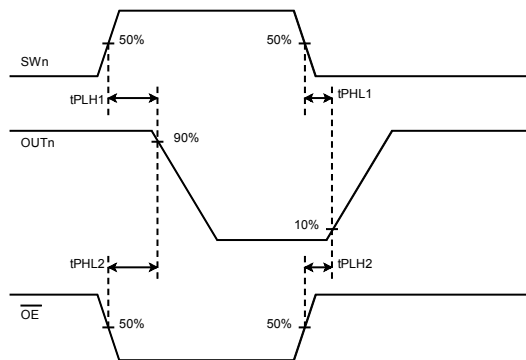


Figure 4.  $t_{PLH}$  -  $t_{PHL}$  time evaluation



## 6 Internal block diagram

Inputs  $\overline{OE}$  and SWx terminals have pull-up and pull-down connection respectively:

Figure 5.  $\overline{OE}$  Terminal

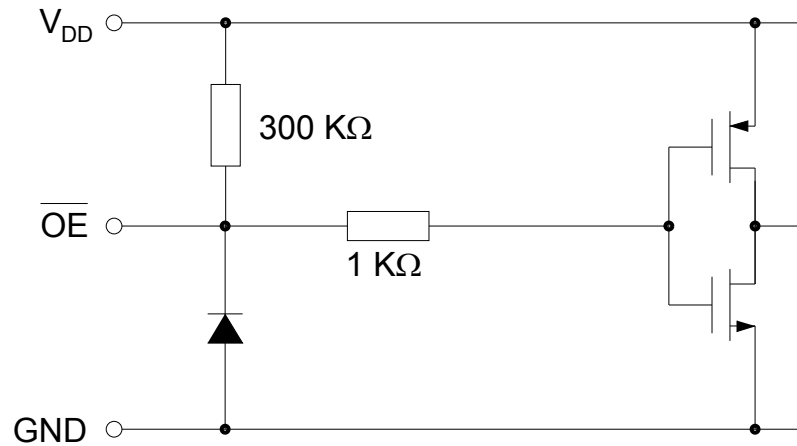
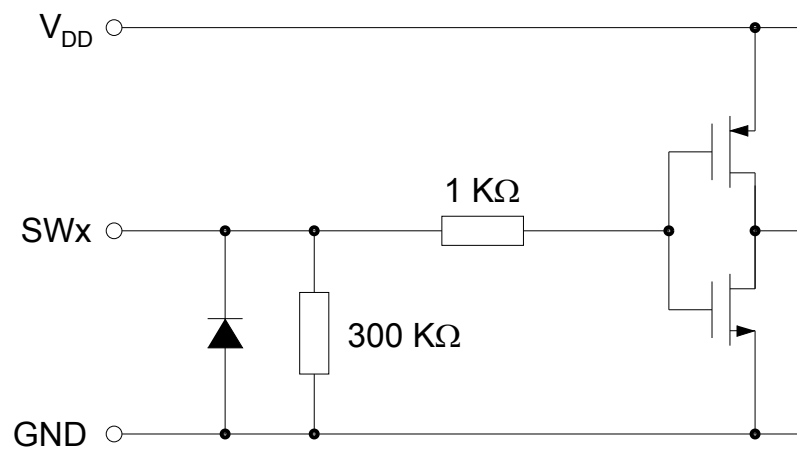


Figure 6. SWx Terminals





## 7 The switch output control

All switch inputs (SWx) are pulled down by a 300 kΩ. If the generic SWx pin is left floating or connected to GND or polarized at low logic level, the corresponding outputs will be in OFF condition. If SWx pin is connected to V<sub>DD</sub> or polarized at high logic level, the corresponding outputs will be in ON condition. See below the complete truth table:

**Table 6. Switches output control**

Switch inputs	Outputs controlled (ON/OFF)
SW1	OUT0 and OUT1 simultaneously
SW2	OUT2 and OUT3 simultaneously
SW3	OUT4 and OUT5 simultaneously
SW4	OUT6 and OUT7 simultaneously

**Table 7. Switches versus output truth table**

SW4	SW3	SW2	SW1	OE	Out0	Out1	Out2	Out3	Out4	Out5	Out6	Out7
0	0	0	0	x	off	off	off	off	off	off	off	off
0	0	0	1	0	on	on	off	off	off	off	off	off
0	0	1	0	0	off	off	on	on	off	off	off	off
0	0	1	1	0	on	on	on	on	off	off	off	off
0	1	0	0	0	off	off	off	off	on	on	off	off
0	1	0	1	0	on	on	off	off	on	on	off	off
0	1	1	0	0	off	off	on	on	on	on	off	off
0	1	1	1	0	on	on	on	on	on	on	off	off
1	0	0	0	0	off	off	off	off	off	off	on	on
1	0	0	1	0	on	on	off	off	off	off	on	on
1	0	1	0	0	off	off	on	on	off	off	on	on
1	0	1	1	0	on	on	on	on	off	off	on	on
1	1	0	0	0	off	off	off	off	on	on	on	on
1	1	0	1	0	on	on	off	off	on	on	on	on
1	1	1	0	0	off	off	on	on	on	on	on	on
1	1	1	1	0	on	on	on	on	on	on	on	on
x	x	x	x	1	off	off	off	off	off	off	off	off

## 8 LED current settings

The current drawn each OUTn channel is set by R<sub>SET</sub> resistor value according to the following formula:

$$I_{OUT} = 1.2 / R_{ext} * 16$$

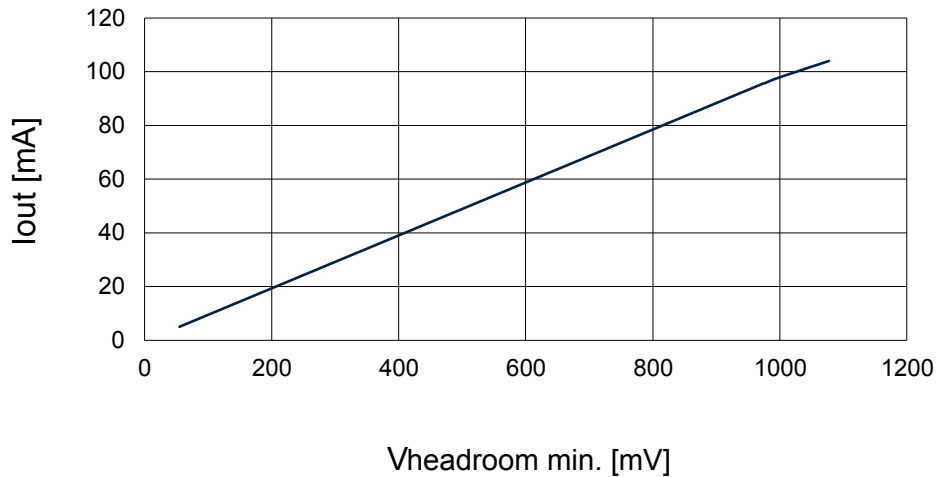
### Driver headroom voltage

In order to correctly regulate the channel current, a minimum output voltage (V<sub>HEADROOM</sub>) across each current generator must be guaranteed.

Figure 7, shows the minimum V<sub>HEADROOM</sub> slightly less than the target value (output MOS transistor in triode region).

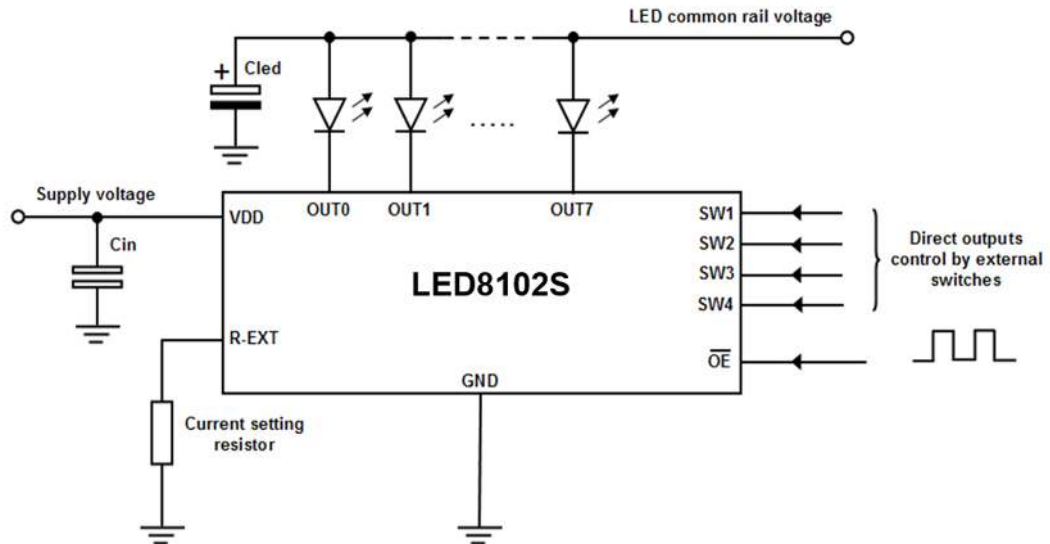
If the V<sub>HEADROOM</sub> is lower than the minimum recommended, the regulation of a current is lower than the expected one. However an excess of V<sub>HEADROOM</sub> increases the power dissipation.

Figure 7. Minimum V<sub>headroom</sub> vs. I<sub>OUT</sub> (T<sub>J</sub> = 25 °C)



## 9 Typical application

Figure 8. Typical application circuit



### Typical application circuit

The figure above shows a typical application schematic for ALED8102S, Cled value depends on common rail voltage connection length and driver total output current, typically it is around 47  $\mu\text{F}$ ; Cin is about 1  $\mu\text{F}$ ; current setting resistor depends on outputs current set (ex. with  $R_{\text{EXT}} = 386 \Omega \rightarrow I_{\text{O}} \approx 50 \text{ mA}$ ). The external programming resistor between R-EXT and GND should be connected as close as possible to the device.

To have proper device functionality it is strongly suggested to follow a correct power-up sequence:  $V_{\text{DD}}$  and  $V_{\text{LED}}$  power supplies must be provided simultaneously or at least,  $V_{\text{DD}}$  must be connected before  $V_{\text{LED}}$  to activate all internal digital control blocks earlier than LEDs power supply. If  $V_{\text{LED}}$  anticipates driver  $V_{\text{DD}}$ , this could result in a visible flash on connected LEDs (output stage undesired activation).

### Device thermal management

The aim of this section is just to provide some recommendation that can be useful in designing the application PCB for a better power dissipation:

- To decrease the device working temperature it is necessary solder the package exposed pad to the board.
- For better thermal performances at least a 4 layers (e.g. 2S2P) PCB should be used.
- The copper area below the package thermal pad should be enlarged as much as possible also outside the package perimeter (using the package sides without pins)
- A reasonable number of vias must connect the copper area below the package to all available PCB layers especially just below the device package (e.g. 3x3 or 4x3 vias array) but also outside package perimeter. Smaller and closely spaced vias is a good solution. Best implementation is represented by copper filled vias.
- On each inner layers a copper area must be provided for dissipation (wider it's better, if possible at least 4 times or more the package dimensions). A good condition is to have at least a power layer as an entire copper area (e.g. GND layer)
- Traces for pins connection must be enlarged as much as layout constrains allow
- Several devices in power dissipation on the same board must be adequately spaced.

Figure 3 shows, once the maximum power dissipation is fixed, which ambient temperature range can be covered according to maximum junction temperature and package thermal resistance: 37.5  $^{\circ}\text{C}/\text{W}$  for HTSSOP16 on Jedec PCB (2S2P) and conditions. With same thermal resistance, figure 4 shows the junction temperature as a function of ambient temperature considering 1 W of power dissipation.

Figure 9. Power dissipation rating vs ambient temperature ( $R_{th} = 37.5 \text{ }^\circ\text{C/W}$ ;  $T_j = 125 \text{ }^\circ\text{C}$ )

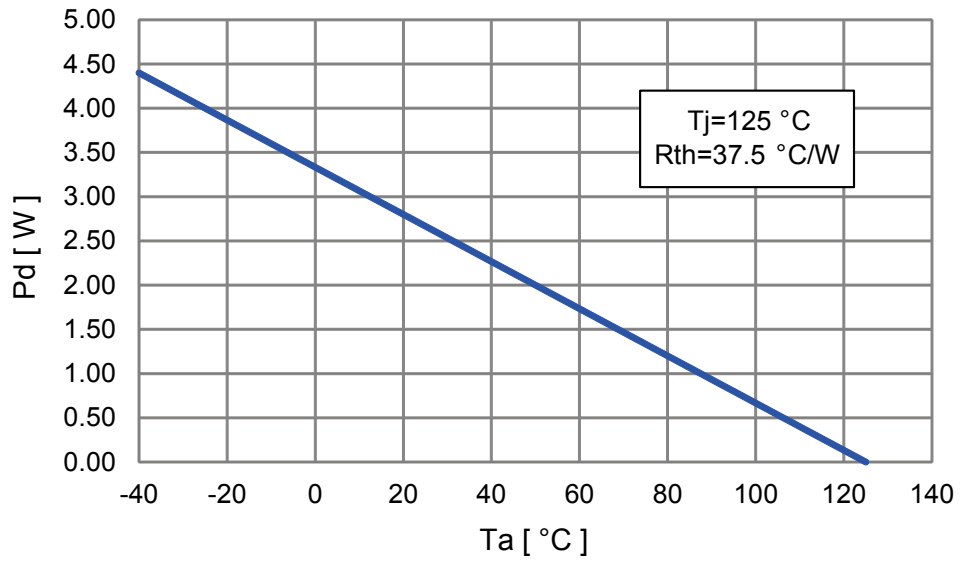
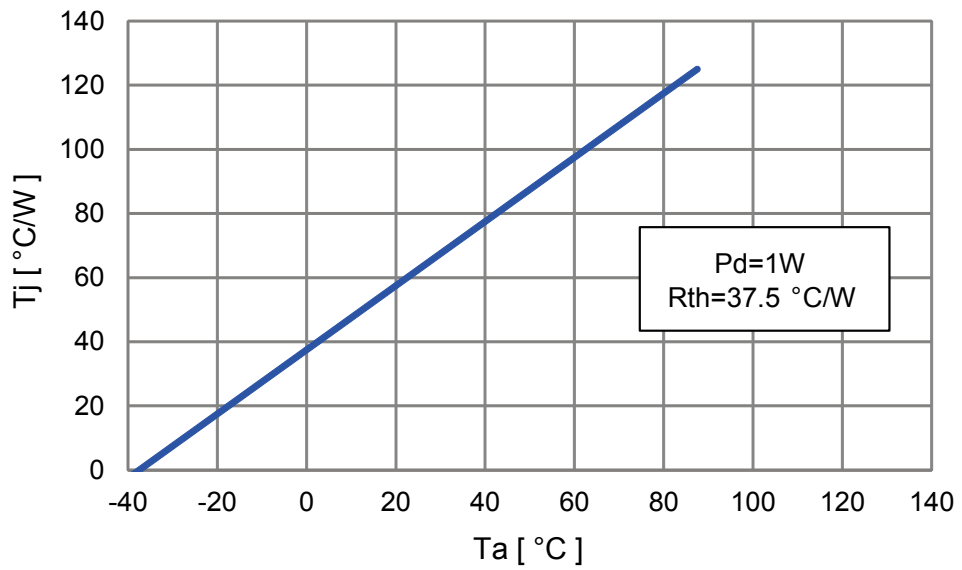


Figure 10. Junction temperature vs ambient temperature ( $R_{th} = 37.5 \text{ }^\circ\text{C/W}$ ;  $P_d = 1 \text{ W}$ )



---

## 10 Package information

---

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

## 10.1 HTSSOP16 package information

Figure 11. HTSSOP16 exposed pad package outline

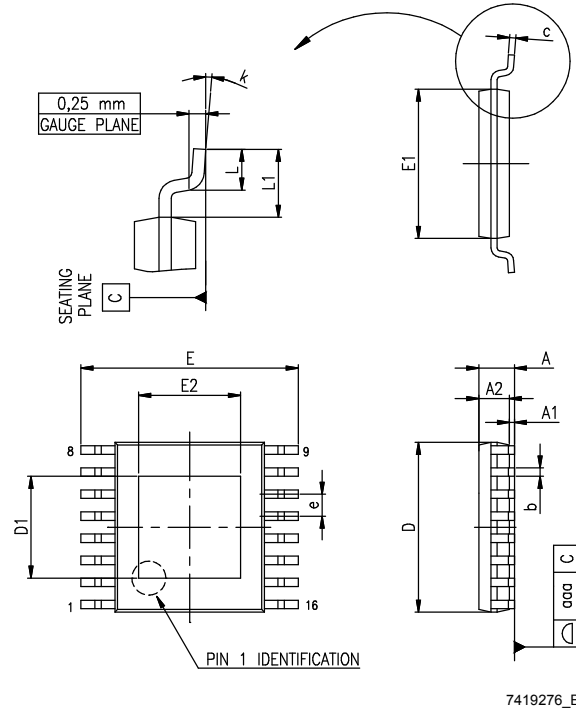
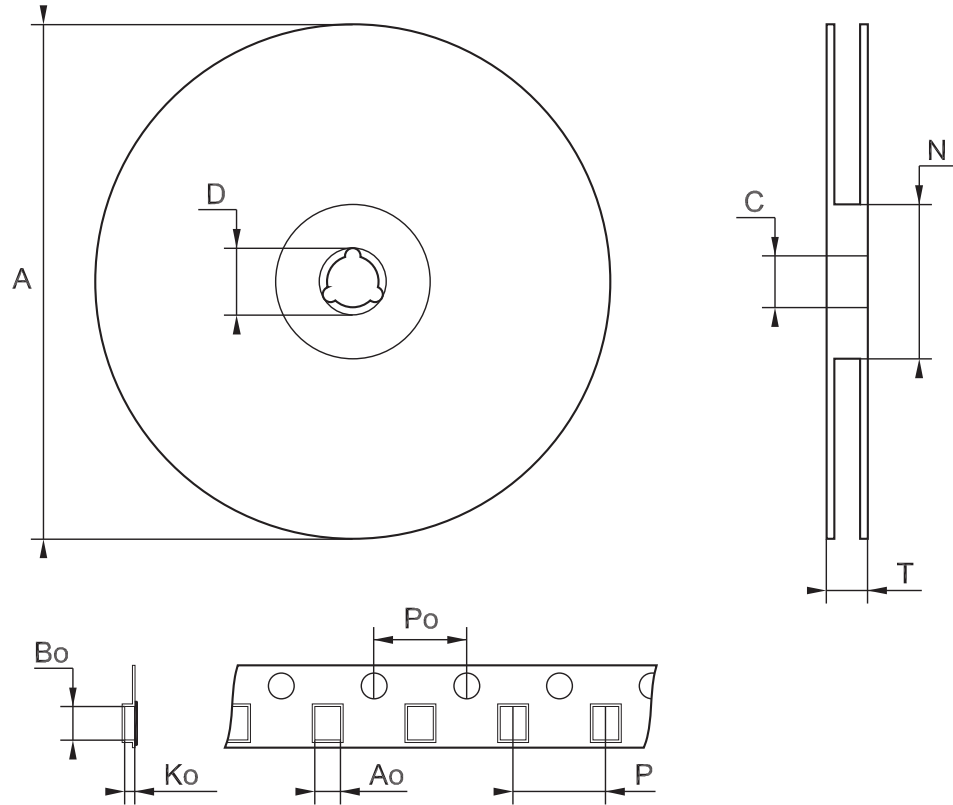


Table 8. HTSSOP16 exposed pad mechanical data

Dim.	mm.		
	Min.	Typ.	Max
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
D1	2.80	3.00	3.20
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.80	3.00	3.20
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
k	0.00		8.00
aaa			0.10

## 10.2 HTSSOP16 packing information

Figure 12. HTSSOP16 tape and reel outline



Note: Drawing not in scale

Table 9. HTSSOP16 tape and reel mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	6.7		6.9
Bo	5.3		5.5
Ko	1.6		1.8
Po	3.9		4.1
P	7.9		8.1

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
29-Apr-2019	1	First release.
06-Apr-2020	2	Minor text changed in description on the cover page. Updated footnote <sup>(4)</sup> .
26-Feb-2021	3	Updated: - Features and description on the cover page. - Figure 1 and Figure 7. - Table 2, Table 3, Switching characteristics and Section 8 .



## Contents

<b>1</b>	<b>Pin description</b> .....	<b>2</b>
<b>2</b>	<b>Simplified internal block diagram</b> .....	<b>3</b>
<b>3</b>	<b>Absolute maximum ratings</b> .....	<b>4</b>
<b>3.1</b>	<b>Thermal characteristics</b> .....	<b>4</b>
<b>4</b>	<b>Electrical characteristics</b> .....	<b>5</b>
<b>5</b>	<b>Switching characteristics</b> .....	<b>6</b>
<b>6</b>	<b>Internal block diagram</b> .....	<b>8</b>
<b>7</b>	<b>Register description</b> .....	<b>9</b>
<b>8</b>	<b>LED current settings</b> .....	<b>10</b>
<b>9</b>	<b>Typical application</b> .....	<b>11</b>
<b>10</b>	<b>Package information</b> .....	<b>13</b>
<b>10.1</b>	<b>HTSSOP16 package information</b> .....	<b>14</b>
<b>10.2</b>	<b>HTSSOP16 packing information</b> .....	<b>15</b>
	<b>Revision history</b> .....	<b>16</b>

## List of tables

<b>Table 1.</b>	Pin description . . . . .	2
<b>Table 2.</b>	Absolute maximum ratings . . . . .	4
<b>Table 3.</b>	Thermal characteristics . . . . .	4
<b>Table 4.</b>	Electrical characteristics . . . . .	5
<b>Table 5.</b>	Switching characteristics . . . . .	6
<b>Table 6.</b>	Switches output control . . . . .	9
<b>Table 7.</b>	Switches versus output truth table . . . . .	9
<b>Table 8.</b>	HTSSOP16 exposed pad mechanical data . . . . .	14
<b>Table 9.</b>	HTSSOP16 tape and reel mechanical data . . . . .	15
<b>Table 10.</b>	Document revision history . . . . .	16

## List of figures

<b>Figure 1.</b>	Pinout for HTSSOP16 . . . . .	2
<b>Figure 2.</b>	LED8102S simplified block diagram . . . . .	3
<b>Figure 3.</b>	$t_{ON}$ - $t_{OFF}$ time evaluation . . . . .	6
<b>Figure 4.</b>	$t_{PLH}$ - $t_{PHL}$ time evaluation . . . . .	7
<b>Figure 5.</b>	$\overline{OE}$ Terminal . . . . .	8
<b>Figure 6.</b>	SWx Terminals . . . . .	8
<b>Figure 7.</b>	Minimum $V_{headroom}$ vs. $I_{OUT}$ ( $T_J = 25\text{ }^\circ\text{C}$ ) . . . . .	10
<b>Figure 8.</b>	Typical application circuit . . . . .	11
<b>Figure 9.</b>	Power dissipation rating vs ambient temperature ( $R_{th} = 37.5\text{ }^\circ\text{C/W}$ ; $T_J = 125\text{ }^\circ\text{C}$ ) . . . . .	12
<b>Figure 10.</b>	Junction temperature vs ambient temperature ( $R_{th} = 37.5\text{ }^\circ\text{C/W}$ ; $P_d = 1\text{ W}$ ) . . . . .	12
<b>Figure 11.</b>	HTSSOP16 exposed pad package outline . . . . .	14
<b>Figure 12.</b>	HTSSOP16 tape and reel outline . . . . .	15

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2021 STMicroelectronics – All rights reserved