6-Bit, Programmable 2-/3-/4-Phase, Synchronous Buck Controller

ADP3194

FEATURES

- Selectable 2-, 3-, or 4-phase operation
- Up to 1 MHz per phase
- ±9.5 mV worst-case differential sensing error over temperature
- Logic-level PWM outputs for interface to external high power drivers
- PWM Flex-Mode™ architecture for excellent load transient performance
- Active current balancing between all output phases
- Built-in power good/crowbar blanking supports OTF VID code changes
- 6-bit digitally programmable 0.8375 V to 1.6 V output
- Programmable short circuit protection with programmable latch-off delay

APPLICATIONS

- Desktop PC power supplies for Next-generation Intel® processors VRM modules
- Games consoles

FUNCTIONAL BLOCK DIAGRAM

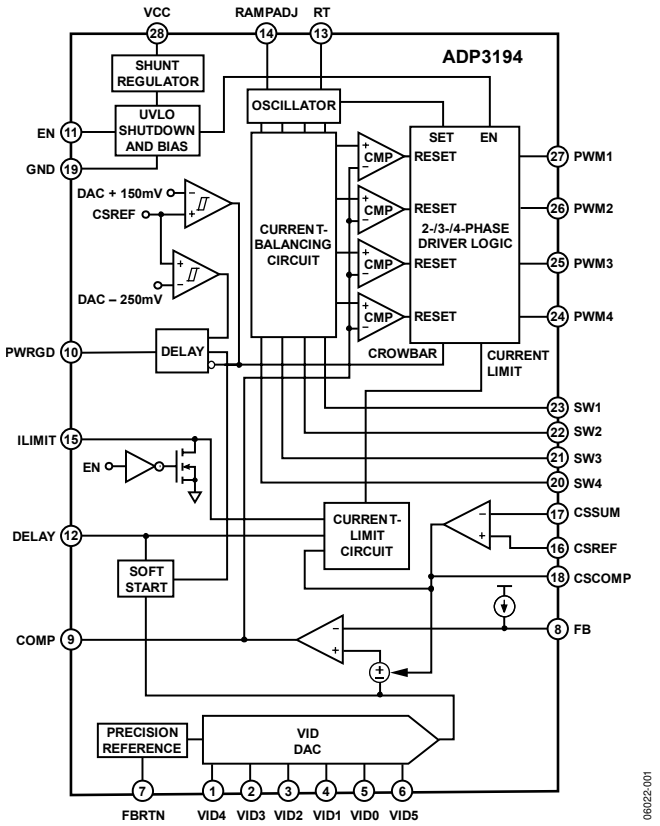


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADP3194[1] is a highly efficient, multiphase, synchronous buck switching regulator controller optimized for converting a 5 V or 12 V main supply into the core supply voltage required by high performance Intel processors. It uses an internal 6-bit DAC to read a voltage identification (VID) code directly from the processor that is used to set the output voltage between 0.8375 V and 1.6 V. The device uses a multimode PWM architecture to drive the logic-level outputs at a programmable switching frequency that can be optimized for VR size and efficiency. The phase relationship of the output signals can be programmed to provide 2-, 3-, or 4-phase operation, allowing for the construction of up to four complementary buck switching stages.

The ADP3194 also includes programmable, no-load offset, and slope functions to adjust the output voltage as a function of the load current, so it is always optimally positioned for a system transient. The ADP3194 also provides accurate and reliable short-circuit protection, adjustable current limiting, and a delayed power good output that accommodates on-the-fly (OTF) output voltage changes requested by the CPU.

The devices are specified over the commercial temperature range of 0°C to +85°C and are available in a 28-lead TSSOP.

[1] Protected by U. S. Patent Number 6,683,441; other patents pending.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

10/06—Revision 0: Initial Version

SPECIFICATIONS

VCC = 5 V, FBRTN = GND, T_A = 0°C to +85°C, unless otherwise noted.[1]

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER						
Output Voltage Range	V_{COMP}		0		VCC	V
Accuracy	V_{FB}	Relative to nominal DAC output, referenced to FBRTN, CSSUM = CSCOMP; V_{OUT} < 1 V	−8.0		+8.0	mV
Accuracy	V_{FB}	Relative to nominal DAC output, referenced to FBRTN, CSSUM = CSCOMP; V_{OUT} > 1 V	−9.5		+9.5	mV
Line Regulation	ΔV_{FB}	VCC = 4.75 V to 5.25 V		0.05		%
Input Bias Current	I_{FB}		14	15.5	17	µA
FBRTN Current	I_{FBRTN}			100	140	µA
Output Current	$I_{O(ERR)}$	FB forced to V_{OUT} − 3%		500		µA
Gain Bandwidth Product	$GBW_{(ERR)}$	COMP = FB		20		MHz
Slew Rate		C_{COMP} = 10 pF		25		V/µs
VID INPUTS						
Input Low Voltage	$V_{IL(VID)}$				0.4	V
Input High Voltage	$V_{IH(VID)}$		0.8			V
Input Current, Input Voltage Low	$I_{IL(VIDX)}$	VID(X) = 0 V		−25	−35	µA
Input Current, Input Voltage High	$I_{IH(VIDX)}$	VID(X) = 1.25 V		5	15	µA
Pull-Up Resistance	R_{VID}		35	60	85	kΩ
Internal Pull-Up Voltage			1.0	1.2		V
VID Transition Delay Time[2]		VID code change to FB change	400			ns
No CPU Detection Turn-Off Delay Time[2]		VID code change to 11111 to PWM going low	400			ns
OSCILLATOR						
Frequency Range[2]	f_{OSC}		0.25		4.5	MHz
Frequency Variation	f_{PHASE}	T_A = +25°C, R_T = 247 kΩ, 4-phase	1.55	2	2.45	MHz
		T_A = +25°C, R_T = 138 kΩ, 4-phase		3		MHz
		T_A = +25°C, R_T = 84 kΩ, 4-phase		4		MHz
Output Voltage	V_{RT}	R_T = 100 kΩ to GND	1.8	2.0	2.3	V
RAMPADJ Output Voltage	$V_{RAMPADJ}$	RAMPADJ – FB	−50		+50	mV
RAMPADJ Input Current Range	$I_{RAMPADJ}$		0		100	µA
CURRENT SENSE AMPLIFIER						
Offset Voltage	$V_{OS(CSA)}$	CSSUM – CSREF	−1.5		+1.5	mV
Input Bias Current	$I_{BIAS(CSSUM)}$		−10		+10	nA
Gain Bandwidth Product	$GBW_{(CSA)}$			10		MHz
Slew Rate		C_{CSCOMP} = 10 pF		10		V/µs
Input Common-Mode Range		CSSUM and CSREF	0		3	V
Positioning Accuracy	ΔV_{FB}		−77	−80	−83	mV
Output Voltage Range			0.05		VCC	V
Output Current	I_{CSCOMP}			500		µA
CURRENT BALANCE CIRCUIT						
Common-Mode Range	$V_{SW(X)CM}$		−600		+200	mV
Input Resistance	$R_{SW(X)}$	SW(X) = 0 V	12	20	28	kΩ
Input Current	$I_{SW(X)}$	SW(X) = 0 V	5	11	17	µA
Input Current Matching[3]	$\Delta I_{SW(X)}$	SW(X) = 0 V	−5		+5	%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CURRENT LIMIT COMPARATOR						
Output Voltage						
Normal Mode	$V_{ILIMIT(NM)}$	EN > 0.8 V, R_{ILIMIT} = 250 kΩ	2.8	3	3.3	V
Shutdown Mode	$V_{ILIMIT(SD)}$	EN < 0.4 V, I_{ILIMIT} = −100 µA			400	mV
Output Current, Normal Mode	$I_{ILIMIT(NM)}$	EN > 0.8 V, R_{ILIMIT} = 250 kΩ		12		µA
Maximum Output Current[2]			60			µA
Current Limit Threshold Voltage	V_{CL}	$V_{CSREF} - V_{CSCOMP}$, R_{ILIMIT} = 250 kΩ	105	125	145	mV
Current Limit Setting Ratio		V_{CL}/I_{ILIMIT}		10.4		mV/µA
DELAY Normal Mode Voltage	$V_{DELAY(NM)}$	R_{DELAY} = 250 kΩ	2.8	3	3.3	V
DELAY Overcurrent Threshold	$V_{DELAY(OC)}$	R_{DELAY} = 250 kΩ	1.6	1.9	2.2	V
Latch-Off Delay Time	t_{DELAY}	R_{DELAY} = 250 kΩ, C_{DELAY} = 12 nF		1.5		ms
SOFT START						
Output Current, Soft Start Mode	$I_{DELAY(SS)}$	During startup, DELAY < 2.8 V	15	20	25	µA
Soft Start Delay Time	$t_{DELAY(SS)}$	R_{DELAY} = 250 kΩ, C_{DELAY} = 12 nF, VID code = 011111		1		ms
ENABLE INPUT						
Input Low Voltage	$V_{IL(EN)}$				0.4	V
Input High Voltage	$V_{IH(EN)}$		0.8			V
Input Current	$I_{IL(EN)}$		−1		+1	µA
POWER GOOD COMPARATOR						
Undervoltage Threshold	$V_{PWRGD(UV)}$	Relative to nominal DAC output	−180	−250	−300	mV
Overvoltage Threshold	$V_{PWRGD(OV)}$	Relative to nominal DAC output	90	150	200	mV
Output Low Voltage	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = 4 mA		225	400	mV
Power Good Delay Time						
During Soft Start		R_{DELAY} = 250 kΩ, C_{DELAY} = 12 nF, VID code = 011111	1			ms
VID Code Changing			100	250		µs
VID Code Static				200		ns
Crowbar Trip Point	$V_{CROWBAR}$	Relative to nominal DAC output	90	150	200	mV
Crowbar Reset Point		Relative to FBRTN	450	550	650	mV
Crowbar Delay Time	$t_{CROWBAR}$	Overvoltage to PWM going low				
VID Code Changing		Blanking time	100	250		µs
VID Code Static				400		ns
PWM OUTPUTS						
Output Low Voltage	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = −400 µA		160	500	mV
Output High Voltage	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = +400 µA	4.0	5		V
SUPPLY—ADP3194		V_{SYSTEM} = 12 V, R_{SHUNT} = 300 Ω				
VCC	VCC		4.75	5		V
DC Supply Current				20	30	mA
UVLO Threshold Voltage	V_{UVLO}	VCC rising	6.3	7	8.0	V
UVLO Hysteresis				0.9		V

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
[2] Guaranteed by design, not production tested.
[3] Relative current matching from each phase to the average of all four phases.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC	–0.3 V to +6 V
VID4 to VID0, VID5	–0.3 V to +6 V
FBRTN	–0.3 V to +0.3 V
SW1 to SW4	–5 V to +25 V
All Other Inputs and Outputs	–0.3 V to VCC + 0.3 V
Storage Temperature Range	–65°C to +150°C
Operating Ambient Temperature Range	0°C to +85°C
Operating Junction Temperature	125°C
Thermal Impedance (θ_{JA})	100°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

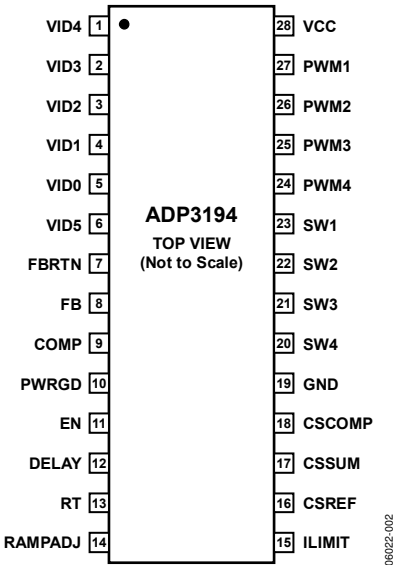


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 6	VID4 to VID0, VID5	Voltage Identification DAC Inputs. These six pins are pulled up to an internal reference, providing Logic 1 is left open. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.8375 V to 1.6 V (see Table 2). Leaving all the VID pins open results in ADP3194 going into a No CPU mode, shutting off their PWM outputs and pulling the PWRGD output low.
7	FBRTN	Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage.
8	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor between this pin and the output voltage sets the no-load offset point.
9	COMP	Error Amplifier Output and Compensation Point.
10	PWRGD	Power Good Output. Open drain output that signals when the output voltage is outside of the proper operating range.
11	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
12	DELAY	Soft Start Delay and Current-Limit Latch-Off Delay Setting Input. An external resistor and capacitor connected between this pin and GND sets the soft start ramp-up time and the overcurrent latch-off delay time.
13	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
14	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
15	ILIMIT	Current Limit Set Point/Enable Output. An external resistor from this pin to GND sets the current limit thresh old of the converter. This pin is actively pulled low when the ADP3194 EN input is low or when VCC is below its UVLO threshold to signal to the driver IC that the driver high-side and low-side outputs should go low.
16	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the power good and crowbar functions. This pin should be connected to the common point of the output inductors.
17	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current.
18	CSCOMP	Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determines the slope of the load line and the positioning loop response time.
19	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.
20 to 23	SW4 to SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. Leave the SW pins of unused phases open.
24 to 27	PWM4 to PMW1	Logic Level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3120A. Connecting the PWM3 and/or PWM4 outputs to GND causes that phase to turn off, allowing the ADP3194 to operate as a 2-, 3-, or 4-phase controller.
28	VCC	A 300 Ω resistor should be placed between the 12 V system supply and the VCC pin to ensure 5 V.

TYPICAL PERFORMANCE CHARACTERISTIC AND TEST CIRCUITS

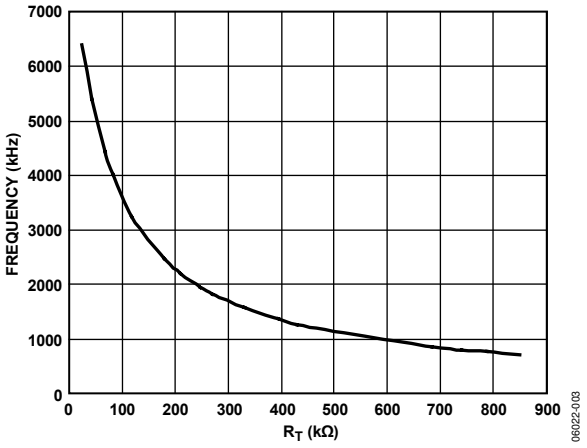


Figure 3. Master Clock Frequency vs. R_T (kΩ)

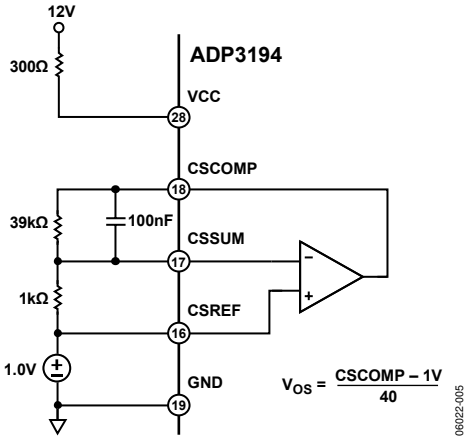


Figure 5. Current Sense Amplifier V_{OS}

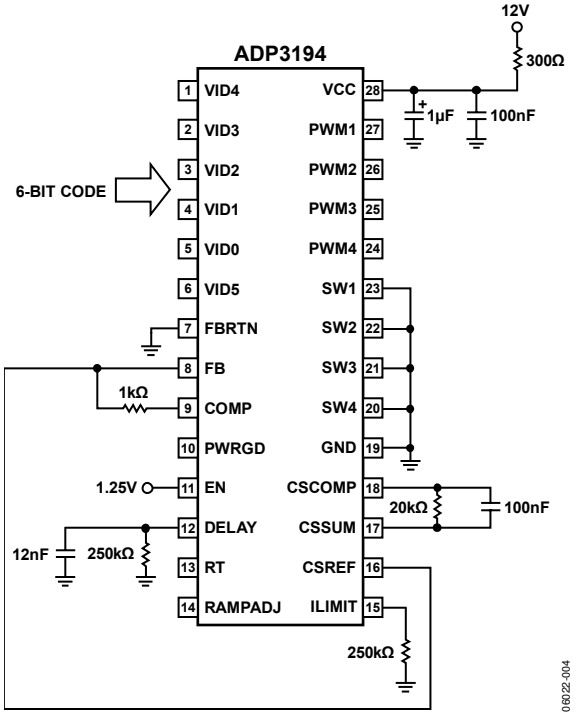


Figure 4. Closed-Loop Output Voltage Accuracy

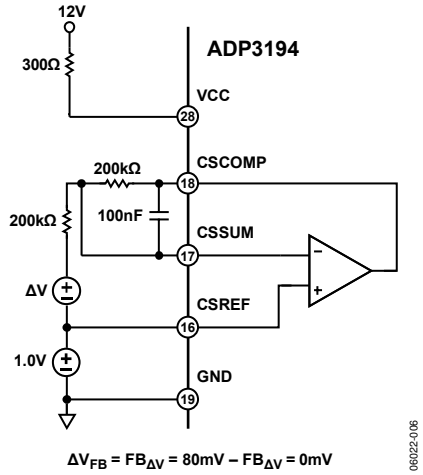


Figure 6. Positioning Voltage

THEORY OF OPERATION

The ADP3194 combines a multimode, fixed frequency PWM control with multiphase logic outputs for use in 2-, 3-, and 4-phase synchronous buck CPU core supply power converters. The internal VID DAC is designed to interface with the Intel 6-bit VRD/VRM 10- and 10.1-compatible CPUs. Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling the high currents in a single-phase converter places high thermal demands on the components in the system, such as the inductors and MOSFETs.

The multimode control of the ADP3194 ensures a stable, high performance topology for

- Balancing currents and thermals between phases
- High speed response at the lowest possible switching frequency and output decoupling
- Minimizing thermal switching losses due to lower frequency operation
- Tight load line regulation and accuracy
- High current output for up to 4-phase operation
- Reduced output ripple due to multiphase cancellation
- PC board layout noise immunity
- Ease of use and design due to independent component selection
- Flexibility in operation for tailoring design to low cost or high performance

STARTUP SEQUENCE

During startup, the number of operational phases and their phase relationship is determined by the internal circuitry that monitors the PWM outputs. Normally, the ADP3194 operate as a 4-phase PWM controller. Grounding the PWM4 pin programs 3-phase operation, and grounding the PWM3 pin and the PWM4 pin programs 2-phase operation.

When the ADP3194 are enabled, the controller outputs a voltage on PWM3 and PWM4, which is approximately 675 mV. An internal comparator checks each pin's voltage vs. a threshold of 300 mV. If the pin is grounded, it is below the threshold, and the phase is disabled. The output resistance of the PWM pins is approximately 5 kΩ during this detection time. Any external pull-down resistance connected to the PWM pins should not be less than 25 kΩ to ensure proper operation. PWM1 and PWM2 are disabled during the phase detection interval that occurs during the first two clock cycles of the internal oscillator.

After this time, if the PWM output is not grounded, the 5 kΩ resistance is removed and it switches between 0 V and 5 V. If the PWM output is grounded, it remains off. The PWM outputs are logic-level devices intended for driving external gate drivers, such as the ADP3120A. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. Also, more than one output can be on at the same time for overlapping phases.

MASTER CLOCK FREQUENCY

The clock frequency of the ADP3194 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 3. To determine the frequency per phase, the clock is divided by the number of phases in use. If PWM4 is grounded, divide the master clock by 3 for the frequency of the remaining phases. If PWM3 and PWM4 are grounded, divide by 2. If all phases are in use, divide by 4.

OUTPUT VOLTAGE DIFFERENTIAL SENSING

The ADP3194 differential sense compares a high accuracy VID DAC and a precision reference to implement a low offset error amplifier. This maintains a worst-case specification of ±9.5 mV differential sensing error over their full operating output voltage and temperature range. The output voltage is sensed between the FB pin and the FBRTN pin. Connect FB through a resistor to the regulation point, usually the remote sense pin of the microprocessor. Connect FBRTN directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 100 μA to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

OUTPUT CURRENT SENSING

The ADP3194 provide a dedicated current sense amplifier (CSA) to monitor the total output current for proper voltage positioning vs. load current and for current-limit detection. Sensing the load current at the output gives the total average current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element, such as the low-side MOSFET. This amplifier can be configured several ways, depending on the objectives of the system:

Output inductor DCR sensing without a thermistor for lowest cost,

Output inductor DCR sensing with a thermistor for improved accuracy with tracking of inductor temperature,

Sense resistors for highest accuracy measurements.

The positive input of the CSA is connected to the CSREF pin, which is connected to the output voltage. The inputs to the amplifier are summed together through resistors from the sensing element (such as the switch node side of the output inductors) to the inverting input, CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor to set the load line required by the microprocessor. The current information is then given as the difference of CSREF − CSCOMP. This difference signal is used internally to offset the VID DAC for voltage positioning and as a differential input for the current-limit comparator.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors, so it can be made extremely accurate.

ACTIVE IMPEDANCE CONTROL MODE

For controlling the dynamic output voltage droop as a function of output current, a signal proportional to the total output current at the CSCOMP pin can be scaled to equal the droop impedance of the regulator multiplied by the output current. This droop voltage is then used to set the input control voltage to the system. The droop voltage is subtracted from the DAC reference input voltage directly to tell the error amplifier where the output voltage should be. This differs from previous implementations and allows an enhanced feed-forward response.

CURRENT-CONTROL MODE AND THERMAL BALANCE

The ADP3194 has individual inputs for each phase, which are used for monitoring the current in each phase. This information is combined with an internal ramp to create a current balancing feedback system, which has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current-balance information is independent of the average output current information used for positioning described previously.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It also monitors the supply voltage for feed-forward control for changes in the supply. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp. Detailed information about programming the ramp is given in the Application Information section.

External resistors can be placed in series with individual phases to create, if desired, an intentional current imbalance such as when one phase may have better cooling and can support higher currents. Resistor R_{SW1} through Resistor R_{SW4} (see the typical application circuit in Figure 19 and Figure 20) can be used for adjusting thermal balance. It is best to have the ability to add these resistors during the initial design, so make sure that placeholders are provided in the layout.

To increase the current in any given phase, make R_{SW} for this phase larger (make R_{SW} = 0 for the hottest phase, and do not change during balancing). Increasing R_{SW} to only 500 Ω makes a substantial increase in phase current. Increase each R_{SW} value by small amounts to achieve balance, starting with the coolest phase first.

VOLTAGE CONTROL MODE

A high gain bandwidth voltage mode error amplifier is used for the voltage-mode control loop. The control input voltage to the positive input is set via the VID logic according to the voltages listed in Table 4. This voltage is also offset by the droop voltage for active positioning of the output voltage as a function of the current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the output sense location with a resistor (R_B) and is used for sensing and controlling the output voltage at this point. A current source from the FB pin flowing through R_B is used for setting the no-load offset voltage from the VID voltage. The no-load voltage is negative with respect to the VID DAC. The main loop compensation is incorporated into the feedback network between FB and COMP.

SOFT START

The power-on ramp-up time of the output voltage is set with a capacitor and resistor in parallel from the DELAY pin to ground. The RC time constant also determines the current-limit latch-off time. In UVLO, or when EN is logic low, the DELAY pin is held at ground. After the UVLO threshold is reached and EN is logic high, the DELAY capacitor is charged with an internal 20 μA current source. The output voltage follows the ramping voltage on the DELAY pin, limiting the inrush current. The soft start time depends on the value of the VID DAC and C_{DLY}, with a secondary effect from R_{DLY}. See the Application Information section for detailed information on setting C_{DLY}.

If EN is taken low or if VCC drops below UVLO, the DELAY capacitor is reset to ground to be ready for another soft start cycle. Figure 7 shows a typical soft start sequence for the ADP3194.

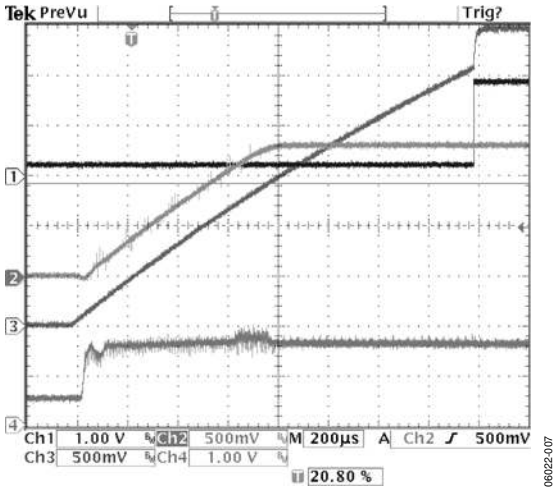


Figure 7. Typical Start-Up Waveforms
Channel 1: PWRGD, Channel 2: CSREF,
Channel 3: DELAY, Channel 4: COMP

CURRENT-LIMIT, SHORT-CIRCUIT, AND LATCH-OFF PROTECTION

The ADP3194 compares a programmable current-limit setpoint to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the ILIMIT pin to ground. During normal operation, the voltage on ILIMIT is 3 V. The current through the external resistor is internally scaled to give a current-limit threshold of 10.4 mV/µA. If the difference in voltage between CSREF and CSCOMP rises above the current-limit threshold, the internal current-limit amplifier controls the internal COMP voltage to maintain the average output current at the limit.

After the limit is reached, the 3 V pull-up on the DELAY pin is disconnected, and the external delay capacitor is discharged through the external resistor. A comparator monitors the DELAY voltage and shuts off the controller when the voltage drops below 1.8 V. The current-limit latch-off delay time is, therefore, set by the RC time constant discharging from 3 V to 1.8 V. The Application Information section discusses the selection of C_{DLY} and R_{DLY}.

Because the controller continues to cycle the phases during the latch-off delay time, the controller returns to normal operation if the short is removed before the 1.8 V threshold is reached. The recovery characteristic depends on the state of PWRGD. If the output voltage is within the PWRGD window, the controller resumes normal operation. However, if a short circuit has caused the output voltage to drop below the PWRGD threshold, a soft start cycle is initiated.

The latch-off function can be reset by either removing and reapplying VCC to the ADP3194 or by pulling the EN pin low for a short time. To disable the short-circuit latch-off function, the external resistor to ground should be left open, and a high value (>1 MΩ) resistor should be connected from DELAY to VCC.

This prevents the DELAY capacitor from discharging, so the 1.8 V threshold is never reached. The resistor has an impact on the soft start time because the current through it adds to the internal 20 µA current source.

During startup, when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit controls the internal COMP voltage to the PWM comparators to 2 V. This limits the voltage drop across the low-side MOSFETs through the current balance circuitry.

An inherent per phase current limit protects individual phases, if one or more phases stops functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage.

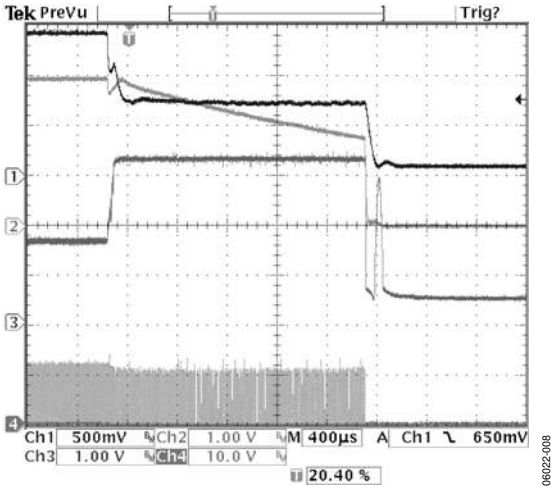


Figure 8. Overcurrent Latch-Off Waveforms
Channel 1: CSREF, Channel 2: DELAY,
Channel 3: COMP, Channel 4: Phase 1 Switch Node

DYNAMIC VID

The ADP3194 has the ability to dynamically change the VID input while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as VID OTF. A VID OTF can occur under either light or heavy load conditions. The processor signals the controller by changing the VID inputs in multiple steps from the start code to the finish code. This change can be positive or negative.

When a VID input changes state, the ADP3194 detects the change and ignores the DAC inputs for a minimum of 400 ns. This time prevents a false code due to logic skew while the six VID inputs are changing. Additionally, the first VID change initiates the PWRGD and crowbar blanking functions for a minimum of 100 µs to prevent a false PWRGD or crowbar event. Each VID change resets the internal timer.

Table 4. VID Codes for the ADP3194

VID4	VID3	VID2	VID1	VID0	VID5	Output
1	1	1	1	1	1	No CPU
1	1	1	1	1	0	No CPU
0	1	0	1	0	0	0.8375 V
0	1	0	0	1	1	0.8500 V
0	1	0	0	1	0	0.8625 V
0	1	0	0	0	1	0.8750 V
0	1	0	0	0	0	0.8875 V
0	0	1	1	1	1	0.9000 V
0	0	1	1	1	0	0.9125 V
0	0	1	1	0	1	0.9250 V
0	0	1	1	0	0	0.9375 V
0	0	1	0	1	1	0.9500 V
0	0	1	0	1	0	0.9625 V
0	0	1	0	0	1	0.9750 V
0	0	1	0	0	0	0.9875 V
0	0	0	1	1	1	1.0000 V
0	0	0	1	1	0	1.0125 V
0	0	0	1	0	1	1.0250 V
0	0	0	1	0	0	1.0375 V
0	0	0	0	1	1	1.0500 V
0	0	0	0	1	0	1.0625 V
0	0	0	0	0	1	1.0750 V
0	0	0	0	0	0	1.0875 V
1	1	1	1	0	1	1.1000 V
1	1	1	1	0	0	1.1125 V
1	1	1	0	1	1	1.1250 V
1	1	1	0	1	0	1.1375 V
1	1	1	0	0	1	1.1500 V
1	1	1	0	0	0	1.1625 V
1	1	0	1	1	1	1.1750 V
1	1	0	1	1	0	1.1875 V
1	1	0	1	0	1	1.2000 V
1	1	0	1	0	0	1.2125 V
1	1	0	0	1	1	1.2250 V
1	1	0	0	1	0	1.2375 V
1	1	0	0	0	1	1.2500 V
1	1	0	0	0	0	1.2625 V
1	0	1	1	1	1	1.2750 V
1	0	1	1	1	0	1.2875 V
1	0	1	1	0	1	1.3000 V
1	0	1	1	0	0	1.3125 V
1	0	1	0	1	1	1.3250 V
1	0	1	0	1	0	1.3375 V
1	0	1	0	0	1	1.3500 V
1	0	1	0	0	0	1.3625 V
1	0	0	1	1	1	1.3750 V
1	0	0	1	1	0	1.3875 V
1	0	0	1	0	1	1.4000 V
1	0	0	1	0	0	1.4125 V
1	0	0	0	1	1	1.4250 V
1	0	0	0	1	0	1.4375 V
1	0	0	0	0	1	1.4500 V
1	0	0	0	0	0	1.4625 V
0	1	1	1	1	1	1.4750 V
0	1	1	1	1	0	1.4875 V
0	1	1	1	0	1	1.5000 V
0	1	1	1	0	0	1.5125 V
0	1	1	0	1	1	1.5250 V
0	1	1	0	1	0	1.5375 V
0	1	1	0	0	1	1.5500 V
0	1	1	0	0	0	1.5625 V
0	1	0	1	1	1	1.5750 V
0	1	0	1	1	0	1.5875 V
0	1	0	1	0	1	1.6000 V

POWER GOOD MONITORING

The power good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open-drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the nominal limits specified in Table 4**.** These limits are based on the VID voltage setting. PWRGD goes low if the output voltage is outside of this specified range, if all of the VID DAC inputs are high, or whenever the EN pin is pulled low. PWRGD is blanked during a VID OTF event for a period of 250 µs to prevent false signals during the time the output is changing.

The PWRGD circuitry also incorporates an initial turn-on delay time based on the DELAY ramp. The PWRGD pin is held low until the DELAY pin reaches 2.6 V. The time between when the PWRGD undervoltage threshold is reached and when the DELAY pin reaches 2.6 V provides the turn-on delay time. This time is incorporated into the soft start ramp. To ensure a 1 ms delay time on PWRGD, the soft start ramp must also be >1 ms. See the Application Information section for detailed information on setting C_{DLY}.

OUTPUT CROWBAR

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low-side MOSFETs) when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 550 mV. Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output overvoltage is due to a short in the high-side MOSFET, this action current-limits the input supply or blows its fuse, protecting the microprocessor from being destroyed.

OUTPUT ENABLE AND UVLO

For the ADP3194 to begin switching, the input supply (VCC) to the controller must be higher than the UVLO threshold, and the EN pin must be higher than its logic threshold. If UVLO is less than the threshold or the EN pin is logic low, the ADP3194 is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and holds the ILIMIT pin at ground.

In the application circuit, the ILIMIT pin should be connected to the $\overline{OD}$ pins of the ADP3120A drivers. Grounding ILIMIT disables the drivers so that both the DRVH and DRVL are also grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs were not disabled, a negative voltage could be generated during output due to the high current discharge of the output capacitors through the inductors.

APPLICATION INFORMATION

The design parameters for a typical Intel VRD 10.1-compliant CPU application are as follows:

- Input voltage (V_{IN}) = 12 V
- VID setting voltage (V_{VID}) = 1.300 V
- Duty cycle (D) = 0.108
- Nominal output voltage at no load (V_{ONL}) = 1.281 V
- Nominal output voltage at 101 A load (V_{OFL}) = 1.159 V
- Static output voltage drop based on a 1.2 mΩ load line (R_O) from no load to full load (V_D) = $V_{ONL} - V_{OFL}$ = 1.281 V − 1.159 V = 121.2 mV
- Maximum output current (I_O) = 120 A
- Maximum output current step (ΔI_O) = 85 A
- Number of phases (n) = 4
- Switching frequency per phase (f_{SW}) = 1.125 MHz

SETTING THE CLOCK FREQUENCY

The ADP3194 uses a fixed-frequency control architecture. The frequency is set by an external timing resistor (R_T). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to switching losses and the sizes of the inductors and/or the input and output capacitors. With $n = 4$ for four phases, a clock frequency of 4 MHz sets the switching frequency (f_{SW}) of each phase to 1 MHz, which represents a practical trade-off between the switching losses and the sizes of the output filter components. Figure 3 shows that to achieve
4 MHz oscillator frequency, the correct value for R_T is 84 kΩ.
3 MHz oscillator frequency, the correct value for R_T is 138 kΩ.
2 MHz oscillator frequency, the correct value for R_T is 247 kΩ.
Alternatively, the value for R_T can be calculated using

$$R_T = \frac{3}{n \times f_{SW} \times 4.6\ \text{pF}} - 79\ \text{k}\Omega \quad (1)$$

where 4.6 pF and 79 kΩ are internal IC component values. For good initial accuracy and frequency stability, a 1% resistor is recommended.

SOFT START AND CURRENT-LIMIT LATCH-OFF DELAY TIMES

Because the soft start and current-limit latch-off delay functions share the DELAY pin, these two parameters must be considered together. The first step is to set C_{DLY} for the soft start ramp. This ramp is generated with a 20 μA internal current source. The value of R_{DLY} has a second-order impact on the soft start time because it sinks part of the current source to ground.

However, as long as R_{DLY} is kept greater than 200 kΩ, this effect is minor. The value for C_{DLY} can be approximated by

$$C_{DLY} = \left(20\ \mu\text{A} - \frac{V_{VID}}{2 \times R_{DLY}}\right) \times \frac{t_{SS}}{V_{VID}} \quad (2)$$

where t_{SS} is the desired soft start time.

Assuming an R_{DLY} of 390 kΩ and a desired soft start time of 3 ms, C_{DLY} is 36 nF. The closest standard value for C_{DLY} is 39 nF. Once C_{DLY} is chosen, R_{DLY} can be calculated for the current-limit latch-off time by

$$R_{DLY} = \frac{1.96 \times t_{DELAY}}{C_{DLY}} \quad (3)$$

If the result for R_{DLY} is less than 200 kΩ, a smaller soft start time should be considered by recalculating Equation 2, or a longer latch-off time should be used. R_{DLY} should never be less than 200 kΩ. In this example, a delay time of 9 ms results in R_{DLY} = 452 kΩ. The closest standard 5% value is 470 kΩ.

INDUCTOR SELECTION

The choice of inductance for the inductor determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and conduction losses in the MOSFETs; but it allows using smaller inductors and, for a specified peak-to-peak transient deviation, less total output capacitance.

Conversely, a higher inductance means lower ripple current and reduced conduction losses but requires larger inductors and more output capacitance for the same peak-to-peak transient deviation. In any multiphase converter, a practical value for the peak-to-peak inductor ripple current is less than 50% of the maximum dc current in the same inductor. Equation 4 shows the relationship between the inductance, oscillator frequency, and peak-to-peak ripple current in the inductor.

$$I_R = \frac{V_{VID} \times (1 - D)}{f_{SW} \times L} \quad (4)$$

Equation 5 can be used to determine the minimum inductance based on a given output ripple voltage.

$$L \geq \frac{V_{VID} \times R_O \times \left(1 - \left(n \times D\right)\right)}{f_{SW} \times V_{RIPPLE}} \quad (5)$$

Solving Equation 5 for a 10 mV p-p output ripple voltage yields

$$L \geq \frac{1.3\ \text{V} \times 1.2\ \text{m}\Omega \times (1 - 0.108)}{1.125\ \text{MHz} \times 4.4\ \text{mV}} = 280\ \text{nH}$$

If the resulting ripple voltage is less than it was designed for, make the inductor smaller until the ripple value is met. This allows optimal transient response and minimum output decoupling.

The smallest possible inductor should be used to minimize the number of output capacitors. For this example, choosing a 280 nH inductor is a good starting point and gives a calculated ripple current of 3.68 A. The inductor should not saturate at the peak current of 31.84 A and should be able to handle the sum of the power dissipation caused by the average current of 30 A in the winding and core loss.

DESIGNING AN INDUCTOR

Once the inductance is known, the next step is either to design an inductor or to find a standard inductor that comes as close as possible to meeting the overall design goals.

The first decision in designing the inductor is to choose the core material. Several possibilities for providing low core loss at high frequencies include the powder cores (for example, Kool-Mμ® from Magnetics, Inc. or from Micrometals) and the gapped soft ferrite cores (for example, 3F3 or 3F4 from Philips). Avoid low frequency powdered iron cores due to their high core loss, especially when the inductor value is relatively low and the ripple current is high.

The best choice for a core geometry is a closed-loop type such as a potentiometer core, PQ, U, or E core or toroid. A good compromise between price and performance is a core with a toroidal shape.

Many useful magnetics design references are available for quickly designing a power inductor, such as Magnetic Designer Software™ by Intusoft and *Designing Magnetic Components for High-Frequency DC-DC Converters*, by William T. McLyman, KG Magnetics, Inc., ISBN 1883107008.

Selecting a Standard Inductor

Power inductor manufacturers can provide design consultation and deliver power inductors optimized for high power applications upon request. Such manufacturers include Coilcraft, Coiltronics, Sumida Electric Company, and Vishay Intertechnology.

SENSE RESISTOR

A dedicated sense resistor can be used for current sensing. An advantage to this is the fact that there is much less temperature variation than using the DCR method. Therefore, a thermistor is not required. The trade-off is that a sense resistor is required for each phase. So, one thermistor is saved, but four sense resistors are needed in a four phase design. Also, there is extra power dissipation due to the sense resistor in series with the power delivery.

SENSE RESISTOR SELECTION

The resistance value of the sense resistor must be chosen to minimize the conduction loss, but be large enough for accurate current measurement. The lower the resistance, the lower the signal to noise ratio that appears at the ADP3194 input. This directly affects the current sense accuracy. A sense resistor of 1 mΩ is chosen. The power loss in the resistor is calculated as:

$$P_{RS} = I^2 \times R_{SENSE} \quad (6)$$

If the design has 30 A per phase, then:

$$P_{RS} = 30\,\text{A} \times 30\,\text{A} \times 1\,\text{m}\Omega = 900\,\text{mW}$$

This results in a 900mW conduction loss through the sense resistor in a 30 A per phase design. Therefore, a 1 mΩ, 1 W sense resistor is chosen. There is a parasitic inductance (L_P) associated with the sense resistor. This value can be found on the data sheet of the sense resistor. A typical value is of the order of 2.2 nH.

OUTPUT DROOP RESISTANCE–SENSE RESISTOR

The design requires the regulator output voltage measured at the CPU pins to drop when the output current increases. The specified voltage drop corresponds to a dc output resistance (R_O).

The output current is measured by summing the voltage across each inductor and passing the signal through a low-pass filter. This summer filter is the CS amplifier configured with resistors $R_{PH(X)}$ (summers), and R_{CS} and C_{CS} (filter). The output resistance of the regulator is set by the following equations:

$$R_O = \frac{R_{CS}}{R_{PH(X)}} \times R_{SENSE} \quad (7)$$

$$C_{CS} = \frac{L_P}{R_{SENSE} \times R_{CS}} \quad (8)$$

where R_{SENSE} is the resistance of the sense resistor.

The user has the flexibility of choosing either R_{CS} or $R_{PH(X)}$. It is best to select R_{CS} equal to 100 kΩ, and then solve for $R_{PH(X)}$ by rearranging Equation 6.

$$R_{PH(X)} = \frac{R_{SENSE}}{R_O} \times R_{CS} \quad (9)$$

$$R_{PH(X)} = \frac{1.0\,\text{m}\Omega}{1.2\,\text{m}\Omega} \times 100\,\text{k}\Omega = 82.5\,\text{k}\Omega$$

Next, use Equation 8 to solve for C_{CS}.

$$C_{CS} = \frac{2.2\,\text{nH}}{1.0\,\text{m}\Omega \times 100\,\text{k}\Omega} = 220\,\text{pF}$$

Therefore, set R_{CS} equal to 100 kΩ, C_{CS} equal to 220 pF, and R_{PH} equal to 82.5 kΩ.

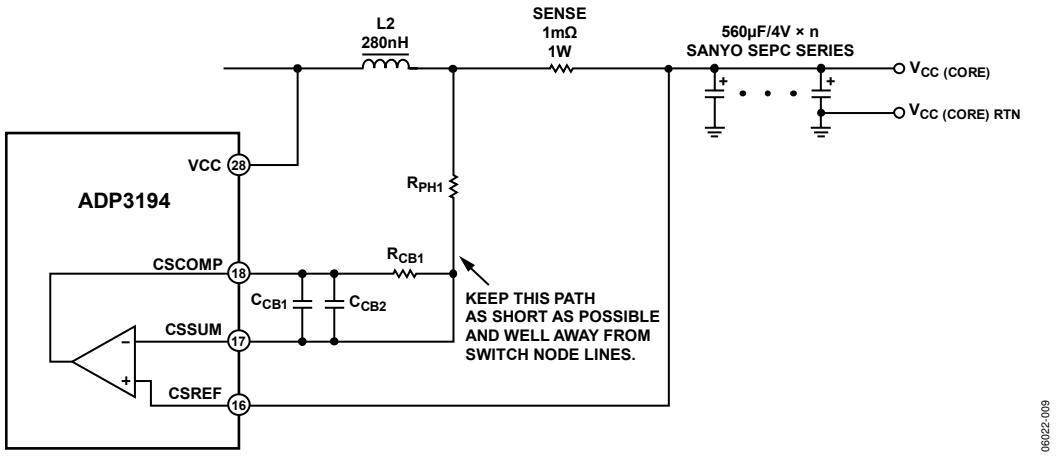


Figure 9. Using a Sense Resistor

OUTPUT OFFSET

The Intel specification requires that at no load should the nominal output voltage of the regulator be offset to a value lower than the nominal voltage corresponding to the VID code. The offset is set by a constant current source flowing out of the FB pin (I_{FB}) and flowing through R_B. The value of R_B can be found using Equation 10:

$$R_B = \frac{V_{VID} - V_{ONL}}{I_{FB}} \quad (10)$$

$$R_B = \frac{1.3\text{ V} - 1.281\text{ V}}{15.5\ \mu\text{A}} = 1.22\ \text{k}\Omega$$

The closest standard 1% resistor value is 1.21 kΩ.

DESIGN COMPARISON TRADE-OFF BETWEEN DCR AND SENSE RESISTOR

Cost

The inductor DCR method requires a thermistor, which costs about $0.03. The R_{SENSE} method requires an extra sense resistors for each phase. This costs about 4 × $0.07 = $0.28. If it can also meet the Intel accuracy specification of 25mV across the full load range, then it is the preferred method in VR applications.

Accuracy

Table 5 shows the accuracy results for a 4-phase VR10.1 application, using DCR method and sense resistor method. As can be seen, the sense resistor method improves the accuracy slightly. However, since the DCR method meets the Intel specification, it is the preferred solution, for cost reasons.

Table 5. Input Parameters

	Design Inputs	
	Sense Resistor Method	**DCR Method**
Parameter	**Value**	**Value**
N	4	4
DCR	1.00 mΩ	1.00 mΩ
Loadline	1.00 mΩ	1.00 mΩ
Imax	120.0 A	120.0 A
Istep	90.0 A	90.0 A
L error	0%	20%
C error	5%	5%
R_{SENSE} error	1%	5%
Temp Rise	70°C	70°C
R_{SENSE} vs. Temp	0.0 %	26.6%
No-load Offset	19.0 mV	19.0 mV
Total Output Vripple	8.0 mV	8.0 mV
Inductor Iripple	6.0 A	6.0 A
Gain Factor for TC	12	12

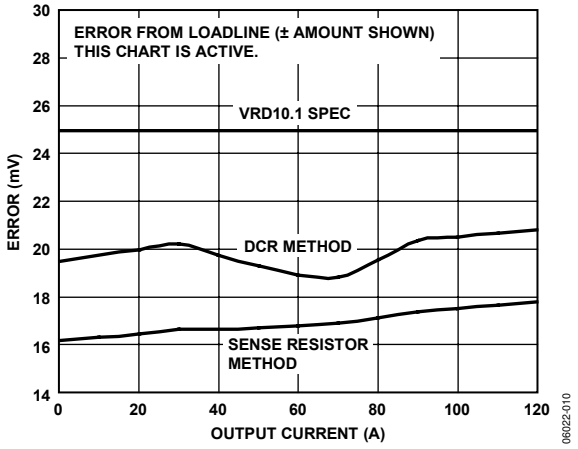


Figure 10. Accuracy Comparison of DCR and Sense Resistor Methods

C_{OUT} SELECTION

The required output decoupling for the regulator is typically recommended by Intel for various processors and platforms. Also, to determine what is required, use some simple design guidelines that are based on having both bulk and ceramic capacitors in the system.

The first thing is to select the total amount of ceramic capacitance. This is based on the number and type of capacitor to be used. The best location for ceramic capacitors is inside the socket, with 12 to 18 of Size 1206 being the physical limit. Additional ceramic capacitors can be placed along the outer edge of the socket as well.

Combined ceramic values of 200 µF to 400 µF are recommended, usually made up of multiple 10 µF or 22 µF capacitors. Select the number of ceramic capacitors, and find the total ceramic capacitance (C_Z).

Next, there is an upper limit imposed on the total amount of bulk capacitance (C_X) when considering the VID OTF voltage stepping of the output (Voltage Step V_V in Time t_V with error of V_{ERR}). A lower limit is based on meeting the capacitance for load release for a given maximum load step, ΔI_O, and a maximum allowable overshoot. The total amount of load release voltage is given as

$$\Delta V_O = \Delta I_O \times R_O + \Delta V_{rl}$$

where ΔV_{rl} is the maximum allowable overshoot voltage.

$$C_{X(MIN)} \geq \left(\frac{L \times \Delta I_O}{n \times \left(R_O + \frac{\Delta V_{rl}}{\Delta I_O} \right) \times V_{VID}} - C_Z \right) \quad (11)$$

$$C_{X(MAX)} = \frac{L}{nK^2 R_O^2} \times \frac{V_V}{V_{VID}} \times \left(\sqrt{1 + \left(t_V \frac{V_{VID}}{V_V} \times \frac{nKR_O}{L} \right)^2} - 1 \right) - C_Z \quad (12)$$

$$\text{where } K = 1n\left(\frac{V_{ERR}}{V_V} \right)$$

To meet the conditions of these equations and transient response, the ESR of the bulk capacitor bank (R_X) should be less than two times the droop resistance (R_O). If the $C_{X(MIN)}$ is larger than $C_{X(MAX)}$, the system cannot meet the VID OTF specification and may require the use of a smaller inductor or more phases (and may need the switching frequency to increase to keep the out-put ripple the same).

This example uses 18, 22 µF 1206 MLC capacitors (C_Z = 396 µF). The VID on-the-fly step change is 450 mV in 230 µs with a settling error of 2.5 mV. The maximum allowable load release overshoot for this example is 50 mV, so solving for the bulk capacitance yields

$$C_{X(MIN)} \leq \left(\frac{280\text{ nH} \times 85\text{ A}}{4 \times \left(1.2\text{ m}\Omega + \frac{50\text{ mV}}{85\text{ A}} \right) \times 1.3\text{ V}} - 396\,\mu\text{F} \right) = 2.16\text{ mF}$$

$$C_{X(MAX)} \leq \frac{280\text{ nH} \times 450\text{ mV}}{4 \times 4.6^2 \times (1.2\text{ m}\Omega)^2 \times 1.3\text{ V}} \times$$

$$\left(\sqrt{1 + \left(\frac{250\,\mu\text{s} \times 1.3\text{ V} \times 4 \times 4.6 \times 1.2\text{ m}\Omega}{450\text{ mV} \times 280\text{ nH}} \right)^2} - 1 \right) - 396\,\mu\text{F} = 40.5\text{ mF}$$

where K = 4.6.

Using four 560 µF Al-Poly capacitors with a typical ESR of 5 mΩ each yields C_X = 2.24 mF with an R_X = 1.25 mΩ.

One last check should be made to ensure that the ESL of the bulk capacitors (L_X) is low enough to limit the high frequency ringing during a load change. This is tested using

$$L_X \leq C_Z \times R_O^2 \times Q^2$$
$$L_X \leq 396\,\mu\text{F} \times (1.2\text{ m}\Omega)^2 \times 2 = 1.14\text{ nH} \quad (13)$$

where Q is limited to the square root of 2 to ensure a critically damped system.

In this example, L_X is approximately 175 pH for the four A1-Polys capacitors, which satisfies this limitation. If the L_X of the chosen bulk capacitor bank is too large, the number of ceramic capacitors may need to be increased if there is excessive ringing.

For this multimode control technique, all ceramic designs can be used as long as the conditions of Equation 11, Equation 12, and Equation 13 are satisfied.

RAMP RESISTOR SELECTION

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. The following equation is used for determining the optimum value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \tag{14}$$

$$R_R = \frac{0.2 \times 280\ \text{nH}}{3 \times 5 \times 6.33\ \text{m}\Omega \times 5\ \text{pF}} = 118\ \text{k}\Omega$$

where:

A_R is the internal ramp amplifier gain
A_D is the current balancing amplifier gain
R_{DS} is the total low-side MOSFET on resistance
C_R is the internal ramp capacitor value.

The internal ramp voltage magnitude can be calculated by using

$$V_R = \frac{A_R \times (1-D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \tag{15}$$

$$V_R = \frac{0.2 \times (1-0.108) \times 1.3\ \text{V}}{118\ \text{k}\Omega \times 5\ \text{pF} \times 1.125\ \text{MHz}} = 350\ \text{m}V$$

The size of the internal ramp can be made larger or smaller. If it is made larger, stability and transient response improve, but thermal balance degrades. Likewise, if the ramp is made smaller, thermal balance improves at the sacrifice of transient response and stability. The factor of 3 in the denominator of Equation 14 sets a ramp size that gives an optimal balance for good stability, transient response, and thermal balance.

COMP PIN RAMP

A ramp signal on the COMP pin is due to the droop voltage and output voltage ramps. This ramp amplitude adds to the internal ramp to produce the following overall ramp signal at the PWM input:

$$V_{RT} = \frac{V_R}{\left(1 - \frac{2 \times (1 - n \times D)}{n \times f_{SW} \times C_X \times R_O}\right)} \tag{16}$$

In this example, the overall ramp signal is 390 mV.

CURRENT-LIMIT SETPOINT

To select the current-limit setpoint, first find the resistor value for R_{LIM}. The current-limit threshold for the ADP3194 is set with a 3 V source (V_{LIM}) across R_{LIM} with a gain of 10.4 mV/μA (A_{LIM}). R_{LIM} can be found using

$$R_{LIM} = \frac{A_{LIM} \times V_{LIM}}{I_{LIM} \times R_O} \tag{17}$$

For values of R_{LIM} greater than 500 kΩ, the current limit can be lower than expected, so some adjustment of R_{LIM} may be needed. Here, I_{LIM} is the average current limit for the output of the supply. In this example, choosing a peak current limit of 185 A for I_{LIM} results in R_{LIM} = 140 kΩ.

The limit of the per-phase current-limit described earlier is determined by

$$I_{PHLIM} \cong \frac{V_{COMP(MAX)} - V_R - V_{BIAS}}{A_D \times R_{DS(MAX)}} + \frac{I_R}{2} \tag{18}$$

For the ADP3194, the maximum COMP voltage ($V_{COMP(MAX)}$) is 3.3 V, the COMP pin bias voltage (V_{BIAS}) is 1.2 V, and the current-balancing amplifier gain (A_D) is 5. Using V_R of 0.35 V and $R_{DS(MAX)}$ of 7 mΩ, the per-phase peak current limit is calculated to be 51.8 A. Although this number may seem high, this current level can be reached only with an absolute short at the output, and the current-limit latch-off function shuts down the regulator before overheating can occur.

This limit can be adjusted by changing the ramp voltage (V_R), but make sure not to set the per-phase limit lower than the average per-phase current (I_{LIM}/n).

The per-phase initial duty cycle limit is determined by

$$D_{MAX} = D \times \frac{V_{COMP(MAX)} - V_{BIAS}}{V_{RT}} \tag{19}$$

In this example, the maximum duty cycle is 0.46.

FEEDBACK LOOP COMPENSATION DESIGN

Optimized compensation of the ADP3194 allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including dc, and equal to the droop resistance (R_O).

With the resistive output impedance, the output voltage droops in proportion to the load current at any load current slew rate. This ensures optimal positioning and allows minimization of the output decoupling.

With the multimode feedback structure of the ADP3194, the feedback compensation must be set to make the converter's output impedance, working in parallel with the output decoupling, to meet this goal. Several poles and zeros created by the output inductor and decoupling capacitors (output filter) need to be compensated for.

A type-three compensator on the voltage feedback is adequate for proper compensation of the output filter. Equation 20 to Equation 28 yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects (see the Layout and Component Placement section).

The first step is to compute the time constants for all of the poles and zeros in the system:

$$R_E = n \times R_O + A_D \times R_{DS} + \frac{R_{SENSE} \times V_{RT}}{V_{VID}} + \frac{2 \times L \times (1 - n \times D) \times V_{RT}}{n \times C_X \times R_O \times V_{VID}} \quad (20)$$

$$T_A = C_X \times (R_O - R') + \frac{L_X}{R_O} \times \frac{R_O - R'}{R_X} \quad (21)$$

$$T_B = (R_X + R' - R_O) \times C_X \quad (22)$$

$$T_C = \frac{V_{RT} \times \left(L - \frac{A_D \times R_{DS}}{2 \times f_{SW}} \right)}{V_{VID} \times R_E} \quad (23)$$

$$T_D = \frac{C_X \times C_Z \times R_O^2}{C_X \times (R_O - R') + C_Z \times R_O} \quad (24)$$

where:

R' is the PCB resistance from the bulk capacitors to the ceramics
R_{DS} is the total low-side MOSFET on resistance per phase.

In this example, A_D is 5, V_{RT} equals 0.39 V, R' is approximately 0.5 mΩ (assuming a 4-layer, 1 ounce motherboard), and L_X is 175 pH for the four Al-Poly capacitors.

The compensation values can then be solved using the following equations:

$$C_A = \frac{n \times R_O \times T_A}{R_E \times R_B} \quad (25)$$

$$R_A = \frac{T_C}{C_A} \quad (26)$$

$$C_B = \frac{T_B}{R_B} \quad (27)$$

$$C_{FB} = \frac{T_D}{R_A} \quad (28)$$

These are the starting values, prior to tuning the design, to account for layout and other parasitic effects (see the Layout and Component Placement section).

The final values selected after tuning are

C_A = 3.3 nF,
R_A = 7.32 kΩ,
C_B = 1 nF,
C_{FB} = 33 pF.

Figure 11 and Figure 12 show the typical transient response using these compensation values.

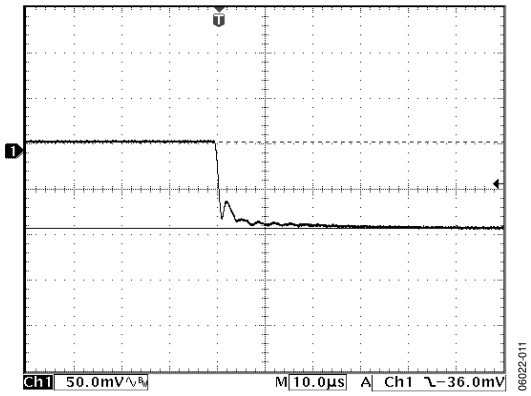


Figure 11. Typical Transient Response for Design Example Load Step

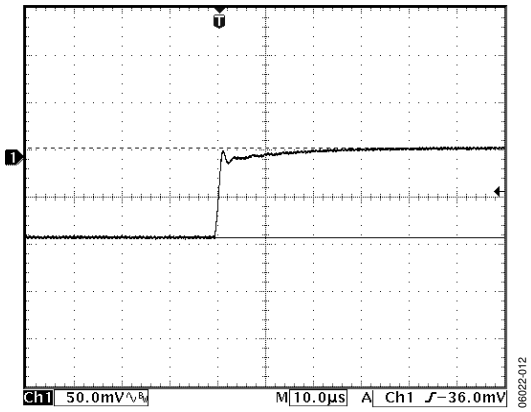


Figure 12. Typical Transient Response for Design Example Load Release

C_{IN} SELECTION AND INPUT CURRENT di/dt REDUCTION

In continuous inductor current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to $n \times V_{OUT}/V_{IN}$ and an amplitude of one-nth the maximum output current. To prevent large voltage transients, a low ESR input capacitor, sized for the maximum rms current, must be used. The maximum rms capacitor current is given by

$$I_{CRMS} = D \times I_O \times \sqrt{\frac{1}{N \times D} - 1} \quad (29)$$

$$I_{CRMS} = 0.108 \times 119\,\text{A} \times \sqrt{\frac{1}{4 \times 0.108} - 1} = 14.7\,\text{A}$$

The capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors can be placed in parallel to meet size or height requirements in the design. In this example, the input capacitor bank is formed by two 2700 µF, 16 V aluminum electrolytic capacitors and eight 4.7 µF ceramic capacitors.

To reduce the input current di/dt to a level below the recommended maximum of 0.1 A/µs, an additional small inductor (L > 370 nH at 18 A) should be inserted between the converter and the supply bus. This inductor also acts as a filter between the converter and the primary power source.

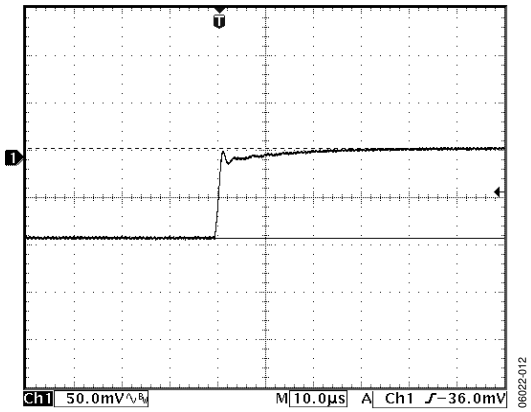


Figure 13. Efficiency of the Circuit of Figure 10 vs. Output Current

TUNING THE ADP3194

1. Build a circuit based on the compensation values computed from the equations used in the example.
2. Hook up the dc load to circuit, turn it on, and verify its operation. Also, check for jitter at no load and full load.

DC Load Line Setting

3. Measure the output voltage at no load (V_{NL}). Verify it is within tolerance.
4. Measure the output voltage at full load cold (V_{FLCOLD}). Let the board sit for ~10 minutes at full load, and then measure the output (V_{FLHOT}). If there is a change of more than a few millivolts, adjust R_{CS1} and R_{CS2}, using Equation 30 and Equation 31.

$$R_{CS2(NEW)} = R_{CS2(OLD)} \times \frac{V_{NL} - V_{FLCOLD}}{V_{NL} - V_{FLHOT}} \quad (30)$$

5. Repeat Step 4 until the cold and hot voltage measurements remain the same.
6. Measure the output voltage from no load to full load, using 5 Amps steps. Compute the load line slope for each change, and then average to get the overall load line slope (R_{OMEAS}).
7. If R_{OMEAS} is off from R_O by more than 0.05 mΩ, use the following to adjust the R_{PH} values:

$$R_{PH(NEW)} = R_{PH(OLD)} \times \frac{R_{OMEAS}}{R_O} \quad (31)$$

8. Repeat Step 6 and Step 7 to check the load line, and repeat adjustments if necessary.
9. Once the dc load line adjustment is complete, do not change R_{PH}, R_{CS1}, R_{CS2}, or R_{TH} for the remainder of the procedure.
10. Measure the output ripple at no load and full load with a scope, and make sure it is within specifications.

$$R_{CS1(NEW)} = \frac{1}{\frac{R_{CS1(OLD)} + R_{TH(25°C)}}{R_{CS1(OLD)} \times R_{TH(25°C)} + \left(R_{CS1(OLD)} - R_{CS2(NEW)}\right) \times \left(R_{CS1(OLD)} - R_{TH(25°C)}\right)} - \frac{1}{R_{TH(25°C)}}} \quad (32)$$

AC Load Line Setting

11. Remove the dc load from the circuit and hook up the dynamic load.
12. Hook up the scope to the output voltage and set it to dc coupling, with the time scale at 100 µs/div.
13. Set the dynamic load for a transient step of about 40 A at 1 kHz with a 50% duty cycle.
14. Measure the output waveform (if not visible, use dc offset on scope to view). Try to use a vertical scale of 100 mV/div or finer. This waveform should look similar to Figure 14.

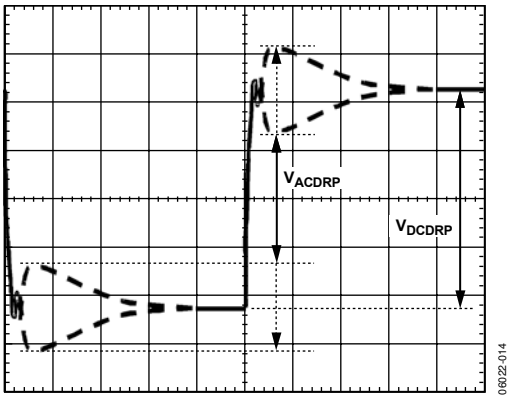


Figure 14. AC Load Line Waveform

15. Use the horizontal cursors to measure V_{ACDRP} and V_{DCDRP}, as shown in Figure 14. Do not measure the undershoot or overshoot that happens immediately after this step.

    If V_{ACDRP} and V_{DCDRP} are different by more than a few millivolts, use Equation 38 to adjust C_{CS}. It may be necessary to parallel different values to get the correct one, because there are limited standard capacitor values available. It is a good idea to have locations for two capacitors in the layout for this.

$$C_{CS(NEW)} = C_{CS(OLD)} \times \frac{V_{ACDRP}}{V_{DCDRP}} \quad (38)$$

16. Repeat Step 11 to Step 13, and repeat the adjustments, if necessary. Once complete, do not change C_{CS} for the remainder of the procedure.
17. Set the dynamic load step to maximum step size. Do not use a step size larger than needed, and verify that the output waveform is square, which means that V_{ACDRP} and V_{DCDRP} are equal.

Initial Transient Setting

18. With the dynamic load still set at the maximum step size, expand the scope time scale to see 2 µs/div to 5 µs/div. The waveform may have two overshoots and one minor undershoot (see Figure 15). Here, V_{DROOP} is the final desired value.

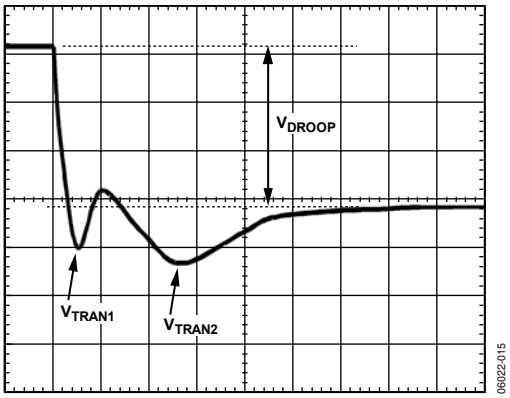


Figure 15. Transient Setting Waveform

19. If both overshoots are larger than desired, try making the following adjustments:

    Make the ramp resistor larger by 25% (R_{RAMP}).

    For V_{TRAN1}, increase C_B, or increase the switching frequency.

    For V_{TRAN2}, increase R_A, and decrease C_A by 25%.

    If these adjustments do not change the response, the output decoupling is the limiting factor. Check the output response every time a change is made, or nodes are switched, to make sure the response remains stable.

20. For load release (see Figure 16), if $V_{TRANREL}$ is larger than V_{TRAN1} (see Figure 15), there is not enough output capacitance. Either more capacitance is needed or the inductor values need to be smaller. If inductors are changed, start the design again using the spreadsheet and this tuning procedure.

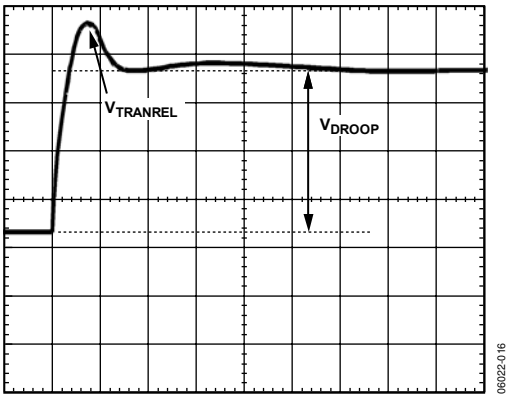


Figure 16. Transient Setting Waveform

Because the ADP3194 turns off all of the phases (switches inductors to ground), there is no ripple voltage present during load release. Thus, headroom does not need to be added for ripple, allowing load release ($V_{TRANREL}$) to be larger than V_{TRAN1} by the amount of ripple and still meet specifications.

If V_{TRAN1} and $V_{TRANREL}$ are less than the desired final droop, this implies that capacitors can be removed. When removing capacitors, also check the output ripple voltage to make sure it is still within specifications.

RAMPADJ FILTER

It is recommended that a filter be placed on the RAMPADJ line. On the ADP3194, the VCC is 5 V, but the RAMPADJ still needs to be connected to the 12 V input supply. Therefore, the filter is needed to remove noise from the 12 V input supply. A 1 kΩ resistor and 1 µF cap are recommended for this filter.

SHUNT RESISTOR DESIGN

When replacing an existing ADP3181 design with the ADP3194, the shunt resistor value needs to be determined. A trade-off can be made between the power dissipated in the shunt resistor and the UVLO threshold. Figure 17 shows the typical resistor value needed to realize certain UVLO voltages. It also gives the maximum power dissipated in the shunt resistor for these UVLO voltages. The maximum power dissipated is calculated using Equation 33.

$$P_{MAX} = \frac{\left(V_{IN(MAX)} - V_{CC(MIN)}\right)^2}{R_{SHUNT}} \quad (33)$$

where:

$V_{IN(MAX)}$ is the maximum voltage from the 12 V input supply. (If the 12 V input supply is 12 V ±5%, then $V_{IN(MAX)}$ = 12.6 V. If the 12 V input supply is 12 V ±10%, then $V_{IN(MAX)}$ = 13.2 V.) Figure 17 shows the power when $V_{IN(MAX)}$ = 12.6 V.

$V_{CC(MIN)}$ is the minimum V_{CC} voltage of the ADP3194. It is specified as 4.75 V.

R_{SHUNT} is the shunt resistor value.

The CECC standard specification for power rating in surface mount resistors is 0603 = 0.1 W, 0805 = 0.125 W, 1206 = 0.25 W. For example, UVLO voltage specification = 8 V.

From Figure 17, a shunt resistor value of 420 Ω is recommended. From Figure 17, the power dissipation is 140 mW. The user can choose any of the following:

Two 840 Ω, 0603 resistors in parallel

Two 840 Ω, 0805 resistors in parallel

One 420 Ω, 1206 resistor.

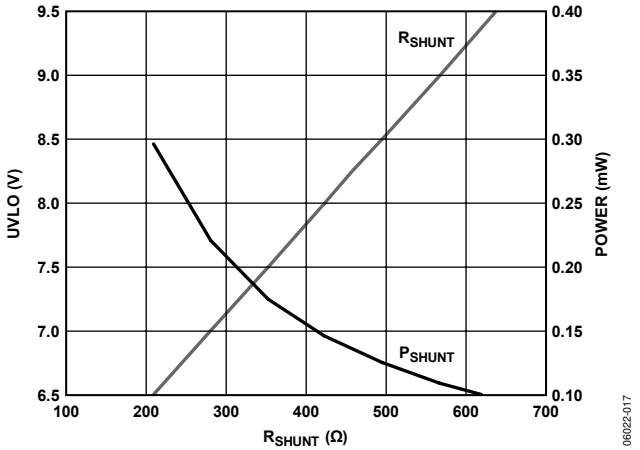


Figure 17. Typical Shunt Resistor Value and Power Dissipation for Different UVLO Voltages

DESIGN EXAMPLE USING DCR METHOD

The following are guidelines for designs that use an inductor DCR method instead of sense resistor method.

INDUCTOR SELECTION USING DCR

Use the method and equations described in the Inductor Selection section to calculate the inductor. An important factor in the inductor design is the DCR, which is used for measuring the phase currents. A large DCR can cause excessive power losses, while too small a value can lead to increased measurement error. A good rule is to have the DCR be about 1 to 1½ times the droop resistance (R_O). For this design, an inductor with a DCR of 1.4 mΩ is used.

DESIGNING AN INDUCTOR USING DCR

Once the inductance and DCR are known, the next step is either to design an inductor or to find a standard inductor that comes as close as possible to meeting the overall design goals. It is also important to have the inductance and DCR tolerance specified to control the accuracy of the system. 15% inductance and 8% DCR (at room temperature) are reasonable tolerances most manufacturers can meet.

INDUCTOR DCR TEMPERATURE CORRECTION

With the inductors DCR being used as the sense element and copper wire being the source of the DCR, compensation is needed for temperature changes of the inductor's winding. Fortunately, copper has a well-known temperature coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite and equal percentage change in resistance to that of the wire, it cancels the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, Resistor R_{CS1} and Resistor R_{CS2} are needed. See Figure 18 to linearize the NTC and produce the desired temperature tracking.

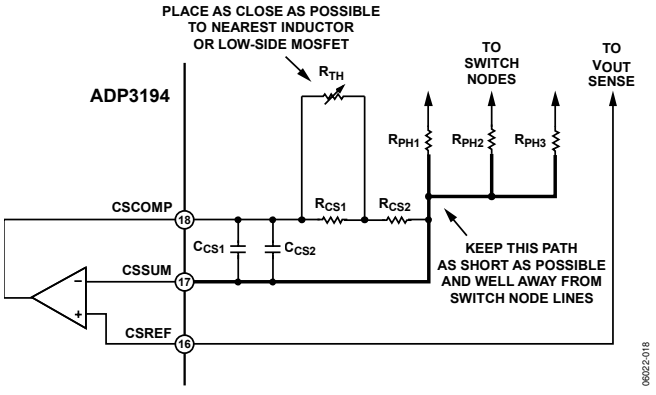


Figure 18. Temperature Compensation Circuit Values

The following procedure and equations yield values to use for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value.

Select an NTC based on type and value. Because there is not a value yet, start with a thermistor with a value close to R_{CS}. The NTC should also have an initial tolerance of better than 5%.

Based on the type of NTC, find its relative resistance value at two temperatures. The temperatures that work well are 50°C and 90°C. These resistance values are called A ($R_{TH(50°C)}/R_{TH(25°C)}$) and B ($R_{TH(90°C)}/R_{TH(25°C)}$). The NTC's relative value is always 1 at 25°C.

Find the relative values of R_{CS} required for each of these temperatures. This is based on the percentage change needed, which in this example is initially 0.39%/°C. These are called r_1 ($1/(1 + TC \times (T_1 - 25))$) and r_2 ($1/(1 + TC \times (T_2 - 25))$), where $TC = 0.0039$ for copper. $T_1 = 50°C$ and $T_2 = 90°C$ are chosen. From this, calculate that $r_1 = 0.9112$ and $r_2 = 0.7978$.

Compute the relative values for R_{CS2}, R_{CS1}, and R_{TH} using

$$R_{CS2} = \frac{(A-B)\times r_1 \times r_2 - A\times(1-B)\times r_2 + B\times(1-A)\times r_1}{A\times(1-B)\times r_1 - B\times(1-A)\times r_2 - (A-B)} \quad (34)$$

$$R_{CS1} = \frac{(1-A)}{\frac{1}{1-R_{CS2}} - \frac{A}{r_1 - R_{CS2}}} \quad (35)$$

$$R_{TH} = \frac{1}{\frac{1}{1-R_{CS2}} - \frac{1}{R_{CS1}}} \quad (36)$$

Calculate $R_{TH} = R_{TH} \times R_{CS}$, then select the closest value of thermistor available. Also, compute a scaling factor k based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \quad (37)$$

Calculate values for R_{CS1} and R_{CS2} using Equation 38 and Equation 39:

$$R_{CS1} = R_{CS} \times k \times R_{CS1} \quad (38)$$

$$R_{CS2} = R_{CS} \times \left((1-k) + \left(k \times R_{CS2}\right)\right) \quad (39)$$

For this example, R_{CS} has been calculated to be 110 kΩ. Start with a thermistor value of 100 kΩ. Next, look through the available 0603-size thermistors, and find a Vishay NTHS0603N01N1003JR NTC thermistor with A = 0.3602 and B = 0.09174. From these, compute $R_{CS1} = 0.3795$, $R_{CS2} = 0.7195$, and $R_{TH} = 1.075$. Solve for R_{TH}, which yields 118.28 kΩ. Then, choose 100 kΩ, which makes $k = 0.8455$. Finally, R_{CS1} and R_{CS2} are 35.3 kΩ and 83.9 kΩ. Choose the closest 1% resistor values, which yield a choice of 35.7 kΩ or 84.5 kΩ.

OUTPUT DROOP RESISTANCE–DCR METHOD

The design requires the regulator output voltage measured at the CPU pins to drop when the output current increases. The specified voltage drop corresponds to a dc output resistance (R_O).

The output current is measured by summing the voltage across each inductor and passing the signal through a low-pass filter. This summer filter is the CS amplifier configured with $R_{PH(X)}$ (summers), R_{CS}, and C_{CS} (filter). The output resistance of the regulator is set by the following equations:

$$R_O = \frac{R_{CS}}{R_{PH(X)}} \times R_L \quad (40)$$

$$C_{CS} = \frac{L}{R_L \times R_{CS}} \quad (41)$$

where R_L is the DCR of the output inductors.

The user has the flexibility of choosing either R_{CS} or $R_{PH(X)}$. It is best to select R_{CS} (equal to 100 kΩ) and then solve for $R_{PH(X)}$ by rearranging Equation 6.

$$R_{PH(X)} = \frac{R_L}{R_O} \times R_{CS} \quad (42)$$

$$R_{PH(X)} = \frac{1.0\ \text{m}\Omega}{1.2\ \text{m}\Omega} \times 100\ \text{k}\Omega = 82.5\ \text{k}\Omega$$

Next, use Equation 41 to solve for C_{CS}.

$$C_{CS} = \frac{280\ \text{nH}}{1.0\ \text{m}\Omega \times 100\ \text{k}\Omega} = 2.8\ \text{nF}$$

It is best to have a dual location for C_{CS} in the layout, so that standard values can be used in parallel to get as close as possible to the value desired. For accuracy, C_{CS} should be a 5% or 10% NPO capacitor. This example uses a 5% combination for C_{CS} of 2.2 nF and 560 pF in parallel.

POWER MOSFETS

This section is only applicable if power MOSFETs need to be selected.

For this example, the N-channel power MOSFETs have been selected for one high-side switch and two low-side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. The minimum gate drive voltage (the supply voltage to the ADP3120A) dictates whether standard threshold or logic-level threshold MOSFETs must be used. With V_{GATE} ~10 V, logic-level threshold MOSFETs ($V_{GS(TH)}$°< 2.5 V) are recommended.

The maximum output current (I_O) determine1s the $R_{DS(ON)}$ requirement for the low-side (synchronous) MOSFETs. With the ADP3194, currents are balanced between phases, thus the current in each low-side MOSFET is the output current divided by the total number of MOSFETs (n_{SF}). With conduction losses being dominant, the following equation shows the total power being dissipated in each synchronous MOSFET in terms of the ripple current per phase (I_R) and average total output current (I_O):

$$P_{SF} = (1-D) \times \left[\left(\frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left(\frac{n\, I_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad (43)$$

Knowing the maximum output current being designed for and the maximum allowed power dissipation, it is possible to find the required $R_{DS(ON)}$ for the MOSFET. For D-PAK MOSFETs up to an ambient temperature of 50°C, a safe limit for P_{SF} is 1 W to 1.5 W at 120°C junction temperature. Thus, for this example (119 A maximum), $R_{DS(SF)}$ (per MOSFET) < 7.5 mΩ. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C, so be certain to account for this temperature when making this selection. This example uses two lower-side MOSFETs at 4.8 mΩ each at 120°C.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input needs to be small (less than 10% is recommended) to prevent accidental turn-on of the synchronous MOSFETs when the switch node goes high.

Also, the time to switch the synchronous MOSFETs off should not exceed the nonoverlap dead time of the MOSFET driver (40 ns typical for the ADP3120A). The output impedance of the driver is approximately 2 Ω,and the typical MOSFET input gate resistances are about 1 Ωto 2 Ω, so a total gate capacitance of less than 6000 pF should be adhered to. Because there are two MOSFETs in parallel, the input capacitance for each synchronous MOSFET should be limited to 3000 pF.

The high-side (main) MOSFET has to be able to handle two main power dissipation components: conduction and switching losses. The switching loss is related to the amount of time it takes for the main MOSFET to turn on and off and to the current and the voltage that are being switched.

Basing the switching speed on the rise and fall time of the gate driver impedance and MOSFET input capacitance, the following equation provides an approximate value for the switching loss per main MOSFET:

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \quad (44)$$

where:

n_{MF} is the total number of main MOSFETs,

R_G is the total gate resistance (2 Ω for the ADP3120A and about 1 Ω for typical high speed switching MOSFETs, making R_G = 3 Ω),

C_{ISS} is the input capacitance of the main MOSFET.

Adding more main MOSFETs (n_{MF}) does not really help the switching loss per MOSFET because the additional gate capacitance slows switching. The best way to reduce switching loss is to use lower gate capacitance devices.

The conduction loss of the main MOSFET is given by the following equation:

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad (45)$$

where $R_{DS(MF)}$ is the on resistance of the MOSFET.

Typically, for main MOSFETs, the highest speed (low C_{ISS}) device is preferred, but these usually have higher on resistance. Select a device that meets the total power dissipation (about 1.5 W for a single D-PAK) when combining the switching and conduction losses.

For this example, an NTD40N03L was selected as the main MOSFET (eight total; n_{MF} = 8), with a C_{ISS} = 584 pF (maximum) and $R_{DS(MF)}$ = 19 mΩ (maximum at T_J = 120°C). An NTD110N02L was selected as the synchronous MOSFET (eight total; n_{SF} = 8), with C_{ISS} = 2710 pF (maximum) and $R_{DS(SF)}$ = 4.8 mΩ (maximum at T_J = 120°C). The synchronous MOSFET C_{ISS} is less than 3000 pF, satisfying that requirement. Solving for the power dissipation per MOSFET at IO = 119 A and IR = 11 A yields 958 mW for each synchronous MOSFET and 872 mW for each main MOSFET. These numbers comply with the guideline to limit the power dissipation to 1 W per MOSFET.

One last thing to consider is the power dissipation in the driver for each phase. This is best described in terms of the Q_G for the MOSFETs and is given by the following equation:

$$P_{DRV} = \left[\frac{f_{SW}}{2 \times n} \times \left(n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF} \right) + I_{CC} \right] \times V_{CC} \quad (45)$$

where:

Q_{GMF} is the total gate charge for each main MOSFET

Q_{GSF} is the total gate charge for each synchronous MOSFET

The standby dissipation factor for the driver is $I_{CC} \times V_{CC}$. For the ADP3120A, the maximum dissipation should be less than 400 mW. In this example (with I_{CC} = 7 mA, Q_{GMF} = 5.8 nC, and Q_{GSF} = 48 nC) 297 mW is found in each driver, which is below the 400 mW dissipation limit. See the ADP3120A data sheet for more details.

LAYOUT AND COMPONENT PLACEMENT

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

GENERAL RECOMMENDATIONS

For good results, a PCB with at least four layers is recommended. This allows the needed versatility for control circuitry interconnections with optimal placement; power planes for ground, input, and output power; and wide interconnection traces in the remainder of the power delivery current paths.

Each square unit of 1 ounce copper trace has a resistance of ~0.53 mΩ at room temperature.

Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths. Then, the resistance and inductance introduced by these current paths is minimized, and the via current rating is not exceeded.

If critical signal lines, including the output voltage sense lines of the ADP3194, must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making the signal ground noisier.

Use an analog ground plane around and under the ADP3194 as a reference for the components associated with the controller. This plane should be tied to the nearest output decoupling capacitor ground and not tied to any other power circuitry. This prevents power currents from flowing in the ground plane.

Locate the components around the ADP3194 close to the controller with short traces. The most important traces to keep short, and away from other traces, are the FB pin and the CSSUM pin. Connect the output capacitors as close as possible to the load (or connector), for example, a microprocessor core that receives the power. If the load is distributed, the capacitors should also be distributed and generally be in proportion to where the load tends to be more dynamic.

Avoid crossing any signal lines over the switching power path loop, as described in the Power Circuitry Recommendations section.

POWER CIRCUITRY RECOMMENDATIONS

The switching power path should be routed on the PCB to encompass the shortest possible length in order to minimize radiated switching noise energy (that is, EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise-related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs, including all interconnecting PCB traces and planes. Using short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing; and it accommodates the high current demand with minimal voltage loss.

Whenever a power dissipating component, (for example, a power MOSFET), is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. This improves current rating through the vias and also improves thermal performance from vias extended to the opposite side of the PCB, where a plane can more readily transfer the heat to the air. Make a mirror image of any pad being used to heat-sink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation to the air around the board. To further improve thermal performance, use the largest possible pad area.

The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.

For best EMI containment, a solid power ground plane should be used as one of the inner layers extending fully under all the power components.

SIGNAL CIRCUITRY RECOMMENDATIONS

The output voltage is sensed and regulated between the FB pin and the FBRTN pin, which connect to the signal ground at the load. To avoid differential-mode noise pickup in the sensed signal, the loop area should be small. Thus, the FB and FBRTN traces should be routed adjacent to each other on top of the power ground plane back to the controller.

The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be Kelvin connected through a 10 Ω resistor to the center point of the copper bar, which is the V_{CORE} common node for the inductors of all the phases (see Figure 19 and Figure 20).

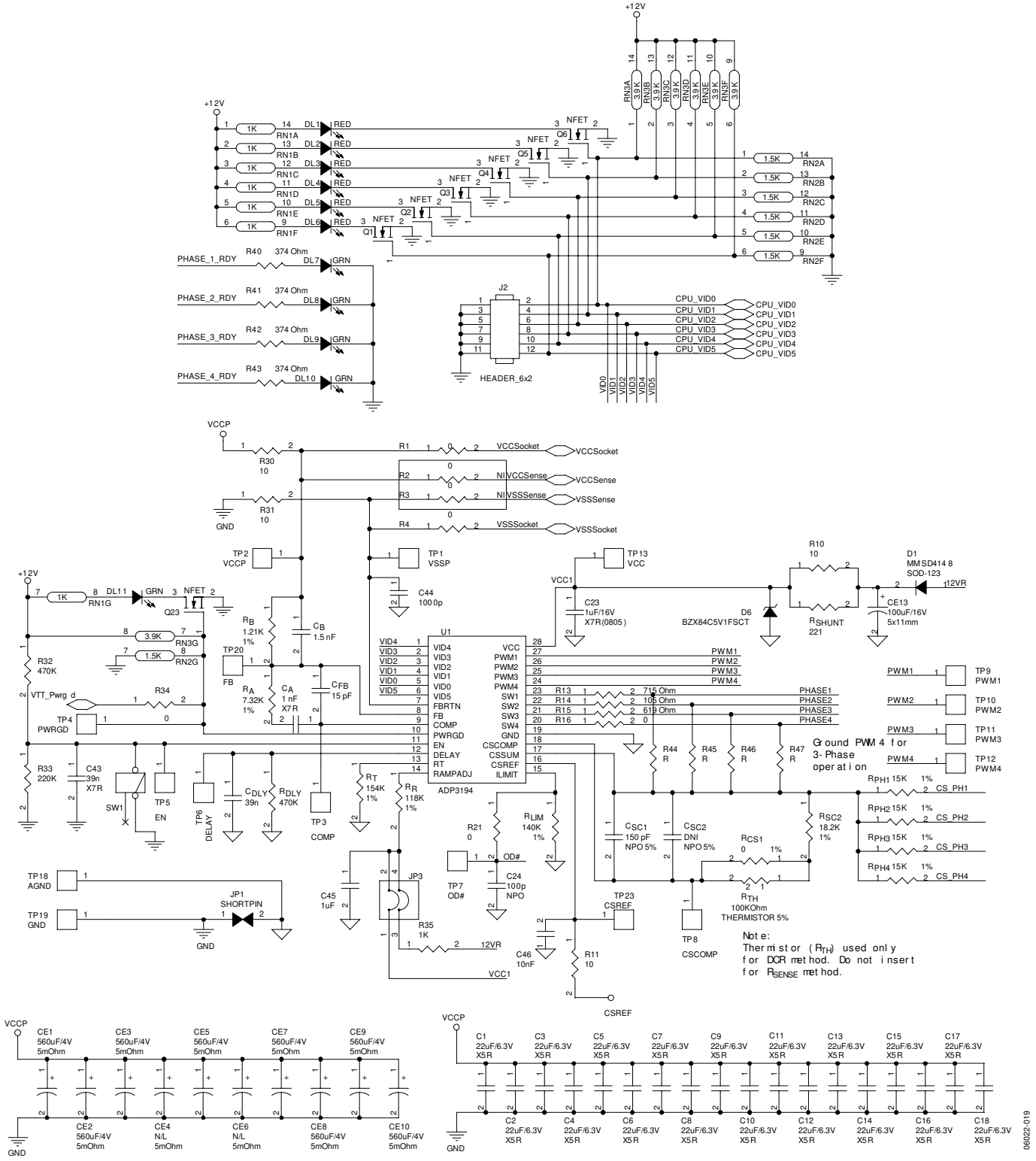


Figure 19. Typical Applications Schematic Part 1

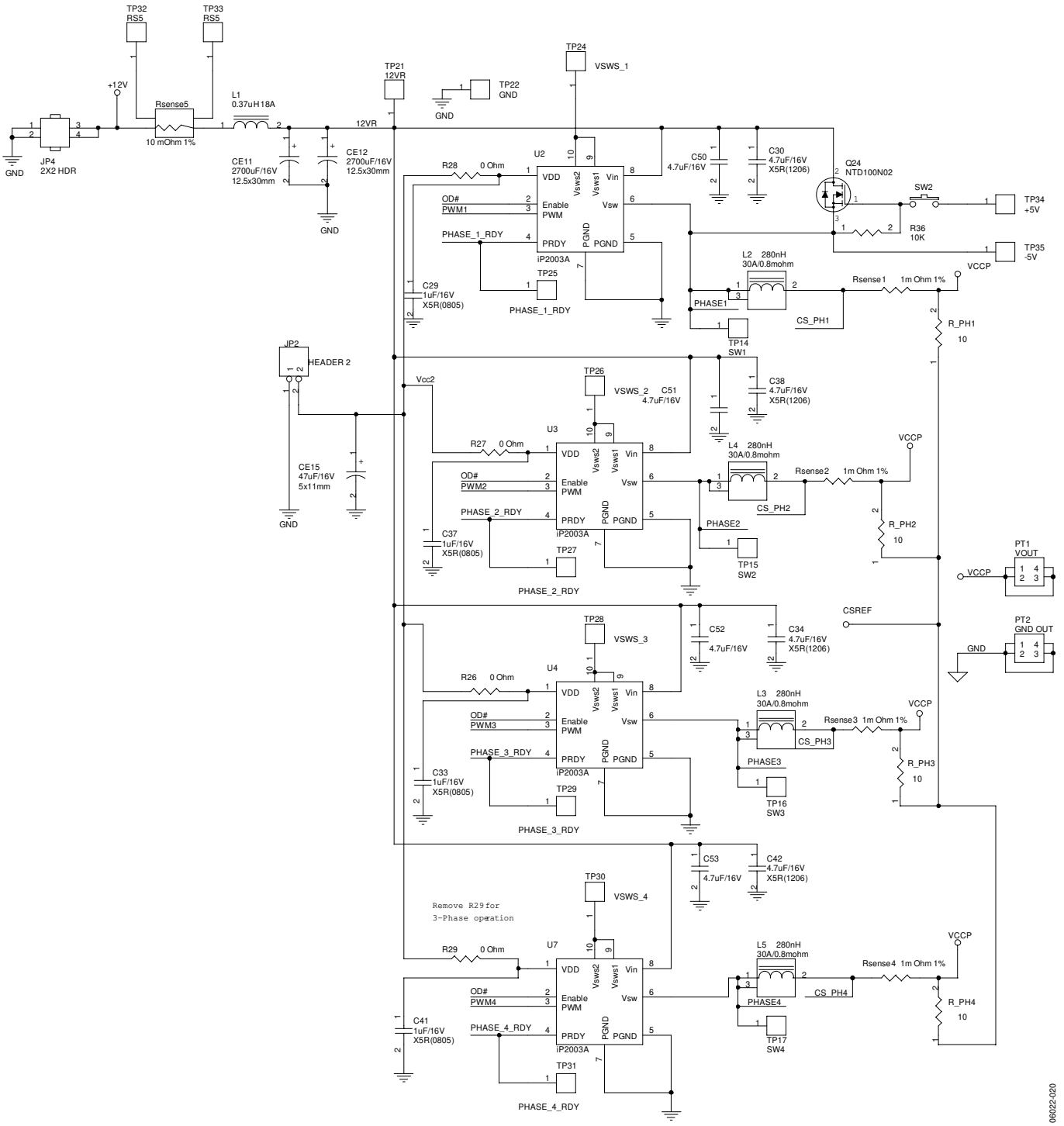
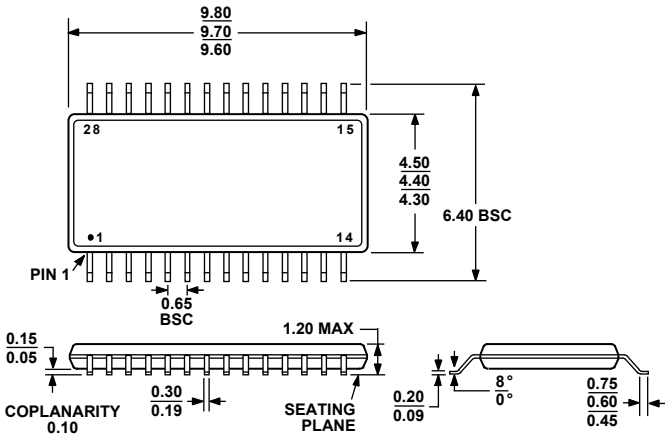


Figure 20. Typical Applications Schematic Part 2

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AE

Figure 21. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADP3194JRUZ-RL[1]	0°C to +85°C	28-Lead TSSOP 13" Reel	RU-28	2500

[1] Z = Pb-free part.

NOTES

NOTES

NOTES

D06022-0-10/06(0)