

TPS65263EVM-645 PMIC with I²C Controlled DVS Evaluation Module

This document presents the information required to operate the TPS65263 power-management integrated circuit (PMIC) as well as the support documentation including schematic, layout, hardware setup, and bill of materials.

1	Backg	round	1	
2	TPS65263EVM Schematic			
3	Board	Layout	4	
4	Bench	Test Setup Conditions	7	
	4.1	Headers Description and Jumper Placement	7	
	4.2	Hardware Requirement	8	
	4.3	Hardware Setup	8	
	4.4	Software Install	9	
	4.5	Software Operation	10	
5	5 Power-Up Procedure		11	
6	Bill of Materials			

List of Figures

1	TPS65263 Schematic	3
2	Component Placement (Top Layer)	4
3	Board Layout (Top Layer)	4
4	Board Layout (Second Layer)	5
5	Board Layout (Third Layer)	5
6	Board Layout (Bottom Layer)	6
7	Headers Description and Jumper Placement	7
8	USB Interface Adapter Quick Connection Diagram	9
9	Screen Capture of TPS65263 Software GUI Interface	10

List of Tables

1	Summary of Performance	2
2	Input/Output Connection	8
3	Jumpers	8
4	Bill of Materials	12

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1 Background

The TPS65263 PMIC is a triple 3-A, 2-A, 2-A output current, synchronous step-down (buck) converter with an operational range of 4.5 V to 18 V.



Background

2

The TPS65263 is equipped with I²C-compatible bus for communication with system on-chip (SoC) to control buck converters. The output voltage of each buck can be dynamically scaled from 0.68 V to 1.95 V in 10-mV step with I²C controlled 7 bits VID. The VID voltage transition slew rate is programmable with 3-bits control through I²C bus to optimize overshoot or undershoot during VID voltage transition. I²C also controls enabling and disabling output voltage, setting the pulse skipping mode (PSM) or force continuous current mode (FCC) at light load condition, and reading the power good status, overcurrent warning, and die temperature warning.

As there are many possible options to set the converters, Table 1 presents the performance specification summary for the EVM.

Test Conditions	Performance
VIN = 4.5 V to 18 V fsw = 600 kHz (25°C ambient)	Buck1, 1.5 V, up to 3 A Buck2, 1.2 V, up to 2 A Buck3, 2.5 V, up to 2 A

Table 1. Summary of Performance

The evaluation module is designed to provide access to the features of the TPS65263. Some modifications can be made to this module to test performance at different input and output voltages for bucks. Contact the TI Field Applications Group for assistance.



TPS65263EVM Schematic

2 TPS65263EVM Schematic

Figure 1 illustrates the EVM schematic.





Board Layout

3 **Board Layout**

Figure 2 through Figure 6 show the PCB board layouts.



Figure 2. Component Placement (Top Layer)



Figure 3. Board Layout (Top Layer)





Figure 4. Board Layout (Second Layer)



Figure 5. Board Layout (Third Layer)

5





Figure 6. Board Layout (Bottom Layer)



4 Bench Test Setup Conditions

4.1 Headers Description and Jumper Placement

Figure 7 illustrates header and jumper placement on the EVM.



Figure 7. Headers Description and Jumper Placement

Test points:

A: LX of VOUT1 B: LX of VOUT2 C: LX of VOUT3

VOUT1, VOUT2, VOUT3, VIN, SDA, SCL



Table 2. Input/Output Connection

No.	Function	Description
J1	Buck1 Connector	Output of Buck1
J2	Buck2 Connector	Output of Buck2
J3	Buck3 Connector	Output of Buck3
J4	Buck1, Buck2, Buck3 VIN Connector	Apply power supply to this connector
J5	I ² C Interface connector	Communication via I ² C Interface

Table 3. Jumpers

No.	Function	Placement	Comment
J6	Buck1 enable (EN1)	Connect EN1 to GND to disable VOUT1, connect EN1 to VIN through a 100- $k\Omega$ resistor to enable VOUT1; leave open to enable VOUT1	
J7	Buck2 enable (EN2)	Connect EN2 to GND to disable VOUT2, connect EN2 to VIN through a 100- $k\Omega$ resistor to enable VOUT2; leave open to enable VOUT2	
J8	Buck3 enable (EN3)	Connect EN3 to GND to disable VOUT3, connect EN3 to VIN through a 100- $k\Omega$ resistor to enable VOUT3; leave open to enable VOUT3	

4.2 Hardware Requirement

This EVM requires an external power supply capable of providing 4.5 V to 18 V at 6 A.

The EVM kit needs a USB-TO-GPIO interface box which, when installed on a PC and connected to the EVM, allows communication with the EVM via a GUI interface. The USB-TO-GPIO interface box can be ordered in the TI store.

The minimum PC requirements are:

- Microsoft® Windows® 2000 or Windows XP operating system
- USB port
- Minimum of 30 MB of free hard disk space (100 MB recommended)
- Minimum of 256 MB of RAM

4.3 Hardware Setup

8

After connecting the power supply to J4, turn on the power supply, and connect J6, J7, and J8 to high or leave open, the EVM regulates the output voltages to the value per Table 1. Additional input capacitance may be required in order to mitigate the inductive voltage droop that may occur during a load-transient event.

In order to change the output voltage by sending the digital control signal via a PC running the TPS65263 controller software and USB-TO-GPIO interface box, perform the following steps:

- Step 1. Connect one end of the USB-TO-GPIO box to the PC using the USB cable and the other end to J5 of the TPS65263 using the supplied 10-pin ribbon cable per Figure 8. The connectors on the ribbon cable are keyed to prevent incorrect installation.
- Step 2. Connect the power supply on J4 and turn on the power supply.
- Step 3. Run the software as explained in Section 4.4.





Figure 8. USB Interface Adapter Quick Connection Diagram

4.4 Software Install

If you are installing from the TI Web site, go to www.ti.com.

NOTE: This installation page is best viewed with Microsoft Internet Explorer® browser (the web page may not work correctly with other browsers).

Click on the *Install* button. Your PC should give you a security warning asking if you want to install this application. Select *Install* to proceed. If a pre-release or Beta version is currently installed on your PC, you must uninstall this version of the software before installing the final version.

The software attempts to install the Microsoft .NET Framework 2.0 (if it is not already installed). This framework is required for the software to run.

To run the software after installation, go to Start \rightarrow All programs \rightarrow Texas Instruments \rightarrow TPS65263 EVM Software.

At start-up, the software first checks the firmware version of the USB-TO-GPIO adapter box. If an incorrect firmware version is installed, the software automatically searches on the Internet (if connected) for updates. If a new update is available, the software notifies of the update, downloads, and installs the software. Note that after the firmware is updated, the USB cable must be disconnected and then reconnected between the adapter and PC, as instructed during the install process. The host PC software also automatically searches on the Internet (if connected) for updates and ownloads and installs it. During future software uses, you may be prompted to install a new version if one becomes available on the Web.

NOTE: VERISIGN® Code Signing is used to prevent any malicious code from changing this application. If at any time in the future the binaries are modified, the code no longer attempts to run.

Bench Test Setup Conditions

4.5 Software Operation

This section provides descriptions of the EVM software.

The supplied software is used to communicate with the TPS65263 EVM. Click on the icon on the host computer to start the software. The software displays the main control panel for the user interface.

c mode selection	option Check "Shutdown" box to shut down	k to output voltage by VID when "Write" button is pushed
Texas Instrumer	nts - TPS65263 EVM - GUI v1.0.0.0	
File Help		
Read Write	Auto Read Every 20 Sec 👻 Write On Change: ON	- 12C Address 60 → 12C Activity R I=60 A=06 D=07 C=45
Vout 1		
Vour		Reg A 7 6 5 4 3 2 1 0 D W
Mode	PSM at Light Load 👻 Shutdown 📃 VID Ena	VOUT1_SEL 00 1 0 0 0 0 0 0 80 W
14-h-	0.001/	VOUT2_SEL 01 1 0 0 0 0 0 0 80 W
voitage	U.00 V	VOUT3_SEL 02 1 0 0 0 0 0 80 W
Slew Rate	10mV/cycle -	VOUT1_COM 03 0 0 0 0 0 0 0 0 0 0 W
	· · · · · · · · · · · · · · · · · · ·	VOUT2_COM 04 0 0 0 0 0 0 0 0 0 W
		VOUT3_COM 05 0 0 0 0 0 0 0 0 W
		SYS_STATUS 06 0 0 0 0 1 1 1 07 🕞
Vout2		
Mode	PSM at Light Load 👻 Shutdown 📃 VID Ena	
		Status
Voltage	0.68 V + U	Die Temperature < 160 DegC
Slaw Rata		BU3 Over Current Limiting Not Triggered
JIGW Hate		BU2 Over Current Limiting Not Triggered
		Verit3 Within PGood Bange
Vout3		Voit 2 Within P Good Range
Mode	PSM at Light Load Shutdown VID Ena	Vout 1 Within PGood Range
Voltage	0.68 V 👻 🖯	
Slew Rate	10mV / cycle 🗸 🗸 🗍	
11		
	USB Bridge Connect	ver. 51.0.9) Texas Instrume

Figure 9. Screen Capture of TPS65263 Software GUI Interface

Figure 9 shows the control GUI interface. There are seven 8-bit registers embedded in TPS65263, three to select the output voltage, three to configure the slew rate of the buck converter, and one for status feedback. Changes can be made by selecting and checking the components in the GUI on the left hand side or by directly clicking the bits of each register. The I²C address is set to 0x60H by default.

An option is to "write on change". If this option is set to ON, any change is sent to the EVM immediately. If this option is set to OFF, "Write" button or "W" button for each register must be clicked to send the control signal.



Register values can be read back from the EVM by clicking "Read" or "R" for each register.

5 Power-Up Procedure

Use the following steps to power-up the EVM:

- 1. Connect I²C adapter to J5.
- 2. Apply 12 V to J4.
- 3. Toggle J6, J7, or J8 to enable VOUT1, VOUT2, and VOUT3, respectively.
- 4. Apply loads to the output connectors.



6 Bill of Materials

Table 4 lists the BOM for this EVM.

Table 4. Bill of Materials

Qty	Designator	Value	Description	Package Reference	Part Number	Manufacturer
1	PCB1		Printed Circuit Board		PWR645	Any
3	C1, C10, C20	0.047µF	CAP, CERM, 0.047 µF, 50 V, ±10%, X7R, 0603	0603	C1608X7R1H473K	TDK
6	C2, C3, C12, C13, C23, C24	22µF	CAP, CERM, 22 µF, 16 V, ±20%, X5R, 1206	1206	1206YD226MAT2A	AVX
3	C4, C9, C27	1μF	CAP, CERM, 1 µF, 25 V, ±10%, X7R, 0603	0603	C1608X7R1E105K080AB	TDK
3	C5, C6, C7	10µF	CAP, CERM, 10 µF, 25 V, ±10%, X5R, 1206	1206	GRM31CR61E106KA12L	Murata
1	C8	82pF	CAP, CERM, 82 pF, 50 V, ±5%, C0G/NP0, 0603	0603	06035A820JAT2A	AVX
4	C11, C14, C16, C26	22pF	CAP, CERM, 22 pF, 50 V, ±5%, C0G/NP0, 0603	0603	06035A220JAT2A	AVX
1	C15	2200pF	CAP, CERM, 2200 pF, 50 V, ±10%, X7R, 0603	0603	C0603C222K5RACTU	Kemet
1	C17	100pF	CAP, CERM, 100 pF, 25 V, ±10%, X7R, 0603	0603	06033C101KAT2A	AVX
2	C18, C19	3300pF	CAP, CERM, 3300 pF, 50 V, ±10%, X7R, 0603	0603	C0603C332K5RACTU	Kemet
3	C21, C22, C25	0.01µF	CAP, CERM, 0.01 µF, 50 V, ±5%, X7R, 0603	0603	C0603C103J5RACTU	Kemet
4	H1, H2, H3, H4		Bumpon, Hemisphere, 0.44 × 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
4	J1, J2, J3, J4		Terminal Block, 6 A, 3.5 mm Pitch, 2-Pos, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
1	J5		Header (shrouded), 100 mil, 5×2, High-Temperature, Gold, TH	5x2 Shrouded header	N2510-6002-RB	3M
3	J6, J7, J8		Header, 100mil, 3×1, Tin plated, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions
3	L1, L2, L3	4.7μΗ	Inductor, Shielded Drum Core, Superflux, 4.7 $\mu H,$ 6 A, 0.02 $\Omega,$ SMD	WE-HC4	744311470	Wurth Elektronik eiSos
1	LBL1		Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll	PCB Label 0.650"H x 0.200"W	THT-14-423-10	Brady
10	R1–R4, R7, R9, R11, R15, R17, R18	0	RES, 0 Ω, 5%, 0.1 W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
7	R5, R8, R10, R12–R14, R21	10.0k	RES, 10.0 kΩ, 1%, 0.1 W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
1	R6	15.0k	RES, 15.0 kΩ, 1%, 0.1 W, 0603	0603	CRCW060315K0FKEA	Vishay-Dale
2	R19, R20	10k	RES, 10 kΩ, 5%, 0.1 W, 0603	0603	CRCW060310K0JNEA	Vishay-Dale
1	R22	31.6k	RES, 31.6 kΩ, 1%, 0.1 W, 0603	0603	CRCW060331K6FKEA	Vishay-Dale
3	R24, R25, R26	100k	RES, 100 kΩ, 1%, 0.1 W, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
3	R27, R28, R29	51k	RES, 51 kΩ, 5%, 0.1 W, 0603	0603	CRCW060351K0JNEA	Vishay-Dale
6	TP1, TP2, TP6, TP9, TP12, TP14	White	Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
5	TP3, TP4, TP7, TP10, TP15	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
1	U1		4.5 V to 18 V Input Voltage, 3 A/2 A/2 A Output Current Triple Synchronous Step-Down Converter with I ² C Controlled Dynamic Voltage Scaling, RHB0032E	RHB0032E	TPS65263RHB	Texas Instruments
0	C28, C29, C30	DNI	CAP, CERM, 0.01 µF, 50 V, ±5%, X7R, 0603	0603	C0603C103J5RACTU	Kemet
0	FID1, FID2, FID3		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A



Table 4. Bill of Materials (continued)

Qty	Designator	Value	Description	Package Reference	Part Number	Manufacturer
0	R16	DNI	RES, 0 Ω, 5%, 0.1 W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
0	R23	DNI	RES, 73.2 kΩ, 1%, 0.1 W, 0603	0603	CRCW060373K2FKEA	Vishay-Dale
0	R30	DNI	RES, 100 kΩ, 1%, 0.1 W, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
0	TP5, TP8, TP11, TP13, TP16, TP17	DNI	Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
Note: Unless otherwise noted in the Alternate Part Number and/or Alternate Manufacturer columns, all parts may be substituted with equivalents.						



Revision History

www.ti.com

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

CI	hanges from Original (May 2018) to A Revision Page				
•	Edited user's guide for clarity.	. 1			
•	Changed the Hardware Requirement	. 8			

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