Technical Note

LED Drivers for LED Decoration

LED Driver for Indicators and Signage

BD7844AEFV

No.11107EBT01

●Description

BD7844AEFV is LED Display Driver. It can control 16ch Nch Open Drain output for LED drive. It can control the luminance of the LEDs by the setting of the internal register, with 256 steps PWM control. It supports I^2C interface. HTSSOP-B28 (with Back-side metal for heat radiation) package.

●Features

1) 16ch × 80mA (Absolute Maximum Rating)
2) Conforming to I^2C -bus I/F (1MHz Fast mode Plus)
3) Either of interactive or single direction can be selected with the I2CSEL pin. (2MHz clock frequency on single direction)
4) Independent setting of output brightness is possible by register setting for each channel. (PWM 256 steps)
5) Power supply voltage : 4.5 ～ 5.5V
6) Max voltage of Open-drain output terminals: 20.0V (Absolute Maximum Rating)
7) Built-in thermal shutdown (TSD) circuit
8) Built-in power-on reset circuit
9) Small package with back-side metal for heat radiation: HTSSOP-B28

●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Power supply voltage	VDDMAX1	-0.3 ～ 7.0	V
Operating voltage range	VDDMAX2	4.5 ～ 5.5	V
Output terminal voltage	VOUTMAX	-0.3 ～ 20.0	V
Output terminal current	IOUTMAX	80 *1	mA/ch
Logic input terminal voltage	VINMAX	-0.3 ～ VDD+0.3 ≦ 7.0	V
Permissible dissipation	Pd	1.45 *2	W
Operating temperature range	Topr	-40 ～ 85	℃
Storage temperature range	Tstr	-55 ～ 150	℃
Junction temperature	Tjmax	150	℃

Please be careful that the anti-radiation design is not applied to this IC.
*1) Please take the IC's power consumption & permissible dissipation into consideration before using it.
*2) Mounted on ROHM standard board (70mm×70mm×1.6mm (thickness), glass-epoxy board).
Ta=25℃ or more, it is reduced with 11.6mW/℃.

●Operating conditions (Ta=-40~85℃)

Parameter	Symbol	Ratings	Unit	Conditions
Power supply voltage	VDD	4.5 ～ 5.5	V	
High level input voltage	VIH	VDDx0.7 ～ VDD	V	SDA,SCL,RESETB, I2CSEL,A0,A1,A2,A3
Low level input voltage	VIL	0 ～ VDDx0.3	V	
Low level output current	IOL	～ 30	mA	SDA

●**Electrical Characteristics** (Unless otherwise specified, Ta=25℃, VDD=5.0V, GND=0V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
VDD Circuit current1(All ch OFF)	IDD1	—	8.7	11.9	mA	Input pin fixed
VDD Circuit current2(All ch full ON)	IDD2	—	9.5	13.0	mA	Input pin fixed
Input/Output leak current	ILEAK1	—	—	1.0	μA	SDA,SCL,A0,A1,A2,A3 VIN = VDD or GND
Pull Up Resistor	RRSTB	30	60	90	kΩ	RESETB
	RI2C	55	110	165	kΩ	I2CSEL
Output pin leak current	ILEAK2	—	—	1.0	μA	OUT0 ～ OUT15 VOUT = 20V
Power On Reset voltage	VPOR	—	2.4	—	V	
Low level output current	IOL	30	—	—	mA	SDA VOL = 0.4V
Low level output voltage	VOL	—	200	550	mV	OUT0 ～ OUT15 IOUT = 80mA
Resistor at ON	RON	—	2.5	6.875	Ω	OUT0 ～ OUT15 IOUT = 80mA
Input capacitance	Ci	—	6	—	pF	SCL,RESETB,I2CSEL, A0,A1,A2,A3
I/O capacitance	Cio	—	12	—	pF	SDA

●**Logic signal timing specification** (Unless otherwise specified, Ta=25℃, VDD=5.0V, GND=0V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
SCL Clock frequency 1	fSCL1	-	-	1.0	MHz	I2CSEL=H : SDA=I/O
SCL Clock frequency 2	fSCL2	-	-	2.0	MHz	I2CSEL =L : SDA=input
Bus free time between a STOP and START condition *1	tBUF	500	-	-	ns	
Hold time (repeated) START condition. After this period, the first clock is generated	tHD;STA	260	-	-	ns	
Set-up time for a repeated START condition	tSU;STA	260	-	-	ns	
Set-up time for STOP condition	tSU;STO	260	-	-	ns	
SDA Data hold time	tHD;DAT	0	-	-	ns	
SDA data valid acknowledge time *2	tVD;ACK	-	-	450	ns	I2CSEL =H : SDA=I/O
SDA data valid time *3	tVD;DAT	-	-	450	ns	I2CSEL =H : SDA=I/O
SDA Data set-up time	tSU;DAT	50	-	-	ns	
SCL clock low period1	tLOW1	500	-	-	ns	I2CSEL =H : SDA=I/O
SCL clock high period1	tHIGH1	260	-	-	ns	I2CSEL =H : SDA=I/O
SCL, SDA fall time1	tf1	-	-	120	ns	I2CSEL =H : SDA=I/O
SCL, SDA rise time1	tr1	-	-	120	ns	I2CSEL =H : SDA=I/O
SCL clock low period2	tLOW2	230	-	-	ns	I2CSEL =L : SDA=input
SCL clock high period2	tHIGH2	250	-	-	ns	I2CSEL =L : SDA=input
SCL, SDA fall time2	tf2	-	-	50	ns	I2CSEL =L : SDA=input
SCL, SDA rise time2	tr2	-	-	50	ns	I2CSEL =L : SDA=input
Pulse width of spikes which must be suppressed by SCL, SDA filter	tSP	-	50	-	ns	
Reset pulse width *4	tW	-	10	-	ns	

*1) Keep more than 100us Bus free time after power on.
*2) tVD;ACK :Time for acknowledge signal from SCL='L' to SDA(output)='L'
*3) tVD;DAT :Time for from SCL='L' to SDA valid data output
*4) Miss-operation is likely to happen with reset in accessing I^2C bus.

●Block Diagram / Application Circuit example

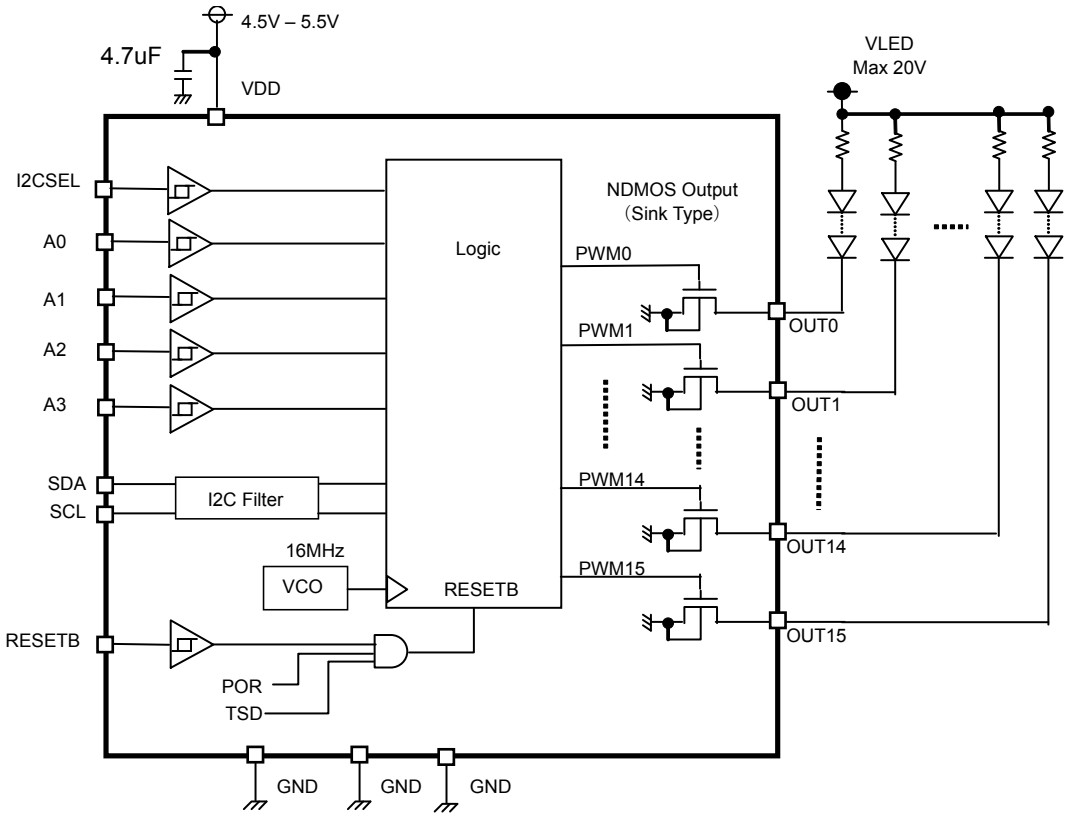


Fig.1 Block Diagram / Application Circuit example

Notes on using BD7844AEFV

- Please do not make output terminal current per one terminal exceed 80mA by putting current limit resistor for open drain output terminal from OUT0 to OUT15.
- Low output drive ability of SDA terminal becomes high, which cause undershoot noise at Low output. It is possible to remove undershoot noise by inserting damping resistor as close as SDA teminal.
- It is recommended that power supply VDD and LED power supply VLED should be used with separted power supply. If using both VDD and VLED with common power supply, malfunction might be occurred by transmitting noise associated with PWM signal of open drain output terminal from VLED wiring to VDD wiring.
  In case of using VDD and VLED with common power supply, please insert bypass capacitor as close as VDD terminal after separating VDD wiring and VLED wiring from the end in order to make common impedance minimum. In addition, please insert bypass capacitor on VLED wiring as necessary in order to prevent noise of VLED wiring side from being transmitted to VDD side as much as possible.

●Pin Arrangement [Top View]

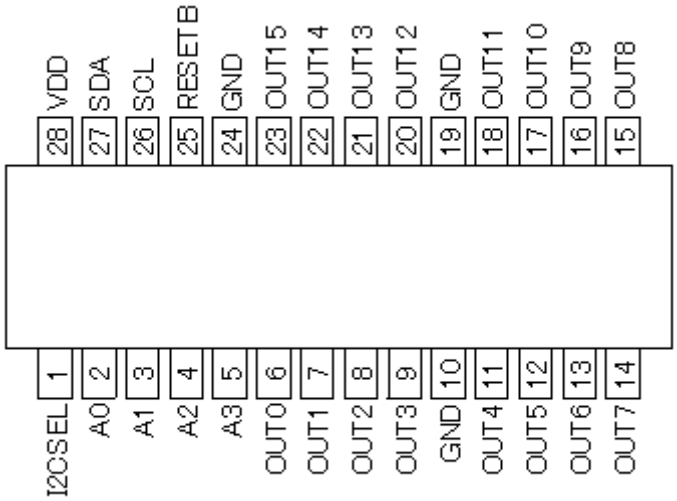


Fig.2 Pin arrangement

●Pin Functions

Pin No	Pin Name	I/O	Pull up Register	Unused Terminal setting	ESD Diode		Functions
					For Power	For Ground	
1	I2CSEL	I	110kΩ	GND	VDD	GND	I^2C access mode select for SDA (H: I/O, L: Input only)
2	A0	I	-	GND	VDD	GND	Slave address setting
3	A1	I	-	GND	VDD	GND	Slave address setting
4	A2	I	-	GND	VDD	GND	Slave address setting
5	A3	I	-	GND	VDD	GND	Slave address setting
6	OUT0	O	-	GND	-	GND	Open Drain output
7	OUT1	O	-	GND	-	GND	Open Drain output
8	OUT2	O	-	GND	-	GND	Open Drain output
9	OUT3	O	-	GND	-	GND	Open Drain output
10	GND	-	-	GND	VDD	-	Ground
11	OUT4	O	-	GND	-	GND	Open Drain output
12	OUT5	O	-	GND	-	GND	Open Drain output
13	OUT6	O	-	GND	-	GND	Open Drain output
14	OUT7	O	-	GND	-	GND	Open Drain output
15	OUT8	O	-	GND	-	GND	Open Drain output
16	OUT9	O	-	GND	-	GND	Open Drain output
17	OUT10	O	-	GND	-	GND	Open Drain output
18	OUT11	O	-	GND	-	GND	Open Drain output
19	GND	-	-	GND	VDD	-	Ground
20	OUT12	O	-	GND	-	GND	Open Drain output
21	OUT13	O	-	GND	-	GND	Open Drain output
22	OUT14	O	-	GND	-	GND	Open Drain output
23	OUT15	O	-	GND	-	GND	Open Drain output
24	GND	-	-	GND	VDD	-	Ground
25	RESETB	I	60kΩ	GND	VDD	GND	Reset input pin (L: reset, H: reset cancel)
26	SCL	I	-	GND	-	GND	Serial clock input pin
27	SDA	I/O	-	GND	-	GND	Serial data I/O pin
28	VDD	-	-	GND	-	GND	Power supply

* Please connect the unused LED pins to the ground.
* It is prohibition to set the registers for unused LED.

●Definition of logic signal timing

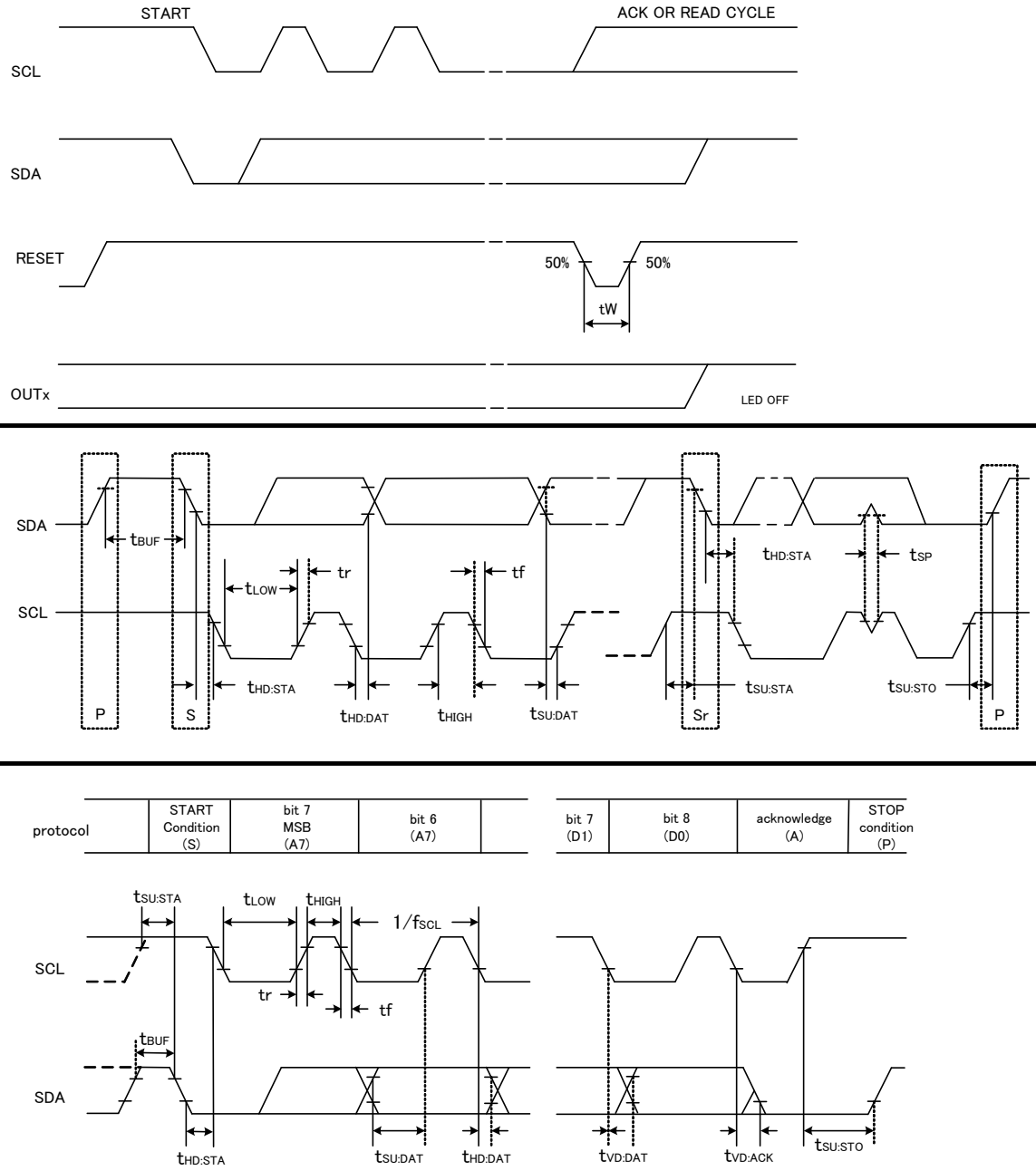


Fig.3 Definition of logic signal timing

●Logic Function explaining

1. Slave address

LED driver BD7844AEFV is a slave device. The master device outputs the transmission clock and the transmission data, and BD7844AEFV who is the slave returns the acknowledgement. The master device transmits the slave address of BD7844AEFV following the START condition. Afterwards, BD7844AEFV can be controlled in the command by transmitting the register address and the register data continuously, and doing the transmission completion under the STOP condition. Fig. 4 shows basic format (I^2C) of the control command of BD7844AEFV.

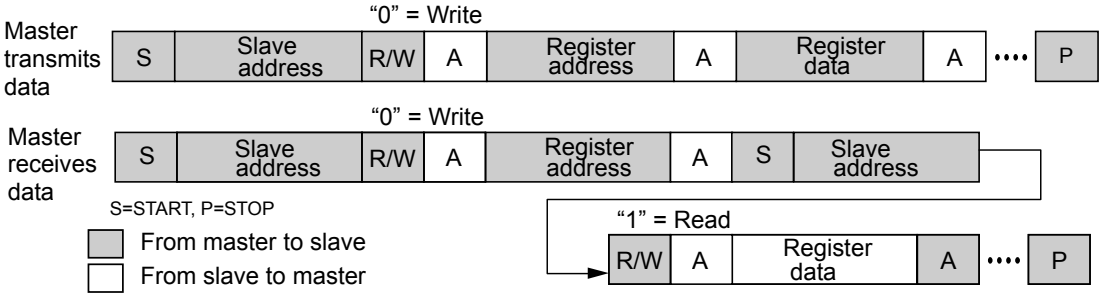


Fig. 4 Basic format of control command（I^2C）

BD7844AEFV has three kinds of slave addresses (for usually, for all calls, and for software reset).

1-1. Usual slave address

Fig. 5 shows the slave address of BD7844AEFV. Because an internal pull-up resistor has not placed to the address terminal (A[3:0]) that can be selected with hardware to save power consumption, it is necessary to connect them with high (=VDD) or low (=GND).

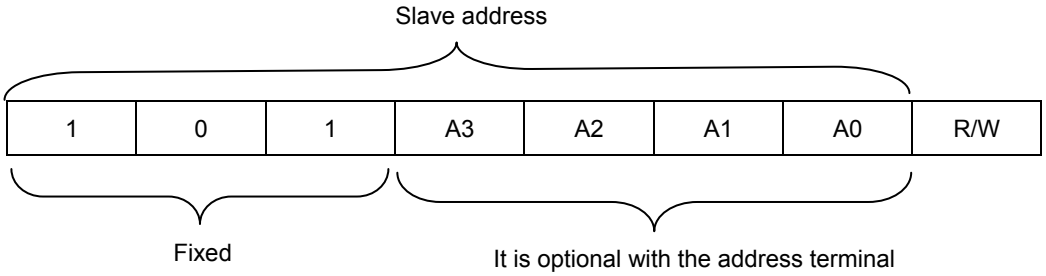


Fig. 5 Usual slave address

The last RW bit of the slave address byte defines the executed operation. Reading is selected when setting it to logic 1, and writing is selected when setting it to logic 0.

Fixed	A3	A2	A1	A0	R/W	Function
101	0	0	0	0	R/W	Usual 1
101	0	0	0	1	R/W	Usual 2
101	0	0	1	0	R/W	Usual 3
101	0	0	1	1	R/W	Usual 4
101	0	1	0	0	R/W	Usual 5
101	0	1	0	1	R/W	Usual 6
101	0	1	1	0	R/W	Usual 7
101	0	1	1	1	R/W	Usual 8
101	1	0	0	0	R/W	All call
101	1	0	0	1	R/W	Usual 9
101	1	0	1	0	R/W	Usual 10
101	1	0	1	1	0	Software reset
101	1	1	0	0	R/W	Usual 11
101	1	1	0	1	R/W	Usual 12
101	1	1	1	0	R/W	Usual 13
101	1	1	1	1	R/W	Usual 14

Table 1. Slave address

1-2. Slave address for all call
[1011000] is used as a slave address for all call. (Fig. 6)

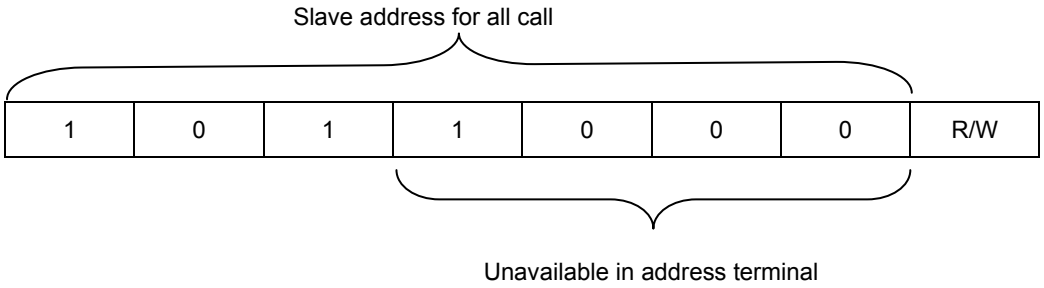


Fig. 6 Slave address for all call

All BD7844AEFV on the bus can control in the command at the same time by the slave address for all call. It enters the state that can respond to all call when power supply (VDD) is turned on.
It can be selected not to respond when the ALL CALL bit of mode1 register is set to logic “0”.
Because the register data is returned from all BD7844AEFV on the bus when the last R/W bit of the slave address byte is set to logic "1" (read) when the slave address for all calls is used, the master cannot read the register data of specific BD7844AEFV.
Please use a usual slave address to read the register data of specific BD7844AEFV.

Take care: Slave address [1011000] for all calls must not use as a usual slave address because it becomes enable when power supply (VDD) is turned on.

1-3. Slave address for software reset
[1011011] is used as a slave address for software reset. (Fig. 7)

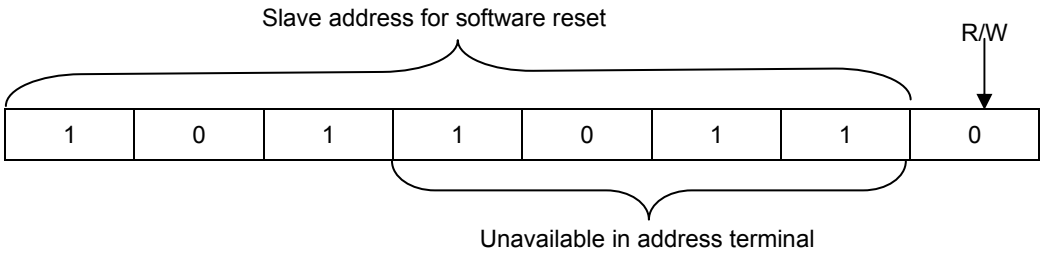


Fig. 7 Slave address for software reset

All BD7844AEFV on the bus can be reset at the same time by the slave address for software reset.
It is necessary to use the slave address for software reset with R/W=0. BD7844AEFV doesn't recognize software reset for R/W=1. Please refer to "3-2. Software reset" for details.

Take care: Because slave address [1011011] for software reset is a reserved address, It is not possible to use it as a usual slave address.

2. Register address

After completing the acknowledgement of the slave address, the master device transmits the register address to BD7844AEFV. Fig. 8 shows the register address.

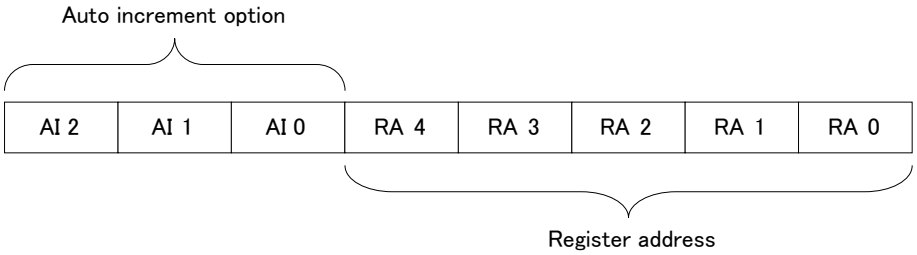


Fig. 8 Register address

The auto increment option is specified for MSB 3bit.The address of the register that wants to be controlled is specified for LSB 5bit. Sending register data continuously with the auto increment option in the three high rank bits can continuously set each brightness control register. (Mode1 register cannot be set by the auto increment option.)

The register of BD7844AEFV is shown in Table 2 and the auto increment option is shown in Table 3

Register address(Hex)	Register name	Initial Value after reset	Access	Function
00	PWM0 [7:0]	00h	R/W	Brightness control (256steps) OUT0
01	PWM1 [7:0]	00h	R/W	Brightness control (256steps) OUT1
02	PWM2 [7:0]	00h	R/W	Brightness control (256steps) OUT2
03	PWM3 [7:0]	00h	R/W	Brightness control (256steps) OUT3
04	PWM4 [7:0]	00h	R/W	Brightness control (256steps) OUT4
05	PWM5 [7:0]	00h	R/W	Brightness control (256steps) OUT5
06	PWM6 [7:0]	00h	R/W	Brightness control (256steps) OUT6
07	PWM7 [7:0]	00h	R/W	Brightness control (256steps) OUT7
08	PWM8 [7:0]	00h	R/W	Brightness control (256steps) OUT8
09	PWM9 [7:0]	00h	R/W	Brightness control (256steps) OUT9
0A	PWM10 [7:0]	00h	R/W	Brightness control (256steps) OUT10
0B	PWM11 [7:0]	00h	R/W	Brightness control (256steps) OUT11
0C	PWM12 [7:0]	00h	R/W	Brightness control (256steps) OUT12
0D	PWM13 [7:0]	00h	R/W	Brightness control (256steps) OUT13
0E	PWM14 [7:0]	00h	R/W	Brightness control (256steps) OUT14
0F	PWM15 [7:0]	00h	R/W	Brightness control (256steps) OUT15
1A*	MODE1 [7:0]	03h	R/W	Mode 1 setting

*MODE1 register cannot be set by the auto increment option.

Table 2. Register

AI2	AI1	AI0	Function
0	0	0	Auto increment none
0	0	1	Address auto increment (+1) for brightness control register PWM0~15only.
0	1	0	Prohibited
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Table 3. Auto increment option

2-1. PWM0 ~ PWM15 register data

The brightness of output terminal OUT0 ~ OUT15 is set by the register data of PWM0(address:00h) ~ PWM15(address:0Fh).
The PWM brightness control in 256 steps is possible from 00h (complete off) to FFh (complete on).

2-2. Mode1 registers data

The operation mode of BD7844AEFV is set according to mode1 register (address: 1Ah) data.
Table 4 shows the allocation of the bit of mode1 register data.

Bit	Bit name	Access	Value	Function
7	LIMITRESET	R/W	0*	Device limitation software reset : off
			1	Device limitation software reset : on
6	PROTECT0	R/W	0	Please write “0”.
				It is not recognized as Mode1 register data at “1”.
5	Reservation	R/W	0*	Please write “0”
			1	Prohibited
4	PWMSLOW	R/W	0*	PWM period is 60kHz
			1	PWM period is 2kHz
3	Reservation	R/W	0*	Please write “0”.
			1	Prohibited
2	Reservation	R/W	0*	Please write “0”.
			1	Prohibited
1	PROTECT1	R/W	1	Please write “1”.
				It is not recognized as Mode1 register data at “0”.
0	ALLCALL	R/W	0	It doesn't respond to the slave address for all call.
			1*	It responds to the slave address for all call.

*Default value after reset

Table 4. Mode1 register (Address: 1Ah) data

Mode1 register data cannot be set by the auto increment option. Please set it alone by the following format. In the correct execution, there should not be device that monopolizes the bus.

2-3. Mode1 register data setting procedure

1. The START condition is sent by the I^2C bus master.
2. The slave address of BD7844AEFV that wants to be set by mode1 register is sent by the master.
3. When the slave address is sent and recognized, the master sends mode1 register address [00011010] (1Ah).
   It is recognized only when LSB 5bit are [11010] and the auto increment option in MSB 3bit are [000].
4. When mode1 register address is sent and recognized, the master sends mode1 register data.
   It recognizes it as data only when the data confirmation bit (bit 6=0 and bit1=1) is all correct.
5. When correct mode1 register data is sent and recognized, the master sends the STOP condition to end mode1 setting command. Afterwards, LIMITRESET, PWMSLOW, and ALLCALL become effective.

3. Reset
BD7844AEFV has four kinds of resets (power on, software, device limitation software, external,).

3-1. Power-on reset
When the power supply is forced to VDD, internal power-on reset maintains BD7844AEFV in the state of reset until VDD reaches Vpor. Reset is liberated at Vpor, and the register and the I^2C bus state machine of BD7844AEFV are initialized in the state of default.

3-2. Software reset
All BD7844AEFV on the I^2C bus can be reset in the power supply on condition by software reset. In the correct execution, there should not be device that monopolizes the bus. Software reset is defined as follows.

1. The START condition is sent by the I^2C bus master.
2. The slave address for software reset that the R/W bit is set to "0" (write) is sent by the I^2C bus master.
3. Only when it is recognized that the slave address for software reset is [10110110] (B6h), BD7844AEFV executes reset. When the R/W bit is set to logic "1" (read), it is not recognized. Even R/W bit is logic "0" and "1", the acknowledgement is returned. But it is only logic "0" that reset is recognized.
4. When the slave address for software reset is sent and recognized, the master sends two bytes with two specific values. Byte 1= A5h: BD7844AEFV recognizes only this value. When byte 1 is not A5h, BD7844AEFV doesn't recognize it. Byte 2= 5Ah: BD7844AEFV recognizes only this value. When byte 2 is not 5Ah, BD7844AEFV doesn't recognize it.
5. The master sends the STOP condition to terminate the software reset command when correct two bytes are sent and it is recognized correctly. Afterwards, BD7844AEFV is reset in the power supply on condition.

3-3. Device limitation software reset
Only BD7844AEFV selected in the slave address can be reset in the power supply on condition by making the LIMITRESET bit of the Mode1 register logic 1.

3-4. External reset
External reset is executed by maintaining RESETB terminal for the period of minimum tW. The register and the I^2C bus state machine of BD7844AEFV is maintained in the state of default until becoming RESETB input becomes “H” level.

Take care: Please connect the RESETB terminal with “H”, when you do not use an active connection.

4. I2CSEL function
It can be set that the SDA terminal accepts only the input by connecting the I2CSEL terminal with “L”.

Take care: Because the acknowledge and reading data of the register is not returned to the master device, control software for I^2C cannot be used as it is.

●Notes for use

1. Absolute Maximum Ratings
   An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

2. Power supply and ground line
   Design PCB pattern to provide low impedance for the wiring between the power supply and the ground lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and ground lines. Especially, when there are ground pattern for small signal and ground pattern for large current included the external circuits, please separate each ground pattern. Furthermore, for all power supply pins to ICs, mount a capacitor between the power supply and the ground pin. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

3. Ground voltage
   Make setting of the potential of the ground pin so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no pins are at a potential lower than the ground voltage including an actual electric transient.

4. Short circuit between pins and erroneous mounting
   In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between pins or between the pin and the power supply or the ground pin, the ICs can break down.

5. Operation in strong electromagnetic field
   Be noted that using ICs in the strong electromagnetic field can malfunction them.

6. Input pins
   In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input pin. Therefore, pay thorough attention not to handle the input pins, such as to apply to the input pins a voltage lower than the ground respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input pins a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

7. External capacitor
   In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

8. Thermal shutdown circuit (TSD)
   This LSI builds in a thermal shutdown (TSD) circuit. When junction temperatures become detection temperature or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

9. Thermal design
   Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

10. About the pin for the test, the un-use pin
    Prevent a problem from being in the pin for the test and the un-use pin under the state of actual use. Please refer to a function manual and an application notebook. And, as for the pin that doesn't specially have an explanation, ask our company person in charge.

11. About the rush current
    For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of wiring.

12. About the function description or application note or more.
    The function description and the application notebook are the design materials to design a set. So, the contents of the materials aren't always guaranteed. Please design application by having fully examination and evaluation include the external elements.

●**Power dissipation** (On the ROHM's standard board)

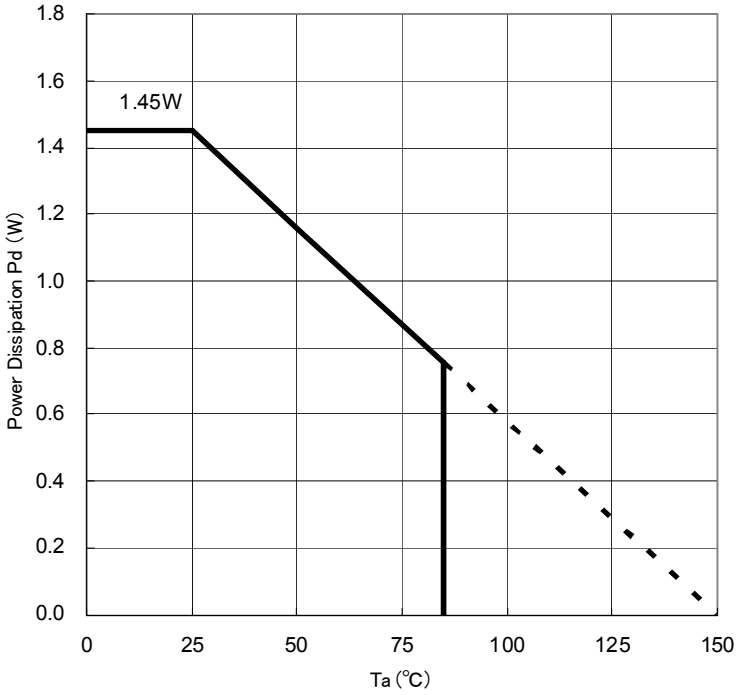


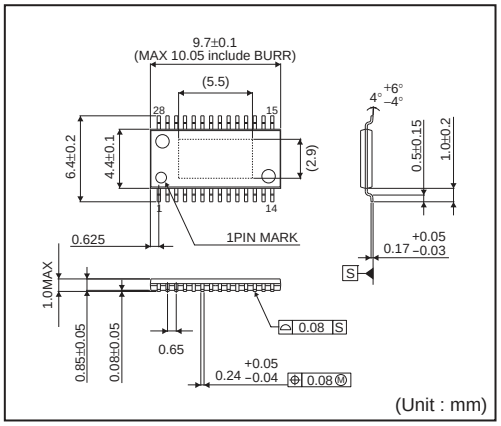
Fig. 9 Power dissipation

●Ordering part number

B	D	7	8	4	4	A	E	F	V	-	E	2

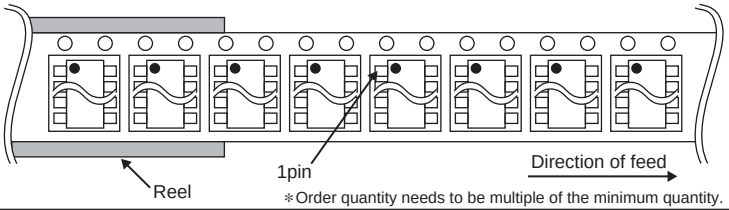
Part No. Part No. Package EFV:HTSSOP-B28 Packaging and forming specification E2: Embossed tape and reel

HTSSOP-B28



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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