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National Semiconductor

August 2006

LM2506
Low Power Mobile Pixel Link (MPL) Level 0, 18-bit RGB Display Interface Serializer and Deserializer

General Description

The LM2506 device adapts RGB style display interfaces to the Mobile Pixel Link (MPL) Level zero serial link. The LM2506 supports one RGB display at up to 18-bit color depth and 800 X 300 pixels (over 216 Mbps and 13.2 MHz PCLK) is supported. A mode pin configures the device as a Serializer (SER) or Deserializer (DES) so the same chip can be used on both sides of the interface.

The interconnect is reduced from 22 signals to only 3 active signals with the LM2506 chipset easing flex interconnect design, size constraints and cost.

The LM2506 in SER mode resides beside an application, graphics or baseband processor and translates a parallel bus from LVCMOS levels to serial Mobile Pixel Link levels for transmission over a flex cable (or coax) and PCB traces to the DES located near the display module.

When the Power_Down (PD*) input is asserted on the SER, the MDn and MC line drivers are powered down to save current. The DES can be controlled by a separate Power-_Down input or via a signal from the SER (PD_{OUT}*).

The LM2506 implements the physical layer of the MPL Level 0 Standard (MPL-0) and a 150 µA I_B current (Class 0).

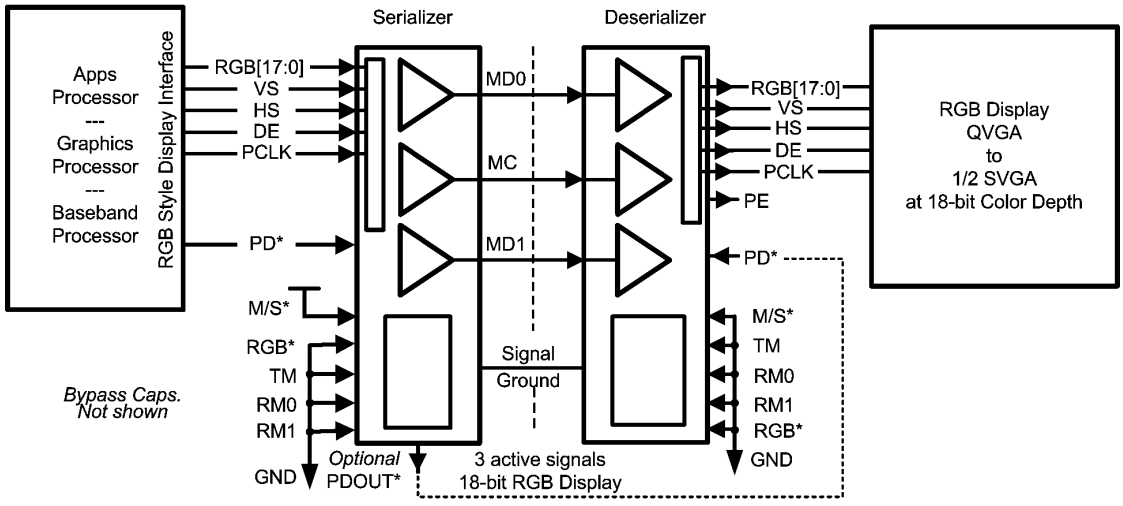
Features

- RGB Display Interface support up to 800 x 300 ½SVGA formats
- MPL-Level 0 Physical Layer using two data and one clock signal
- Low Power Consumption
- Pinout mirroring enables straight through layout with minimal vias
- Level translation between host and display
- Auto Power Down on STOP PCLK
- Link power down mode reduces quiescent power under < 10 µA
- 1.74V to 2.0V core / analog supply voltage range
- 1.74V to 3.0V I/O supply voltage range
- –30C to 85C Operating temperature range

System Benefits

- Small Interface
- Low Power
- Low EMI
- Intrinsic Level Translation

Typical Application Diagram - Bridge Chips



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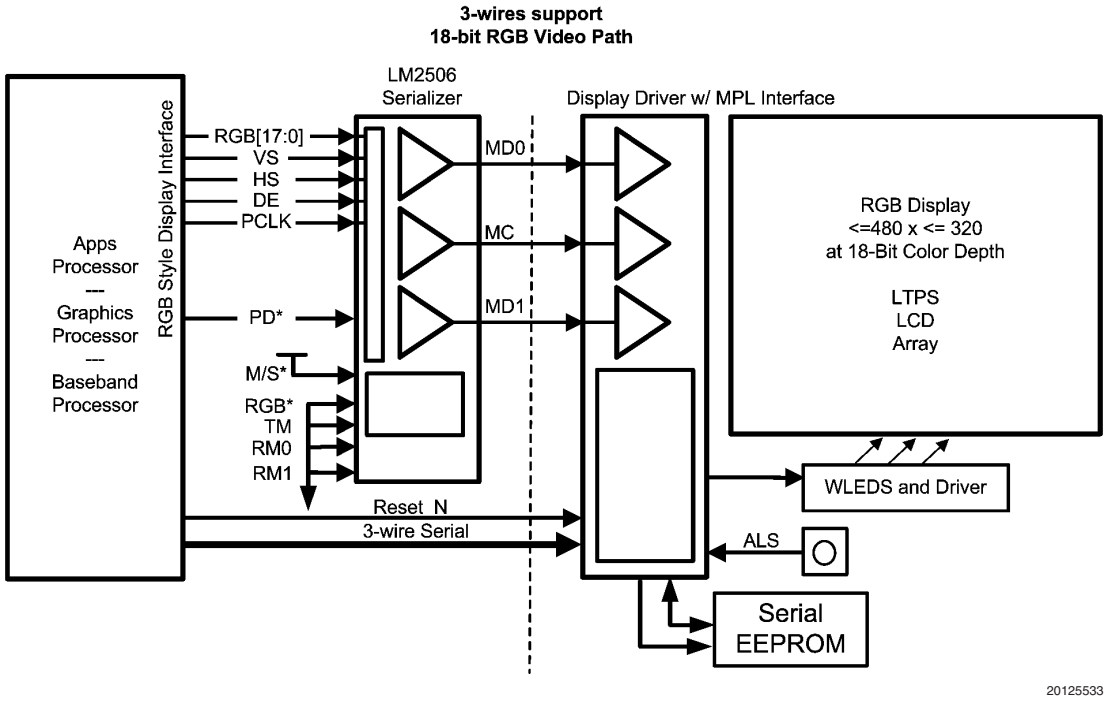
Typical Application Diagram - RGB Mode to Display Driver



Ordering Information

NSID	Package Type	Package ID
LM2506GR	49L MicroArray, 4.0 X 4.0 X 1.0 mm, 0.5 mm pitch	GRA49A
LM2506SQ	40L LLP, 5.0 X 5.0 X 0.8 mm, 0.4 mm pitch	SQF40A

Pin Descriptions - RGB Mode

Pin Name	No. of Pins	I/O, Type	Description	
			RGB Serializer	RGB Deserializer
MPL SERIAL BUS PINS				
MD[1:0]	2	IO, MPL	MPL Data Line Driver	MPL Data Receiver
MC	1	IO, MPL	MPL Clock Line Driver	MPL Clock Receiver
V_{SSA}		Ground	MPL Ground - see Power/Ground Pins	
CONFIGURATION/PARALLEL BUS PINS				
RGB*	1	I, LVCMOS	RGB Mode Input **Tie Low**	
M/S*	1	I, LVCMOS	Tie High for Serializer (Master)	Tie Low for Deserializer (Slave)
TM	1	I, LVCMOS	Test Mode control input **Tie Low (normal mode)**	
RM0	1	I, LVCMOS	RGB Mode control input zero **Tie Low**	
RM1	1	I, LVCMOS	RGB Mode control input one **Tie Low**	
CLOCK / POWER DOWN SIGNALS				
PCLK	1	IO, LVCMOS	PCLK input	PCLK output
PD_{OUT*}	1	O, LVCMOS	Power Down Output, L = device in Power Down H = Device active.	NA
PD*	1	I, LVCMOS	Power Down input, L = Powered down (sleep mode) H = active mode	
PARALLEL INTERFACE SIGNALS				
D[17:0]	18	IO, LVCMOS	RGB Data Bus inputs	RGB Data Bus outputs
VS	1	IO, LVCMOS	Vertical Sync. Input	Vertical Sync. Output
HS	1	IO, LVCMOS	Horizontal Sync. Input	Horizontal Sync. Output
DE	1	IO, LVCMOS	Data Enable Input	Data Enable Output
PE	1	O, LVCMOS	NA	Parity Error Output
POWER/GROUND PINS				
V_{DDA}	1	Power	Power Supply Pin for the SER PLL and MPL Interface. 1.74V to 2.0V	
V_{SSA}	1	Ground	Ground Pin for the MPL Interface, and analog circuitry.	
V_{DDcore}	1	Power	Power Supply Pin for the digital core. 1.74V to 2.0V	
V_{SScore}	1	Ground	Ground Pin for the digital core.	
V_{DDIO}	2	Power	Power Supply Pin for the parallel interface I/Os. 1.74V to 3.0V	
V_{SSIO}	2	Ground	Ground Pin for the parallel interface I/Os.	
V_{bulk}	9		Connect to Ground - uArray Package	
DAP	1		Connect to Ground - LLP Package	

Note:
I = Input, O = Output, IO = Input/Output. **Do not float input pins.**

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DDA})	−0.3V to +2.2V
Supply Voltage (V_{DD})	−0.3V to +2.2V
Supply Voltage (V_{DDIO})	−0.3V to +3.6V
LVCMOS Input/Output Voltage	−0.3V to (V_{DDIO} +0.3V)
MPL Input/Output Voltage	−0.3V to V_{DDA}
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature Soldering, 40 Seconds	+260˚C
ESD Ratings:	
HBM, 1.5 kΩ, 100 pF	≥±2 kV
EIAJ, 0Ω, 200 pF	≥±200V
Maximum Package Power Dissipation Capacity at 25˚C	
GRA Package	1.8W
Derate GRA Package above 25˚C	15mW/˚C
SQF Package	1.8W
Derate SQF Package above 25˚C	15mW/˚C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage				
V_{DDA} to V_{SSA} and V_{DDcore} to V_{SScore}	1.74	1.8	2.0	V
V_{DDIO} to V_{SSIO}	1.74		3.0	V
PCLK Frequency	2		13.3	MHz
Ambient Temperature	−30	25	85	˚C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
MPL							
I_{OLL}	Logic Low Current (5X I_B)			3.67 I_B	5.0 I_B	6.33 I_B	µA
I_{OMS}	Mid Scale Current (Notes 4, 9)			2.1I_B	3.0 I_B	3.9I_B	µA
I_{OLH}	Logic High Current (1X I_B)			0.7 I_B	1.0 I_B	1.4 I_B	µA
I_B	Current Bias				150		µA
I_{OFF}	MPL Leakage Current	V_{MPL} = 0.8V		−2		+2	µA
LVCMOS (1.74V to 3.0V Operation)							
V_{IH}	Input Voltage High Level			0.7 V_{DDIO}		V_{DDIO}	V
V_{IL}	Input Voltage Low Level			GND		0.3 V_{DDIO}	V
V_{HY}	Input Hysteresis	V_{DDIO} = 1.74V			150		mV
		V_{DDIO} = 3.0V			200		mV
I_{IH}	Input Current High Level	Includes I_{OZ}	Vin = V_{DDIO}	−1	0	+1	µA
I_{IL}	Input Current Low Level		Vin = GND	−1	0	+1	µA
V_{OH}	Output Voltage High Level	I_{OH} = −2 mA		0.75 V_{DDIO}		V_{DDIO}	V
V_{OL}	Output Voltage Low Level	I_{OL} = 2 mA		V_{SSIO}		0.2 V_{DDIO}	V
SUPPLY CURRENT							
I_{DD}	Total Supply Current — Enabled Conditions: MC = 80 MHz, MD = 160 Mbps (Note 5)	SER	V_{DDIO}		20	66	µA
			V_{DD}/V_{DDA}		5	12	mA
		DES	V_{DDIO}		4	10	mA
			V_{DD}/V_{DDA}		6	11	mA
	Supply Current — Enabled 1.8V (Note 6)	SER	V_{DDIO}		10		µA
			V_{DD}/V_{DDA}		4.7		mA
		DES	V_{DDIO}		2.3		mA
			V_{DD}/V_{DDA}		6.2		mA

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
MPL							
I_{DDZ}	Supply Current—Disable T_A = 25˚C Power Down Modes	SER PD* = L	V_{DDIO}		<1	2	µA
			V_{DD}/V_{DDA}		<1	2.2	µA
		SER Stop Clock	V_{DDIO}		<1	2	µA
			V_{DD}/V_{DDA}		<1	2.2	µA
		DES PD* = L	V_{DDIO}		<1	2	µA
			V_{DD}/V_{DDA}		<1	2.2	µA
PD	Power Dissipation	RGB (Note 6)	SER		8.5		mW
			DES		15.3		mW

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
PARALLEL BUS TIMING See							
t_{SET}	Set Up Time	RGB Mode Inputs *Figure 11*		5			ns
t_{HOLD}	Hold Time			5			ns
t_{RISE}	Rise Time	PCLK Output C_L = 15 pF, *Figure 2*	V_{DDIO} = 1.74V		7	12	ns
			V_{DDIO} = 3.0V		3	7	ns
t_{FALL}	Fall Time		V_{DDIO} = 1.74V		7	11	ns
			V_{DDIO} = 3.0V		2	6	ns
SERIAL BUS TIMING							
t_{DVBC}	Serial Data Valid before Clock (Set Time)	DES Input *Figure 1*	MC = 80MHz (Note 9)	1.5			ns
t_{DVAC}	Serial Data Valid after Clock (Hold Time)			1.5			ns
POWER UP TIMING							
t_0	SER PLL Lock Counter				4,096		PCLK cycles
t_1	MC Pulse Width Low				180		MC cycles
t_2	MC Pulse Width High				180		MC cycles
t_3	MC H-L to Active State				180		MC cycles
t_{PZXclk}	Enable Time - Clock Start RGB Mode	CLK to PDout*	*Figure 4*		7		PCLK cycles
MPL POWER OFF TIMING							
t_{PAZ}	Disable Time to Power Down	(Note 8)				2	ms
t_{PXZclk}	Disable Time - Clock Stop	PCLK to PD_{OUT*} *Figure 3*			7		PCLK cycles

Recommended Input Timing Requirements

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SER PIXEL CLOCK (PCLK)						
f	Pixel Clock Frequency		2		13.3	MHz
t_{CP}	Pixel Clock Period		75.2		500	ns
$PCLK_{DC}$	Pixel Clock Duty Cycle		30	50	70	%
t_T	Transition Time	(Note 7)	2			ns
$t_{STOPpclk}$	PClock Stop Gap		300			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{DDIO} = 1.8V and V_{DD} = V_{DDA} = 1.8V and T_A = 25˚C.

Note 3: Current into a device pin is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to Ground unless otherwise specified.

Note 4: MPL Current Threshold is set to be $3XI_B$ by the MPL start up Sequence - this is a functional specification only.

Note 5: Total Supply Current Conditions: RGB Mode, worse case data pattern, 13.3MHz PCLK, DES C_L = 15pF, TYP V_{DDIO} = V_{DDA} = V_{DDcore} = 1.8V, MAX VDDIO = 3.0V, MAX VDDA = VDDcore = 2.0V.

Note 6: Supply Current Conditions: RGB Mode, PRBS case data pattern, 13.3MHz PCLK, DES C_L = 15pF, TYP V_{DDIO} = V_{DDA} = V_{DDcore} = 1.8V.

Note 7: Maximum transition time is a function of clock rate and should be less than 30% of the clock period to preserve signal quality.

Note 8: Guaranteed functionally by the I_{DDZ} parameter. See also *Figure 8*.

Note 9: This is a functional parameter and is guaranteed by design or characterization.

Timing Diagrams

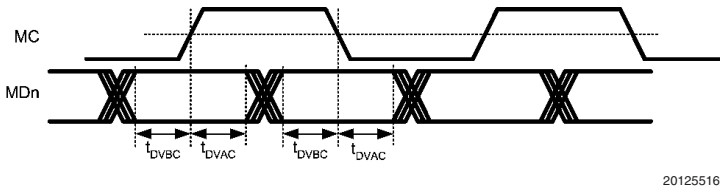


FIGURE 1. Serial Data Valid—DES Input Set and Hold Time

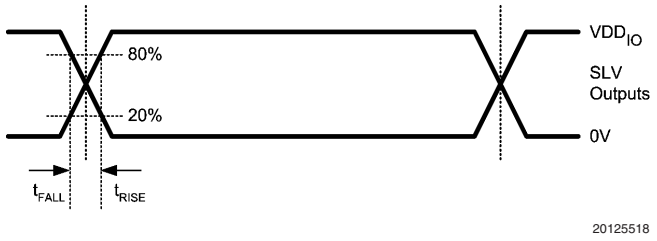


FIGURE 2. DES Output Rise and Fall Time (PCLK)

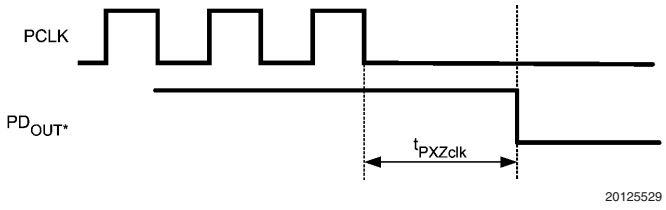


FIGURE 3. Stop Clock Power Down (SER)

Timing Diagrams (Continued)

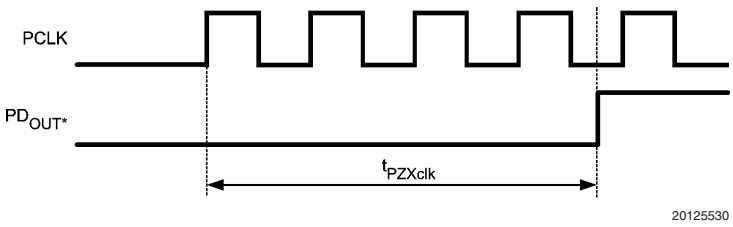


FIGURE 4. Stop Clock Power Up (SER)

Functional Description

BUS OVERVIEW

The LM2506 is a dual link SER/DES configurable part that supports an 18-bit RGB Display interface. The MPL physical layer is purpose-built for an extremely low power and low EMI data transmission while requiring the fewest number of signal lines. No external line components are required, as termination is provided internal to the MPL receiver. A maximum raw throughput of 320 Mbps (raw) is possible with this chipset. When the protocol overhead is taken into account, a maximum data throughput of 240 Mbps is possible. The MPL interface is designed for use with common 50Ω to 100Ω lines using standard materials and connectors. Lines may be microstrip or stripline construction. Total length of the interconnect is expected to be less than 20cm.

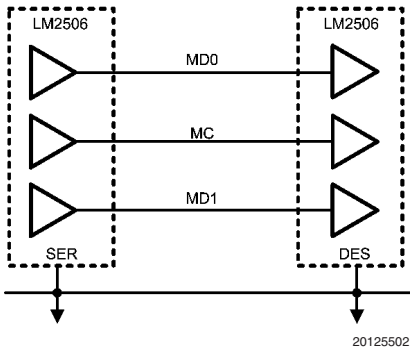


FIGURE 5. MPL Point-to-Point Bus

SERIAL BUS TIMING

Data valid is relative to both edges for a RGB transaction as shown in *Figure 6*. Data valid is specified as: Data Valid before Clock, Data Valid after Clock, and Skew between data lines should be less than 500ps.

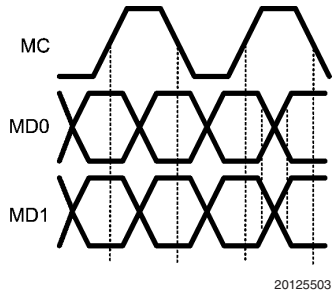


FIGURE 6. Dual Link Timing (WRITE)

SERIAL BUS PHASES

There are three bus phases on the MPL serial bus. These are determined by the state of the MC and MD lines. The MPL bus phases are shown in *Table 1*.

The LM2506 supports MPL Level 0 Enhanced Protocol with a Class 0 PHY.

TABLE 1. Link Phases

Name	MC State	MDn State	Phase Description	Pre-Phase	Post-Phase
OFF (O)	0	0	Link is Off	A, I or LU	LU
ACTIVE (A)	A	X	Data Out	LU, A, or I	A, I, or O
LINK-UP (LU)	H	-	SER initiated Link-Up	O	A, I, or O

Notes on MC/MD Line State:
0 = no current (off)
L = Logic Low — The higher level of current on the MC and MD lines
H = Logic High — The lower level of current on the MC and MD lines
X = Low or High
A = Active Clock

SERIAL BUS START UP TIMING

In the Serial Bus OFF phase, SER transmitters for MD0, MD1 and MC are turned off such that zero current flows over the MPL lines. In addition, both the SER and the DES are internally held in a low power state. When the PD* input pins are de-asserted (driven High) the SER enables its PLL and waits for enough time to pass for its PLL to lock. After the SER's PLL is locked (t0 = 4,096 PCLK Cycles), the SER will perform an MPL start up sequence. The DES will power up and await the start up sequence from the SER once its PD* input is driven High.

Functional Description (Continued)

The MPL start up sequence gives the DES an opportunity to optimize the current sources in its receivers to maximize noise margins. The SER begins the sequence by driving the MC line logically Low for 180 MC cycles (t1). At this point, the DES's receiver samples the MC current flow and adjusts itself to interpret that amount of current as a logical Low. Next the SER drives the MC line logically HIGH for 180 MC cycles (t2). The optimized current configuration is held as long as the MPL remains active. Next, the SER drives both the MC and the MD lines to a logical Low for another 180 MC cycles (t3), after which it begins to toggle the MC line at 6X the PCLK rate. The SER will continue to toggle the MC line as long as its PD* pin remains de-asserted (High). At this point, video data is streaming to the DES.

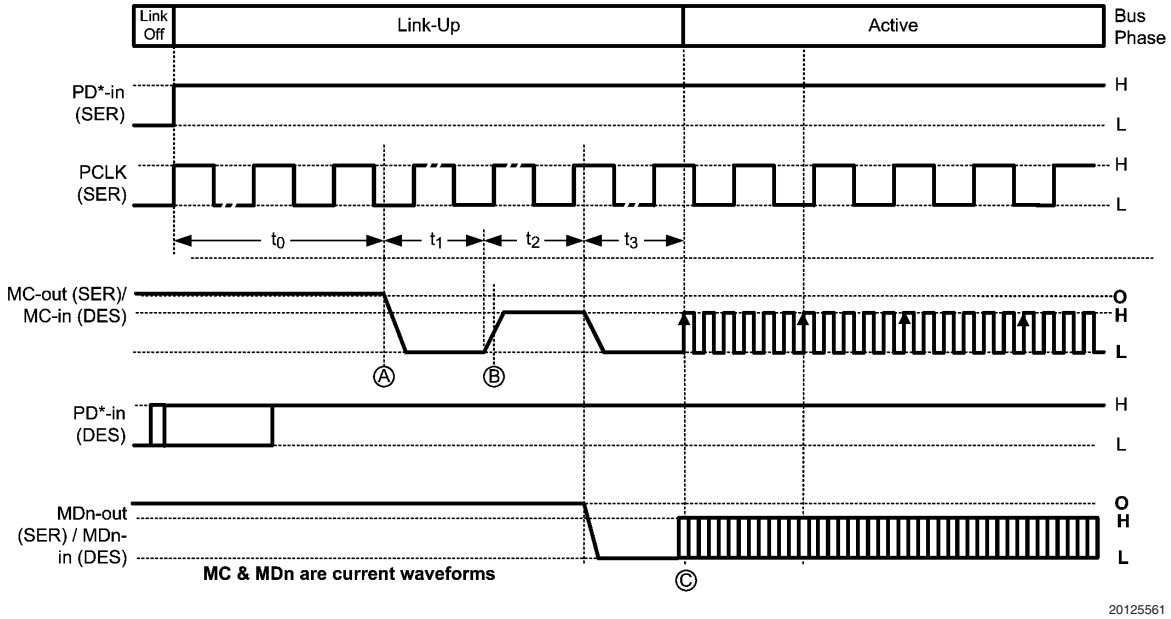


FIGURE 7. Bus Power Up Timing

Once power is applied and stable, the PCLK should be applied to the SER. Next the PD* inputs are driven High to enable the SER and DES. The DES PD* input may be driven High first, at the same time, or slightly later than the SER's PD* input. The SER's PLL locks to the PCLK and the SER drives the MC line to the 5I (Logic Low) state at point "A" for t1. Next the SER drives the MC line to the 1I (Logic High) state for t2. On the T1 to t2 transition - point "B", the DES calibrates its current to that of the SER to maximize noise margins. Next the SER drives the MC and MD lines to the 5I (logic Low) state for t3. At point "C", video data is now sampled and streamed to the DES.

OFF PHASE

In the OFF phase, both SER and DES MPL transmitters are turned off with zero current flowing on the MC and MDn lines. *Figure 8* shows the transition of the MPL bus into the OFF phase. If an MPL line is driven to a logical Low (high current) when the OFF phase is entered it may temporarily pass through as a logical High (low current) before reaching the zero line current state.

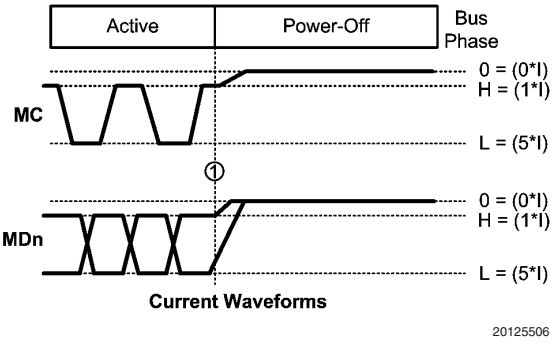


FIGURE 8. Bus Power Down Timing

RGB VIDEO INTERFACE

The LM2506 is transparent to data format and control signal timing. Each PCLK, data inputs, HS, VS and DE are sampled. A PCLK by PCLK representation of these signals is duplicated on the opposite device after being transferred across the MPL Level-0 interface.

The LM2506 uses a multiple range PLL and an on-chip multiplier to accommodate a wide range of display formats. QVGA to ½SVGA can be supported within the 2 MHz to 13.3 MHz PCLK input range.

Pixel Bandwidth = H. X V. X Color Depth X Frames

Functional Description (Continued)

Pixel bandwidth is equal to display resolution times color depth times frame rate.

Net Bandwidth = (Pixel BW)(24/18)(1.0 + % Blanking)

Net bandwidth is equal to the pixel bandwidth times the overhead times the blanking overhead.

PCLK Rate = Net Bandwidth / 24

The PCLK rate is equal to the net bandwidth divided by the total number of bits.

Format	Hor. Pixels	Ver. Pixels	Color Depth	Frames fps	Pixel BW Mbps	Percent Blanking	Net BW Mbps	PCLK rate MHz
½SVGA	800	300	18	50	216	10	316	13.2
¾VGA	640	320	16	55	180	10	265	11
½VGA	320	480	18	55	152	10	223	9.3
QVGA	320	240	18	55	76	20	122	5.1

Other RGB Color Depths

When transporting color depth below 18-bit, the 18-bit protocol can be used by offsetting the color data. The LSBs of the RGB are not used and data is offset toward the upper (MSB) end of the bit fields. Unused inputs should be tied off.

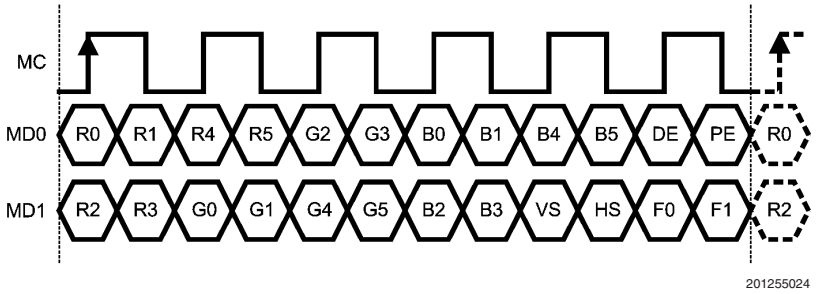


FIGURE 9. 18-bit RGB Display Mode Transaction

Parity Error Output

Parity Status is output as a pulse on the Parity Error (PE) output pin (DES) whenever there is a parity error. These pulses could be counted or used by various diagnostic equipment. PE is a high going pulse that is 3 MC cycles long for each frame containing an error. The PCLK output can be used to sample the PE bit. SET time is nominally 2 MC cycles and a HOLD time of 1 MC cycle. The serial PE bit is Odd Parity and is based on the RGB, and Control (VS, HS, DE) bits only. See *Figure 10*.

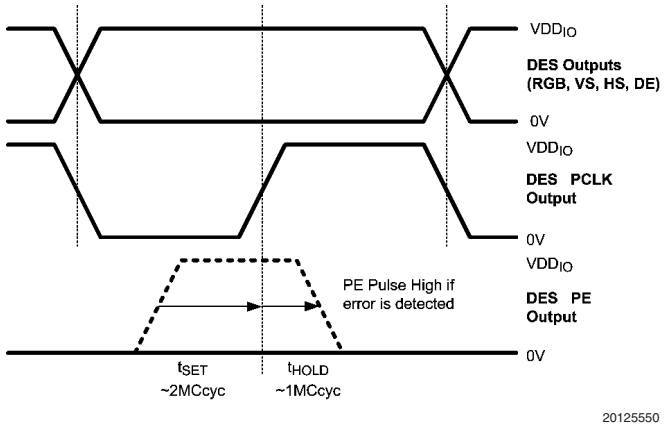


FIGURE 10. PE Output Timing

SYNCHRONIZATION DETECT AND RECOVERY

If a data error or clock slip error occurs over the MPL link, the LM2506 can detect this condition and recover from it. The method chosen is a data transparent method, and has very little overhead because it does not use a data expansion coding method. For the 18-bit color transaction (or frame), it

Functional Description (Continued)

uses two bits that are already required in the 6-MC cycle transaction. Since double-edge clocking is used with two data signals, adding one clock cycle to the transaction actually adds four bits. One of these bits is absolutely required - data enable - thus the others are allocated to Parity and the frame sequence (F[1:0]). Therefore total overhead for each pixel is 3/24 or 12.5% in 18-bit RGB mode.

HOST SIDE FUNCTION

The LM2506 in serializer mode simply increments the two bit field F[1:0] on every pixel or frame transmitted. Therefore every four frames, the pattern will repeat. It is very unlikely that this pattern would be found within the payload data, and if it were found, the probability that it would repeat for many frames becomes infinitely small.

DISPLAY SIDE FUNCTION

The LM2506 in deserializer mode, upon a normal power up sequence, starts in the proper synchronization. It looks for the incrementing pattern for N (N = 4 or 8) pixels (frames) and finding it, starts to output the pixel gray scale data and timing signals.

If a random bit error occurs in the F[1:0] field, the hysteresis counter decrements by one, but the chip continues to output data normally. The next frame will likely recover, incrementing the hysteresis counter back to the maximum and things will continue normally. Likewise if a random bit error occurs in the gray scale data, it only effects that bit and transmission will continue normally on the next frame (pixel). The worst case data bit error would cause a one pixel wide glitch in the HS, VS or DE signals. This would likely cause a visible jump in the display, but it would recover in a maximum of one display frame time. (typically under 20mS)

If however, a clock slip or error occurs, the next N frames will be bad and the F[1:0] field will not be detected properly for each frame after the clock error. In this case, the hysteresis counter will decrement to zero quickly (again where N=4 or 8 pixels). This action shuts down the output data (output PCLK held Low), and initiates a search function for the incrementing sequence.

Detecting the Incrementing Sequence

Acquiring synchronization from a random position requires looking only at the MD1 line, as this line contains the incrementing sequence F[1:0]. This is done by examining six two-bit pairs and comparing each pair to an incrementing sequence. A snapshot of the data is first taken and loaded into six two-bit adders. The adders increment by one and then compare the same bit positions in the next 12-bits. If a match is found a flag is set for that bit pair. This same procedure is followed until there is only one flag set. After only one flag is set, the synchronization is tested for the full count of the hysteresis counter (4 or 8 pixels) and then a valid synchronization is declared and pixel data and strobes are again output to the display.

In the best case, this parallel method of detecting sync is very fast. If only one flag exists on the first frame tested, then resynchronization can occur in as little as 6 pixel times (assuming NNE = no new errors). If however, random data emulates an incrementing sequence for several pixels of time, the process can take longer. It is data dependant.

It is important to note that a pathological case exists, as it does for most pattern detection methods, where the data can forever emulate this incrementing sequence, when in fact the true F[1:0] is not detected. This F'[1:0] (F prime) may occur for several pixels, but becomes linearly less probable as more and more data passes through the system.

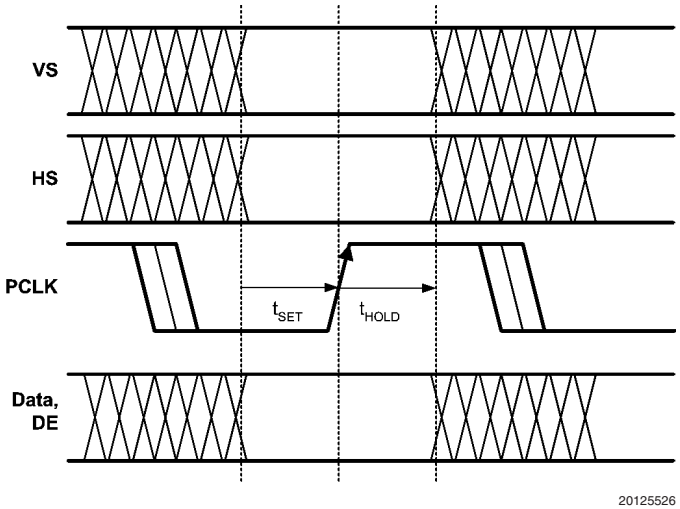


FIGURE 11. Serializer Mode Input Timing for RGB Interface

Functional Description (Continued)

TABLE 2. Serializer Input Timing Parameters for RGB Interface

Sym.	Parameter	Min	Typ	Max	Units
t_{SET}	Data (RGB, DE, VS or HS) to PCLK - Set Time	5			ns
t_{HOLD}	PCLK to Data (RGB, DE, VS or HS) - Hold Time	5			ns

Note 10: Signal rise and fall times are equal to or less than 20ns

Note 11: Measurement of signal timing is made using 0.3 x VDDIO for the low sate and 0.7 x VDDIO for the high state.

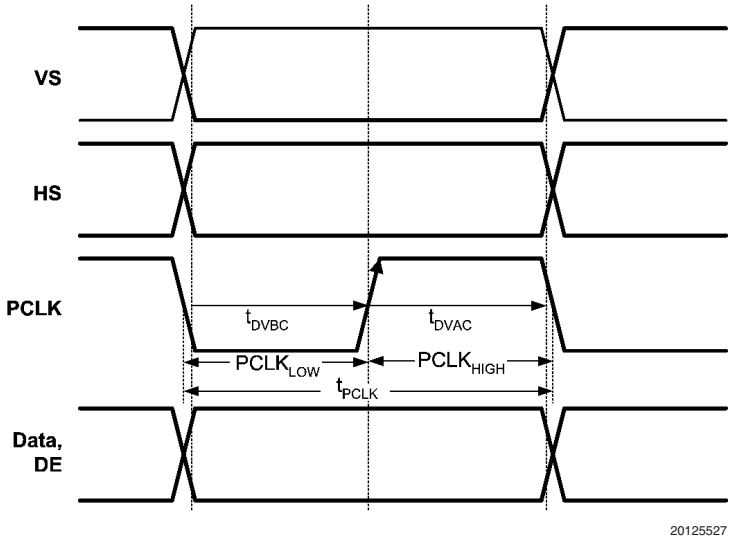


FIGURE 12. Deserializer Mode Output Timing for RGB Interface

TABLE 3. Deserializer Output Timing Parameters for RGB Interface

Sym.	Parameter		Min	Typ	Max	Units
t_{DVBC}	Data Valid before PCLK (rise) (Note 9)	PCLK = 2 MHz	230			ns
		PCLK = 13.3 MHz	30			ns
t_{DVAC}	Data Valid after PCLK (rise) (Note 9)	PCLK = 2 MHz	230			ns
		PCLK = 13.3 MHz	30			ns
t_{PCLK}	Pixel Clock Period		75.2		500	ns
$PCLK_{LOW}$	Pixel Clock Low			50		%
$PCLK_{HIGH}$	Pixel Clock High			50		%

LM2506 Features and Operation

POWER SUPPLIES

The V_{DDcore} and V_{DDA} (MPL and PLL) must be connected to the same potential between 1.74V and 2.0V. V_{DDIO} powers the logic interface and may be powered between 1.74 and 3.0V to be compatible with a wide range of host and target devices. **On this device, V_{DDIO} should be powered up before V_{DDcore}/V_{DDA} or at the same time as V_{DDcore}/ $V_{DDA}$for proper device configuration.**

BYPASS RECOMMENDATIONS

Bypass capacitors should be placed near the power supply pins of the device. Use high frequency ceramic (surface mount recommended) 0.1 µF capacitors. A 2.2 to 4.7 µF Tantalum capacitor is recommended near the SER V_{DDA} pin for PLL bypass. Connect bypass capacitors with wide traces and use dual or larger via to reduce resistance and inductance of the feeds. Utilizing a thin spacing between power and ground planes will provide good high frequency bypass above the frequency range where most typical surface mount capacitors are less effective. To gain the maximum benefit from this, low inductance feed points are important. Also, adjacent signal layers can be filled to create additional capacitance. Minimize loops in the ground returns also for improved signal fidelity and lowest emissions.

UNUSED/OPEN PINS

Unused inputs must be tied to the proper input level — do not float them. Unused outputs should be left open to minimize power dissipation.

PHASE-LOCKED LOOP

When the LM2506 is configured as a RGB Serializer, a PLL is enabled to generate the serial link clock. The Phase-locked loop system generates the serial data clock at 6X of the input clock. The MC rate must be between 12 and 80 MHz (PCLKs from 2 to 13.3 MHz).

MASTER(SER)/SLAVE(DES) SELECTION

The M/S* pin is used to configure the device as either a SER or DES device. When the M/S* pin is a Logic High, the Serializer (SER) configuration is selected. The Driver block is enabled for the MC line, and the MD lines. When the M/S* pin is a Logic Low, the Deserializer (DES) configuration is selected. The Receiver block is enabled for the MC line, and the MD lines.

POWER DOWN/OFF CONFIGURATION / OPTIONS AND CLOCK STOP

Power Up Operation - Upon the application of power to the LM2506, devices configured as a DES activate all outputs. Outputs are held in deasserted states, with all zeros on the data busses until valid data is received from the SER. If PD* is asserted (Low) prior to the application of power, then the part remains in its power down state.

On both the SER and the DES, the PD* pin resets the logic. **The PD* pins should be held low until the power supply has ramped up and is stable and within specifications.**

Power Down and the use of the PD* Input - When the PD* signal is asserted low, the entire chip regardless of mode, powers down. A Low on the PD* input pin will power down the entire device and turn off the line current to MD0, MD1, and MC. In this state the following outputs are driven to:

SER:

PD_{OUT} = Low

DES:

DATAn = PCLK = Low,

VS = HS = DE = PE = Low

Multiple configurations for PowerDown are possible with the chipset. These depend on the operating mode and configuration chosen. Two possible applications are shown in *Figure 14*. RGB Modes are shown in (A) and (B). "A" provides PD* input pins on both devices, this may be common or seperate. In (B), the SER is controlled by the PCLK STOP feature and a PDOUT* pin is provided to control the DES. When using the SER PD_{OUT*} mode, the V_{DDIO} rails of the devices should be the same to meet the PD* input thresholds of the DES.

The LM2506 provides a PCLK STOP feature on the SER device. Gating of the pixel clock signal can be used to generate a control signal for the SER to Power down or start up. When a loss of pixel clock is detected (PLL out of lock), the SER PD_{OUT*} pin is driven Low and the SER powers down. When a PCLK is reapplied, the SER powers up, and the PLL locks to the incoming clock signal. After 4,096 cycles (t0), the SER MPL outputs are enabled and the DES is calibrated. Once this is complete (t1 + t2 + t3), data transmission can occur. See *Figures 3, 4*. The stopping of the pixel clock should be done cleanly. Floating of the PCLK input pin is not recommended.

LM2506 Features and Operation (Continued)

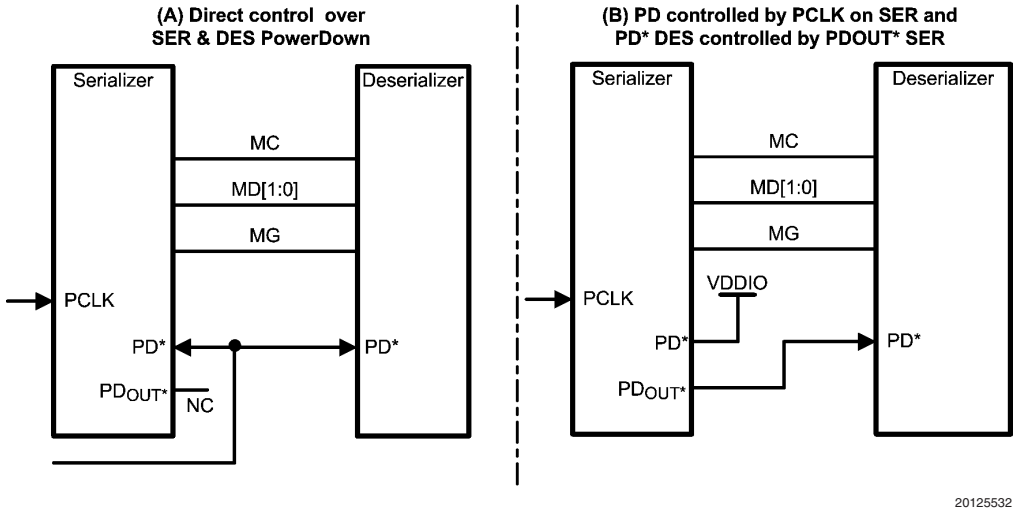


FIGURE 13. Power Down Control Options

Application Information

SYSTEM CONSIDERATIONS

When employing the MPL SER/DES chipset in place of a parallel bus, a few system considerations must be taken into account. VDDIO levels of the Host and SER must be compatible. VDDIO levels of the DES and the Display must be compatible. The LM2506 only supports **rising** edge clocking, both the Host and Display must be compatible with this.

MPL SWAP FEATURE

The LM2506 provides a swap function of MPL MD lines depending upon the state of the M/S* pin. This facilitates a straight through MPL interface design eliminating the needs for via and crossovers as shown on *Figure 14.* The parallel bus pins are also swapped to facilitate a flow though orientation of parallel bus signals.

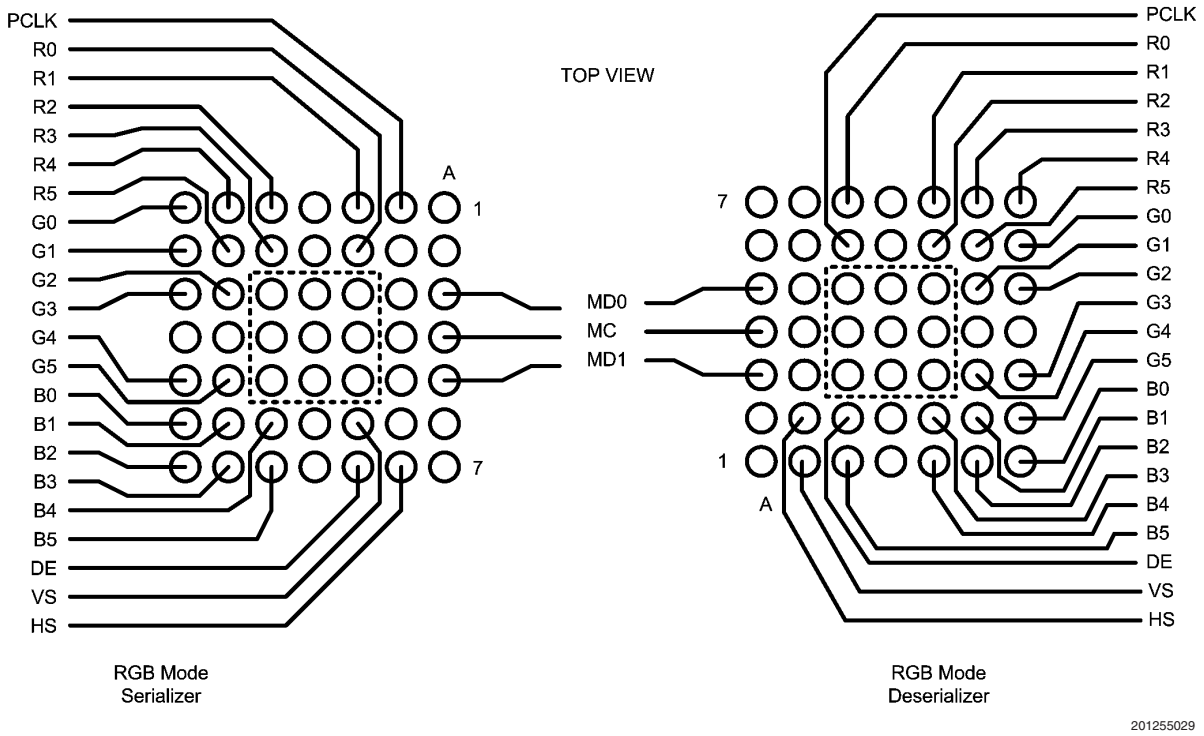
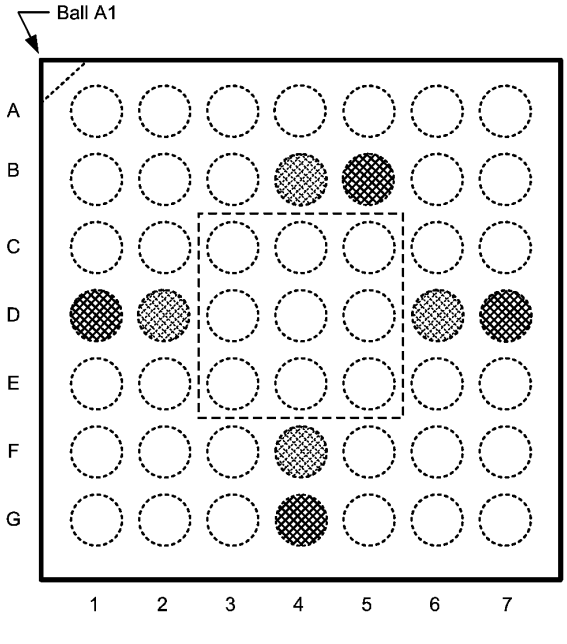


FIGURE 14. MPL Interface Layout

Application Information (Continued)

Power and Ground - Bumped Package

Power and ground bump assignments are shown in *Figure 15*. The nine center balls must be connected ground on the PCB for the microArray package. See also, National's Application Note AN-1126, Ball Grid Array, for information on land pattern recommendations and escape routing guidelines.



BALL	Description
B4	V_{SSA}
B5	V_{DDA}
D1	V_{DDIO}
D2	V_{SSIO}
D6	V_{SSIO}
D7	V_{DDIO}
F4	V_{SScore}
G4	V_{DDcore}

FIGURE 15. LM2506 PWR (V_{DD}) and GND (V_{SS}) Bumps (TOP VIEW)

FLEX CIRCUIT RECOMMENDATIONS

The three MPL lines should generally run together to minimize any trace length differences (skew). For impedance control and also noise isolation (crosstalk), guard ground traces are recommended in between the signals. Commonly a Ground-Signal-Ground (GSGSGSG) layout is used. Locate fast edge rate and large swing signals further away to also minimize any coupling (unwanted crosstalk). In a stacked flex interconnect, crosstalk also needs to be taken into account in the above and below layers (vertical direction). To minimize any coupling locate MPL traces next to a ground layer. Power rails also tend to generate less noise than LVCMOS so they are also good candidates for use as isolation and separation.

The interconnect from the SER to the DES typically acts like a transmission line. Thus impedance control and ground returns are an important part of system design. Impedance should be in the 50 to 100 Ohm nominal range for the LM2506. Testing has been done with cables ranging from 40 to 110 Ohms without error (BER Testing). To obtain the impedance, adjacent grounds are typically required (1 layer flex), or a ground shield / layer. Total interconnect length is intended to be in the 20cm range, however 30cm is possible at lower data rates. Skew should be less than 500ps to maximize timing margins.

GROUNDING

While the LM2506 employs three separate types of ground pins, these are intended to be connected together to a common ground plane. The separate ground pins help to isolate switching currents from different sections of the integrated circuit (IC). Also required is a nearby signal return (ground) for the MPL signals. These should be provided next to the MPL signals, as that will create the smallest current loop area. The grounds are also useful for noise isolation and impedance control.

PCB RECOMMENDATIONS

General guidelines for the PCB design:

- Floor plan – locate MPL SER near the connector to limit chance of cross talk to high speed serial signals.
- Route serial traces together, minimize the number of layer changes to reduce loading.
- Use ground lines are guards to minimize any noise coupling (guarantees distance).
- Avoid parallel runs with fast edge, large LVCMOS swings.
- Also use a GSGSG pinout in connectors (Board to Board or ZIF).
- DES device - follow similar guidelines.
- Bypass the device with MLC surface mount devices and thinly separated power and ground planes with low inductance feeds.
- High current returns should have a separate path with a width proportional to the amount of current carried to minimize any resulting IR effects.

Application Information (Continued)

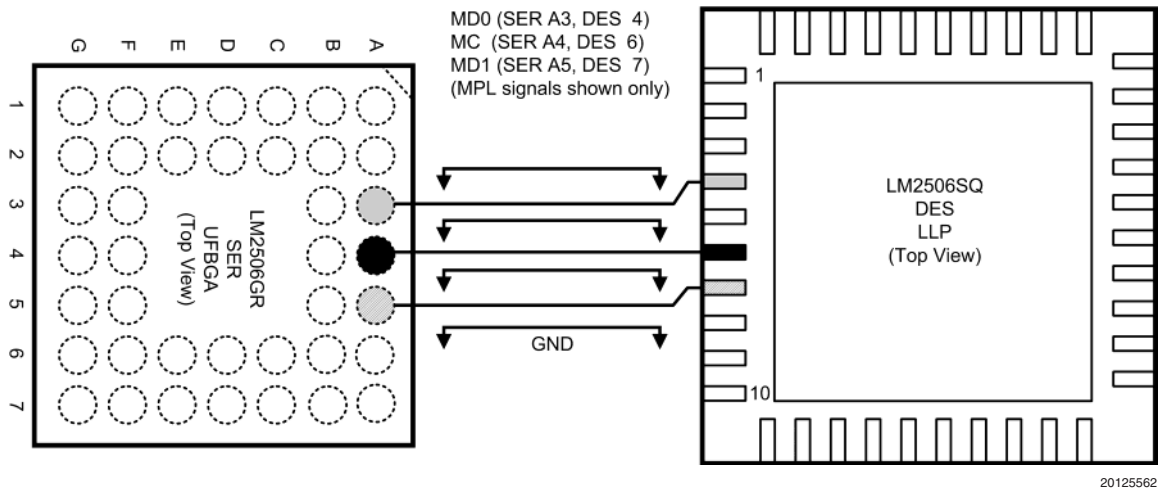
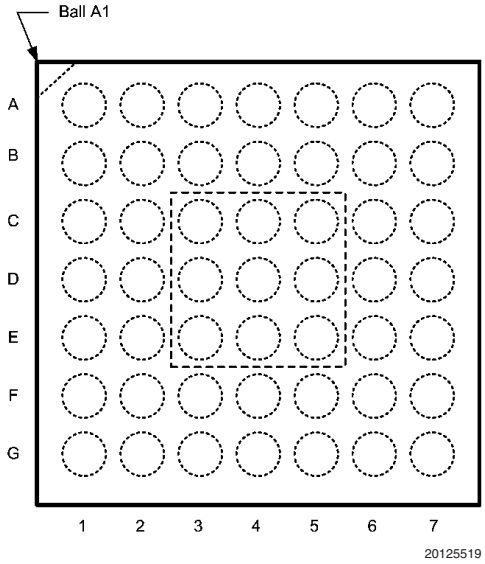


FIGURE 16. MPL Interface Layout

Connection Diagram microArray Package



TOP VIEW
(not to scale)

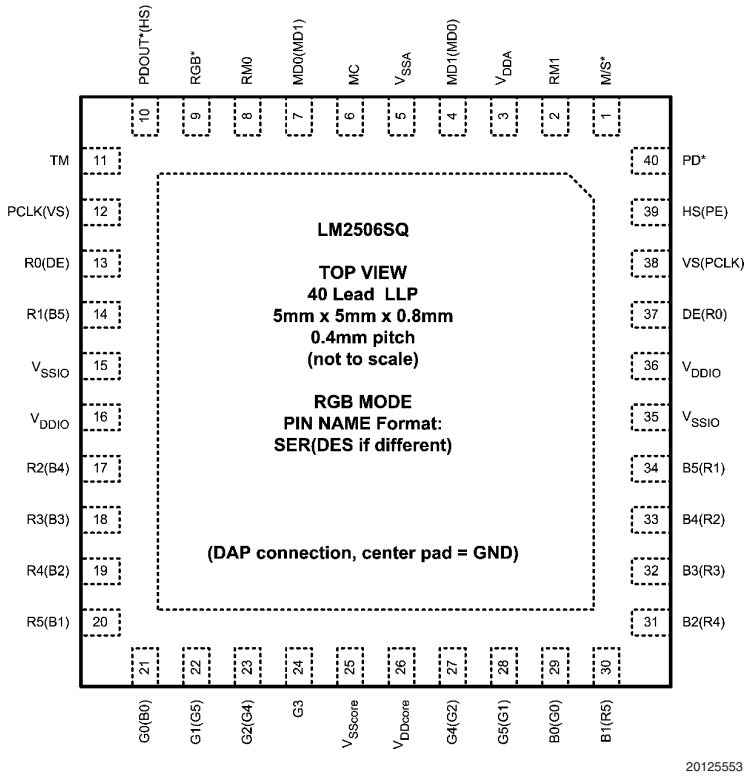
RGB SER Pinout

SER	1	2	3	4	5	6	7
A	TM	RGB*	MD0	MC	MD1	RM1	M/S*
B	PCLK	PD_{OUT*}	RM0	V_{SSA}	V_{DDA}	PD*	HS
C	R1	R0	V_{bulk}	V_{bulk}	V_{bulk}	VS	DE
D	V_{DDIO}	V_{SSIO}	V_{bulk}	V_{bulk}	V_{bulk}	V_{SSIO}	V_{DDIO}
E	R2	R3	V_{bulk}	V_{bulk}	V_{bulk}	B4	B5
F	R4	R5	G2	V_{SScore}	G5	B1	B3
G	G0	G1	G3	V_{DDcore}	G4	B0	B2

RGB DES Pinout

DES	1	2	3	4	5	6	7
A	TM	RGB*	MD1	MC	MD0	RM1	M/S*
B	VS	HS	RM0	V_{SSA}	V_{DDA}	PD*	PE
C	B5	DE	V_{bulk}	V_{bulk}	V_{bulk}	PCLK	R0
D	V_{DDIO}	V_{SSIO}	V_{bulk}	V_{bulk}	V_{bulk}	V_{SSIO}	V_{DDIO}
E	B4	B3	V_{bulk}	V_{bulk}	V_{bulk}	R2	R1
F	B2	B1	G4	V_{SScore}	G1	R5	R3
G	B0	G5	G3	V_{DDcore}	G2	G0	R4

Connection Diagram - LLP Package



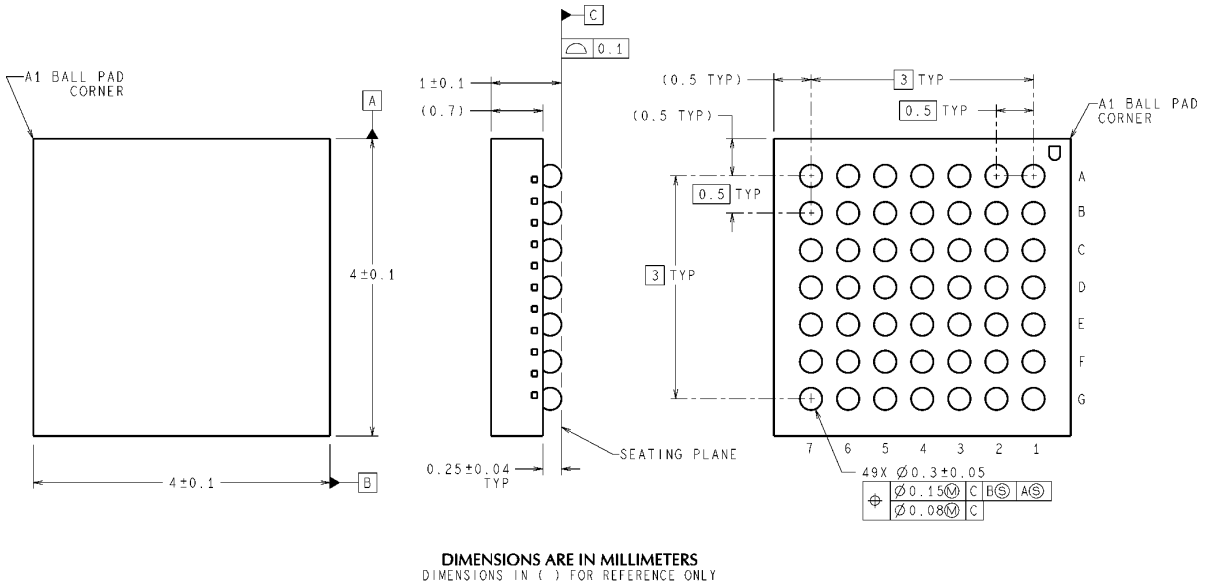
TOP VIEW — (not to scale)

TABLE 4. RGB Mode Pad Assignment

Pin #	SER	DES		Pin #	SER	DES
1	M/S*			21	G0	B0
2	RM1			22	G1	G5
3	V_{DDA}			23	G2	G4
4	MD1	MD0		24	G3	
5	V_{SSA}			25	V_{SScore}	
6	MC			26	V_{DDcore}	
7	MD0	MD1		27	G4	G2
8	RM0			28	G5	G1
9	RGB*			29	B0	G0
10	PDOUT*	HS		30	B1	R5
11	TM			31	B2	R4
12	PCLK	VS		32	B3	R3
13	R0	DE		33	B4	R2
14	R1	B5		34	B5	R1
15	V_{SSIO}			35	V_{SSIO}	
16	V_{DDIO}			36	V_{DDIO}	
17	R2	B4		37	DE	R0
18	R3	B3		38	VS	PCLK
19	R4	B2		39	HS	PE
20	R5	B1		40	PD*	
DAP	GND			DAP	GND	

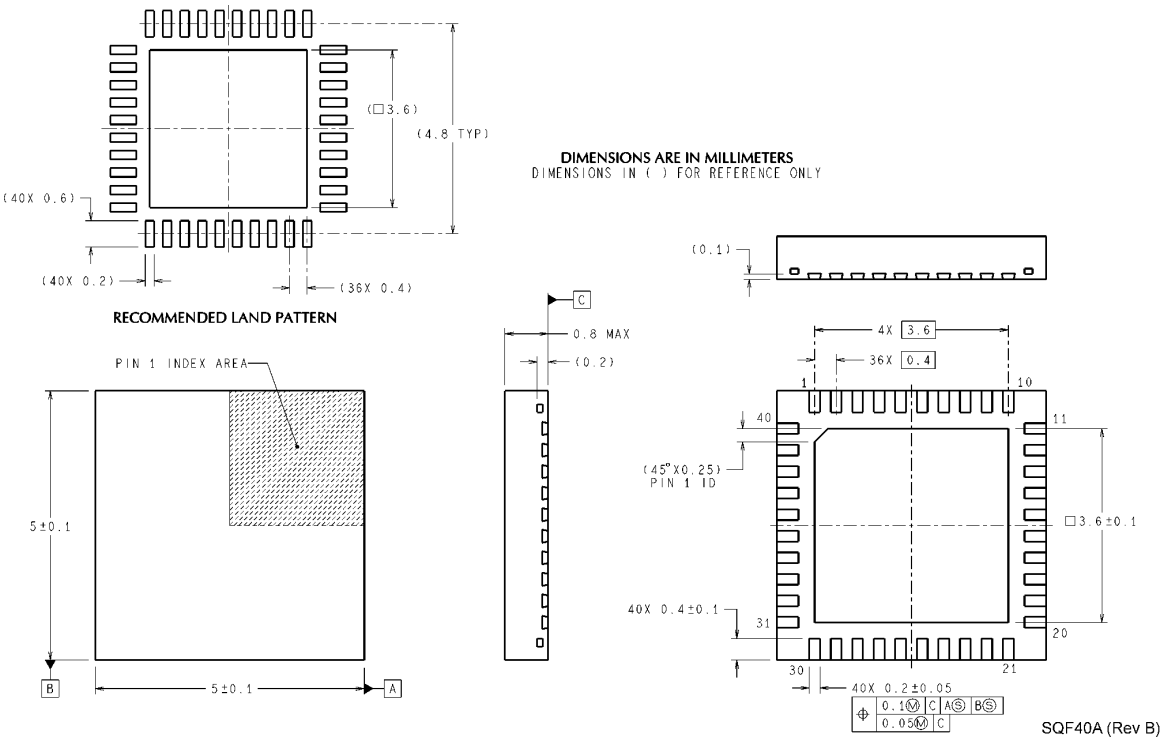
Note: Pins are different between SER and DES configurations.

Physical Dimensions inches (millimeters) unless otherwise noted



GRA49A (Rev A)

49L MicroArray, 0.5mm pitch
Order Number LM2506GR
NS Package Number GRA49A



SQF40A (Rev B)

40L LLP, 0.4mm pitch
Order Number LM2506SQ
NS Package Number SQF40A

Notes

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