National Semiconductor

MM54HCT640/MM74HCT640 Inverting Octal TRI-STATE® Transceiver MM54HCT643/MM74HCT643 True-Inverting Octal TRI-STATE Transceiver

General Description

These TRI-STATE bi-directional transceivers utilize advanced silicon-gate CMOS technology and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

All devices are TTL input compatible and can drive up to 15 LS-TTL loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Both the MM54HCT640/MM74HCT640 and the MM54HCT643/ MM74HCT643 have one active low enable input ($\overline{G}$), and a direction control (DIR). When the DIR input is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A. The MM54HCT640/MM74HCT640 transfers inverted data from one bus to the other. The MM54HCT643/MM74HCT643 transfers inverted data from the A bus to the B bus and non-inverted data from the B bus to the A bus.

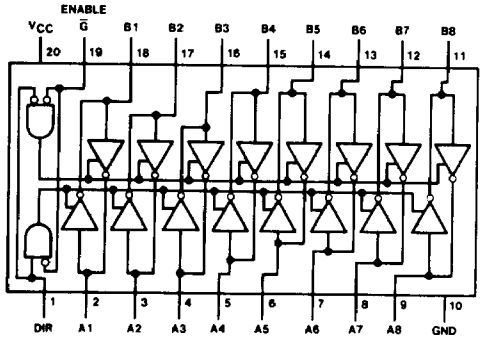
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input compatible
- Octal TRI-STATE outputs for μP bus applications: 6 mA, typical
- High speed: 16 ns typical propagation delay
- Low power: 80 μA maximum (74HCT)

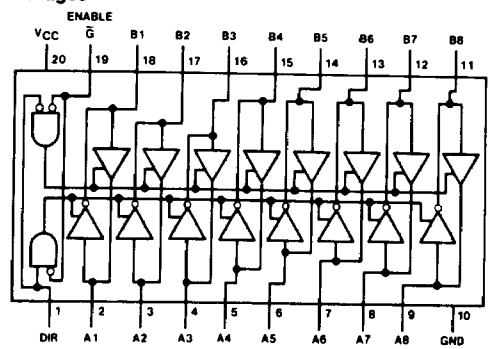
Connection Diagram

Dual-In-Line Packages



TL/F/5370–1

Top View
Order Number MM54HCT640* or MM74HCT640*



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Top View
Order Number MM54HCT643* or MM74HCT643*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Control Inputs		Operation	
$\overline{G}$	DIR	640	643
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

AC Electrical Characteristics MM54HCT640/MM74HCT640

V_{CC} = 5.0V ± 10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C		74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF	17	23	29	34	ns
		C_L = 150 pF	24	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1kΩ, C_L = 50 pF	23	30	38	45	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1kΩ, C_L = 50 pF	21	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	8	12	15	18	ns
C_{IN}	Maximum Input Capacitance		10	15	15	15	pF
C_{OUT}	Maximum Output/ Input Capacitance		20	25	25	25	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output) $\overline{G} = V_{CC}$	7				pF
		$\overline{G}$ = GND	100				pF

AC Electrical Characteristics MM54HCT643/MM74HCT643

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 45 pF	16	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L = 45 pF, R_L = 1 kΩ	29	40	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L = 5 pF, R_L = 1 kΩ	20	25	ns

AC Electrical Characteristics MM54HCT643/MM74HCT643

V_{CC} = 5.0V ± 10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C		74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
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C_{PD}	Power Dissipation Capacitance (Note 5)	(per output) $\overline{G} = V_{CC}$	7				pF
		$\overline{G}$ = GND	100				pF

Note 5: C_{PD} determines the no load power consumption. $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. The no load dynamic current consumption, $I_S = C_{PD} V_{CC} + I_{CC}$.

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