S-585AA

BUILT-IN ARP FUNCTION 2-WIRE SERIAL E²PROM WITH TEMPERATURE SENSOR

www.ablic.com

Rev.1.0_00

This IC is a 2-wire serial E²PROM with temperature sensor built in Address Resolution Protocol (ARP) function which operates in 1.7 V to 3.6 V voltage ranges. This IC has the capacity of 4 K-bit and the organization of 2 pages × 256-word × 8-bit. Page write and sequential read are available.
This IC operates with the SMBus and I²C-Bus at 1.0 MHz maximum.
A substantial reduction in current consumption may be achieved by using shutdown mode which can be set by the I²C-Bus.
In addition, the SMBus ARP function is supported; therefore, this IC is optimal for SSDs that communicate over the SMBus.

Caution **This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, it is imperative to contact our sales representatives.**

■ Features

E²PROM block

- Page write: 16 bytes / page
- Sequential read
- Write protect function during low power supply voltage
- Write protect:
  Individual software data protection for each of four 128-byte blocks
- Endurance: 10^6 cycle / word*1 (Ta = +25°C)
- Data retention: 100 years (Ta = +25°C)
- Memory capacity: 4 K-bit
- Initial delivery state: FFh

Temperature sensor block

- Temperature accuracy: ±0.25°C typ. / ±1.0°C max. (Ta = 0°C to +85°C)
  ±0.25°C typ. / ±1.5°C max. (Ta = –40°C to +125°C)
- Temperature sample rate: 8 samples / s min.
- Selectable hysteresis width: No hysteresis, 1.5°C, 3.0°C, 6.0°C

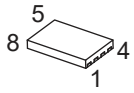
Overall

- Support for SMBus ARP function
- Support for Alert Response Address function (ARA)
- Support for Default Slave Address (DSA)
- Current consumption:
  E²PROM in standby mode and temperature sensor in shutdown mode: 3.0 µA max.
  E²PROM in standby mode and temperature sensor in active mode: 0.1 mA max.
  E²PROM in read operation mode and temperature sensor in active mode: 0.4 mA max.
  E²PROM in write operation mode and temperature sensor in active mode: 2.0 mA max.
- Operation voltage range: 1.7 V to 3.6 V
- Operation frequency: 1.0 MHz max. (V_{DD} = 2.2 V to 3.6 V)
  400 kHz max. (V_{DD} = 1.7 V to 3.6 V)
- Noise suppression: Schmitt trigger and noise filter on input pins (SCL, SDA)
- Operation temperature range: Ta = –40°C to +125°C
- Lead-free (Sn 100%), halogen-free

***1.** For each address (Word: 8-bit)

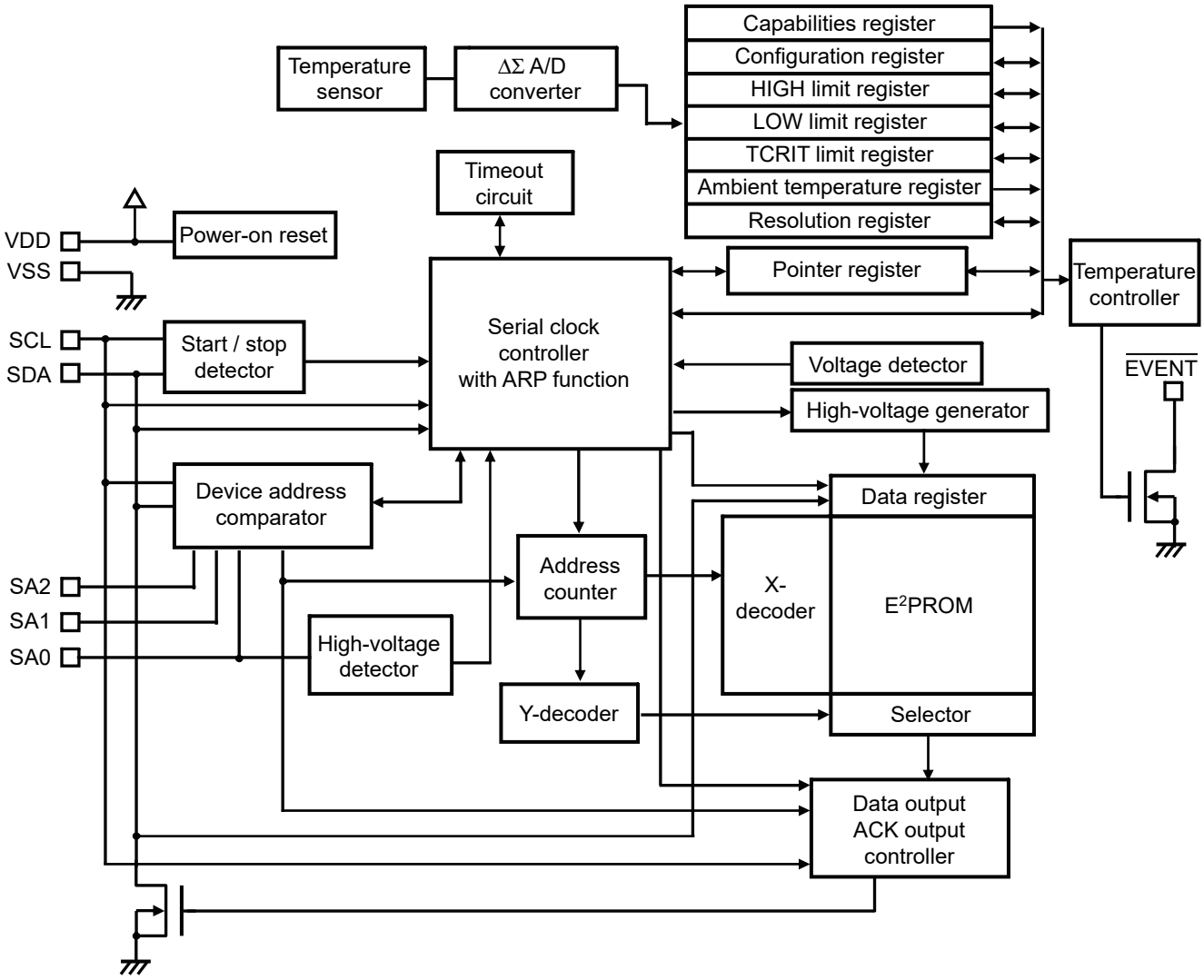
■ Package

- DFN-8(2030)B



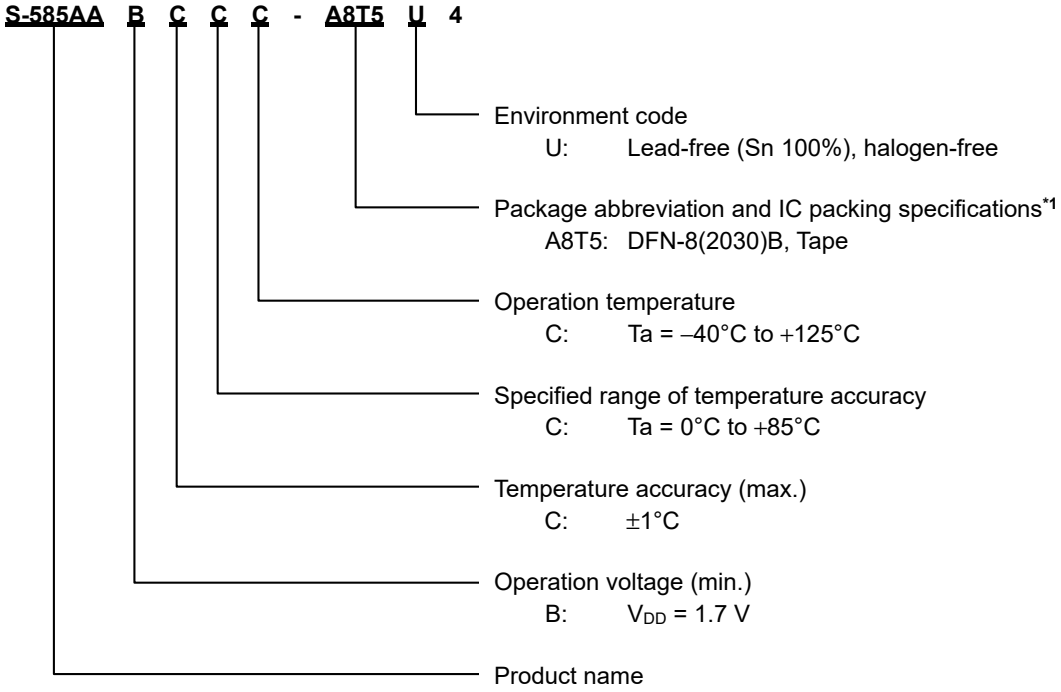
(3.0 × 2.0 × t0.8 mm max.)

■ Block Diagram



■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.

2. Package

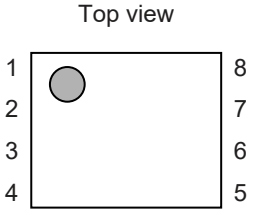
Package Name	Dimension	Tape	Reel	Land
DFN-8(2030)B	PQ008-B-P-SD	PQ008-B-C-SD	PQ008-B-R-SD	PQ008-B-L-SD

3. Product name list

Product Name	Capacity	Package Name
S-585AABCCC-A8T5U4	4 K-bit	DFN-8(2030)B

■ Pin Configuration

1. DFN-8(2030)B



Pin No.	Symbol	Description
1	SA0	Select address input
2	SA1	Select address input
3	SA2	Select address input
4	VSS	Ground
5	SDA*1	Serial data I/O
6	SCL*1	Serial clock input
7	$\overline{\text{EVENT}}$	Temperature event output
8	VDD	Power supply

***1.** Do not use it in "High-Z".

Remark For DFN-8(2030)B package, connect the heatsink of back side to the board, and set electric potential open or V_{SS}. However, do not use it as the function of electrode.

■ Absolute Maximum Ratings

Table 1

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	–0.3 to +4.3	V
Input voltage (SCL, SA1, SA2)	V_{IN}	–0.3 to +4.3	V
SA0 pin high level input voltage	V_{HV}	–0.3 to +10.0	V
I/O voltage (SDA)	V_{IO}	–0.3 to +4.3	V
Output voltage ($\overline{EVENT}$)	V_{OUT}	–0.3 to +4.3	V
Operation ambient temperature	T_{opr}	–40 to +125	°C
Storage temperature	T_{stg}	–65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operation Conditions

Table 2

Item	Symbol	Condition	Min.	Max.	Unit
Power supply voltage	V_{DD}	–	1.7	3.6	V
Operation ambient temperature	T_{opr}	–	–40	+125	°C
High level input voltage	V_{IH}	–	$0.7 \times V_{DD}$	$V_{DD} + 0.5$	V
Low level input voltage	V_{IL}	–	–0.3	$0.3 \times V_{DD}$	V
SA0 pin high level input voltage	V_{HV}	$V_{HV} - V_{DD} \geq 4.8$ V	7.0	10.0	V

■ Pin Capacitance

Table 3

(Ta = +25°C, f = 1.0 MHz, V_{DD} = 2.5 V)

Item	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V (SCL, SA0, SA1, SA2)	–	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V (SDA)	–	8	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V ($\overline{EVENT}$)	–	8	pF

■ Endurance

Table 4

Item	Symbol	Condition	Min.	Max.	Unit
Endurance	N_W	Ta = +25°C	10^6	–	cycle / word*1

***1.** For each address (Word: 8-bit)

■ Data Retention

Table 5

Item	Symbol	Condition	Min.	Max.	Unit
Data retention	–	Ta = +25°C	100	–	year

■ DC Electrical Characteristics

Table 6

Item	Symbol	Condition	Ta = –40°C to +125°C, V_{DD} = 1.7 V to 3.6 V		Unit
			Min.	Max.	
Shutdown current consumption	I_{SD}	E²PROM: standby mode Temperature sensor: shutdown mode	–	3.0	μA
Standby current consumption	I_{DD1}	E²PROM: standby mode Temperature sensor: active mode	–	0.1	mA
Current consumption (READ)	I_{DDR}	E²PROM: read mode Temperature sensor: active mode f_{SCL} = 1000 kHz	–	0.4	mA
Current consumption (WRITE)	I_{DDW}	E²PROM: write mode Temperature sensor: active mode f_{SCL} = 1000 kHz	–	2.0	mA
Input leakage current	I_{LI}	SCL, SDA V_{IN} = V_{SS} to V_{DD}	–	1.0	μA
Output leakage current	I_{LO}	SDA, $\overline{EVENT}$ V_{OUT} = V_{SS} to V_{DD}	–	1.0	μA
Input current 1	I_{IL}	SA0, SA1, SA2 $V_{IN} < 0.3 \times V_{DD}$	–	50.0	μA
Input current 2	I_{IH}	SA0, SA1, SA2 $V_{IN} > 0.7 \times V_{DD}$	–	2.0	μA
Input impedance 1	Z_{IL}	SA0, SA1, SA2 $V_{IN} = 0.3 \times V_{DD}$	30	–	kΩ
Input impedance 2	Z_{IH}	SA0, SA1, SA2 $V_{IN} = 0.7 \times V_{DD}$	800	–	kΩ
Low level output voltage	V_{OL}	SDA, $\overline{EVENT}$ I_{OL} = 3.0 mA	–	0.4	V
Low level output current 1	I_{OL1}	SDA, $\overline{EVENT}$ V_{OL} = 0.4 V, 2.2 V ≤ V_{DD} ≤ 3.6 V	20	–	mA
Low level output current 2	I_{OL2}	SDA, $\overline{EVENT}$ V_{OL} = 0.6 V, f_{SCL} ≤ 400 kHz, 1.7 V ≤ V_{DD} ≤ 2.2 V	6	–	mA
Power-on reset threshold voltage	V_{PON}	–	1.6	–	V
Power-off threshold voltage	V_{POFF}	–	–	0.9	V

■ AC Electrical Characteristics

Table 7 Measurement Conditions

Input pulse voltage	$0.2 \times V_{DD}$ to $0.8 \times V_{DD}$
Input pulse rising / falling time	20 ns or less
Output reference voltage	$0.3 \times V_{DD}$ to $0.7 \times V_{DD}$
Output load	100 pF

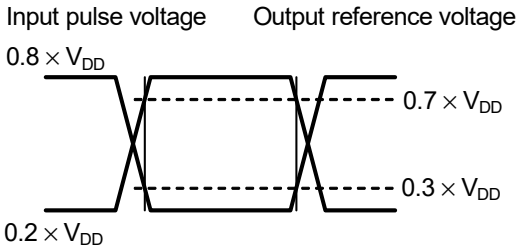


Figure 1 Input / Output Waveform during AC Measurement

Table 8

Item	Symbol	Ta = –40°C to +125°C						Unit
		V_{DD} = 1.7 V to 3.6 V				V_{DD} = 2.2 V to 3.6 V		
		f_{SCL} = 100 kHz		f_{SCL} = 400 kHz		f_{SCL} = 1000 kHz		
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	10	100	10	400	10	1000	kHz
SCL clock time "L"	t_{LOW}	4.7	–	1.3	–	0.5	–	µs
SCL clock time "H"	t_{HIGH}	4.0	–	0.6	–	0.26	–	µs
SCL clock "L" timeout	$t_{TIMEOUT}$	25	35	25	35	25	35	ms
SCL, SDA rising time	t_R	0.02	1.0	0.02	0.3	–	0.12	µs
SCL, SDA falling time	t_F	0.02	0.3	0.02	0.3	–	0.12	µs
Data input setup time	$t_{SU.DAT}$	250	–	100	–	50	–	ns
Data input hold time	$t_{HD.DI}$	0	–	0	–	0	–	ns
Data output hold time	$t_{HD.DAT}$	0	–	0	–	0	–	ns
Start condition setup time	$t_{SU.STA}$	4.7	–	0.6	–	0.26	–	µs
Start condition hold time	$t_{HD.STA}$	4.0	–	0.6	–	0.26	–	µs
Stop condition setup time	$t_{SU.STO}$	4.0	–	0.6	–	0.26	–	µs
Bus release time	t_{BUF}	4.7	–	1.3	–	0.5	–	µs
Noise suppression time	t_I	–	50	–	50	–	50	ns
Power-off time	t_{POFF}	1	–	1	–	1	–	ms
Initialize time	t_{INIT}	10	–	10	–	10	–	ms

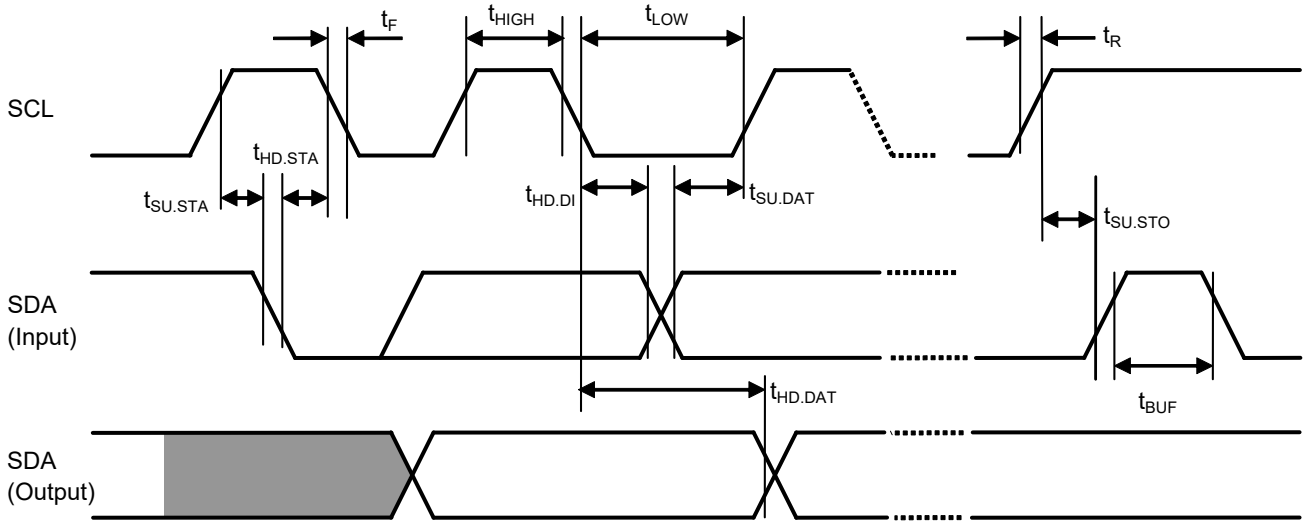


Figure 2 Bus Timing

Table 9

Item	Symbol	Ta = –40°C to +125°C V_{DD} = 1.7 V to 3.6 V		Unit
		Min.	Max.	
Write time	t_{WR}	–	5.0	ms

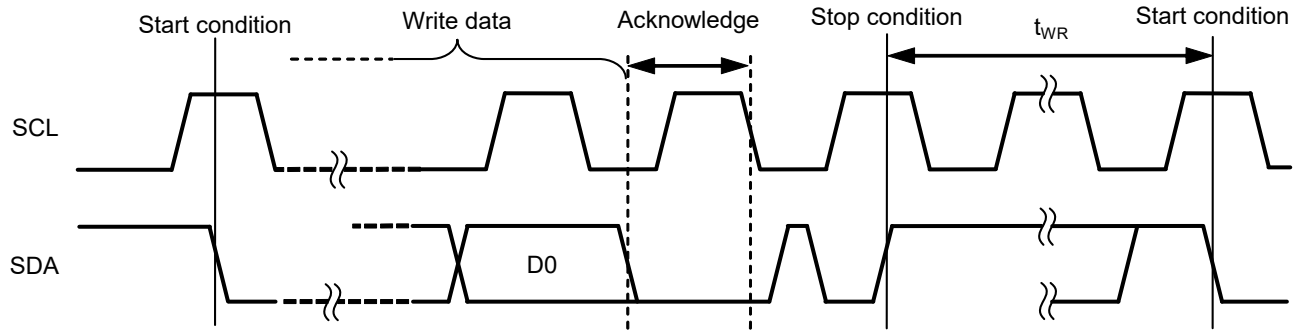


Figure 3 Write Cycle Timing

■ Temperature Characteristics

Table 10

Item	Symbol	Condition	V_{DD} = 1.7 V to 3.6 V			Unit
			Min.	Typ.	Max.	
Temperature sensor accuracy	T_{ACC1}	Ta = 0°C to +85°C	–	±0.25	±1.0	°C
	T_{ACC2}	Ta = –40°C to +125°C	–	±0.25	±1.5	°C
Resolution	T_{RES}	Default value	–	0.25	–	°C
Temperature conversion time	t_{CONV}	All TRES [1:0] settings	–	–	125	ms

■ SMBus / I²C-Bus

1. Overview

This IC operates as a slave device only on the I²C-Bus and the SMBus. Connections to the bus are made through the open drain I/O lines, SDA and SCL. Normal communication is based on the I²C-Bus protocol, and Addressing is based on the SMBus protocol.

2. SMBus addressing

This IC addrress is assigned using SMBus ARP Protocol. The temperature sensor and E²PROM default slave address is set by connecting each of the SA0 pin, SA1 pin and SA2 pin to the VSS pin or the VDD pin. When you assign address to this IC, you shoud assign an address to Temperature Sensor function and E²PROM function respectively. The SWPn, CWP, RPSn write protect commands and SPAn, RPA E²PROM page address commands don't support SMBus ARP Protocol. These address are fixed default slave address and must not be assigned to any SMBus slave device.

3. Start and stop condition

Start is identified by a "H" to "L" transition of the SDA line while the SCL line is stable at "H".
Every operation begins from a start condition.
Stop is identified by a "L" to "H" transition of the SDA line while the SCL line is stable at "H".

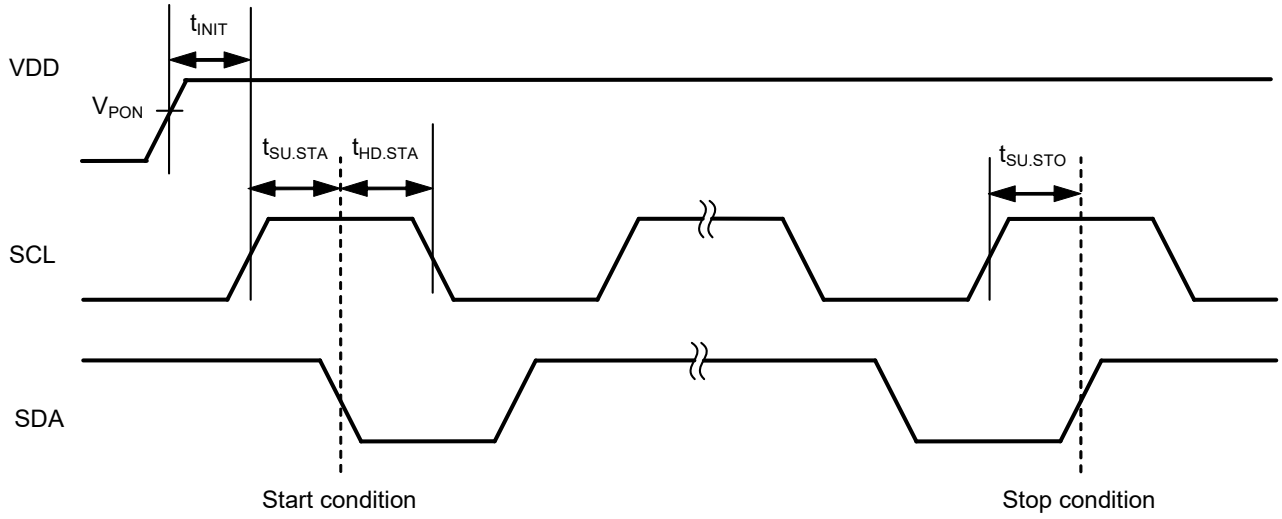


Figure 4 Start / Stop Conditions after Power-on

4. Data transmission

Changing the SDA line while the SCL line is "L", data is transmitted.
Changing the SDA line while the SCL line is "H", a start or stop condition is recognized.

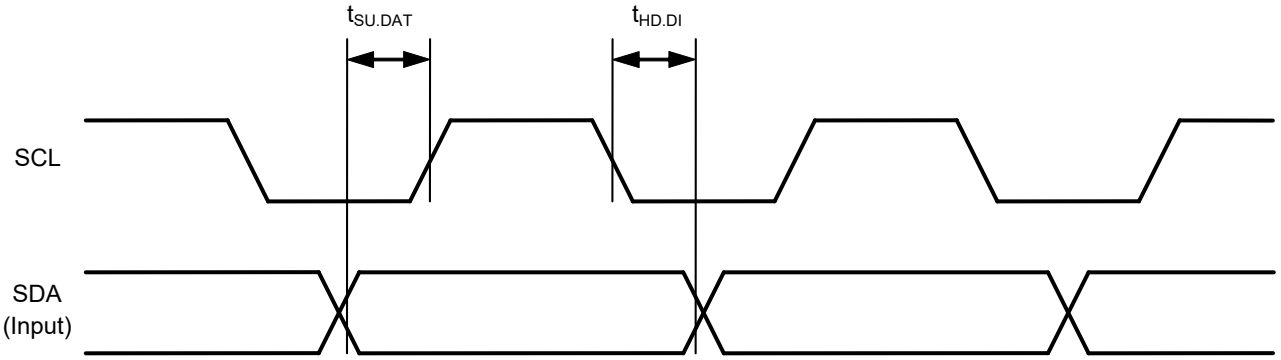


Figure 5 Data Transmission Timing

5. Acknowledge

The unit of data transmission is 8 bits. During the 9th clock cycle period the receiver on the bus pulls down the SDA line to acknowledge the receipt of the 8-bit data.

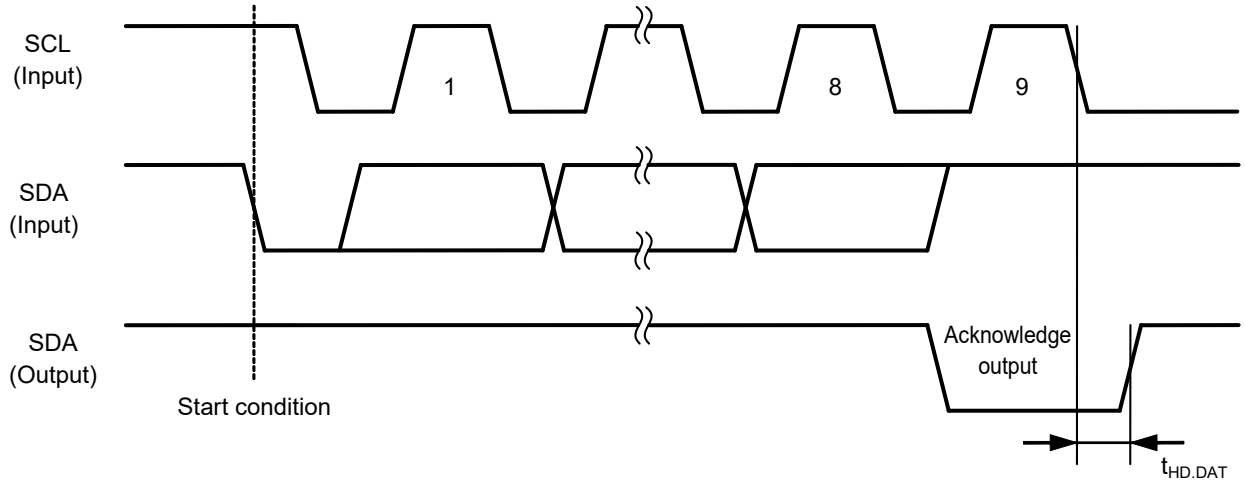
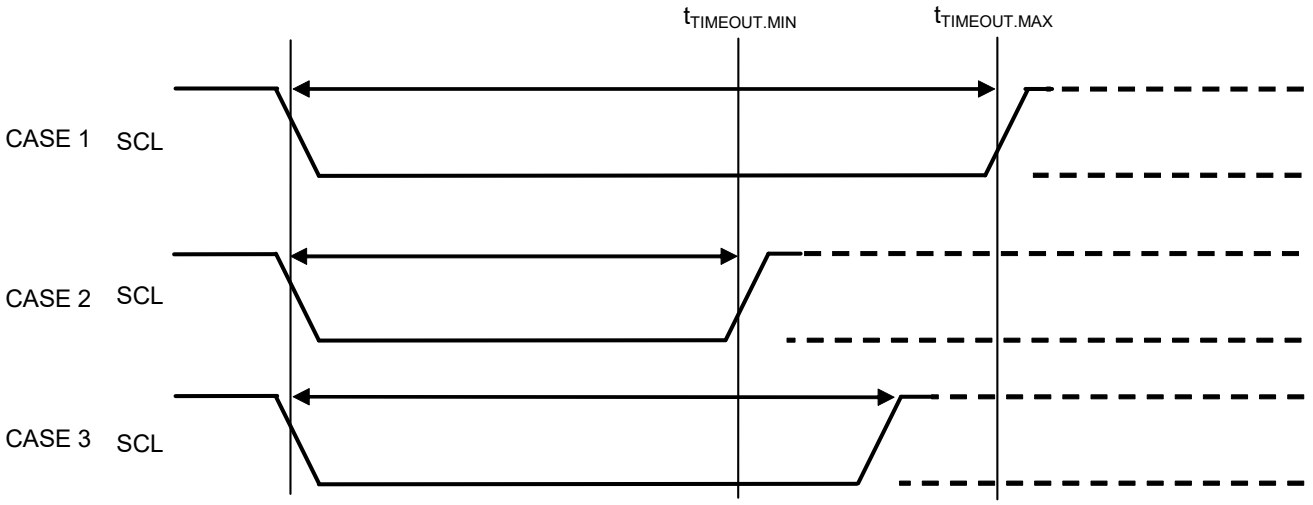


Figure 6 Acknowledge Output Timing

6. Timeout

This IC has the timeout function. If the SCL stays "L" for the SCL clock "L" timeout ($t_{TIMEOUT}$) or more, this IC resets the serial interface and becomes to standby mode. If the SCL stays "L" for less than the $t_{TIMEOUT}$, this IC does not reset the serial interface. The $t_{TIMEOUT}$ is 30 ms typ.
When this IC is not in the range of the clock frequency specified by AC characteristics, it may not perform communication normally.



CASE 1: SCL clock time "L" (t_{LOW}) ≥ $t_{TIMEOUT.MAX}$, this IC will reset the bus communication and return to standby mode.
CASE 2: t_{LOW} < $t_{TIMEOUT.MIN}$, this IC will not reset the bus communication.
CASE 3: $t_{TIMEOUT.MIN}$ ≤ t_{LOW} < $t_{TIMEOUT.MAX}$, this IC may or may not reset the bus communication.

Figure 7 Examples of the Timeout Timing

7. Packet Error Code (PEC) support

PEC is defined in the SMBus specification. It is an extra byte at the end of the SMBus transaction, which is a CRC-8 calculated on all of the preceding bytes (not including ACKs, NACKs, STARTs, or STOPs) in the SMBus transaction. The polynomial for this CRC-8 is:

$$x8 + x2 + x + 1$$

8. Collision and arbitration

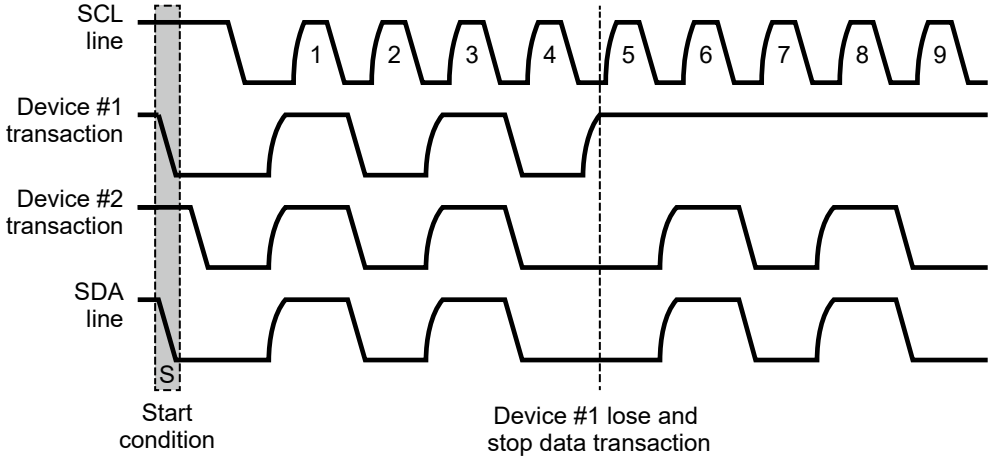


Figure 8 Bus Collision Detection

This IC monitors bus collision at each rising edge of the clock during data transaction. In the event of a bus collision, when SCL is "H", a device that sends "H" while other device is sending "L" will stop its data transaction until the stop condition is received. This IC does not support the Notify ARP Master command.

The arbitration period is the first byte from the start condition of all command and the UDID transaction period during Get UDID (general) command. If a bus collision occurs during the arbitration period, the devices that detect it simply stop data transaction.

9. SMBus ARP function

This IC supports the SMBus ARP protocol as defined in the SMBus specification.
This IC is a DSA device, meaning its slave address is valid after power up (by set SA pin). This IC supports all SMBus ARP commands defined in the SMBus specification except Notify ARP Master command, both general and directed.
This function can be switched enable / disable. The method is same as the UDID Write / Read mode.

9. 1 SMBus ARP flow

SMBus ARP flow is based on the status of one flag:

- AR (Address Resolved): This flag is set when the slave address is resolved (slave address was assigned by the SMBus ARP process).

Remark This flag is internal this IC flag and is not shown to external devices. This flag is provided for Temperature Sensor function and E²PROM function respectively.

The AR flag is cleared after power on until the SMBus ARP process completes. This IC always has a valid slave address.

When the HOST wants to start a SMBus ARP process, it resets (in terms of ARP functionality) all the devices on the Bus by issuing either Prepare to ARP or Reset Device commands. When this IC accepts Prepare to ARP commands, it clears its AR flag (if set from previous SMBus ARP process). When this IC accepts Reset Device (general) or Reset device ARP (directed), it clears its AR flag and assume their default slave addresses.

With the AR flag cleared, this IC answers the following SMBus ARP transactions that are issued by the HOST. The HOST then issues a Get UDID command (general or directed) to identify the devices on the Bus. This IC responds to the Directed command every time and to the General command only if its AR flag is not set. After a Get UDID command, the HOST assigns this IC new slave addresses by issuing an Assign Address command. This IC checks whether the UDID matches its own UDID and if matched, switches its slave address to the address assigned by the command (byte 17). After accepting the Assign Address command, the AR flag is set, and from this point on (as long as the AR flag is set) this IC does not respond to the Get UDID (general) command, while all other commands should be processed even if the AR flag is set. **Figure 9** shows the SMBus ARP flow.

For detecting the hot-plugged, the HOST can use Get UDID command. The HOST issues the Get UDID (general) command at least once every 10 seconds to discover newly added devices that require address resolution but that don't support the Notify ARP Master command. Newly added device will enter the system with a power-on reset, which will reset its AR flag. It will respond the Get UDID (general) command with its UDID. The HOST may choose to assign such a newly added device a non-conflicting address or to do re-ARP the entire bus. For more the command detail, refer to "**9. 3. 4 Get UDID (general)**".

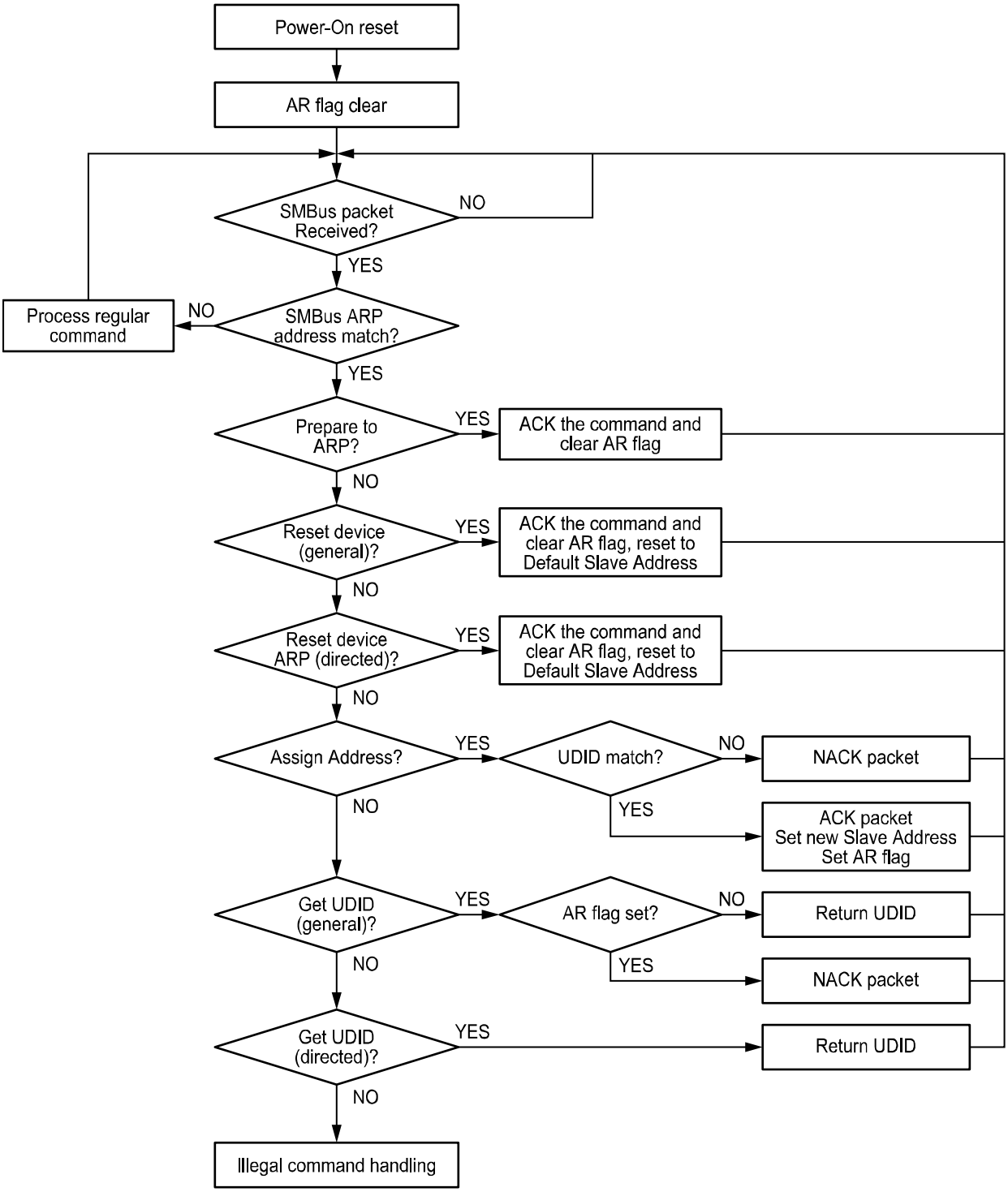


Figure 9 SMBus ARP Flow

9. 2 SMBus ARP UDID content

The Unique Device Identifier (UDID) provides a mechanism to isolate each device for the purpose of address assignment. Each device has a unique identifier. The 128-bit number is comprised of the following fields:

Table 11 UDID Value

Bit No.	Field Name	Function	Value
[127:120]	Device Capabilities	Indicates whether address assignment and PEC are possible	1000_0000
[119:112]	Version / Revision	The version of UDID format being adopted The device revision	0000_1XXX*1
[111:96]	Vendor ID	An ABLIC ID decided by PCI SIG (1C85h)	0001_1100 1000_0101
[95:80]	Device ID	Indicates the type of device	XXXX_XXXX XXXX_XXX*1Y*2
[79:64]	Interface	Identifies the protocol layer interfaces supported over the SMBus connection by the device. For example, ASF and IPMI	0000_0000 0000_0101
[63:48]	Subsystem Vendor ID	A customer ID who makes a product using this IC	1111_1111 1111_1111*3
[47:32]	Subsystem Device ID	ID indicating the type of product using this IC	1111_1111 1111_1111*3
[31:0]	Vendor-specific ID	Chip specific value	XXXX_XXXX XXXX_XXXX XXXX_XXXX XXXX_XXXX*1

***1** Any value
***2** This value is "0" for temperature sensor and "1" for E²PROM.
***3** Rewritable

9. 3 SMBus ARP transaction

All SMBus ARP transactions include a PEC byte. For the layout of these transactions refer to the SMBus specification.

Table 12 Supported SMBus ARP Transactions

Transaction	Command Code	Function
Prepare to ARP	01h	Notify all devices on the SMBus to start the SMBus ARP flow.
Reset device (general)	02h	Initialize all devices on the SMBus.
Reset device ARP (directed)	Slave Address and LSB "0"	Initialize only the specified device on the SMBus
Get UDID (general)	03h	Let all devices on the SMBus send its UDID
Get UDID (directed)	Slave Address and LSB "1"	Let only the specified device on the SMBus send its UDID
Assign address	04h	Assign new slave address to the specified UDID device on the SMBus

9. 3. 1 Prepare to ARP

The HOST uses this command to notify all devices on the SMBus to start the SMBus ARP flow.
When this IC receives a 7-bit long SMBus ARP Address and a 1-bit read / write instruction code set to "0", following a start condition, this IC generates an acknowledge.
Then, it receives an 8-bit command and generates an acknowledge. Furthermore, after receiving an 8-bit PEC byte, generating an acknowledge, and then receiving a stop condition, the notification of the start of the ARP process is completed.

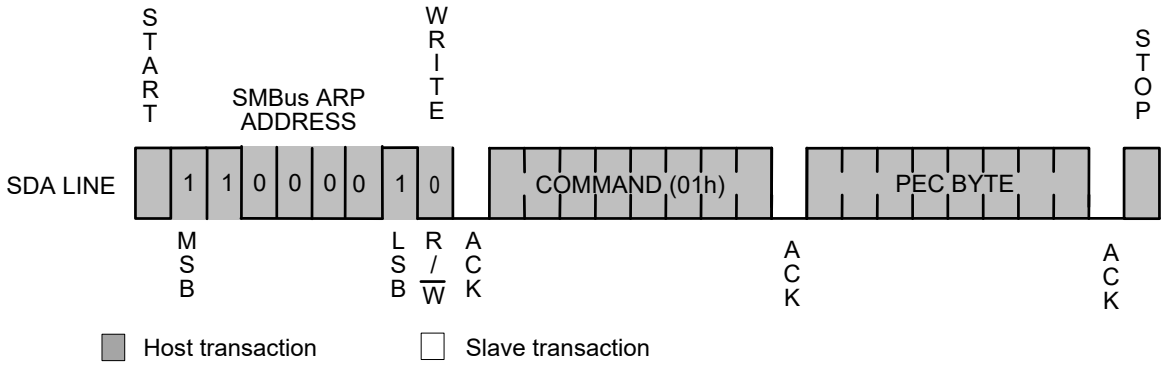


Figure 10 Prepare to ARP

9. 3. 2 Reset device (general)

The HOST uses this command to initialize all devices on the SMBus. All devices that receive this command reset their assigned slave address to the default slave address.
This command has the same format as the "Prepare to ARP" command, only the command code is different.

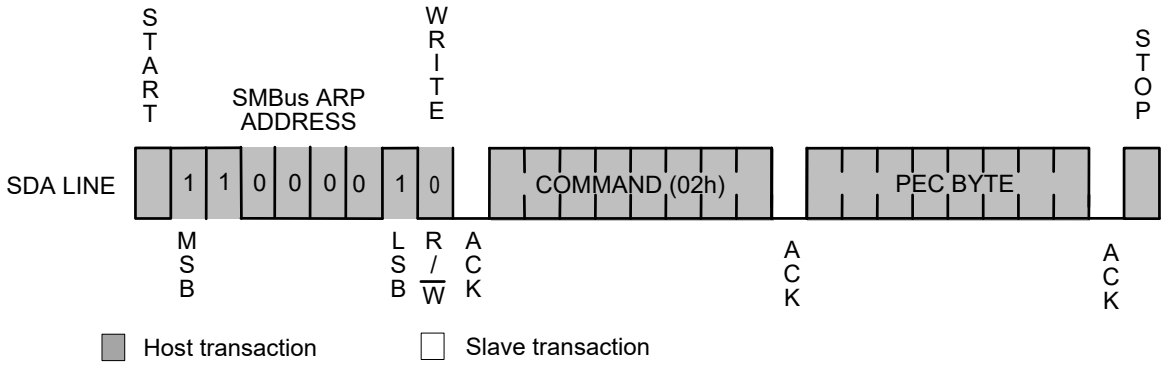


Figure 11 Reset Device (general)

9. 3. 3 Reset device ARP (directed)

The HOST uses this command to initialize only the specified device on the SMBus. The device that receives this command reset their assigned slave address to the default slave address.
This command has the same format as the "Reset Device (general)" command, only the command code is different.
The command code is 1 byte including the 7-bit long slave address of the targeted device and a LSB "0".

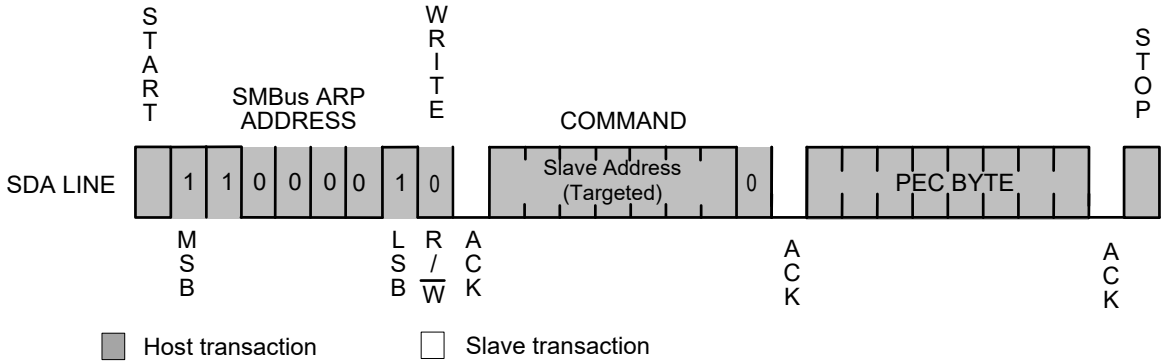


Figure 12 Reset Device ARP (directed)

9. 3. 4 Get UDID (general)

The HOST uses this command to let all devices on the SMBus send its UDID.
When this IC receives a 7-bit long SMBus ARP Address and a 1-bit read / write instruction code set to "0", following a start condition, this IC generates an acknowledge.
Then, it receives an 8-bit command and generates an acknowledge. After that, the HOST sends a new start condition.
When this IC receives a 7-bit long SMBus ARP Address and a 1-bit read / write instruction code set to "1", following a new start condition, this IC generates an acknowledge. After that, the devices send the data in the order of byte count, UDID Byte 15 to 0, the slave address and PEC byte.
Atter receiving all the data, the HOST sends a stop condition without an acknowledge, ending the Get UDID (general) command.

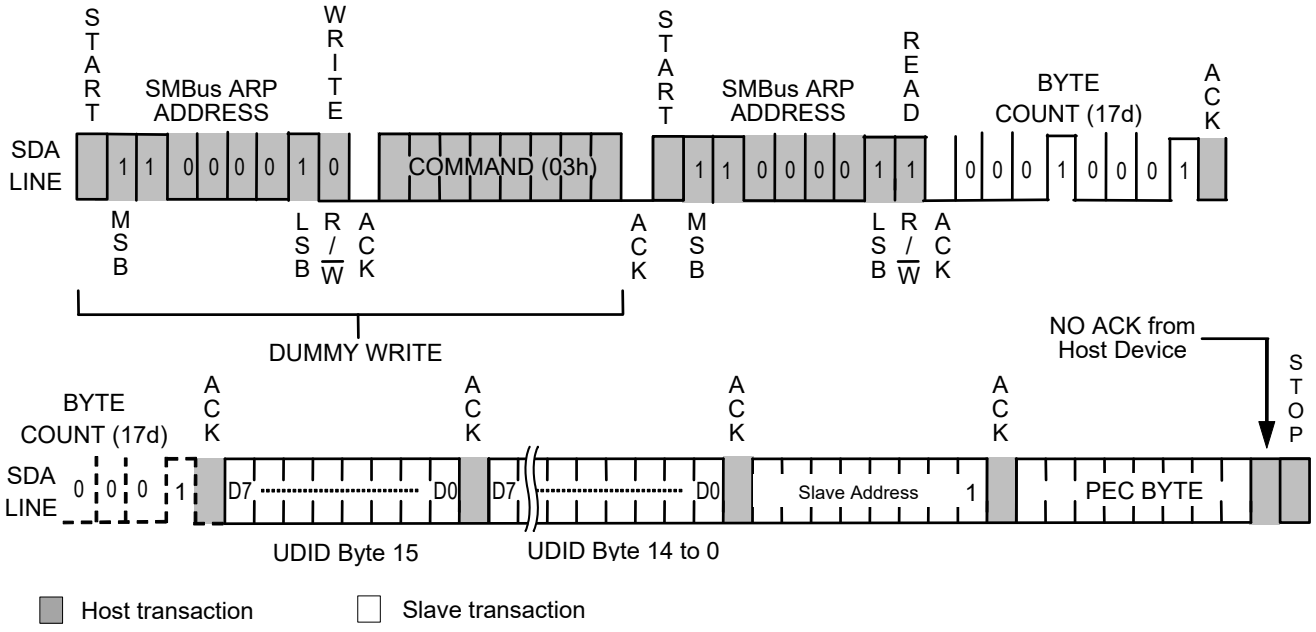


Figure 13 Get UDID (general)

9. 3 .5 Get UDID (directed)

The HOST uses this command to let only the specified device on the SMBus send its UDID.
This command has the same format as the "Get UDID (general)" command, only the command code is different.
The command code is 1 byte including the 7-bit long slave address of the targeted device and a LSB "1".

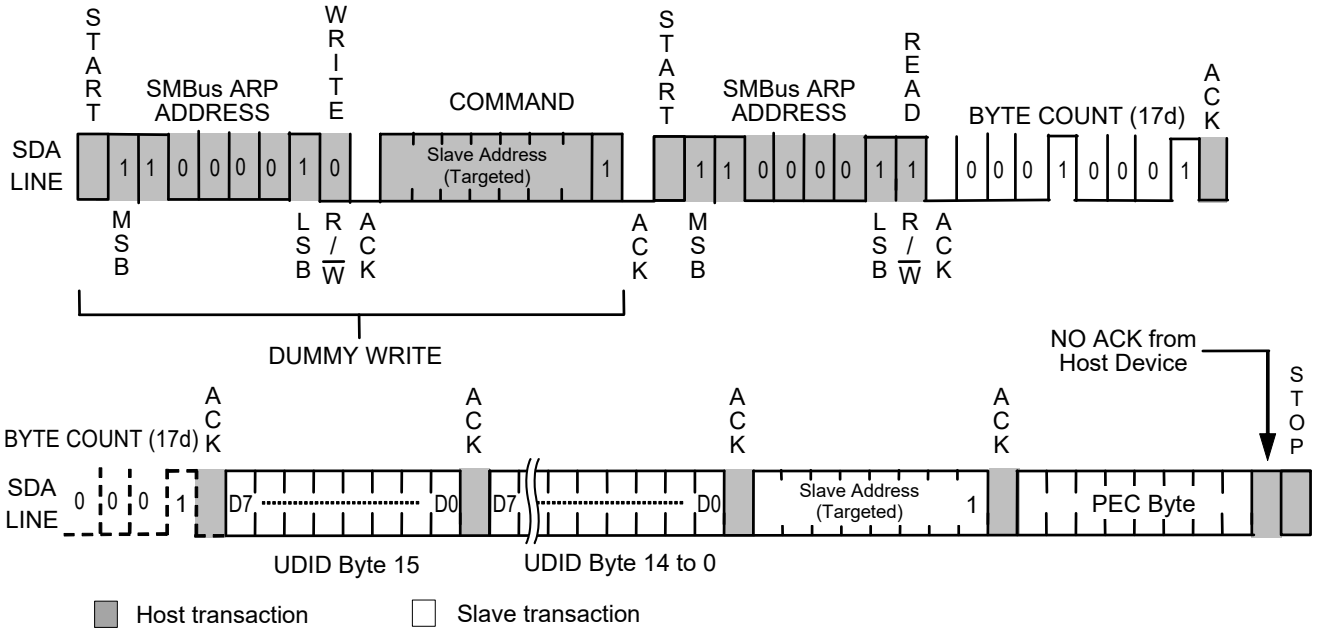
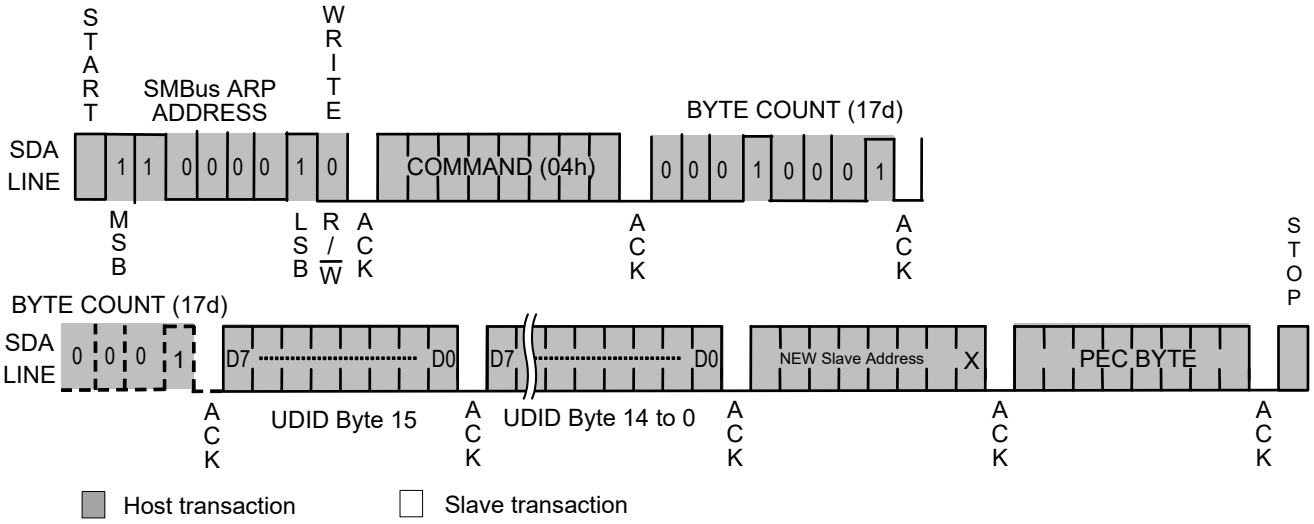


Figure 14 Get UDID (directed)

9. 3. 6 Assign address

The HOST uses this command to assign new slave address to the specified UDID device on the SMBus.
When this IC receives a 7-bit long SMBus ARP Address and a 1-bit read / write instruction code set to "0", following a start condition, this IC generates an acknowledge.
Then, it receives an 8-bit command and generates an acknowledge. Furthermore, the device receives the data in the order of byte count, targetd UDID Byte 15 to 0, new slave address and PEC byte.
Atter receiving the stop condition, The slave address rewriting operation of the specified UDID device begins.



備考 X : Don't care

Figure 15 Assign Address

■ Pin Functions

1. VDD (Power supply) pin

The VDD pin is used to apply positive supply voltage. Regarding the applied voltage value, refer to "■ **Recommended Operation Conditions**". Set a bypass capacitor of about 0.1 μF between the VDD pin and the VSS pin for stabilization as close to IC as possible.

2. SA0, SA1 and SA2 (Select address input) pins

In this IC, to set the temperature sensor and E²PROM default slave address, connect each of the SA0 pin, SA1 pin and SA2 pin to the VSS pin or the VDD pin. Therefore the users can set 8 types of slave address by a combination of the SA0 pin, SA1 pin, SA2 pin. If you assign new address in the ARP flow, the default slave address are ignored.
The SWPn, CWP, RPSn write protect commands and SPAn, RPA E²PROM page address commands don't support SMBus ARP Protocol. These address are fixed default slave address and must not be assigned to any SMBus slave device.
Comparing the slave address transmitted from the master device and one that you set, makes possible to select one slave address from other devices connected onto the bus.
Each of the SA0 pin, SA1 pin and SA2 pin has a built-in pull-down resistor. In open, the pin is set to the same status as it connected to the VSS pin.
The SA0 pin is used to detect the V_{HV} voltage, when decoding an SWPn or CWP instruction. Refer to "**Table 13 Default Slave Address**" for pin setting and slave address.

3. SDA (Serial data I/O) pin

The SDA pin is used for the bi-directional transmission of serial data. This pin is a signal input pin, and an Nch open-drain output pin.
In use, generally, connect the SDA line to any other device which has the open-drain or open-collector output with Wired-OR connection by pulling up to V_{DD} by a resistor.

4. SCL (Serial clock input) pin

The SCL pin is used for the serial clock input. Since the signals are processed at a rising or falling edge of the SCL clock, pay attention to the rising and falling time and comply with the specification.

5. $\overline{\text{EVENT}}$ (Temperature event output) pin

The $\overline{\text{EVENT}}$ pin is an open-drain output that requires a pull-up resistor to V_{DD} on the system motherboard or integrated into the master controller. $\overline{\text{EVENT}}$ pin has three operating modes, depending on the configuration register settings, and the output status is defined by the measured temperature and the temperature limit register setting. These modes are interrupt, comparator, or TCRIT only.
"**Figure 16 $\overline{\text{EVENT}}$ pin (Active "L")**" shows an example of the measured temperature versus time, with the corresponding behavior of the $\overline{\text{EVENT}}$ pin in each of these three modes.

5. 1 Interrupt mode

In interrupt mode, the $\overline{\text{EVENT}}$ pin will be asserted when the measured temperature crosses any temperature limit setting. Once the pin has been asserted, the pin will remain asserted until it is released by writing "1" to the CLEAR bit in the configuration register. After the pin is de-asserted, the pin will be re-asserted when the measured temperature crosses any temperature limit setting.

5. 2 Comparator mode

In comparator mode, the $\overline{\text{EVENT}}$ pin will be asserted when the measured temperature is above the high limit or below "the low limit – hysteresis width". The pin will clear itself when the measured temperature is below "the high limit – hysteresis width" and above the low limit.

5. 3 TCRIT only mode

In TCRIT only mode, the $\overline{\text{EVENT}}$ pin will only be asserted if the measured temperature exceeds the critical temperature. Once the pin has been asserted, it will remain asserted until the temperature drops below "the critical temperature – hysteresis width".

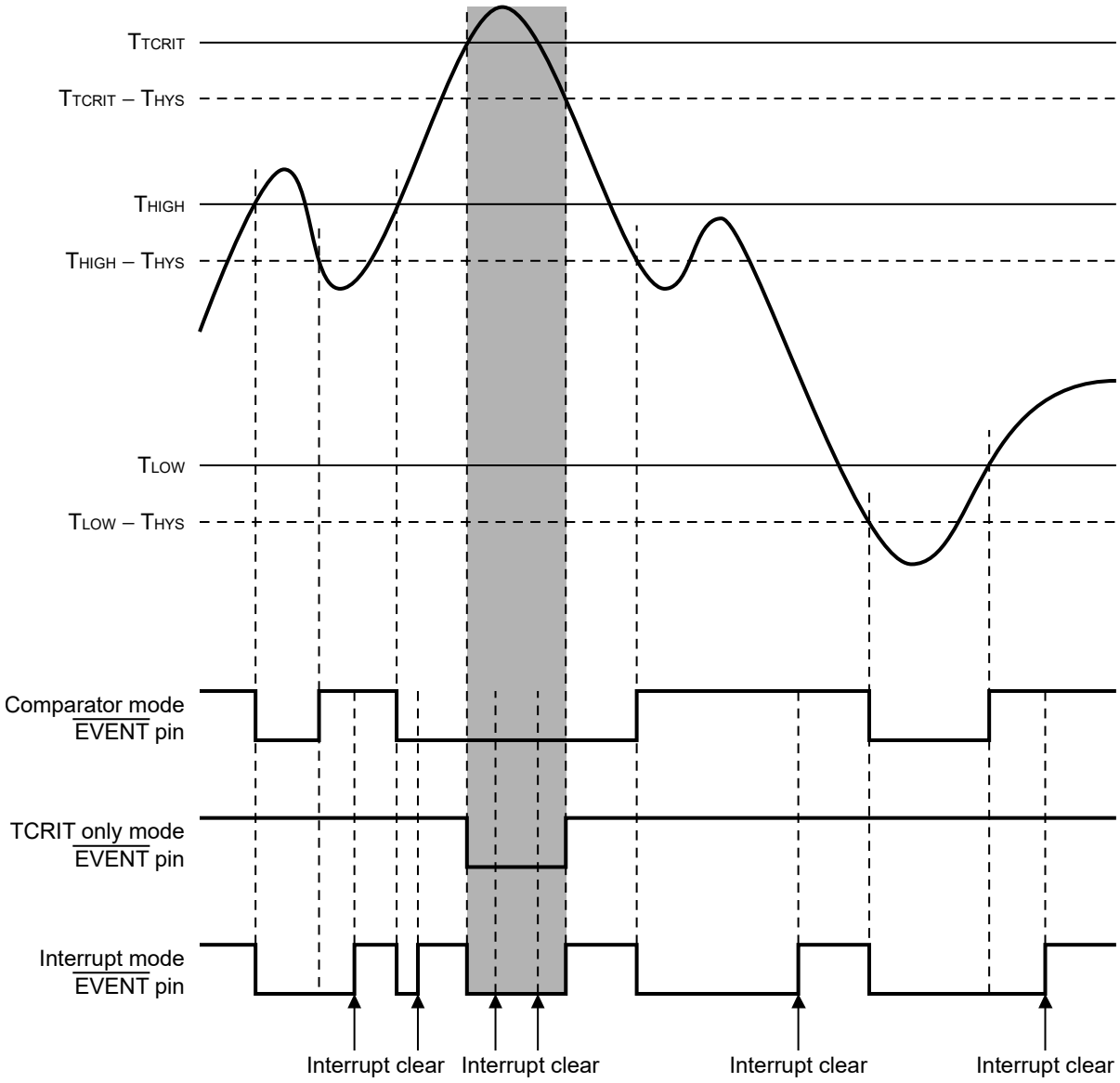


Figure 16 $\overline{\text{EVENT}}$ Pin (Active "L")

5. 4 Alert Response Address function

This IC supports the Alert Response Address (ARA) function. You can use this function when using this IC in Interrupt mode (EVENT_MODE = 1).

When the HOST senses that the $\overline{\text{EVENT}}$ pin is asserting, the HOST sends an SMBus alert command to the SDA line. If the $\overline{\text{EVENT}}$ pin is active, this IC acknowledges the SMBus alert command and responds by returning the slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates whether the current measured temperature is safe or danger. The LSB is "1" if the current measured temperature is the danger value above the high limit or below the low limit.

If multiple devices on the bus respond to the SMBus alert command, arbitration during the slave address portion of the SMBus alert command determines which device de-assert the $\overline{\text{EVENT}}$ pin. If this IC wins the arbitration, its $\overline{\text{EVENT}}$ pin de-assert at the completion of this command. If this IC loses the arbitration, its $\overline{\text{EVENT}}$ pin remains asserting. Also when the measured temperature exceeds the critical temperature, even if this IC win the arbitration, its $\overline{\text{EVENT}}$ pin remains asserting.

This function can be switched enable / disable. The method is same as the UDID Write / Read mode.

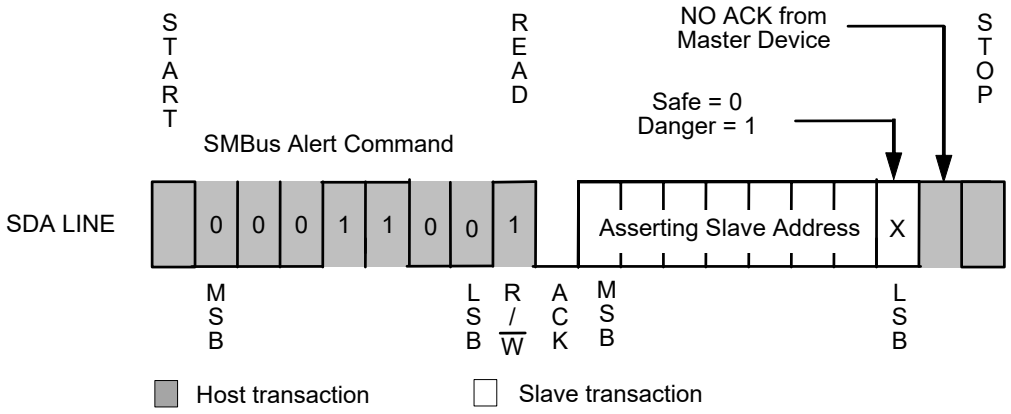


Figure 17 Alert Response Address

■ Initial Delivery State

Initial delivery state of all address E²PROM is "FFh". All write protects are cleared.

■ Operation

This IC behaves as a slave device in the I²C-bus and SMBus protocol.
This IC has unrelated two functions as 4 K-bit E²PROM with software write protection and temperature sensor measuring ambient temperature.
All operations are synchronized by the serial clock. Read and write operations are initiated by a start condition, generated by the master device. The start condition is followed by a slave address and read / write bit, and this IC generates an acknowledge bit.
When writing data to this IC, this IC generates an acknowledge bit during the 9th bit time, following the master device's 8-bit transmission. When data is read by the master device, the master device acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a master device which generates stop condition after an acknowledge for write, and after no acknowledge for read.
This IC has the timeout function. This IC shall not initiate clock stretching, which is an optional I²C-bus feature.

1. Selecting function

Operation function is identified by slave address. The E²PROM memory and the temperature sensor may be accessed using a default slave address or assigned slave address, and to perform the software write protection or the E²PROM page address operations a default slave address is required.

2. E²PROM function

This IC has a 4 K-bit E²PROM array. The E²PROM array is devided into two pages consisting of a lower 256-byte page and an upper 256-byte page, which change over by the set E²PROM page address order. Each page has two 128-byte blocks. Each block can be set to write-protected by software write protect function. Page write operation up to 16 bytes and sequential read operation are available.
All operations of the E²PROM section are inhibited to be performed during E²PROM write time.
For more detail, refer to "**■ E²PROM Operation**".

3. Temperature sensor function

This IC has a digital temperature sensor. With the nine types of temperature sensor registers, this IC can be performed to read measured ambient temperature from register and to write configration data to register. This IC can output comparison result of ambient temperature and specified limit value from $\overline{\text{EVENT}}$ pin.
Temperature sensor regularly refresh temperature register value after power-on, and can go into shutdown condition when SHDN bit is set. During shutdown condition, temperature sensor circuit is stopped and holds temperature sensor register value, reducing current consumption.
All operations of the temperature sensor section are performed anytime.
For more detail, refer to "**■ Temperature Sensor Operation**".

4. Initialization operation after power-on

By a power-on reset circuit, this IC initializes the internal circuit at the time of power-on. Perform the beginning (start condition) of the instruction transmission to this IC after the initialization by the power-on reset circuit. Regarding the datails of power-on reset, refer to "■ **Reset and Initialization**".

5. Device addressing

To start communication, the HOST device on the system generates a start condition to the slave device. Following this, the HOST device sends the slave address.
Slave devices that are assigned addresses in the ARP flow will use the assigned slave address regardless of the SA pin connection.
The SWPn, CWP, RPSn write protect commands and SPAn, RPA E²PROM page address commands don't support SMBus ARP Protocol.

Table 13 Default Slave Address

Instruction	Default Slave Address							R/$\overline{W}$	SA Pin		
	Device Type Identifier				Select Address Signal						
	B7	B6	B5	B4	B3	B2	B1	B0	SA2	SA1	SA0
Read / write E²PROM*1	1	0	1	0	SA2	SA1	SA0	R/$\overline{W}$	SA2	SA1	SA0
Set write protection, block 0 (SWP0)	0	1	1	0	0	0	1	0	–*2	–*2	V_{HV}
Set write protection, block 1 (SWP1)	0	1	1	0	1	0	0	0	–*2	–*2	V_{HV}
Set write protection, block 2 (SWP2)	0	1	1	0	1	0	1	0	–*2	–*2	V_{HV}
Set write protection, block 3 (SWP3)	0	1	1	0	0	0	0	0	–*2	–*2	V_{HV}
Clear write protection for all blocks (CWP)	0	1	1	0	0	1	1	0	–*2	–*2	V_{HV}
Read SWP0 status (RPS0)	0	1	1	0	0	0	1	1	–*2	–*2	–*2
Read SWP1 status (RPS1)	0	1	1	0	1	0	0	1	–*2	–*2	–*2
Read SWP2 status (RPS2)	0	1	1	0	1	0	1	1	–*2	–*2	–*2
Read SWP3 status (RPS3)	0	1	1	0	0	0	0	1	–*2	–*2	–*2
Set page address to 0 (SPA0)	0	1	1	0	1	1	0	0	–*2	–*2	–*2
Set page address to 1 (SPA1)	0	1	1	0	1	1	1	0	–*2	–*2	–*2
Read page address (RPA)	0	1	1	0	1	1	0	1	–*2	–*2	–*2
Read / write temperature register*1	0	0	1	1	SA2	SA1	SA0	R/$\overline{W}$	SA2	SA1	SA0

***1.** Slave addresses (SA2, SA1, SA0) are compared by the select address input pins (SA0, SA1, SA2) of a memory device with the address value which is set beforehand.
***2.** Connected to the VSS pin or VDD pin.

When using this IC with the default slave address, up to eight devices can be connected on a single Bus. Address select signals (SA2 pin, SA1 pin, SA0 pin) should be set on each device, respectively.
The SWPn, CWP, RPSn write protect commands and SPAn, RPA E²PROM page address commands affect all devices on the Bus simultaneously.

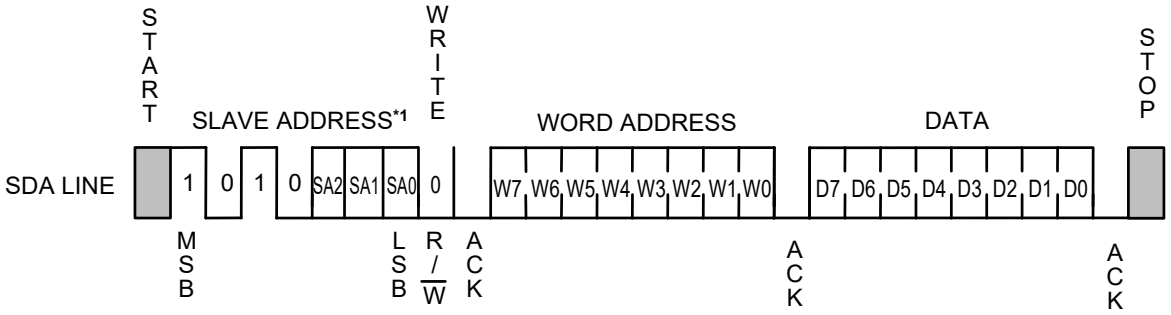
The 8th bit is the read / write bit (R/$\overline{W}$). This bit is set to "1" for read and "0" for write operations. If a match occurs on the slave address, the corresponding device gives an acknowledge on serial data (SDA) during the 9th bit time. If the device does not match the slave address, this IC goes into standby mode automatically.

■ E²PROM Operation

1. Write

1. 1 Byte write

When this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "0", following a start condition, this IC generates an acknowledge.
This IC then receives an 8-bit word address and responds with an acknowledge. After this IC receives 8-bit write data and responds with an acknowledge, it receives a stop condition and that initiates the write cycle at the designated memory address.
When the certain word address is protected by the write instruction, this IC does not generate an acknowledge after data byte coding, and write operation is not performed.
During the write operation to this IC, access to the temperature sensor section of this IC is permitted, but all operations of the E²PROM section are inhibited to be performed and the E²PROM section does not send back an acknowledge.

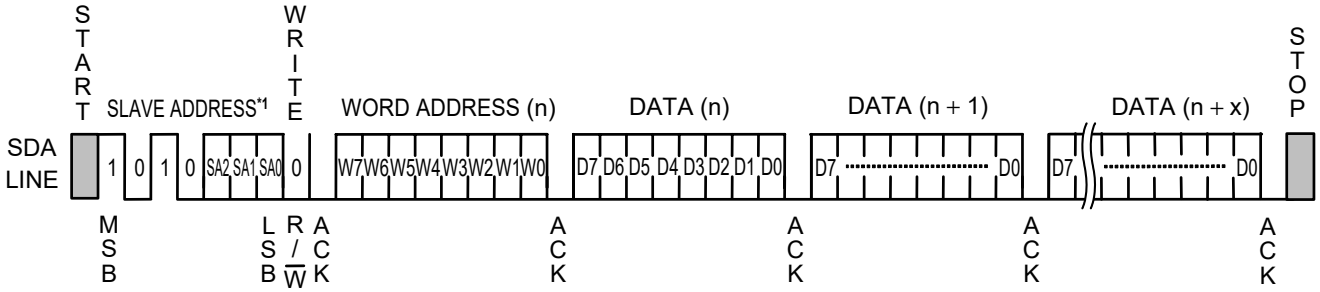


***1.** The default slave address is shown in "**Table 13 Default Slave Address**". It can also be arbitrarily assigned by the user using ARP commands.

Figure 18 Byte Write

1. 2 Page write

The page write mode allows up to 16 bytes to be written in a single write operation in this IC.
Its basic process to transmit data is as same as byte write, but it operates page write by sequentially receiving 8-bit write data as much data as the page size has.
When this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "0", following a start condition, it generates an acknowledge. Then this IC receives an 8-bit word address, and responds with an acknowledge. After this IC receives 8-bit write data and responds with an acknowledge, it receives 8-bit write data corresponding to the next word address, and generates an acknowledge. This IC repeats reception of 8-bit write data and generation of acknowledge in succession. This IC can receive as many write data as the maximum page size.
Receiving a stop condition initiates a write cycle of the area starting from the designated memory address and having the page size equal to the received write data.



***1.** The default slave address is shown in "**Table 13 Default Slave Address**". It can also be arbitrarily assigned by the user using ARP commands.

Figure 19 Page Write

The lower 4 bits of the word address are automatically incremented every time when it receives 8-bit write data. If the size of the write data exceeds 16 bytes, the higher 4 bits (W7 to W4) of the word address remain unchanged, and the lower 4 bits are rolled over and the last 16-byte data that this IC received will be overwritten.

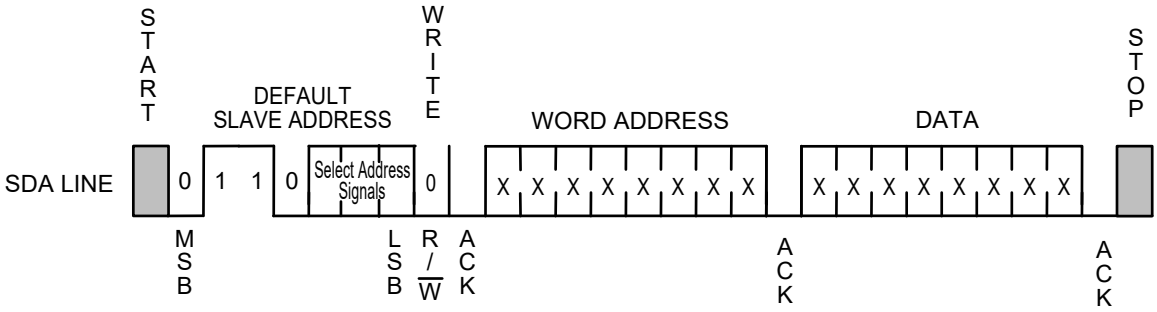
1. 3 Software write protect

This IC has set write protection for block n (SWPn), clear write protection for all blocks (CWP) and read protection status for block n (RPSn).
There are four independent memory blocks, and each block may be independently protected. The memory blocks are:

- Block 0 = word addresses 00h to 7Fh, page address = 0
- Block 1 = word addresses 80h to FFh, page address = 0
- Block 2 = word addresses 00h to 7Fh, page address = 1
- Block 3 = word addresses 80h to FFh, page address = 1

1. 3. 1 Set write protect (SWPn) and clear write protect (CWP)

If the software write protect has been set with the SWPn instruction, the block n in memory is write-protected.
The four independent blocks are protected by SWPn instructions. The write-protected block can be cleared with the CWP instruction.
The CWP instruction clears write protection for all blocks, therefore the CWP instruction can not clear write protection for each block.
The SWPn and CWP instructions have the same format as a byte write instruction, but have a different slave address. Like the byte write instruction, it is followed by an address byte and a data byte, but in this case the contents can be set in all "Don't care". In the instructions of SWPn and CWP, be sure to apply the high voltage of V_{HV} to the SA0 pin, and input "H" or "L" to the SA1 pin and SA2 pin.
The slave address for each block is shown in "**Table 13 Default Slave Address**".



Remark X: Don't care

Figure 20 Software Write Protect

1. 3. 2 Read protection status (RPSn)

The RPSn are the instructions to find the write protection status in block n. If a certain block is not protected by SWPn instruction, this IC generates an acknowledge after the device receives the default slave address of the block. If a certain block is protected by SWPn instruction, this IC does not generate an acknowledge after the device receives the default slave address of the block.

1. 3. 3 Set E²PROM page address (SPAn)

The SPAn are the instructions to select the lower 256-byte page (SPA0) or the higher 256-byte page (SPA1). The E²PROM page address selects the lower 256 bytes (SPA0) after power-on reset.

1. 3. 4 Read E²PROM page address (RPA)

The RPA are the instructions to find the current page address status. If the current page address is "0", this IC generates an acknowledge after the device receives the default slave address. If the current page address is "1", this IC does not generate an acknowledge.

Table 14 Acknowledge for Write Instruction (R/$\overline{W}$ bit = 0)

Status	Instruction	ACK Output	Word Address	ACK Output	Data	ACK Output	Write
Software Write Protect (SWPn)	SWPn in protected block	No	Don't care	No	Don't care	No	No
	SWPn in no protected block	Yes	Don't care	Yes	Don't care	Yes	Yes
	CWP	Yes	Don't care	Yes	Don't care	Yes	Yes
	Page write or byte write in protected block	Yes	Word address	Yes	Don't care	No	No
	Page write or byte write in no protected block	Yes	Word address	Yes	Data	Yes	Yes
No Software Write Protect	SWPn or CWP	Yes	Don't care	Yes	Don't care	Yes	Yes
	Page write or byte write	Yes	Word address	Yes	Data	Yes	Yes

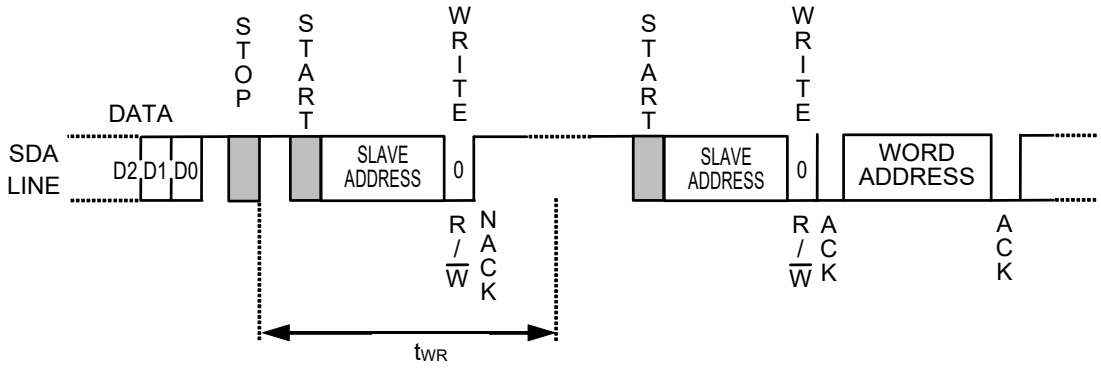
Table 15 Acknowledge for Read Instruction (R/$\overline{W}$ bit = 1)

Status	Instruction	ACK Output	Word Address	ACK Output	Data	ACK Output
Software Write Protect (SWPn)	RPSn	No	Don't care	No	Don't care	No
No Software Write Protect	RPSn	Yes	Don't care	No	Don't care	No

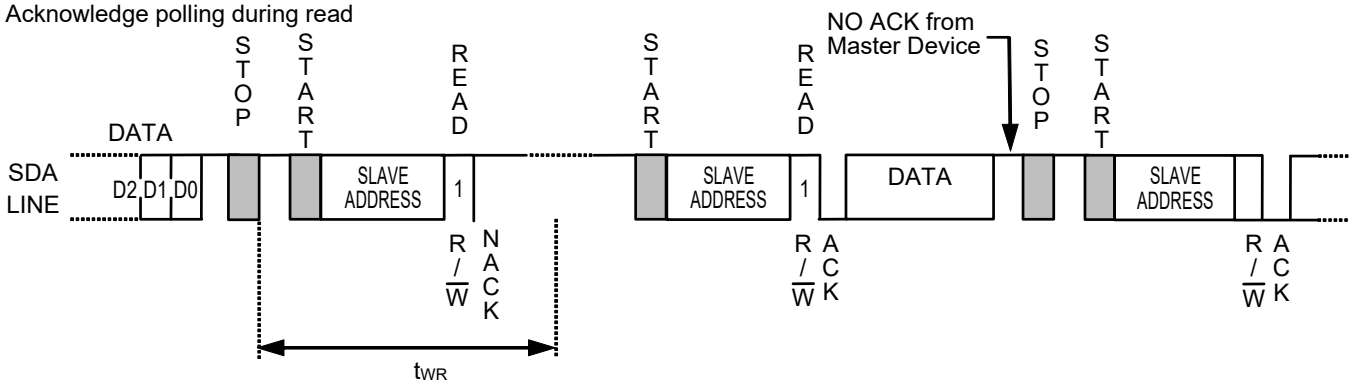
1. 4 Acknowledge polling

Acknowledge polling is used to know the completion of the write cycle in this IC.
After this IC receives a stop condition and once starts the write cycle, E²PROM operations are forbidden and no response is made to the signal transmitted by the master device.
Accordingly the master device can recognize the completion of the write cycle in this IC (slave device) by detecting a response from the slave device after transmitting the start condition, the device address and the read / write instruction code to this IC, namely to the slave devices.
That is, if this IC does not generate an acknowledge, the write cycle is in progress and if this IC generates an acknowledge, the write cycle has been completed.
It is recommended to use the read instruction "1" as the read / write instruction code transmitted by the master device.

Acknowledge polling during write



Acknowledge polling during read



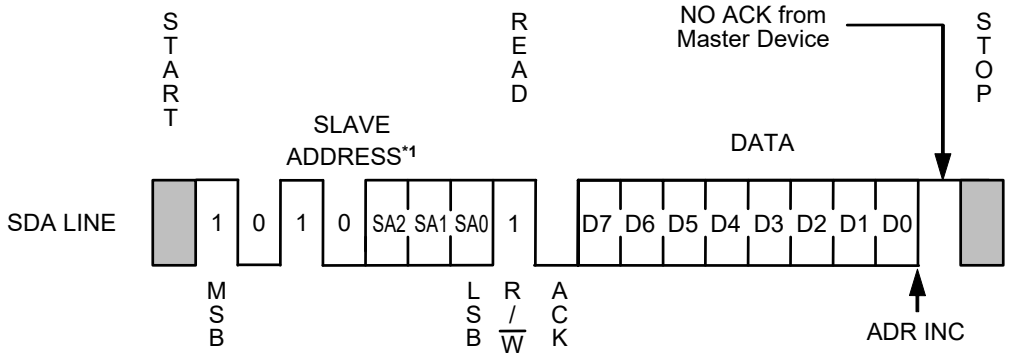
Remark Users are able to input data after acknowledge output in acknowledge polling during write.
Users are able to read data after acknowledge output in acknowledge polling during read.
However, after that users input the write instruction, a start condition may not be input during data output. Input a stop condition and the next instruction after acknowledge output and data output.

Figure 21 Usage Example of Acknowledge Polling

2. Read

2. 1 Current address read

Either in writing or in reading this IC holds the last accessed memory address. The memory address is maintained when the instruction transmission is not interrupted, and the memory address is maintained as long as the power voltage does not decrease less than the power-on reset threshold voltage (V_{PON}).
The master device can read the data at the memory address of the current address pointer without assigning the word address as a result, when it recognizes the position of the address pointer in this IC. This is called "current address read".
In the following the address counter in this IC is assumed to be "n".
When this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "1" following a start condition, it responds with an acknowledge.
Next an 8-bit data at the address "n" is sent from this IC synchronous to the SCL clock. The address counter is incremented and the content of the address counter becomes n + 1. The master device outputs stop condition not an acknowledge, the reading of this IC is ended.



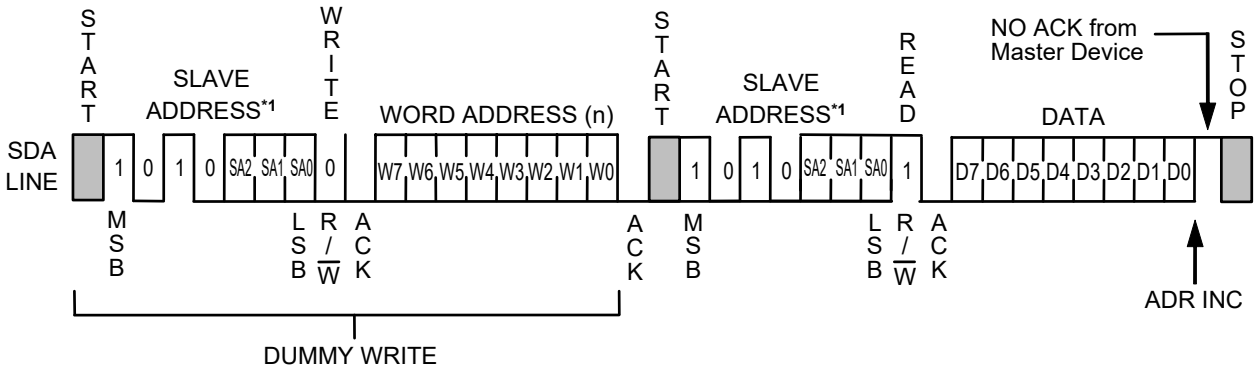
***1.** The default slave address is shown in "**Table 13 Default Slave Address**". It can also be arbitrarily assigned by the user using ARP commands.

Figure 22 Current Address Read

Attention should be paid to the following point on the recognition of the address pointer in this IC.
In read, the memory address counter in this IC is automatically incremented after output of the 8th bit of the data. In write, on the other hand, the higher bits of the memory address (the higher 4 bits of the word address) are left unchanged and are not incremented.

2. 2 Random read

Random read is used to read the data at an arbitrary memory address.
A dummy write is performed to load the memory address into the address counter.
When this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "0" following a start condition, it responds with an acknowledge.
This IC then receives an 8-bit word address and responds with an acknowledge. The memory address is loaded to the address counter in this IC by these operations. Reception of write data does not follow in a dummy write whereas reception of write data follows in byte write and in page write.
Since the memory address is loaded into the memory address counter by dummy write, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition and performing the same operation in the current address read.
That is, when this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "1", following a start condition signal, it responds with an acknowledge. Next, 8-bit data is transmitted from this IC synchronously with the SCL clock. The master device outputs stop condition not an acknowledge, the reading of this IC is ended.



***1.** The default slave address is shown in "**Table 13 Default Slave Address**". It can also be arbitrarily assigned by the user using ARP commands.

Figure 23 Random Read

2. 3 Sequential read

When this IC receives a 7-bit device address and a 1-bit read / write instruction code set to "1" following a start condition both in current address read and random read, it responds with an acknowledge.
When an 8-bit data is output from this IC synchronously with the SCL clock, the address counter is automatically incremented.
When the master device responds with an acknowledge, the data at the next memory address is transmitted. Response with an acknowledge by the master device has the memory address counter in this IC incremented and makes it possible to read data in succession. This is called sequential read.
The master device outputs stop condition not an acknowledge, the reading of this IC is ended.
Data can be read in succession in the sequential read mode. When the memory address counter reaches the last word address, it rolls over to the first word address of same page address.

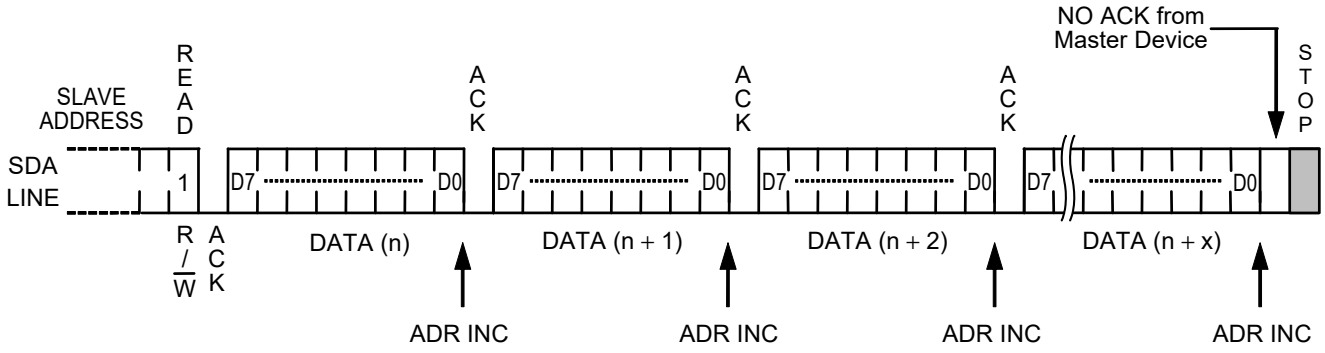


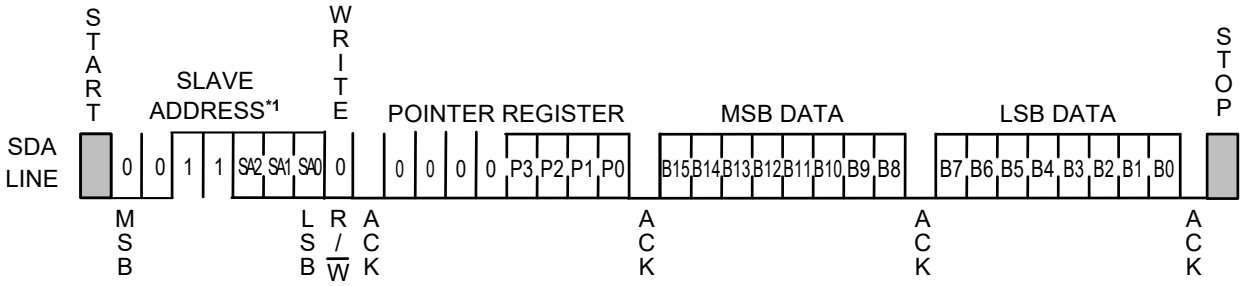
Figure 24 Sequential Read

■ Temperature Sensor Operation

Temperature sensor goes into active condition and regularly refresh ambient temperature register value by ambient temperature and the comparison value between ambient temperature and temperature limit after power-on.
The Temperature registers store the ambient temperature data, limits, and configuration values. All registers in the address space from "00h" through "08h" are 16-bit registers, accessed through block read and write commands.
Temperature sensor goes into shutdown condition by setting SHDN bit of configuration register.
Temperature sensor circuit including temperature sensor device and A/D converter circuit are stopped to control the current consumption during shutdown mode. Ambient temperature register value is held during shutdown condition.
Temperature sensor goes into active condition again by clearing SHDN bit of configuration register.

1. Temperature sensor register write operation

Writing to the temperature registers are accomplished through continuous write operations for 2-byte data. After the write operation of the slave address, the master device writes data to the pointer register, then it writes the 16-bit data every 8 bits. The 16-bit data is stored internally at the time when this IC generates an acknowledge after receiving the 16-bit data.



***1.** The default slave address is shown in "**Table 13 Default Slave Address**". It can also be arbitrarily assigned by the user using ARP commands.

Figure 25 Temperature Sensor Register Write

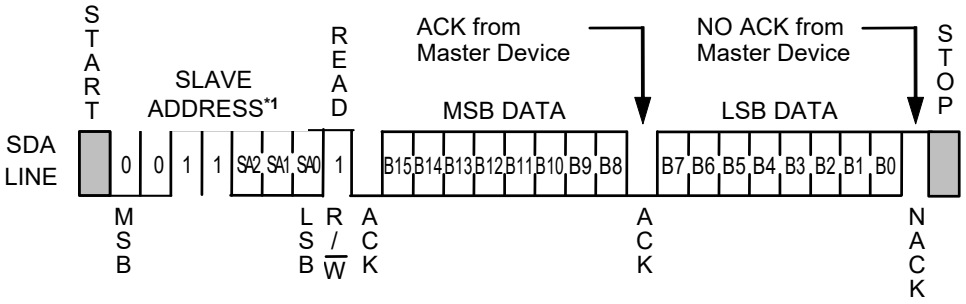
2. Temperature sensor register read operation

Reading data from temperature sensor register may be accomplished in the following ways:

(1) If the location latched in the pointer register is correct, the read sequence may consist of an operation in which R/W bit of slave address is set to "1", and a following operation in which the 2-byte data is output every 8 bits from this IC.
This way is used to read data from the ambient teperature register repeatedly.

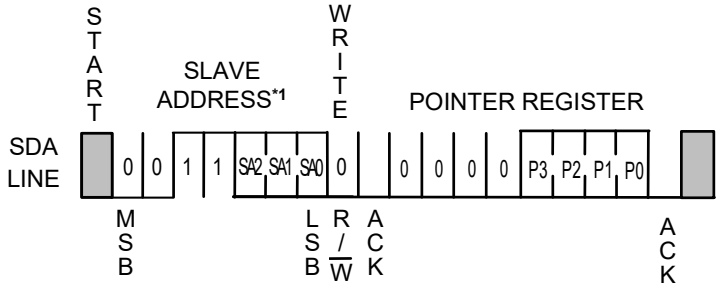
(2) The master device transfers the slave address and the R/W bit "0" and it is followed by the pointer register. The current location latched in the pointer register becomes clear by sending stop condition after this IC generates an acknowledge.
After that, reading data from the temperature sensor will be accomplished in the way of (1).

The master device is able to transfer the reading instrcution by sending start condition instead of stop condition after the pointer regiser is set in the way of (2).



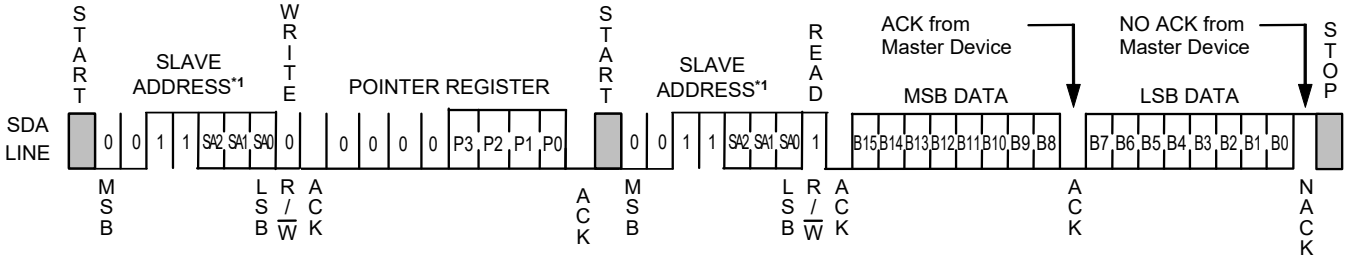
***1.** The default slave address is shown in "**Table 13 Default Slave Address**". It can also be arbitrarily assigned by the user using ARP commands.

Figure 26 Temperature Sensor Register Read



***1.** The default slave address is shown in "**Table 13 Default Slave Address**". It can also be arbitrarily assigned by the user using ARP commands.

Figure 27 Pointer Register Write



***1.** The default slave address is shown in "**Table 13 Default Slave Address**". It can also be arbitrarily assigned by the user using ARP commands.

Figure 28 Pointer Register Write and Temperature Sensor Register Read

3. Temperature sensor register

The register addresses are shown in **Table 16**.

Table 16 Pointer Register Mapping

Address	R/W	Name	Function	Default
Not applicable	W	Address pointer	Address storage for subsequent operations	Undefined
00h	R	Capabilities register	Indicates the functions and capabilities of the temperature sensor	00EFh
01h	R/W*1	Configuration register	Controls the operation of the temperature sensor	0000h
02h	R/W	HIGH limit register	Temperature high limit	0000h
03h	R/W	LOW limit register	Temperature low limit	0000h
04h	R/W	TCRIT limit register	Critical temperature	0000h
05h	R	Ambient temperature register	Current ambient temperature	Not applicable
06h	R	Manufacturer ID register	PCI-SIG manufacturer ID	1C85h
07h	R	Device ID / revision register	Device ID and revision number	2243h
08h	R/W	Resolution register	Sets temperature resolution	0001h
09h to FFh	–*2	Undefined register	Undefined	Undefined

***1.** There are read-only bits, write-only bits, and readable and writable bits in configuration register.
***2.** Behavior on accesses to invalid pointer register locations is not assured.

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	P3	P2	P1	P0
Fixed 0				Pointer register bits			

Figure 29 Pointer Register Structure

3. 1 Capabilities register

The capabilities register indicates the supported features of the temperature sensor.

B15	B14	B13	B12	B11	B10	B9	B8
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU

B7	B6	B5	B4	B3	B2	B1	B0
EVSD	TMOUT	VHV	TRES[1:0]		RANGE	ACC	EVENT

Address : 00h
R/W : Read only
Default : 00EFh

Figure 30 Capabilities Register Structure

Bit 15 to 8 : RFU
Reserved for future use. These bits are always "0".

Bit 7 : EVSD
$\overline{\text{EVENT}}$ pin operation during shutdown mode.
"1": $\overline{\text{EVENT}}$ pin output de-asserts during shutdown.

Bit 6 : TMOUT
Bus timeout period access during normal operation.
"1": $t_{TIMEOUT}$ is supported within the range of 25 ms to 35 ms.

Bit 5 : VHV
Support SA0 high level input voltage (V_{HV}) for SA0 pin.
"1": A voltage up to 10 V is supported on the SA0 pin.

Bit 4 to 3 : TRES[1:0]
Indicates the temperature resolution. Temperature resolution is set on the resolution register. Refer to "**3. 7 Resolution Register**" for resolution register.
"00": 9-bit temperature resolution (0.5°C resolution)
"01" (default): 10-bit temperature resolution (0.25°C resolution)
"10": 11-bit temperature resolution (0.125°C resolution)
"11": 12-bit temperature resolution (0.0625°C resolution)

Bit 2 : RANGE
Indicates the supported temperature range.
"1": Lower than 0°C can be read and the sign bit will be set appropriately.

Bit 1 : ACC
Indicates the supported temperature accuracy.
"1": ±1.5°C max. (–40°C to +125°C)

Bit 0 : EVENT
Indicates whether interrupt mode is supported.
"1": Interrupt mode is supported.

3. 2 Configuration register

The configuration register holds the status bits and setting data of the $\overline{\text{EVENT}}$ pin, as well as temperature hysteresis width setting data.

B15	B14	B13	B12	B11	B10	B9	B8
RFU	RFU	RFU	RFU	RFU	HYST[1:0]		SHDN

B7	B6	B5	B4	B3	B2	B1	B0
TCRIT_LOCK	EVENT_LOCK	CLEAR	EVENT_STS	EVENT_CTRL	TCRIT_ONLY	EVENT_POL	EVENT_MODE

Address : 01h
R/W : Readable and Writable
Default : 0000h

Figure 31 Configuration Register Structure

Bit 15 to 11 : RFU
Reserved for future use. These bits are always "0".

Bit 10 to 9: HYST[1:0]
Control the hysteresis width shown in **Table 17**. This hysteresis width applies to temperature high limit, temperature low limit and critical temperature. Once the ambient temperature is above a given threshold, it must drop below the threshold minus the hysteresis width in order to be flagged as an interrupt event.
Note that hysteresis width is also applied to the $\overline{\text{EVENT}}$ pin functionality. When either of the lock bits is set, these bits HYST[1:0] cannot be altered.

Table 17 Hysteresis Width Setting

HYST1	HYST0	Hysteresis Width
0	0	No hysteresis
0	1	1.5°C
1	0	3.0°C
1	1	6.0°C

Bit 8 : SHDN
Shutdown setting. The temperature sensing device and A/D converter are disabled to save power, no events will be generated. When either of the lock bits is set, this bit cannot be set until unlocked. However it can be cleared at any time.
"0" (default): The temperature sensor is active and converting.
"1": The temperature sensor is disabled and will not generate interrupts or update the temperature data.

Bit 7 : TCRIT_LOCK
Locks the TCRIT limit register from being updated.
"0" (default): The TCRIT limit register can be updated normally.
"1": The TCRIT limit register is locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power-on reset.

Bit 6 : EVENT_LOCK
Locks the HIGH and LOW limit registers from being updated.
"0" (default): The HIGH and LOW limit registers can be updated normally.
"1": The HIGH and LOW limit registers are locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power-on reset.

Bit 5 : CLEAR

Clears the $\overline{\text{EVENT}}$ pin when it has been asserted. This bit is write-only and will always be read "0".

"0": Nothing happens.

"1": In interrupt mode, the $\overline{\text{EVENT}}$ pin is reset and will not be asserted until a new interrupt condition occurs. This bit is ignored if the device is operating in comparator mode and when detecting the critical temperature. This bit is self clearing. The read value is fixed to "0".

Bit 4 : EVENT_STS

Indicates if the $\overline{\text{EVENT}}$ pin is asserted. This bit is read only.

"0" (default): The $\overline{\text{EVENT}}$ pin is not being asserted.

"1": The $\overline{\text{EVENT}}$ pin is being asserted.

Bit 3 : EVENT_CTRL

Controls the asserted state of the $\overline{\text{EVENT}}$ pin. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

"0" (default): The $\overline{\text{EVENT}}$ pin can not be asserted.

"1": The $\overline{\text{EVENT}}$ pin can be asserted.

Bit 2 : TCRIT_ONLY

Controls whether the $\overline{\text{EVENT}}$ pin will be asserted from a high / low out-of-limit condition. When the EVENT_LOCK bit is set, this bit cannot be altered.

"0" (default): The $\overline{\text{EVENT}}$ pin will be asserted if the measured temperature is above the temperature high limit or below the temperature low limit in addition to if the temperature is above the critical temperature.

"1": The $\overline{\text{EVENT}}$ pin will only be asserted if the measured temperature is above the critical temperature.

Bit 1 : EVENT_POL

Controls the active "H" state of the $\overline{\text{EVENT}}$ pin. The $\overline{\text{EVENT}}$ pin is driven to this state when it is asserted. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

"0" (default): The $\overline{\text{EVENT}}$ pin is active "L". The active "L" state of the pin will be logical "0".

"1": The $\overline{\text{EVENT}}$ pin is active "H". The active "H" state of the pin will be logical "1".

Bit 0 : EVENT_MODE

Controls the behavior of the $\overline{\text{EVENT}}$ pin. The $\overline{\text{EVENT}}$ pin may function in either comparator or interrupt mode. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

"0" (default): The $\overline{\text{EVENT}}$ pin will function in comparator mode.

"1": The $\overline{\text{EVENT}}$ pin will function in interrupt mode.

3. 3 Temperature limit register (HIGH limit / LOW limit / TCRIT limit)

Temperature in the HIGH limit register, LOW limit register and TCRIT limit register are set and described in 2's complement format of Sign bit + 10-bit.
Examples of temperature limit register are shown in "**Table 17 Hysteresis Width Setting**".

B15	B14	B13	B12	B11	B10	B9	B8
–	–	–	Sign	2^7°C	2^6°C	2^5°C	2^4°C

B7	B6	B5	B4	B3	B2	B1	B0
2^3°C	2^2°C	2^1°C	2^0°C	2^{-1}°C	2^{-2}°C	–	–

HIGH limit register
Address : 02h
R/W : Readable and writable
Default : 0000h
LOW limit register
Address : 03h
R/W : Readable and writable
Default : 0000h
TCRIT limit register
Address : 04h
R/W : Readable and writable
Default : 0000h

Figure 32 Temperature Limit Register Structure

3. 4 Ambient temperature register

3 status bits of TCRIT, HIGH and LOW and ambient temperature data described in 2's complement format of Sign bit + 12-bit can be read.
Examples of ambient temperature register are shown in "**Table 18 Examples of Temperature**".

B15	B14	B13	B12	B11	B10	B9	B8
TCRIT	HIGH	LOW	Sign	2^7°C	2^6°C	2^5°C	2^4°C

B7	B6	B5	B4	B3	B2	B1	B0
2^3°C	2^2°C	2^1°C	2^0°C	2^{-1}°C	2^{-2}°C*1	2^{-3}°C*1	2^{-4}°C*1

Address : 05h
R/W : Read-only
Default : Not applicable (0000h)

***1**. The bits may not be used according to the resolution defined based on value of TRES[1:0] bit of the capabilities register. Unused / unsupported bits will read as 0.

Figure 33 Ambient Temperature Register Structure

Bit 15 : TCRIT
When set, the ambient temperature is above the critical temperature. This bit will remain set so long as the ambient temperature is above the critical temperature and will automatically clear once the ambient temperature has dropped below the limit minus the hysteresis width.

Bit 14 : HIGH
When set, the ambient temperature is above the high limit. This bit will remain set so long as the ambient temperature is above the high limit. Once set, it will only be cleared when the ambient temperature drops below or equal to the high limit minus the hysteresis width.

Bit 13 : LOW
When set, the ambient temperature is below the low limit. This bit will remain set so long as the ambient temperature is below the low limit minus the hysteresis. Once set, it will only be cleared when the ambient temperature meets or exceeds the low limit.

Bit 12 to 0 : TAMB
Ambient temperature data in 2's complement format of Sign bit + 12-bit.

Table 18 Examples of Temperature

B15 to B0 (binary)	Value	Unit
xxx0 0111 1101 00xx	+125.00	°C
xxx0 0101 0101 00xx	+85.00	°C
xxx0 0001 1001 00xx	+25.00	°C
xxx0 0000 0010 11xx	+2.75	°C
xxx0 0000 0001 00xx	+1.00	°C
xxx0 0000 0000 01xx	+0.25	°C
xxx0 0000 0000 00xx	+0.00	°C
xxx1 1111 1111 11xx	−0.25	°C
xxx1 1111 1111 00xx	−1.00	°C
xxx1 1111 1101 01xx	−2.75	°C
xxx1 1110 1100 00xx	−20.00	°C

3. 5 Manufacturer ID register

PCI-SIG ID number of ABLIC Inc. can be read.

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	1	1	1	0	0

B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	0	0	1	0	1

Address : 06h
R/W : Read-only
Default : 1C85h

Figure 34 Manufacturer ID Register Structure

3. 6 Device ID / revision register

Device ID and revision number of product can be read.

B15	B14	B13	B12	B11	B10	B9	B8
0	0	1	0	0	0	1	0

B7	B6	B5	B4	B3	B2	B1	B0
0	1	0	0	0	0	1	1

Address : 07h
R/W : Read-only
Default : 2243h

Figure 35 Device ID / Revision Register Structure

3. 7 Resolution register

Resolution register defines temperature sensor resolution.

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	0	0	0	0	0

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	RES[1:0]	

Address : 08h
R/W : Readable and writable
Default : 0001h

Figure 36 Resolution Register Structure

Bit 15 to 2 : –
Unimplemented bit. These bits are always "0".

Bit 1 to 0 : RES[1:0]
These bits define resolution.
The resolution here is reflected by TRES[1:0] value of capabilities register.
"00": LSB = 0.5°C ($t_{CONV} \leq 35$ ms max.)
"01" (default): LSB = 0.25°C ($t_{CONV} \leq 70$ ms max.)
"10": LSB = 0.125°C ($t_{CONV} \leq 125$ ms max.)
"11": LSB = 0.0625°C($t_{CONV} \leq 125$ ms max.)

■ Reset and Initialization

This IC has a power-on reset circuit which prevents malfunction, cancels write at power-on.
At power-on status, the master device should not transfer the data from the time that the power supply voltage reaches V_{DD} min. to t_{INIT}. And at power-off, all registers are reset when the power supply voltage drops below V_{POFF}. Therefore if the power supply voltage remains below V_{POFF} for t_{POFF}, all operations of this IC are reset.
Operating this IC will be required to apply the stable power supply voltage (V_{DD}). The power supply voltage must remain stable until the end of the transmission of the data and, for a write instruction and temperature conversion time.

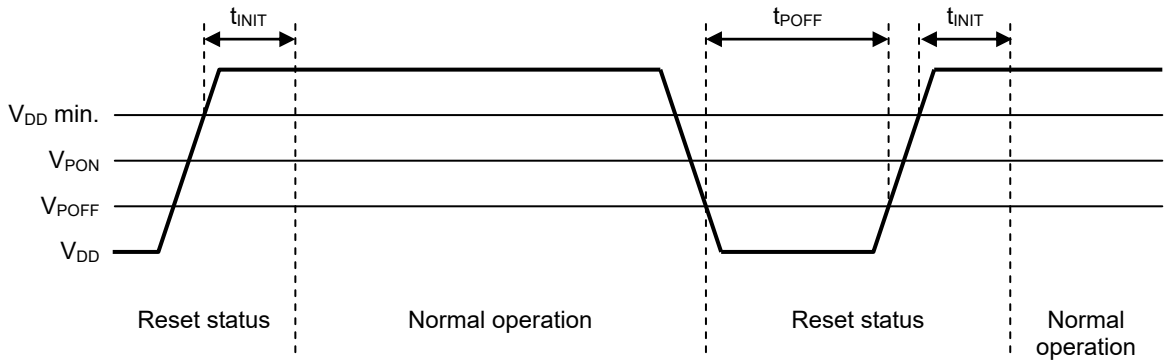


Figure 37 Operation when Power Supply Voltage Drops and Power-on

■ Usage

1. A pull-up resistor to SDA I/O pin and SCL input pin

In consideration of I²C-bus / SMBus protocol function, the SDA I/O pin and SCL input pin should be connected with a pull-up resistor. This IC cannot transmit normally without using a pull-up resistor.

In case that the SCL input pin of this IC is connected to the Nch open-drain output pin of the master device, connect the SCL pin with a pull-up resistor. As well, in case the SCL input pin of this IC is connected to the tri-state output pin of the master device, connect the SCL pin with a pull-up resistor in order not to set it in "High-Z". This prevents this IC from error caused by an uncertain output (High-Z) from the tri-state pin when resetting the master device during the voltage drop.
Pull-up resistor of the $\overline{\text{EVENT}}$ pin is also required to transmit $\overline{\text{EVENT}}$ behavior.

2. Equivalent circuits of input pin and I/O pin

The SCL pin and the SDA pin of this IC do not have a built-in pull-down or pull-up resistor. Each of the SA0 pin, SA1 pin and SA2 pin has a built-in pull-down resistor. The SDA pin is an open-drain output. The followings are equivalent circuits of the pins.

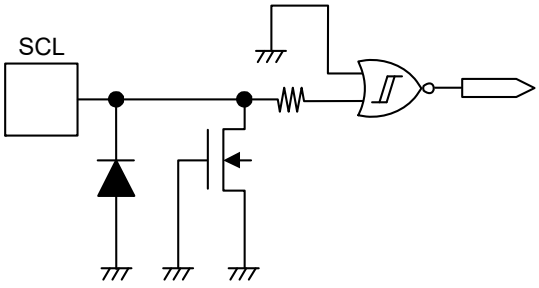


Figure 38 SCL Pin

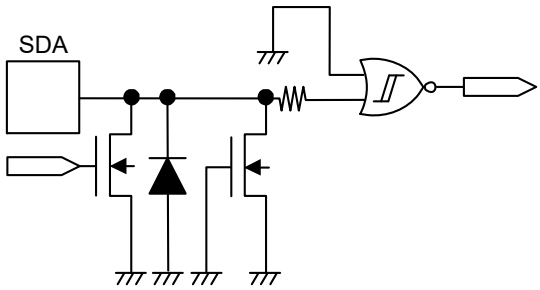


Figure 39 SDA Pin

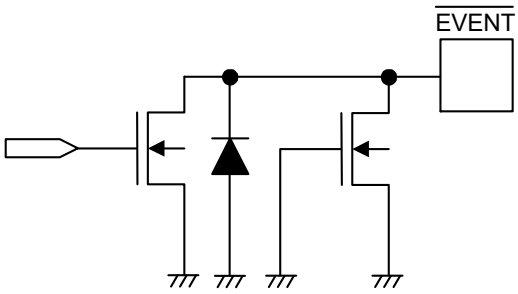


Figure 40 $\overline{\text{EVENT}}$ Pin

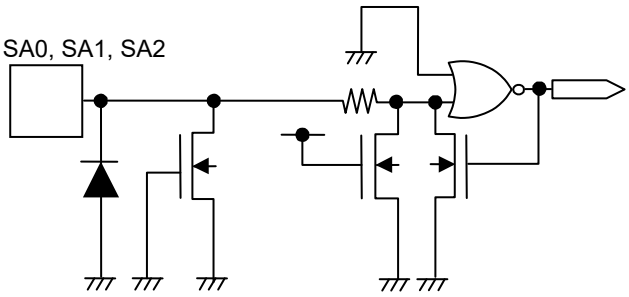


Figure 41 SA0, SA1, SA2 Pin

3. Acknowledge check

The I²C-bus / SMBus protocol include an acknowledge check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the master device and this IC. This function is effective to prevent malfunction, so it is recommended to perform an acknowledge check with the master device.

4. SDA pin and SCL pin noise suppression time

This IC includes a built-in low-pass filter at the SDA pin and the SCL pin to suppress noise. If the power supply voltage is 1.7 V, noise with a pulse width of 90 ns or less can be suppressed.
For details of the assurable value, refer to noise suppression time (t_I) in **Table 8** in "■ **AC Electrical Characteristics**".

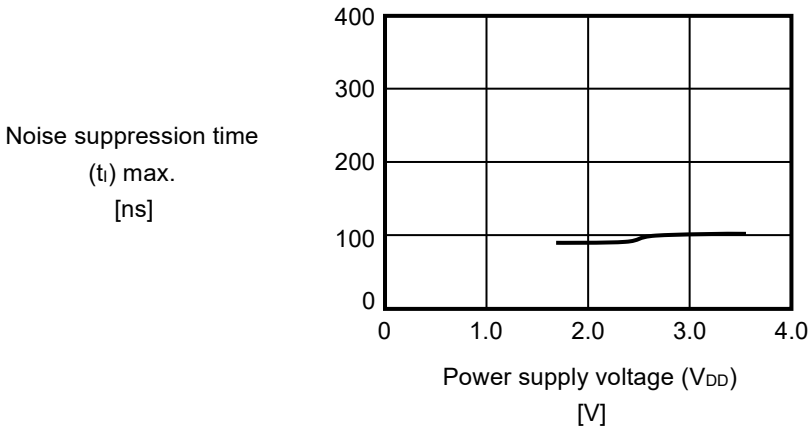
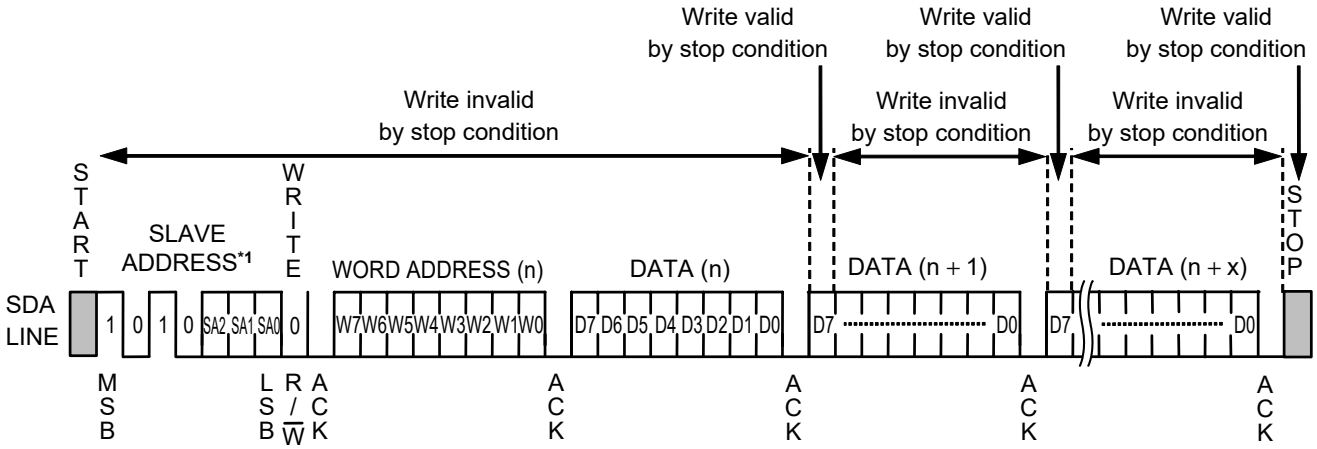


Figure 42 Noise Suppression Time for SDA Pin and SCL Pin

5. Operation when inputting stop condition during write

This IC does the E²PROM write operation only when it receives data of 1 byte or more and receives a stop condition immediately after an acknowledge output.
Refer to **Figure 43** for details.



***1.** The default slave address is shown in "**Table 13 Default Slave Address**". It can also be arbitrarily assigned by the user using ARP commands.

Figure 43 Write Operation by Inputting Stop Condition during Write

6. Command cancel by start condition

By a start condition, users are able to cancel command which is being input. However, users are not able to input a start condition when this IC is outputting "L". When users cancel the command, there may be a case that the address will not be identified. Use random read for the read operation, not current address read.

7. UDID Write / Read mode

This IC has a dedicated mode for rewriting the UDID. It is possible to rewrite the UDID by sending the special command from the tester.

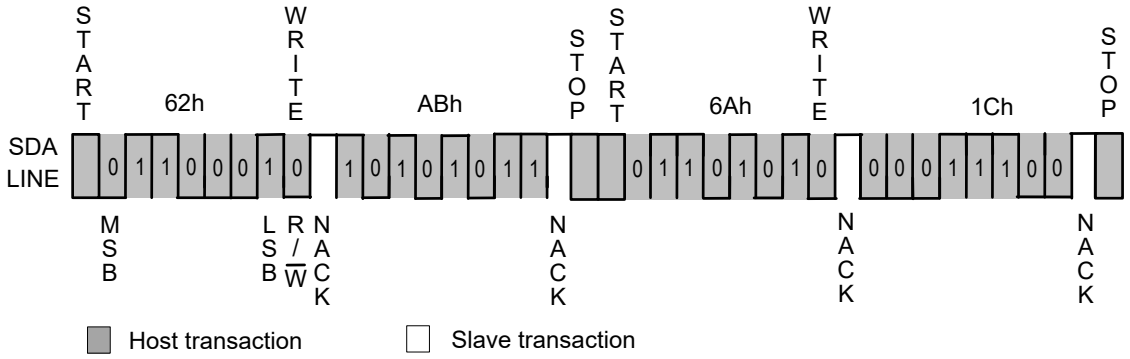


Figure 44 UDID Write / Read mode In

The tester sends a 7-bit long data "0110_001" and a 1-bit read / write instruction code set to "0". This IC received it doesn't generate an acknowledge. In addition, the tester sends a 8-bit long data "1010_1011". This IC received it doesn't generate an acknowledge and the tester sends stop condition.
Then, the tester sends a 7-bit long data "0110_101" and a 1-bit read / write instruction code set to "0". This IC received it doesn't generate an acknowledge. In addtion, the tester sends a 8-bit long data "0001_1100". This IC received it doesn't generate an acknowledge.
After receiving the stop condition, this IC enter into UDID Write / Read mode.

After entering into UDID Write / Read mode, for rewriting the UDID, the tester used E²PROM Write / Read command, only the slave address is different. The readable and writable area is limited to the Subsystem Vendor ID, the Subsystem Device ID, the ARP enable / disable setting byte and the ARA enable / disable setting byte. The UDID except the Subsystem Vendor ID and the Subsystem Device ID is read-only. When the power is turned on again, the written UDID is reflected. At the same time, this IC also exits from the UDID Write / Read mode.

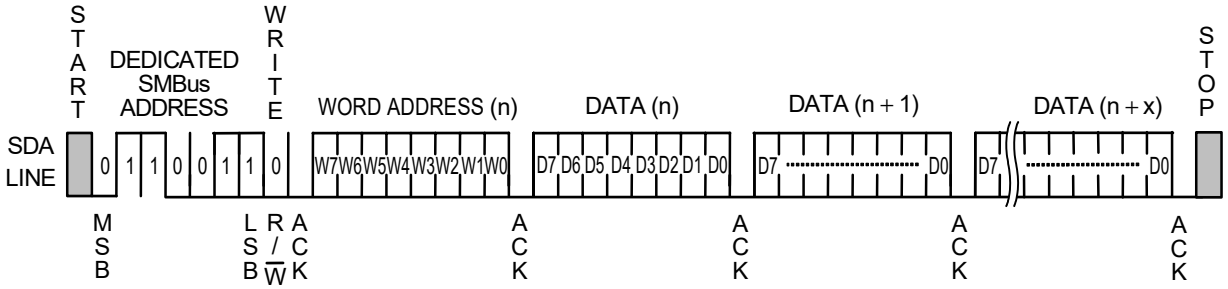
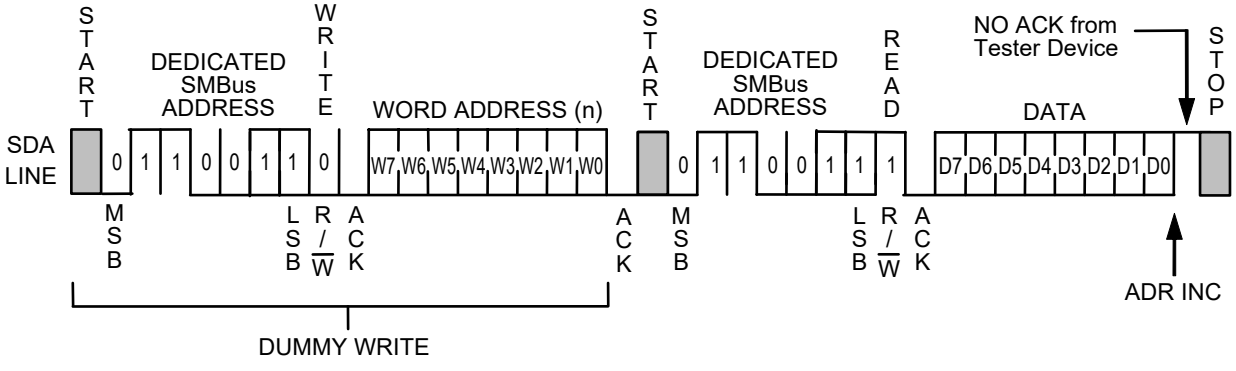


Figure 45 Write UDID



Remark Sequential Read is also possible

Figure 46 Read UDID

Table 19 Readable and Writable Area

Name	Pointer	R/W
ARA function Enable / Disable*1	xx01 1111	Readable and writable
Device Capabilities	xx00 0000	Read-only
Version/Revision	xx00 0001	Read-only
Vendor ID	xx00 0010	Read-only
	xx00 0011	Read-only
Device ID	xx00 0100	Read-only
	xx00 0101	Read-only
Interface	xx00 0110	Read-only
	xx00 0111	Read-only
Subsystem Vendor ID	xx00 1000	Readable and writable
	xx00 1001	Readable and writable
Subsystem Device ID	xx00 1010	Readable and writable
	xx00 1011	Readable and writable
Vendor specific ID	xx00 1100	Read-only
	xx00 1101	Read-only
	xx00 1110	Read-only
	xx00 1111	Read-only
ARP function Enable / Disable*2	xx11 0000	Readable and writable

***1.** Only one of the following values can be written as the value of ARA function Enable / Disable.
FEh : ARA Enable
00h : ARA Disable

***2.** Only one of the following values can be written as the value of ARP function Enable / Disable.
FFh : EE ARP Enable / TS ARP Enable
AAh : EE ARP Enable / TS ARP Disable
55h : EE ARP Disable / TS ARP Enable
00h : EE ARP Disable / TS ARP Disable

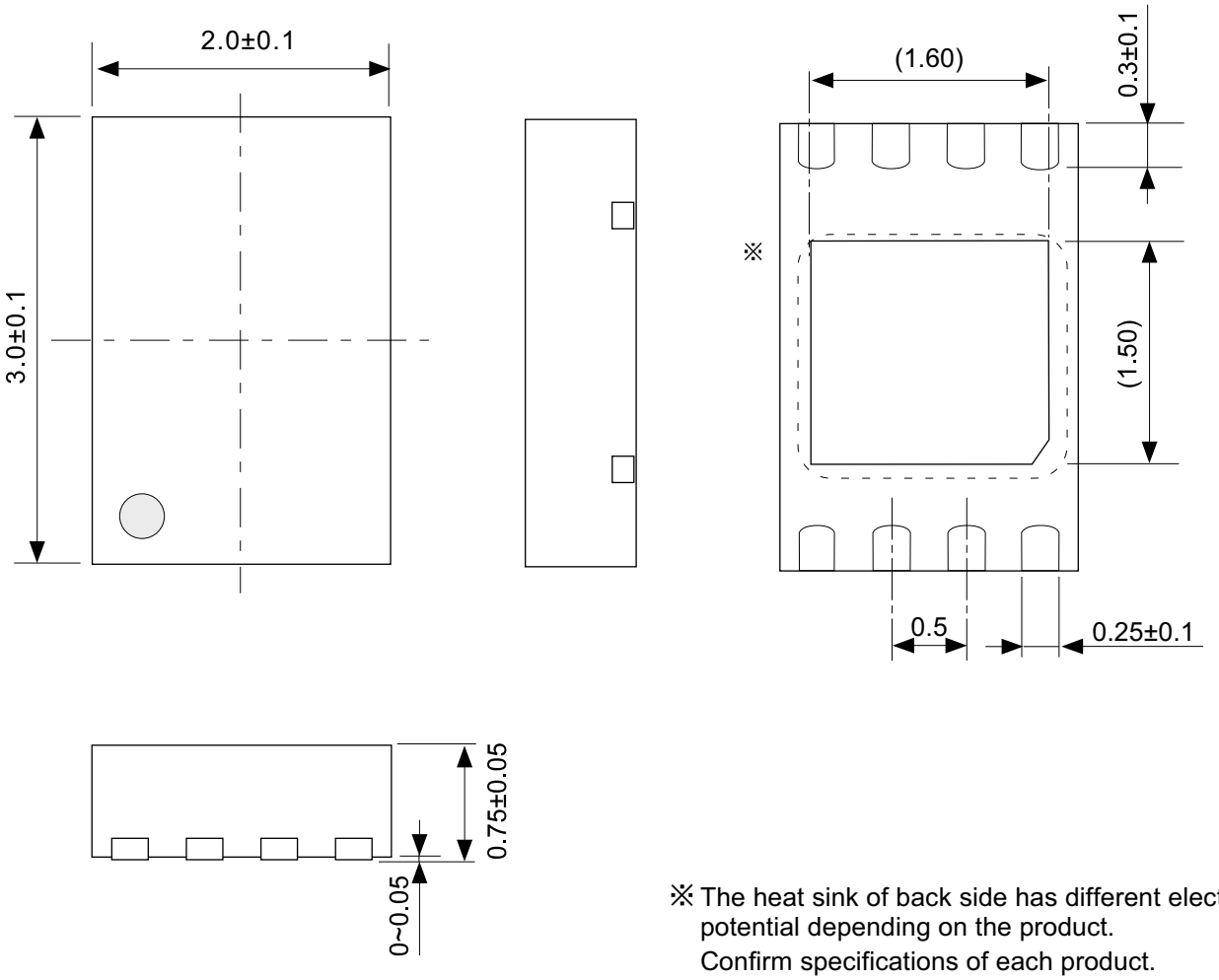
■ Precautions

- Do not operate these ICs in excess of the absolute maximum ratings. Attention should be paid to the power supply voltage, especially. The surge voltage which exceeds the absolute maximum ratings can cause latch-up and malfunction. Perform operations after confirming the detailed operation condition in the data sheet.

- Operations with moisture on this IC's pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking this IC up from low temperature tank during the evaluation. Be sure that not remain frost on this IC's pin to prevent malfunction by short-circuit.
  Also attention should be paid in using on environment, which is easy to dew for the same reason.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

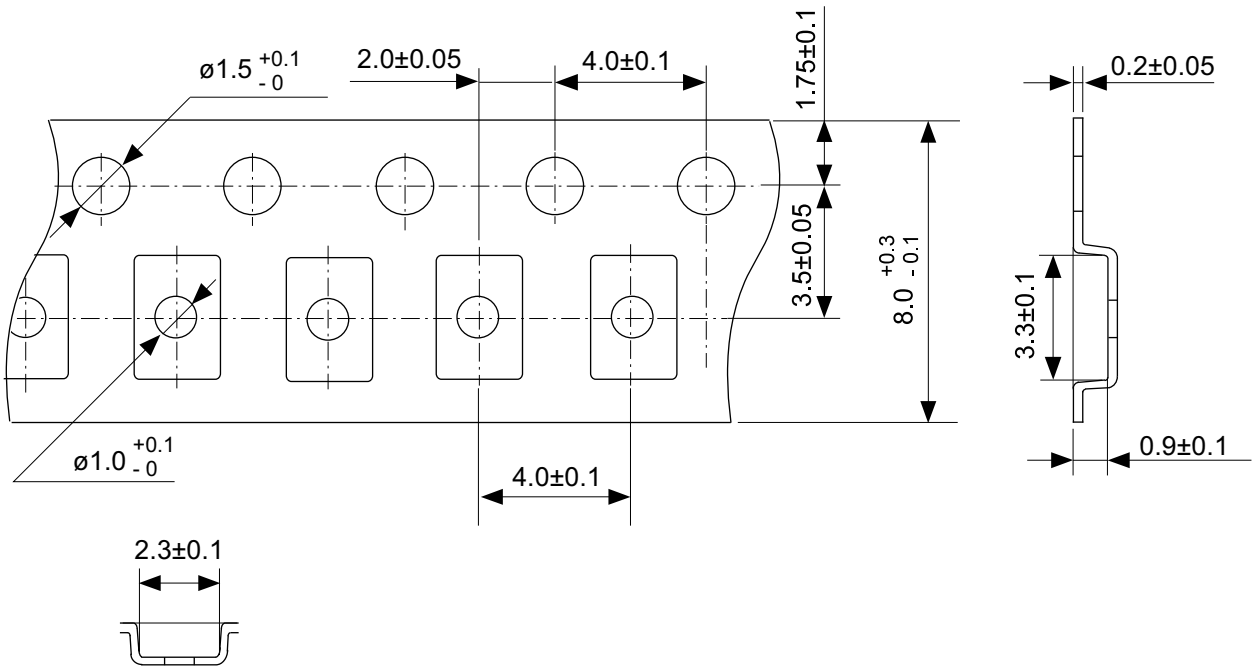
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

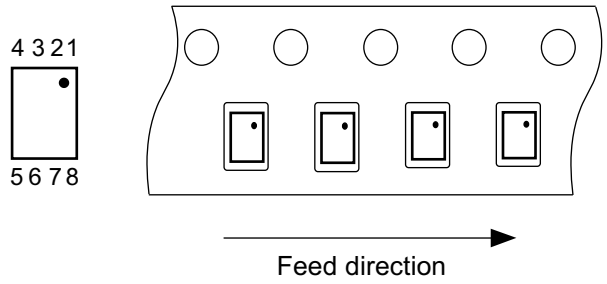


※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

No. PQ008-B-P-SD-1.0

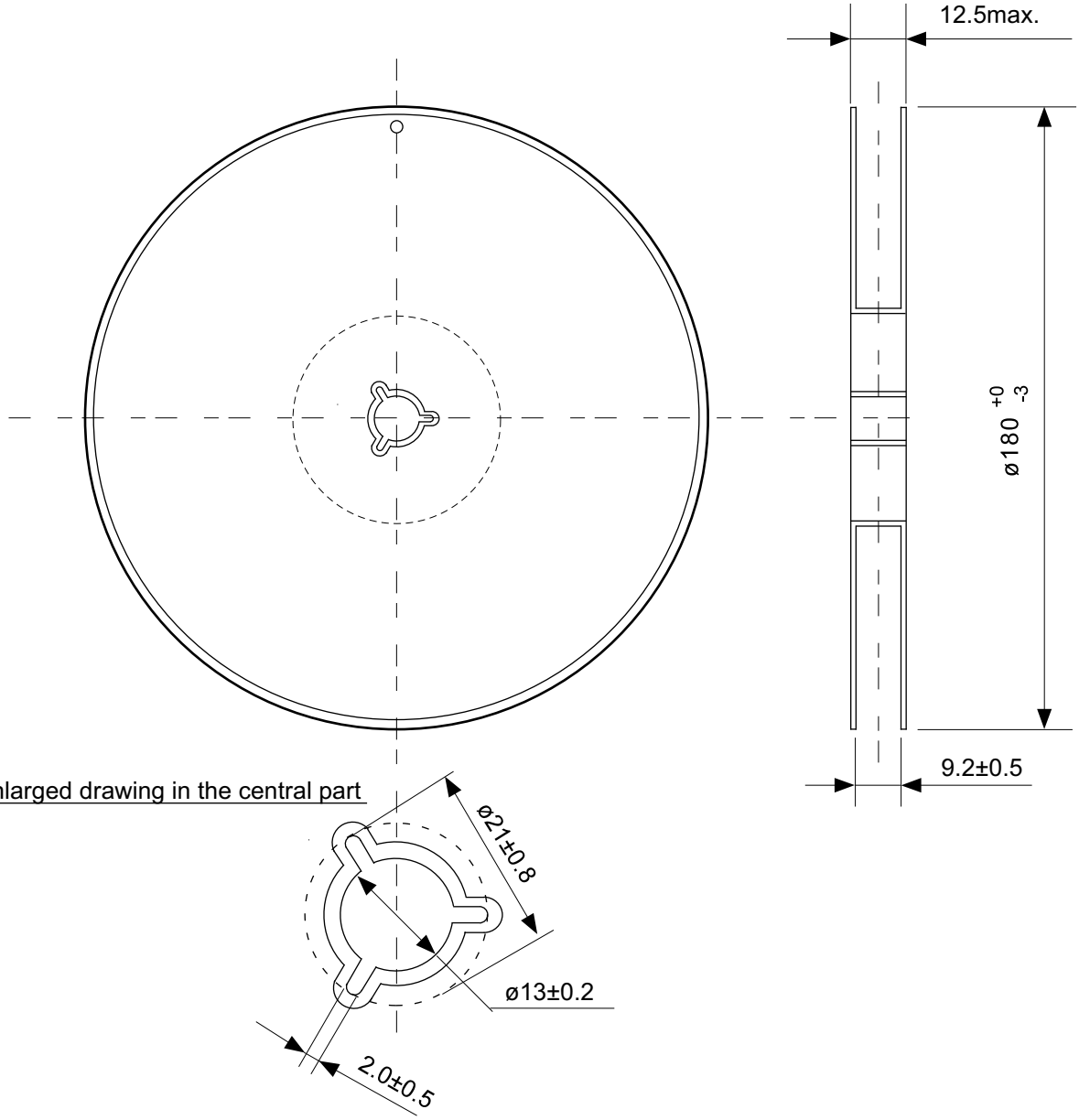
TITLE	DFN-8-B-PKG Dimensions
No.	PQ008-B-P-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	





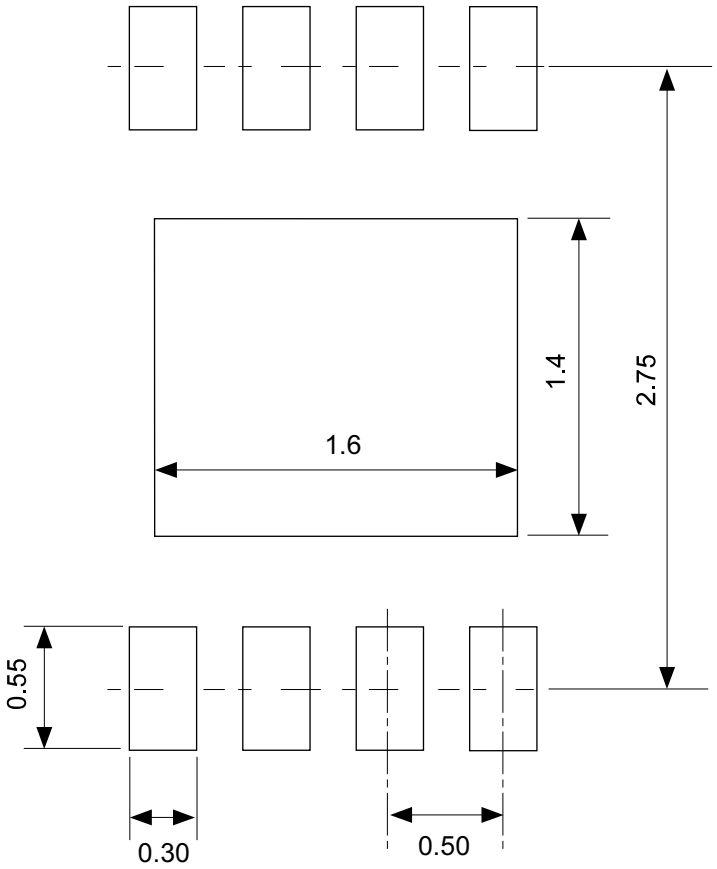
No. PQ008-B-C-SD-1.0

TITLE	DFN-8-B-Carrier Tape
No.	PQ008-B-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



No. PQ008-B-R-SD-1.0

TITLE	DFN-8-B-Reel		
No.	PQ008-B-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			



No. PQ008-B-L-SD-1.0

TITLE	DFN-8-B-Land Recommendation
No.	PQ008-B-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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