NCP1835

Integrated Li-Ion Charger

NCP1835 is an integrated linear charger specifically designed to charge 1−cell Li−Ion batteries with a constant current, constant voltage (CCCV) profile. It can charge at currents of up to 1.0 A.

Its low input voltage capability, adjustable charge current, ability to maintain regulation without a battery, and its onboard thermal foldback make it versatile enough to charge from a variety of wall adapters. The NCP1835 can charge from a standard voltage−source wall adapter as a CCCV charger, or from a current limited adapter to limit power dissipation in the pass device.

Features

- Integrated Voltage and Current Regulation
- No External MOSFET, Sense Resistor or Blocking Diode Required
- Charge Current Thermal Foldback
- Integrated Pre−charge Current for Conditioning Deeply Discharged Battery
- Integrated End−of−Charge (EOC) Detection
- 1% Voltage Regulation
- 4.2 V or 4.242 V Regulated Output Voltage
- Regulation Maintained without a Battery Present
- Programmable Full Charge Current 300 – 1000 mA
- Open−Drain Charger Status and Fault Alert Flags
- 2.8 V Output for AC Present Indication and Powering Charging Subsystems
- Minimum Input Voltage of 2.4 V Allows Use of Current Limited Adapters
- Automatically Recharging if Battery Voltage Drops after Charging Cycle is Completed
- Low Profile 3x3 mm DFN Package
- Pb−Free Packages are Available

Typical Applications

- Cellular Phones
- PDAs, MP3 Players
- Stand−Alone Chargers
- Battery Operated Devices

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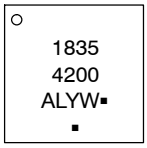
http://onsemi.com

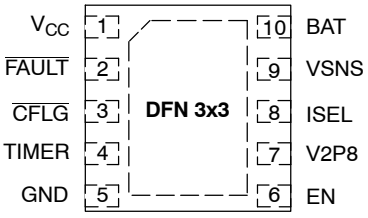
MARKING DIAGRAMS

DFN 3x3
MN SUFFIX
CASE 485C



1835 = Device Code
4200 = 4.2 V
4242 = 4.242 V
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

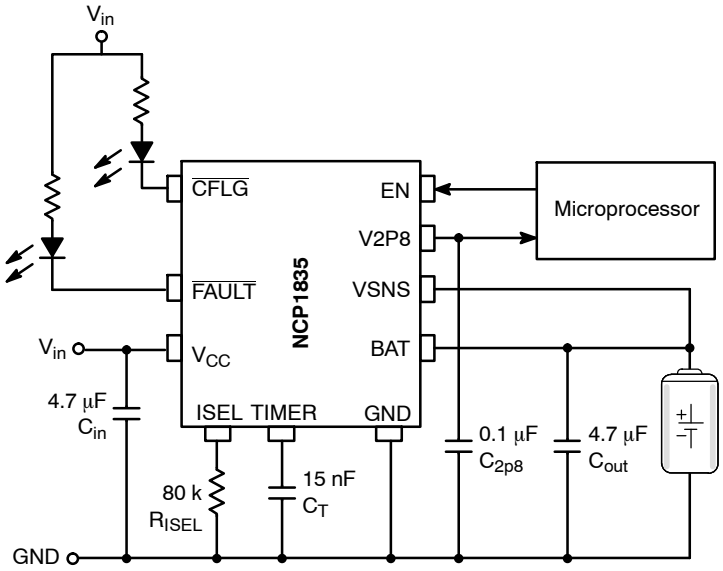


Figure 1. Typical Application Circuit

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	V_{CC}	Input Supply Voltage. Provides power to the charger. This pin should be bypassed with at least a 4.7 μF ceramic capacitor to ground.
2	$\overline{FAULT}$	An open−drain output indicating fault status. This pin is pulled LOW under any fault conditions. A $\overline{FAULT}$ condition resets the counter.
3	$\overline{CFLG}$	An open−drain output indicating charging or end−of−charge states. The $\overline{CFLG}$ pin is pulled LOW when the charger is charging a battery. It is forced open when the charge current drops to I_{EOC}. This high impedance mode will be latched until a recharge cycle or a new charge cycle starts.
4	TIMER	Connecting a timing capacitor, C_{TIME} between this pin and ground to set end−of−charge timeout timer. TIMEOUT = $14*C_{TIME}/1.0$ nF (minute). The total charge for CC and CV mode is limited to the length of TIMEOUT. Trickle Charge has a time limit of 1/8 of the TIMEOUT period.
5	GND	Ground pin of the IC. For thermal consideration, it is recommended to solder the exposed metal pad on the backside of the package to ground.
6	EN	Enable logic input. Connect the EN pin to LOW to disable the charger or leave it floating to enable the charger.
7	V2P8	2.8 V reference voltage output. This pin outputs a 2.8 V voltage source when an adapter is present. The maximum loading for this pin is 2.0 mA.
8	ISEL	The full charge current (I_{FCHG}) can be set by connecting a resistor, R_{ISEL}, from the ISEL pin to ground. $I_{FCHG} = (0.8*10^5 / R_{ISEL})$ A, the pre−charge current $I_{PC} = (0.1*I_{FCHG})$ A and the end−of−charge threshold current $I_{EOC} = (0.1*I_{FCHG})$ A. For best accuracy, a resistor with 1% tolerance is recommended.
9	VSNS	Battery voltage sense pin. Connect this as close as possible to the battery input connection.
10	BAT	Charge current output. A minimum 4.7 μF capacitor is needed for stability when the battery is not attached.

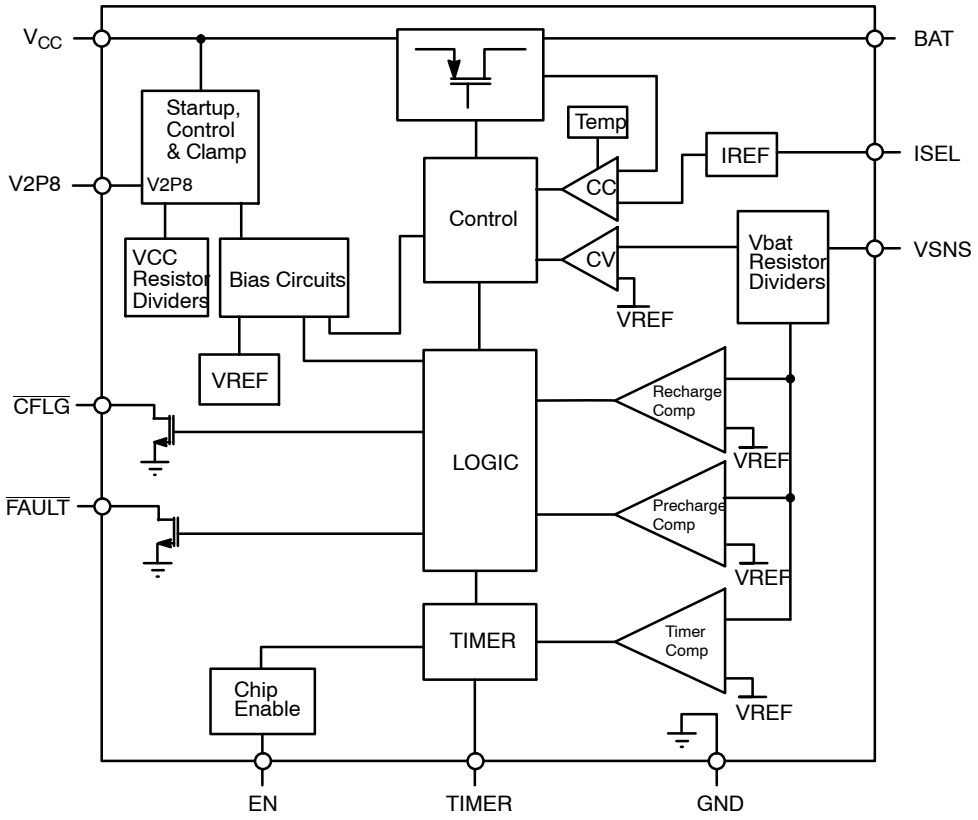


Figure 2. Detailed Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	V
Status Flag Output Pins	$V_{\overline{FAULT}}$, $V_{\overline{CFLG}}$	7.0	V
Voltage Range for Other Pins	V_{io}	5.5	V
Current Out from BAT Pin	I_O	1.2	A
Thermal Characteristics Thermal Resistance, Junction−to−Air (Note 3) Power Dissipation, T_A = 25°C (Note 3)	 $R_{\theta JA}$ P_D	 68.5 1.09	 °C/W W
Moisture Sensitivity (Note 4)	MSL	Level 1	
Operating Ambient Temperature	T_A	−20 to 70	°C
Storage Temperature	T_{stg}	−55 to 125	°C
ESD Human Body Model Machine Model	 HBM MM	 2000 200	 V V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and is tested per the following standards:
   Human Body Model (HBM) per JEDEC standard: JESD22−A114.
   Machine Model (MM) per JEDEC standard: JESD22−A115.
2. Latchup Current Maximum Rating: 150 mA per JEDEC standard: JESD78.
3. Measure on 1 inch sq. of 1 oz. copper area. $R_{\theta JA}$ is highly dependent on the PCB heatsink area. For example, $R_{\theta JA}$ can be 38°C/W on 1 inch sq. of 1 oz. copper area on 4 layer PCB that has 1 single signal layer with the additional 3 solid ground or power planes. The maximum package power dissipation limit must not be exceeded:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

   with $R_{\theta JA}$ = 68.5°C/W, $T_{J(max)}$ = 100°C, P_D = 1.09 W.
4. Moisture Sensitivity Level per IPC/JEDEC standard: J−STD−020A.

ELECTRICAL CHARACTERISTICS (Typical values are tested at V_{CC} = 5.0 V and room temperature, maximum and minimum values are guaranteed over 0°C to 70°C with a supply voltage in the range of 4.3 V to 6.5 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} SUPPLY					
Operating Supply Range	V_{CC}	2.8	–	6.5	V
Rising V_{CC} Threshold	V_{RISE}	3.0	3.4	3.95	V
Falling V_{CC} Lockout Threshold	V_{FALL}	2.0	2.4	2.8	V
Quiescent V_{CC} Pin Supply Current Shutdown (EN = Low) Normal Operation (EN = High)	 I_{VCC} I_{VCC}	 – –	 30 1.0	 – –	 μA mA
Battery Drain Current Manual Shutdown (V_{CC} = 5.0 V, VSNS = 4.0 V, EN = Low)	I_{BMS}	–	–	3.0	μA
CHARGING PERFORMANCE					
Regulated Output Voltage in Constant Voltage (CV) Mode 4.2 V Version, I_{CHG} = 10 mA 4.242 V Version, I_{CHG} = 10 mA	V_{REG}	 4.158 4.200	 4.200 4.242	 4.242 4.284	V
Dropout Voltage (V_{BAT} = 3.7 V, I_{CHG} = 0.5 A)	–	–	200	300	mV
Pre−Charge Threshold Voltage	V_{PC}	2.52	2.8	3.08	V
Pre−Charge Current (R_{ISEL} = 80 kΩ, V_{BAT} = 2.0 V)	I_{PC}	78	100	122	mA
Recommended Full Charge Current	I_{FCHG}	300	–	1000	mA
Full−Charge Current in Constant Current (CC) Mode (R_{ISEL} = 80 kΩ, V_{BAT} = 3.7 V)	I_{FCHG}	0.9	1.0	1.1	A
End−of−Charge Threshold (R_{ISEL} = 80 kΩ, V_{BAT} = V_{REG})	I_{EOC}	78	100	122	mA
Recharge Voltage Threshold	V_{RECH}	3.9	4.03	4.155	V
Thermal Foldback Limit (Junction Temperature) (Note 5)	T_{LIM}	–	100	–	°C
OSCILLATOR					
Oscillation Period (C_{TIME} = 15 nF)	T_{OSC}	2.4	3.0	3.6	ms
STATUS FLAGS					
$\overline{CFLG}$ Pin Recommended Maximum Operating Voltage	$V_{\overline{CFLG}}$	–	–	6.5	V
$\overline{FAULT}$ Pin Recommended Maximum Operating Voltage	$V_{\overline{FAULT}}$	–	–	6.5	V
$\overline{CFLG}$ Pin Sink Current (V_{CFLG} = 0.8 V)	$I_{\overline{CFLG}}$	5.0	–	–	mA
$\overline{FAULT}$ Pin Sink Current (V_{FAULT} = 0.8 V)	$I_{\overline{FAULT}}$	5.0	–	–	mA
EN PIN					
EN Pin High Level Threshold (Note 6)	V_{ENH}	0.95	–	1.15	V
EN Pin Low Level Threshold (Note 6)	V_{ENL}	0.73	–	0.88	V

5. Guaranteed by design. Not tested in production.
6. Not tested in production, but guaranteed by design and characterization at +25°C.

TYPICAL OPERATING CHARACTERISTICS

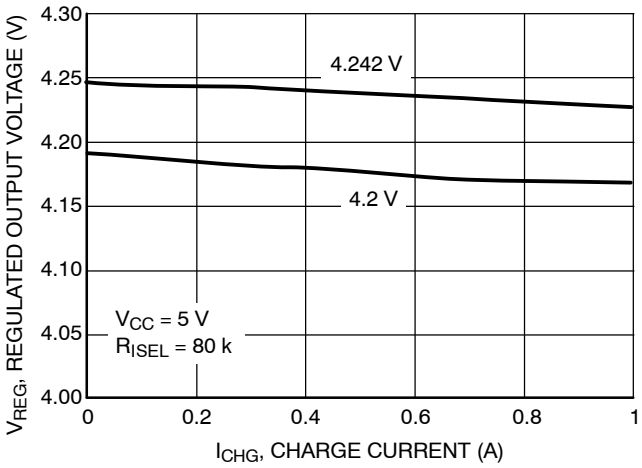


Figure 3. Regulated Output Voltage vs. Charge Current

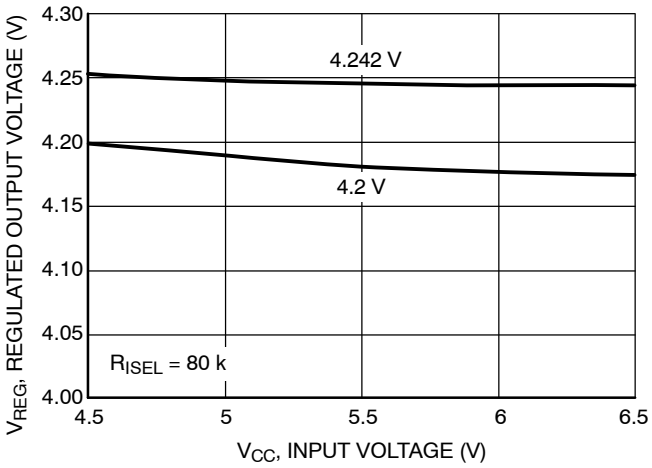


Figure 4. Regulated Output Voltage (floating) vs. Input Voltage

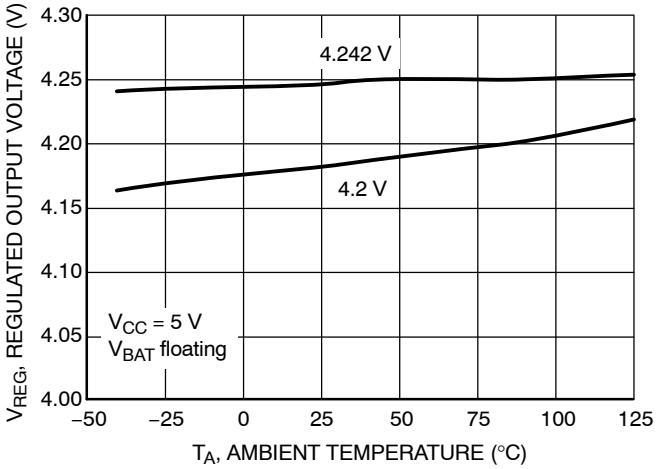


Figure 5. Regulated Output Voltage vs. Temperature

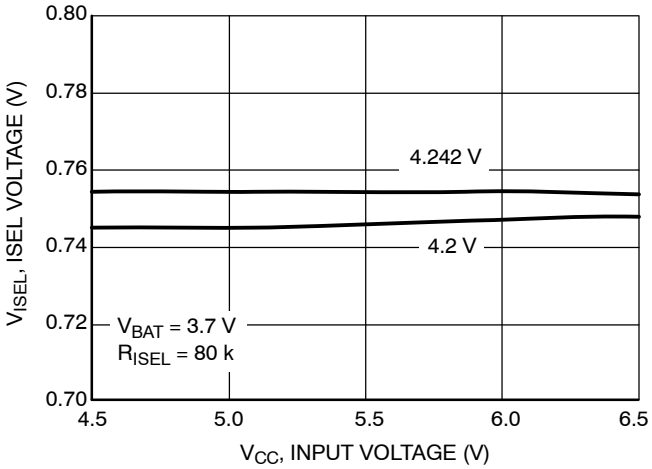


Figure 6. ISEL Voltage vs. Input Voltage

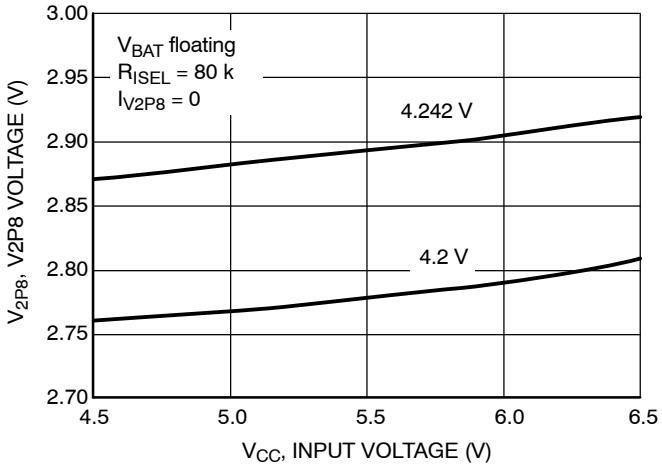


Figure 7. V2P8 Voltage vs. Input Voltage

TYPICAL OPERATING CHARACTERISTICS

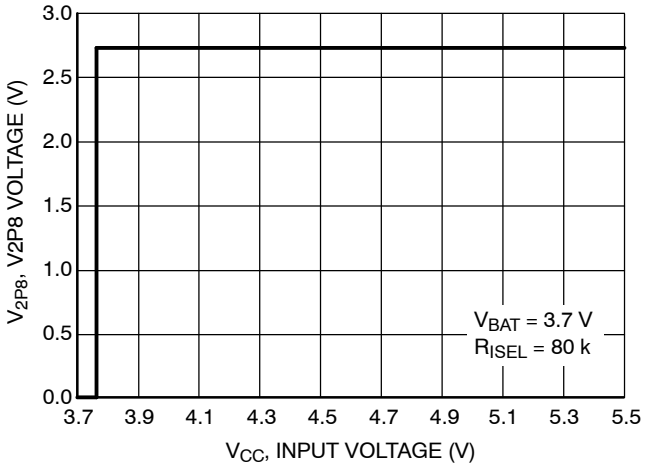


Figure 8. V2P8 Voltage vs. Input Voltage

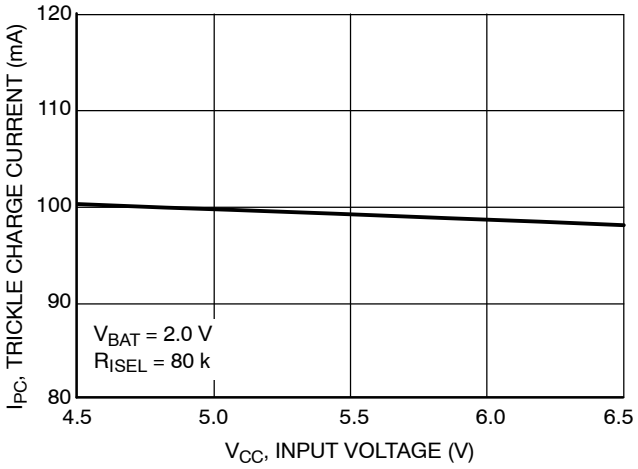


Figure 9. Trickle Charge Current vs. Input Voltage

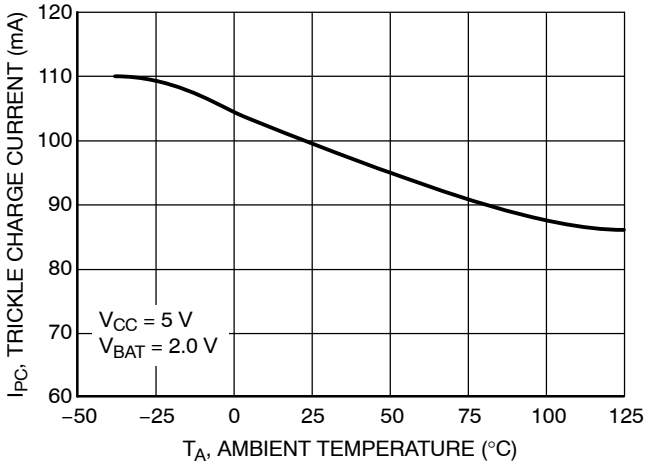


Figure 10. Trickle Charge Current vs. Temperature

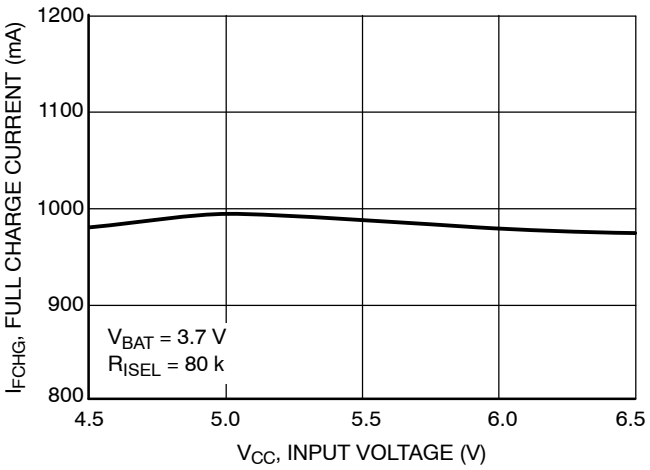


Figure 11. Full Charge Current vs. Input Voltage

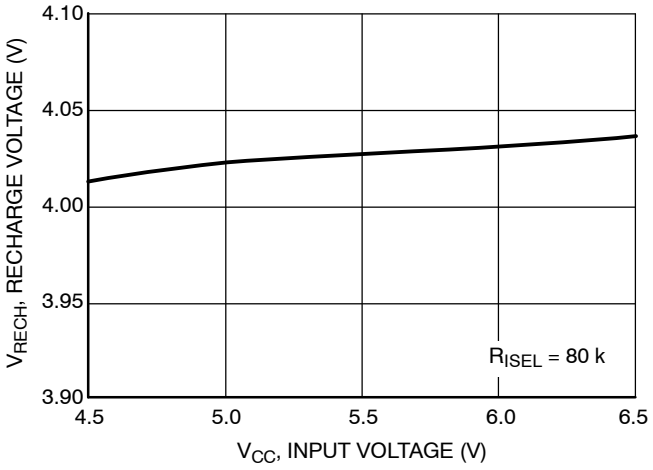


Figure 12. Recharge Voltage vs. Input Voltage

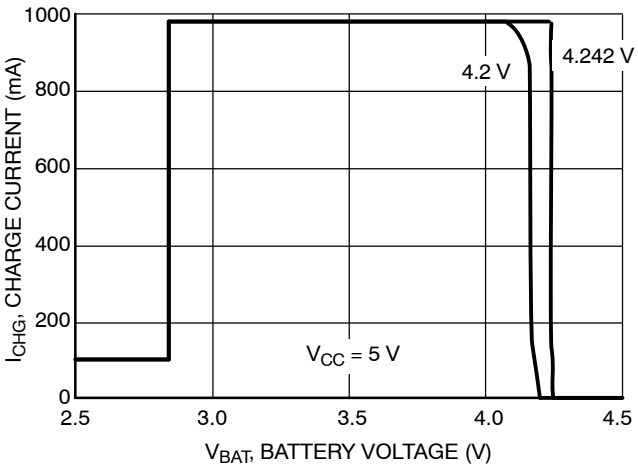


Figure 13. Charge Current vs. Battery Voltage

DETAILED OPERATING DESCRIPTION

Overview

Rechargeable Li−Ion/Polymer batteries are normally charged with a constant current (CC) until the terminal voltage reaches a fixed voltage threshold, at which point a constant voltage (CV) is applied and the current drawn by the battery decays. The charging rate is determined by the specific rating of the battery. For example, if the battery is rated at 800 mA−hours, then the recommended maximum charge rate is 800 mA. For a severely discharged cell, it takes approximately 2.5−3.5 hours to recharge the battery at the maximum rate. So, when one charges at less than the maximum charge rate, the recharge time increases. Also, the battery should not be continuously charged or the battery could age faster than necessary. Because of this, Li−Ion charging systems need to stop charging within a prescribed time limit regardless of the charge rate.

The NCP1835 is a fully integrated, stand−alone 1−cell Li−Ion charger which performs the primary battery charging functions and includes a timer which will terminate charging if the battery has not completed charging within a prescribed time period. The charging rate is user programmable up to 1.0 A and the end−of−charge timer is also programmable. The NCP1835 has a thermal foldback loop which reduces the charge rate if the junction temperature is exceeded. The device also includes several outputs which can be used to drive LED indicators or interface to a microprocessor to provide status information. The adapter providing power to the charger can be a standard fixed output voltage such as a 5.0 V wall adapter or it can be a simple current limited adapter.

The NCP1835 comes in two versions with output voltage regulation thresholds of 4.2 or 4.242 V depending on the requirements of the specific battery pack being used. The user determines the charge current by selecting the resistor R_{ISEL} and determines the length of the end−of−charge timeout timer by selecting the capacitor, C_{TIME}.

Charging Operation

Figure 13 outlines the charging algorithm of the NCP1835 and Figure 14 graphically illustrates this. When the charger is powered up and the input voltage rises above the power−on, rising threshold (nominally 3.4 V), the charger initiates the charging cycle.

The NCP1835 first determines the cell voltage. If it is less than the pre−charge threshold (2.8 V), the IC recognizes the battery as severely discharged. In this state, the NCP1835 pre−conditions (trickle charges) the battery by charging it at 10% of the full charge rate (I_{PC}). This slow charge prevents the battery from being damaged from high fast charge currents when it is in a deeply discharged state. The battery voltage should be trickle charged up to 2.8 V before 1/8 of the preset end−of−charge time is expired. If it cannot reach this voltage, than the battery is possibly shorted or damaged. Therefore, the NCP1835 stops charging and the pre−charge timeout signal asserts the $\overline{\text{FAULT}}$ flag.

Once the cell voltage crosses the pre−charge threshold, the device will transition to normal (full−rate) charging at 100% of the programmed full rate charge current (I_{FCHG}). As the NCP1835 charges the battery, the cell voltage rises until it reaches the V_{REG} threshold, (4.2 or 4.242 V). At the maximum charge rate, it normally takes about 1 hour to reach this point from a fully discharged state, and the battery will be approximately 70−80% recharged. At this point, the charge transitions to constant voltage mode where the IC forces the battery to remain at a constant voltage, V_{REG}. During this constant voltage state, the current required to maintain V_{REG} steadily decreases as the battery approaches full charge. Charge current eventually falls to a very low value as the battery approaches a fully charged condition.

The NCP1835 monitors the current into the battery until it drops to 10% of the full charge rate. This is the End−of−Charge (EOC) threshold. Normally it takes 1.5−2.5 hours to reach this point. Once the NCP1835 reaches end−of−charge it opens the $\overline{\text{CFLG}}$ pin and enters the EOC state. The IC continues to charge the battery until it reaches TIMEOUT. At that point, the NCP1835 stops charging. If the system does not reach EOC during the TIMEOUT period, the NCP1835 views this as a system fault and asserts the $\overline{\text{FAULT}}$ flag. If the battery voltage drops below the recharge threshold (which can occur if the battery is loaded), the IC reinitializes the charging sequence and begins a new charge cycle. The recharge voltage threshold, V_{RECH}, is nominally 4.03 V.

In the inhibit state, the NCP1835 continues to monitor the battery voltage, but does not charge the battery. Again, if the battery voltage drops below the recharge threshold the IC reinitializes the charging sequence and begins a new charge cycle.

Charging Flow Chart

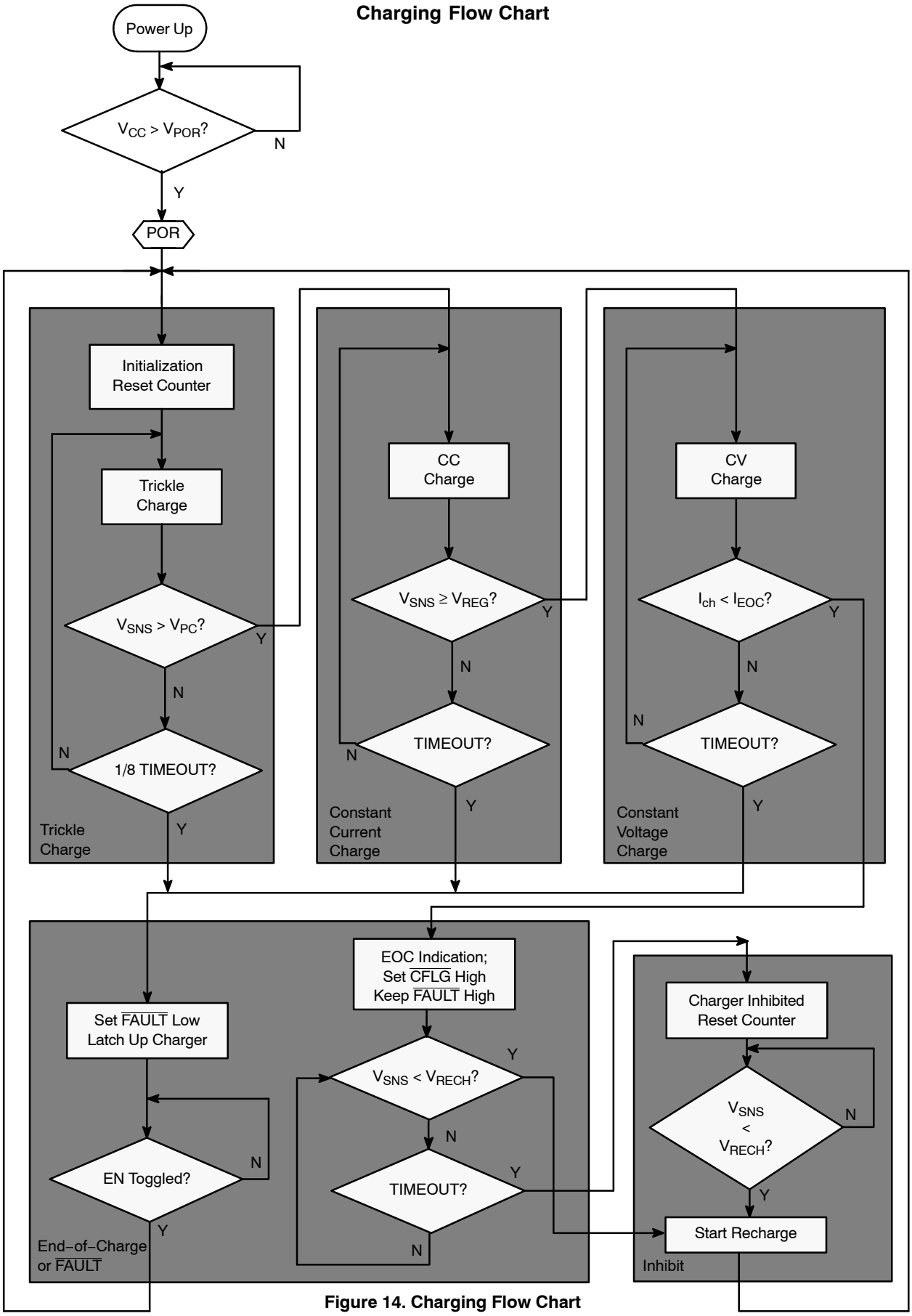


Figure 14. Charging Flow Chart

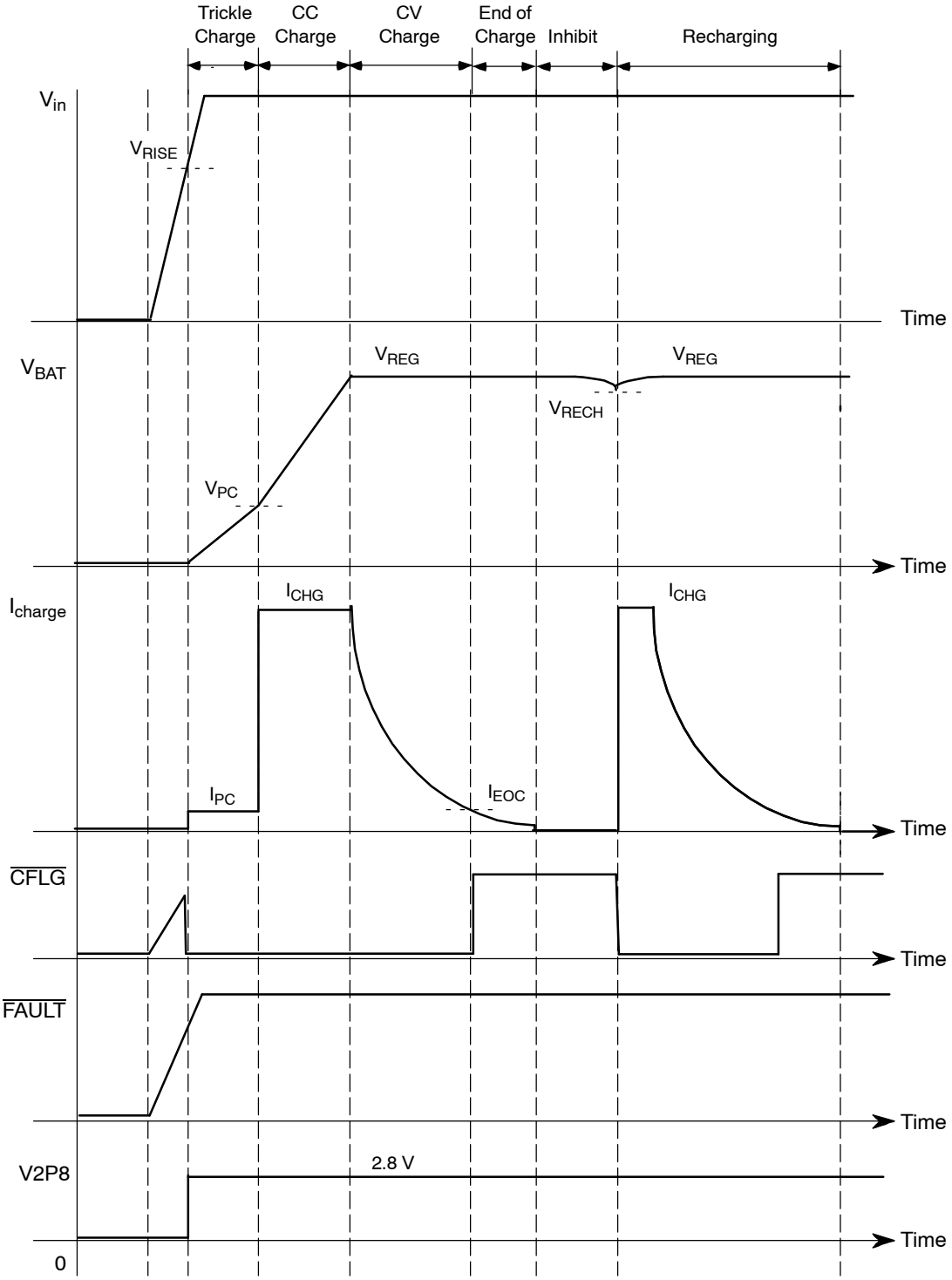


Figure 15. Typical Charging Diagram

Table 1. Charge Status

Condition	$\overline{CFLG}$	$\overline{FAULT}$
Trickle, Constant Current and Constant Voltage Charge	Low	High
End−of−Charge or Shutdown Mode	High	High
Timeout Fault, V_{ISEL} < 0.35 V or V_{ISEL} > 1.4 V	High	Low

Charge Status Indicator ($\overline{\text{CFLG}}$)

$\overline{\text{CFLG}}$ is an open−drain output that indicates battery charging or End−of−Charge (EOC) status. It is pulled low when charging in constant current mode and constant voltage mode. It will be forced to a high impedance state when the charge current drops to I_{EOC}. When the charger is in shutdown mode, $\overline{\text{CFLG}}$ will also stay in the high impedance state.

Fault Indicator ($\overline{\text{FAULT}}$)

$\overline{\text{FAULT}}$ is an open−drain output that indicates that a charge fault has occurred. It has two states: low or high impedance. In a normal charge cycle, it stays in a high impedance state. At fault conditions, it will be pulled low and terminate the charge cycle. A timeout fault occurs when the full charge or pre−charge timeouts are violated, or if the voltage on ISEL is greater than 1.4 V or lower than 0.35 V. There are two ways to get the charger out of a fault condition and back to a normal charge cycle. One can either toggle the EN pin from GND to a floating state or reset the input power supply.

Adapter Present Indicator (V2P8)

V2P8 is an input power supply presence indicator. When the input voltage, V_{CC}, is above the power on threshold (V_{RISE}, nominally 3.4 V) and is also 100 mV above the battery voltage, it provides a 2.8 V reference voltage that can source up to 2.0 mA. This voltage can also be used to power a microprocessor I/O.

Enable/Disable (EN)

Pulling the EN pin to GND disables the NCP1835. In shutdown mode, the internal reference, oscillator, and control circuits are all turned off. This reduces the battery drain current to less than 3.0 μA and the input supply current to 30 μA. Floating the EN pin enables the charger.

Thermal Foldback

An internal thermal foldback loop reduces the programmed charge current proportionally if the die temperature rises above the preset thermal limit (nominally 100°C). This feature provides the charger protection from over heating or thermal damage. Figure 16 shows the full charge current reduction due to die temperature increase across the thermal foldback limit. For a charger with a 1.0 A constant charge current, the charge current starts decreasing when the die temperature hits 100°C and is reduced to zero when the die temperature rises to 110°C.

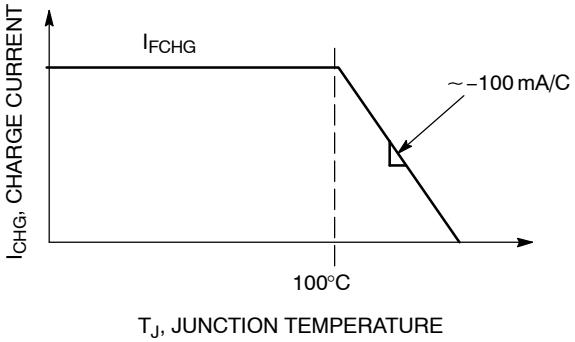


Figure 16. Full Charge Current vs. Junction Temperature

APPLICATION INFORMATION

Input and Output Capacitor Selection

A 4.7 μF or higher value ceramic capacitor is recommended for the input bypass capacitor. For the output capacitor, when there is no battery inserted and the NCP1835 is used as an LDO with 4.2 V or 4.242 V output voltage, a 4.7 μF or higher value tantalum capacitor is recommended for stability. With the battery attached, the output capacitor can be any type with the value higher than 0.1 μF.

R_{ISEL} Resistor Selection for Programming Charge Current

A single resistor, R_{ISEL}, between the ISEL pin and ground programs the pre−charge current, full charge current, and end−of−charge detection threshold. The nominal voltage of ISEL is 0.8 V. The charge current out of BAT pin is 100,000 times the current out of ISEL pin. Therefore, the full charge current (I_{FCHG}) is:

$$I_{FCHG} = 100,000 \times \frac{0.8}{R_{ISEL}} \text{ (A)} \qquad \text{(eq. 1)}$$

I_{PC} and I_{EOC} are 10% of the value programmed above with the R_{ISEL} resistor.

The following table and curves show the selection of the resistance value for desired currents.

Table 2. Charge Current vs. R_{ISEL}

I_{FCHG} (mA)	I_{PC} / I_{EOC} (mA)	R_{ISEL} (kΩ)
300	30	267
500	50	160
600	60	133.3
700	70	114.3
800	80	100
900	90	88.9
1000	100	80

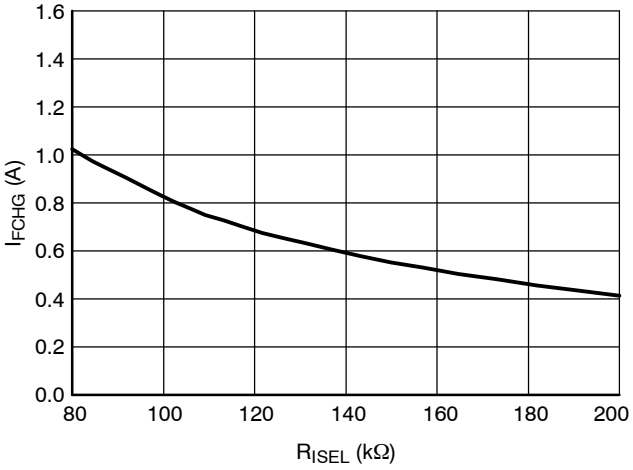


Figure 17. Full−Charge Current (I_{FCHG}) vs. Current Select Resistor (R_{ISEL})

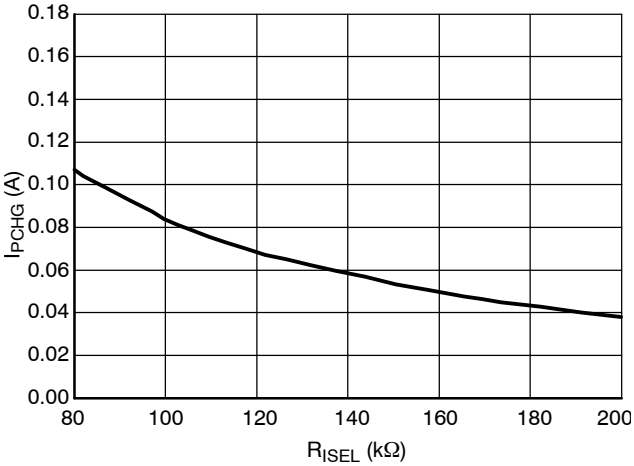


Figure 18. Pre−Charge Current (I_{PCHG}) vs. Current Select Resistor (R_{ISEL})

C_{TIME} Selection for Programming Charge Time

The NCP1835 offers an end−of−charge timeout timer to prevent the battery from continuously charging which can cause premature aging or safety issues. The timing capacitor between TIMER pin and ground, C_{TIME}, sets the end−of−charge time, TIMEOUT, and the pre−charge timeout. This capacitor is required for proper device operation.

The internal oscillator charges C_{TIME} to 1.2 V and then discharges it to 0.6 V with 6 μA current in one period. Therefore, the period of the oscillator is:

$$T_{OSC} = 2 \times \frac{C_{TIME} \times dV_C}{I_C} = 0.2 \times 10^6 \times C_{TIME} \text{ (sec)} \qquad \text{(eq. 2)}$$

A 22−binary counter counts every oscillator period until it reaches the maximum number corresponding to end−of−charge time, TIMEOUT.

$$\text{TIMEOUT} = 2^{22} \times T_{OSC} = 14 \times \frac{C_{TIME}}{1 \text{ nF}} \text{ (minute)} \qquad \text{(eq. 3)}$$

The NCP1835 will terminate charging and give a timeout signal if the battery has not completed charging within the TIMEOUT period. The timeout signal then forces the $\overline{\text{FAULT}}$ pin low.

The following Table 3 shows the desired TIMEOUT vs. C_{TIME} sizes. The C_{TIME} is required for proper device operation.

Table 3. TIMEOUT vs. C_{TIME} Size

C_{TIME} (nF)	TIMEOUT (minute)
0.47	6.6
1	14
5.6	78
8.2	115
10	140
15	210
33	462
56	784

Thermal Considerations

The NCP1835 is housed in a thermally enhanced 3x3 mm DFN package. In order to deliver the maximum power dissipation under all conditions, it is very important that the user solders exposed metal pad under the package to the ground copper area and then connect this area to a ground plane through thermal vias. This can greatly reduce the thermal impedance of the device and further enhance its power dissipation capability and thus its output current capability.

Charging with Constant Voltage Adapters or Current Limited Adapters

The NCP1835 can be powered from two types of regulated adapters: a traditional constant voltage type or a current limited type. Figure 19 illustrates the operation of the linear charger powered with a standard constant voltage adapter. The power dissipation in the linear charger is:

$$P_{dis} = (V_{CC} - V_{BAT}) \times I_{CHG} \quad \text{(eq. 4)}$$

The maximum power dissipation P1 happens at the beginning of a full current charge, since this is the point that the power supply and the battery voltage have the largest difference. As the battery voltage rises during charging, the power dissipation drops. After entering the constant voltage mode, the power dissipation drops further due to the decreasing charge current. The maximum power that the linear charger can dissipate is dependent on the thermal resistance of the device. In case the device can not handle the maximum power P1, the thermal foldback loop reduces the charge current which limits the power dissipation to the sustained level P2. Figure 19 shows this.

Using the adapter's current limit can provide better thermal performance than the above example. A current limited adapter operates as a constant voltage adapter before the charge current reaches the current limit. I_{LIM} must be less than the programmed full charge current I_{FCHG}. Once the current limit is reached, the adapter will source the current limit I_{LIM} while its output voltage will drop to follow the battery voltage. If the application uses the adapter to power its systems while the battery is being charged, this drooping voltage can be an issue.

The worst case power dissipation with a current limited adapter occurs at the beginning of the constant voltage mode, which is shown at point P3 in Figure 20. If P3 is higher than P2, the maximum power dissipation that the charger can handle, then the thermal foldback function will be activated.

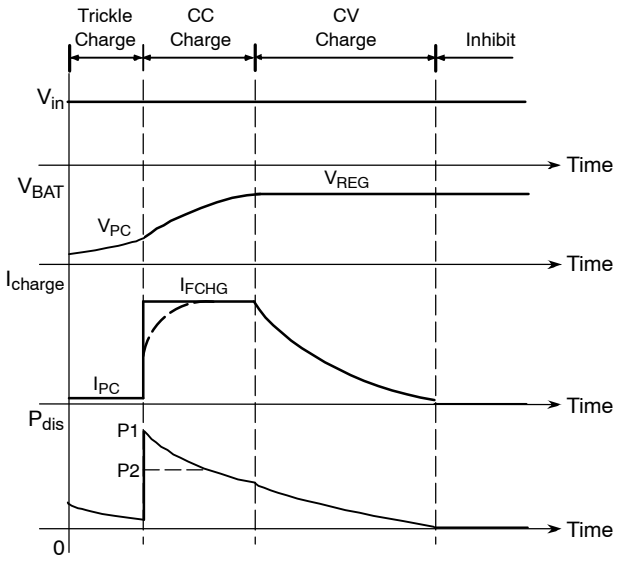


Figure 19. Typical Charge Curves with a Constant Voltage Adapter

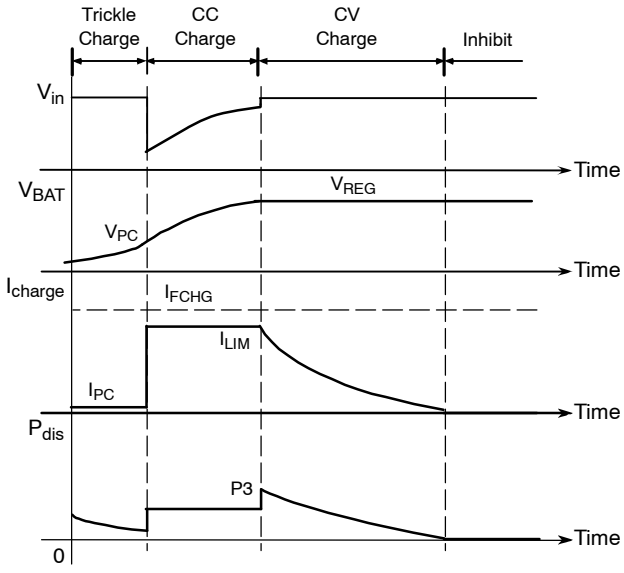


Figure 20. Typical Charge Curves with a Current Limited Adapter

PCB Layout Recommendations

The recommended footprint for the 3x3 mm DFN package is included on the Package Dimension page. It is critical that the exposed metal pad is properly soldered to the ground copper area and then connected to a ground plane through thermal vias. The maximum recommended thermal via diameter is 12 mils (0.305 mm). Limited by the size of the pad, six thermal vias should allow for proper thermal regulation without sacrificing too much copper area within the pad. The copper pad is the primary heatsink and should be connected to as much top layer metal as possible to minimize the thermal impedance. Figure 21 illustrates graphically the recommended connection for the exposed pad with vias.

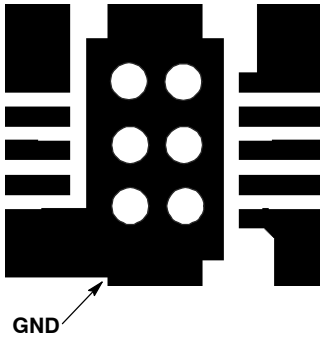


Figure 21. Recommended Footprint

The following is a NCP1835 Demo Board Schematic, Layout, and suggested Bill of Materials.

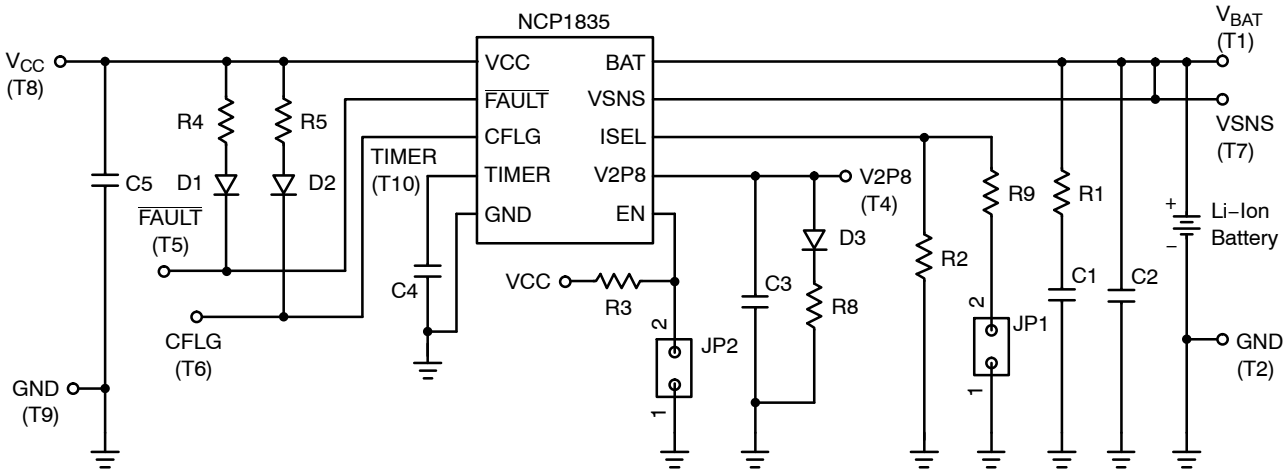


Figure 22. Demo Board Schematic

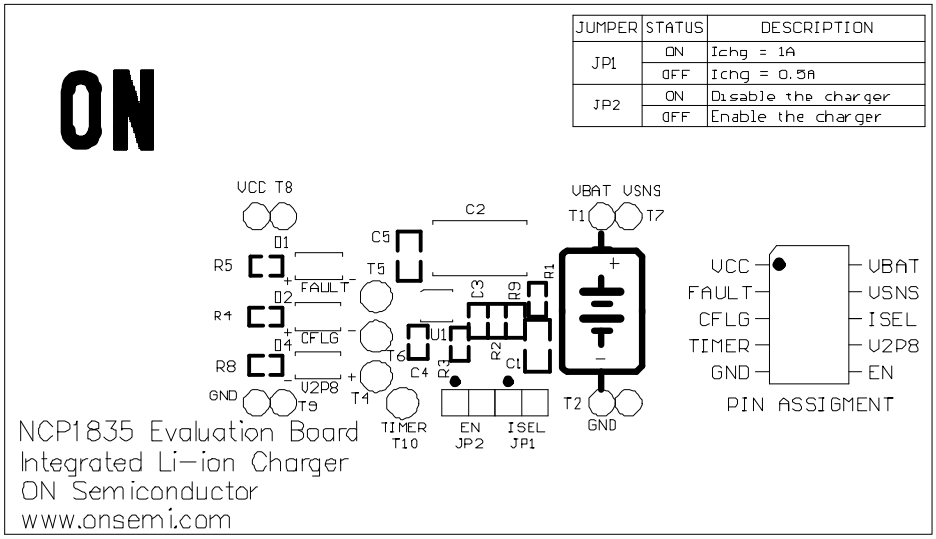


Figure 23. Silkscreen Layer

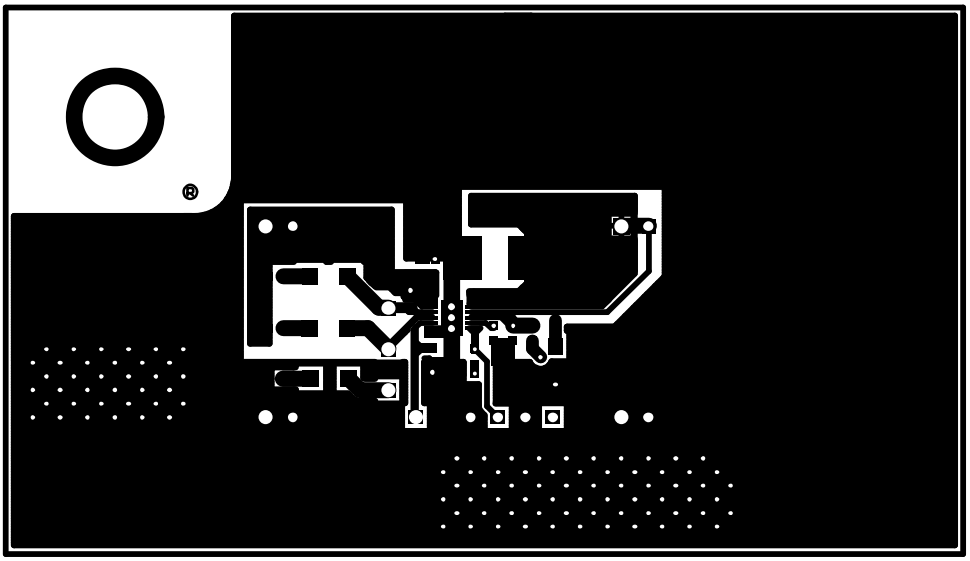


Figure 24. Top Layer

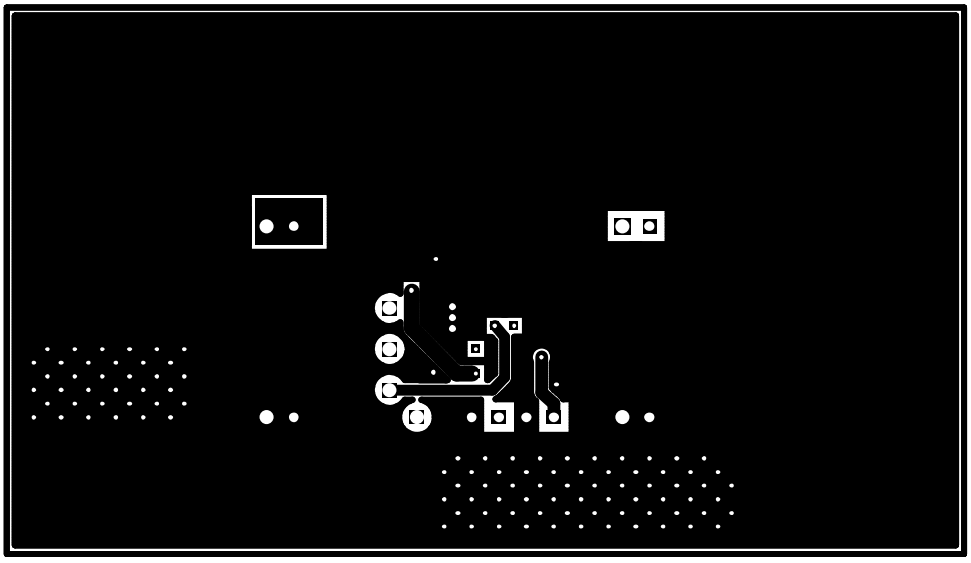


Figure 25. Bottom Layer

Table 4. Bill of Materials

Item	Qty.	Part Description	Designators	Suppliers	Part Number
1	1	NCP1835 Integrated Li−Ion Charger (DFN−10)	U1	ON Semiconductor	NCP1835
2	1	Chip Resistor ±1% 0 Ω (0603)	R1	Vishay	CRCW06030R00F
3	2	Chip Resistor ±1% 160 kΩ (0603)	R2, R9	Vishay	CRCW06031603F
4	1	Chip Resistor ±1% 100 kΩ (0603)	R3	Vishay	CRCW06031003F
5	2	Chip Resistor ±1% 1.0 kΩ (0603)	R4, R5	Vishay	CRCW06031001F
6	1	Chip Resistor ±1% 432 Ω (0603)	R8	Vishay	CRCW06034320F
8	1	Chip Capacitor 1.0 μF/16 V, ±20% (0805)	C1	Panasonic	ECJGVB1C105M
9	1	Chip Capacitor 4.7 μF/10 V, ±20% (3528−21)	C2	Kemet	T491B475K010AS
10	1	Chip Capacitor 0.1 μF/10 V, ±10% (0402)	C3	Panasonic	ECJ0EB1A104K
11	1	Chip Capacitor 15 nF/16 V, ±10% (0402)	C4	Panasonic	ECJ0EB1C153K
12	1	Chip Capacitor 4.7 μF/25 V, ±20% (0805)	C5	Panasonic	ECJ2FB1E475M
13	1	SMT Chip LED Red	D1	Agilent	HSMH−C150
14	1	SMT Chip LED Green	D2	Agilent	HSMG−C150
15	1	SMT Chip LED Yellow	D4	Agilent	HSMY−C150
16	5	Test Pin	T1, T2, T7, T8, T9, T10	AMP/Tyco	4−103747−0
17	2	Header Pin Pinch = 2.54 mm	JP1, JP2	AMP/Tyco	4−103747−0

ORDERING INFORMATION

Device	Voltage Option	Package	Shipping†
NCP1835MN20R2	4.2 V	DFN−10	3000 / Tape & Reel
NCP1835MN20R2G	4.2 V	DFN−10 (Pb−Free)	3000 / Tape & Reel
NCP1835MN24T2	4.242 V	DFN−10	3000 / Tape & Reel
NCP1835MN24T2G	4.242 V	DFN−10 (Pb−Free)	3000 / Tape & Reel

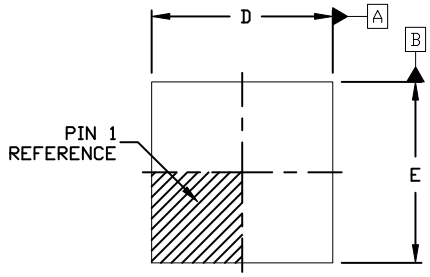
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

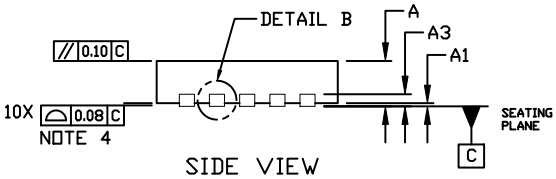
DFN10, 3x3, 0.5P
CASE 485C
ISSUE F

DATE 16 DEC 2021

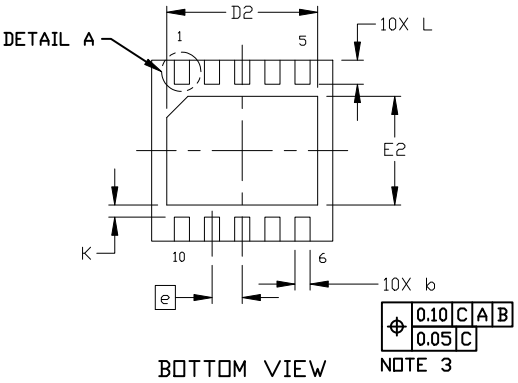
SCALE 2:1



TOP VIEW

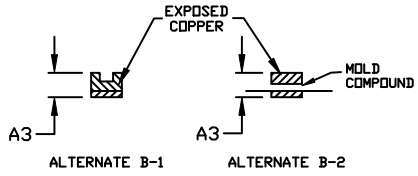


SIDE VIEW

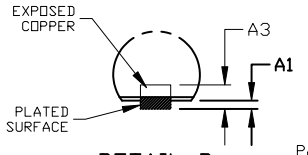


BOTTOM VIEW

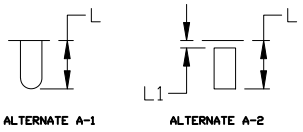
NOTES:
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



DETAIL B
ALTERNATE CONSTRUCTION

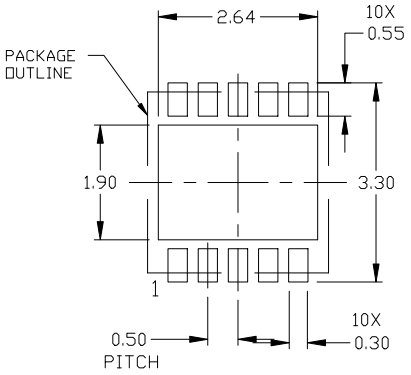


DETAIL B
WETTABLE FLANK
CONSTRUCTION



DETAIL A
ALTERNATE CONSTRUCTION

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.20 REF	
L	0.30	0.40	0.50
L1	---	---	0.03



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFN10, 3X3 MM, 0.5 MM PITCH**		**PAGE 1 OF 1**

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