NCV891234, NCV891334

2 MHz Low-I_Q Dual-Mode Step-Down Regulator for Automotive

The NCV891x34 is a Dual Mode regulator intended for Automotive, battery−connected applications that must operate with up to a 45 V input supply. Hybrid Low Power Mode allows the NCV891x34 to operate either as a PWM Buck Converter or as a Low Drop−Out Linear Regulator, and the NCV891x34 is suitable for systems with Low Noise and Low Quiescent Current requirements often encountered in automotive driver information systems. A reset (with fixed delay) and a fault pin (flagging low input voltage and high temperature warnings) simplify interfacing with a microcontroller.

Two pins are provided to synchronize switching to a clock, or to another NCV891x34. The NCV891x34 also provides several protection features expected in automotive power supply systems such as current limit, short circuit protection, and thermal shutdown. In addition, the high switching frequency produces low output voltage ripple even when using small inductor values and an all−ceramic output filter capacitor – forming a space−efficient switching regulator solution.

Features

- 40 μA Iq in Light Load Condition
- 2.0 A Maximum Output Current in PWM Mode in NCV891234
- 3.0 A Maximum Output Current in PWM Mode in NCV891334
- Internal N−channel Power Switch
- V_{IN} Operating Range 3.7 V to 36 V, Withstands Load Dump to 45 V
- Logic Level Enable Pin can be Tied to Battery
- Fixed Output Voltage of 5.0 V or 3.3 V with ±2% Accuracy
- 2 MHz Free−running Switching Frequency
- Input and Output Synchronization Pins
- NCV Prefix for Automotive Requiring Site and Control Changes
- Wettable Flanks DFN (pin edge plating)
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Safety−Vision Systems
- Audio, Infotainment
- Instrumentation
- Telematics

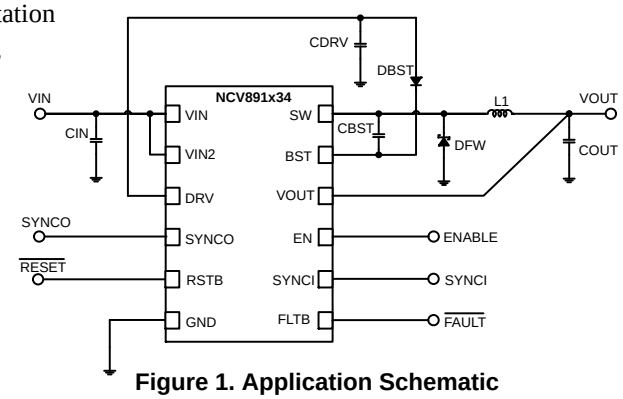

Figure 1. Application Schematic

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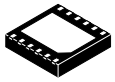


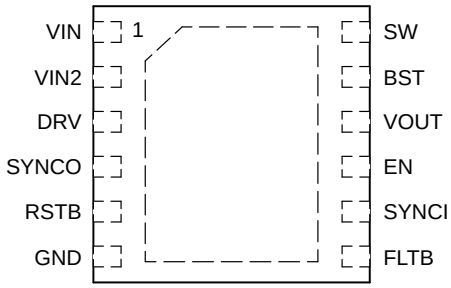
DFN12
MW SUFFIX
CASE 506CE

MARKING DIAGRAM

891x34XX = Specific Device Code
x = 2, 3
XX = 33, 50
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Device

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

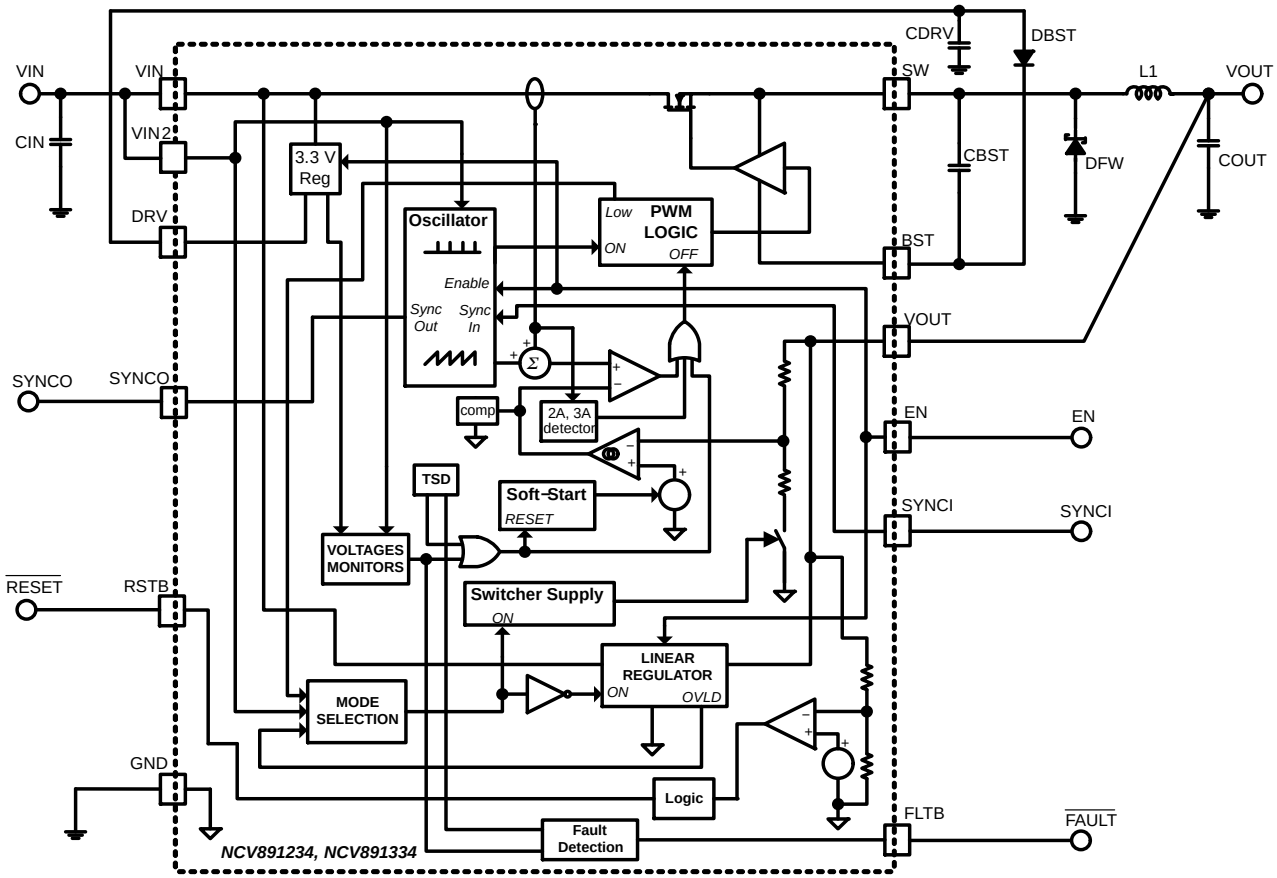


Figure 2. Simplified Block Diagrams

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	VIN	Input voltage from battery. Place an input filter capacitor in close proximity to this pin.
2	VIN2	Input voltage pin – must be connected to VIN (pin 1)
3	DRV	Output voltage to provide a regulated voltage to the Power Switch gate driver.
4	SYNCO	Out−of−phase synchronization output. Turn−on of the Power Switch causes the SYNCO signal to fall (and rise half a switching period later).
5	RSTB	Reset function. Open drain output, pulling down to ground when the output voltage is out of regulation.
6	GND	Battery return, and output voltage ground reference.
7	FLTB	Fault flag indicating various fault conditions for the part
8	SYNCI	Synchronization input. Connecting an external clock to this pin synchronizes switching to the rising edge of the SYNCI signal.
9	EN	This TTL compatible Enable input allows the direct connection of Battery as the enable signal. Grounding this input stops switching and reduces quiescent current draw to a minimum.
10	VOUT	Output voltage feedback and LDO output. Feedback of output voltage used for regulation, as well as LDO output in LDO mode.
11	BST	Bootstrap input provides drive voltage higher than VIN to the N−channel Power Switch for minimum switch Rdson and highest efficiency.
12	SW	Switching node of the Regulator. Connect the output inductor and cathode of the freewheeling diode to this pin.
EPAD		Connect to Pin 6 (electrical ground) and to a low thermal resistance path to the ambient temperature environment.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Min/Max Voltage VIN		−0.3 to 45	V
Max Voltage VIN to SW		45	V
Min/Max Voltage SW		−0.7 to 40	V
Min Voltage SW − 20 ns		−3.0	V
Min/Max Voltage EN		−0.3 to 40	V
Min/Max Voltage BST		−0.3 to 43	V
Min/Max Voltage BST to SW		−0.3 to 3.6	V
Min/Max Voltage SYNCI, RSTB and FLTB		−0.3 to 6	V
Min/Max Voltage VOUT		−0.3 to 18	V
Min/Max Voltage DRV, SYNCO		−0.3 to 3.6	V
Thermal Resistance, DFN12−4x4 Junction–to–Ambient (Note 1)	$R_{\theta JA}$	35	°C/W
Storage Temperature Range		−55 to +150	°C
Operating Junction Temperature Range	T_J	−40 to +150	°C
ESD Withstand Voltage (Note 2) − Human Body Model	VESD	2.0	kV
Moisture Sensitivity	MSL	Level 1	
Peak Reflow Soldering Temperature (Note 3)		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Value based on 4 layers of 645 mm^2 (or 1 in^2) of 1 oz copper thickness on FR4 PCB substrate.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 3. ELECTRICAL CHARACTERISTICS
V_{IN} = 4.5 to 28 V, V_{EN} = 5 V, V_{BST} = V_{SW} + 3 V, C_{DRV} = 0.1 μF, for typical values T_J = 25°C, min/max values are valid for T_J = −40°C to 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation (Notes 4, 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
QUIESCENT CURRENT						
Quiescent Current, enabled	V_{IN} = 13.2 V, I_{OUT} = 100 μA, 25°C	I_q		40	49	μA
Quiescent Current, shutdown	V_{IN} = 13.2 V, V_{EN} = 0 V, 25°C	I_{qSD}		9	12	μA
UNDERVOLTAGE LOCKOUT – VIN (UVLO)						
UVLO Start Threshold	V_{IN} rising	V_{UVLSTT}	4.1		4.5	V
UVLO Stop Threshold	V_{IN} falling	V_{UVLSTP}	3.1		3.7	V
UVLO Hysteresis		V_{UVLOHY}	0.4		1.4	V
SOFT−START (SS)						
Soft−Start Completion Time		t_{SS}	0.8	1.4	2.0	ms
OUTPUT VOLTAGE						
Output Voltage during regulation 100 μA < I_{OUT} < 2.5 A 5.0 V option 3.3 V option		V_{OUTreg}	 4.9 3.234	 5.0 3.3	 5.1 3.366	V
OSCILLATOR						
Frequency 4.5 < V_{IN} < 18 V 20 V < V_{IN} < 28 V		F_{SW} $F_{SW(HV)}$	1.8 0.9	2.0 1.0	2.2 1.1	MHz
VIN FREQUENCY FOLDBACK MONITOR						
Frequency Foldback Threshold V_{IN} rising V_{IN} falling		 V_{FLDUP} V_{FLDDN}	 18.4 18		 20 19.8	V
Frequency Foldback Hysteresis		V_{FLDHY}	0.2	0.3	0.4	V
MODE TRANSITION						
Normal to Low−Iq mode Current Threshold		I_{NtoL}	3		40	mA
Mode Transition Duration Switcher to Linear Linear to Switcher		 $t_{SWtoLIN}$ $t_{LINtoSW}$		 300 1	 2	μs
Minimum time in Normal Mode before starting to monitor output current		$t_{SWblank}$		500		μs
Linear to switcher transition at high Vin at low Vin	 V_{OUT} = 3.3 V	 $V_{LINtoSW(HV)}$ $V_{LINtoSW(LV)}$	 19 3.6		 28 4.5	V
PEAK CURRENT LIMIT						
Current Limit Threshold NCV891334		I_{LIM}	3.9	4.4	4.9	A
Current Limit Threshold NCV891234		I_{LIM}	2.9	3.25	3.6	A
POWER SWITCH						
ON Resistance	V_{BST} = V_{SW} + 3.0 V	R_{DSON}		180	360	mΩ
Leakage current VIN to SW	V_{SW} = 0, −40°C ≤ T_J ≤ 85°C	I_{LKSW}			10	μA
Minimum ON Time	Measured at SW pin	t_{ONMIN}	45		70	ns
Minimum OFF Time Measured at SW pin At F_{SW} = 2 MHz (normal) At F_{SW} = 500 kHz (max duty ratio)		t_{OFFMIN}	 30	 30 50	 70	ns

4. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

Table 3. ELECTRICAL CHARACTERISTICS
V_{IN} = 4.5 to 28 V, V_{EN} = 5 V, V_{BST} = V_{SW} + 3 V, C_{DRV} = 0.1 μF, for typical values T_J = 25°C, min/max values are valid for T_J = −40°C to 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation (Notes 4, 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SLOPE COMPENSATION						
Ramp Slope (With respect to switch current)	4.5 < V_{IN} < 18 V 20 V < V_{IN} < 28V	S_{ramp} $S_{ramp(HV)}$	1.45 0.65	2.0 1.0	2.8 1.3	A/μs
LOW POWER LINEAR REGULATOR						
Line Regulation	I_{OUT} = 5 mA, 6 V < V_{IN} < 18 V	$V_{REG(line)}$		5	25	mV
Load Regulation	V_{IN} = 13.2 V, 0.1 mA < I_{OUT} < 50 mA	$V_{REG(load)}$		5	35	mV
Power Supply Rejection	$V_{OUT(ripple)}$ = 0.5 Vp−p, F = 100 Hz	PSRR		65		dB
Current Limit		$I_{LIN(lim)}$	50		80	mA
Output clamp current	V_{OUT} = $V_{OUTreg(typ)}$ + 10%	$I_{CL(OUT)}$	0.5	1.0	1.5	mA
SHORT CIRCUIT DETECTOR						
Switching frequency in short−circuit condition Analog Foldback Analog foldback – high V_{IN} Hiccup Mode	 V_{OUT} = 0 V, 4.5 V < V_{IN} < 18 V V_{OUT} = 0 V, 20 V < V_{IN} < 28 V	 F_{SWAF} F_{SWAFHV} F_{SWHIC}	 450 225 24	 550 275 32	 650 325 40	kHz
RESET						
Leakage current into RSTB pin					1	μA
Output voltage threshold at which the RSTB signal goes low	V_{OUT} decreasing 5.0 V option 3.3 V option	V_{RESET}	 4.50 2.97	 4.625 3.05	 4.75 3.14	V
Hysteresis on RSTB threshold	V_{OUT} increasing 5.0 V option 3.3 V option	V_{REShys}	 25 17	 60 40	 100 66	mV
Noise−filtering delay	From V_{OUT} < V_{RESET} to RSTB pin going low	t_{filter}	10		25	μs
Restart Delay time	From V_{OUT} > V_{RESET} + V_{REShys} to high RSTB	t_{delay}	14	16	18	ms
Low RSTB voltage	$R_{RSTBpullup}$ = V_{OUTreg}/1 mA, V_{OUT} > 1 V	$V_{RSTBlow}$			0.4	V
GATE VOLTAGE SUPPLY (DRV pin)						
Output Voltage		V_{DRV}	3.1	3.3	3.5	V
DRV UVLO START Threshold		V_{DRVSTT}	2.7	2.9	3.05	V
DRV UVLO STOP Threshold		V_{DRVSTP}	2.5	2.8	3.0	V
DRV UVLO Hysteresis		V_{DRVHYS}	50		200	mV
DRV Current Limit	V_{DRV} = 0 V	I_{DRVLIM}	21		50	mA
VIN OVERVOLTAGE SHUTDOWN MONITOR						
Overvoltage Stop Threshold	V_{IN} increasing	V_{OVSTP}	36.5	37.7	39.0	V
Overvoltage Start Threshold	V_{IN} decreasing	V_{OVSTT}	36.0	37.3	38.8	V
Overvoltage Hysteresis		V_{OVHY}	0.25	0.40	0.50	V
ENABLE (EN)						
Logic low threshold voltage		V_{ENlow}	0.8			V
Logic high threshold voltage		V_{ENhigh}			2	V
EN pin input current		I_{ENbias}	0.2		1	μA

4. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
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Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SYNCHRONIZATION						
SYNCI pin input resistance to GND	V_{SYNCI} = 5 V	RHsynci	50		200	kΩ
High threshold voltage		VHsynci			2	V
Low threshold voltage		VLsynci	0.8			V
Minimum high pulse width	$V_{SYNCI} > V_{Hsynci(max)}$	tHsynci	40			ns
Minimum low pulse width	$V_{SYNCI} < V_{Lsynci(min)}$	tLsynci	40			ns
Synchronization frequency		Fsynci	1.8		2.5	MHz
Master reassertion time	Time from last rising SYNCI edge to first unsynchronized turn−on.			650		ns
SYNCO pulse duty ratio	$C_{SYNCO(load)}$ = 40 pF	D_{SYNCO}	40		60	%
SYNCO pulse transition time (rise and fall)	$C_{SYNCO(load)}$ = 40 pF, 10−90%	$t_{tran(SYNCO)}$		4		ns
FLTB						
Leakage current into FLTB pin					1	μA
Low FLTB voltage	$R_{FLTBpullup} = V_{OUTreg}$/1 mA, V_{OUT} > 1 V	$V_{FLTBlow}$			0.4	V
Low Voltage Indicator threshold VIN decreasing VIN increasing		 $V_{LVIdown}$ V_{LVIup}	 6.8 6.95	 7.1 7.47	 7.4 8.0	V
Low Voltage Indicator Threshold Hysteresis		V_{LVIhys}	0.15	0.37	0.6	V
Temperature Warning Threshold Temperature increasing Temperature decreasing		 T_{WARNup} $T_{WARNdown}$	 140 120	 158	 175 170	°C
Temperature Warning Threshold Hysteresis		$T_{WARNhys}$	5		20	°C
TWARN to TSD margin		$T_{WARNmargin}$	8		20	°C
THERMAL SHUTDOWN						
Activation Temperature		TSD	155		190	°C
Reset temperature		$TSD_{restart}$	135		185	
Hysteresis		T_{HYS}	5		20	°C

4. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

APPLICATION INFORMATION

Hybrid Low−Power Mode

A high−frequency switch−mode regulator is not very efficient in light load conditions, making it difficult to achieve low−Iq requirements for sleep−mode operation. To remedy this, the NCV891x34 includes a low−Iq linear regulator that turns on at light load, while the PWM regulator turns off, ensuring a high−efficiency low−power operation. Another advantage of the low−power mode is the tight regulation free of voltage ripple usually associated with low−Iq switchers in light load conditions. In either mode, the NCV891x34 meets the 2% output voltage regulation specification.

At initial start−up the NCV891x34 will soft−start into PWM converter mode regardless of output current. During a 300 μs period, the NCV891x34 will assess the level of output current. The NCV891x34 will not make the assessment if RSTB is low. If the output current is above the I_{Ntol} threshold, the NCV891x34 will stay in PWM mode. Otherwise, the NCV891x34 will transition to low power mode.

It will stay in this low−power mode until the output current exceeds the $I_{LIN(lim)}$ limit: it then transitions back to PWM converter mode. This low−power mode to PWM mode transition happens within 2 μs. The transient response is not affected by the mode change.

Once the NCV891x34 has transitioned to switcher mode, a 500 μs blanking period will occur. After the blanking period, the NCV891x34 will reassess the output current level. If the output current level is below the I_{NtoL} threshold, the NCV891x34 will enter low−Iq mode.

If the NCV891x34 is in low−power mode and in normal battery range, it will transition to switcher mode when V_{IN} increases above $V_{LINtoSW(HV)}$, regardless of the output current. Similarly, if the NCV891x34 is in PWM mode and V_{IN} is higher than V_{FLDUP}, it will not transition to low−power mode even if the output current becomes lower than I_{NtoL}.

At low input voltage, the NCV891x34 stays in low−power mode down to $V_{LINtoSW(LV)}$ if it entered this mode while in normal battery range. However it may not enter low−power mode below 8 V depending on the charge of the bootstrap capacitor (see Bootstrap section for details).

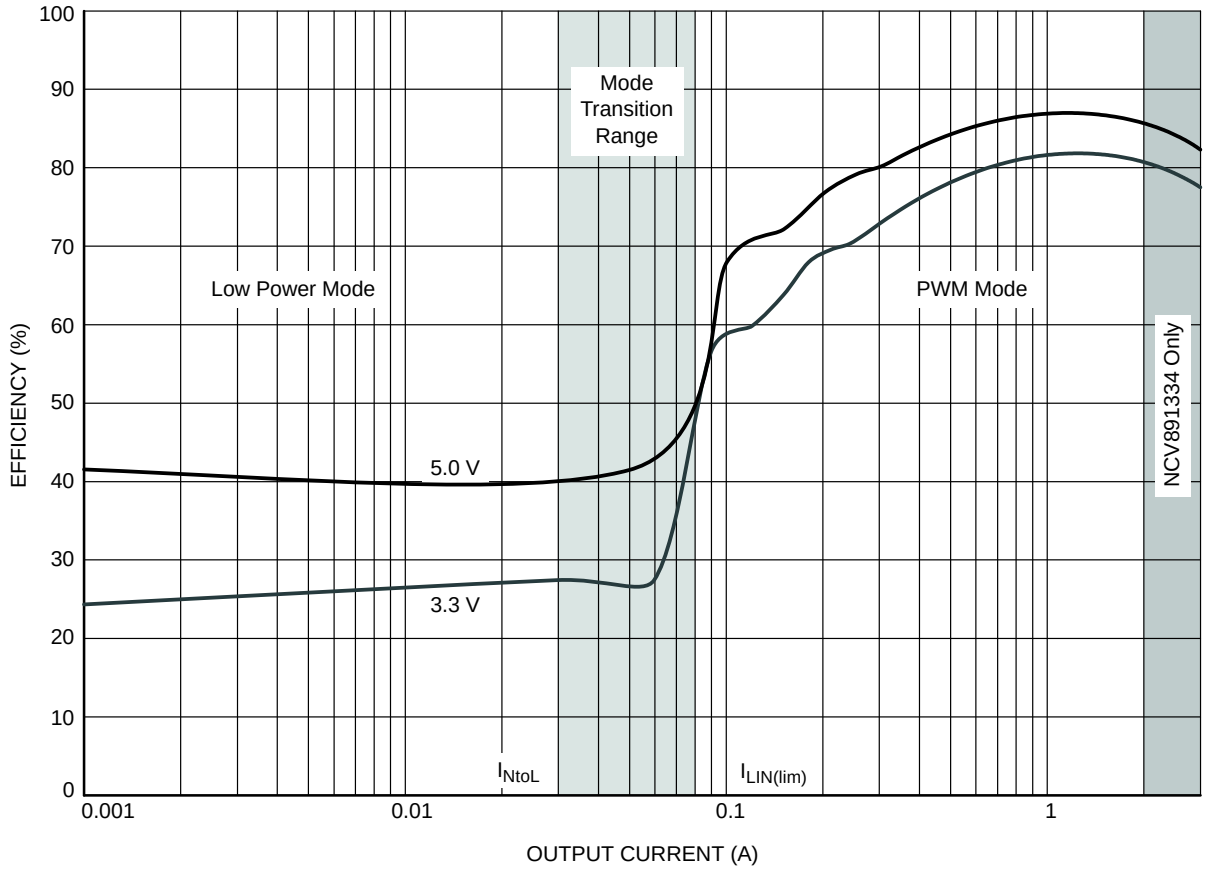


Figure 3. Measured NCV891334 Efficiency at V_{IN} = 12 V with Hybrid Low Power Mode

Input Voltage

An Undervoltage Lockout (UVLO) circuit monitors the input, can inhibit switching, and resets the Soft−start circuit if there is insufficient voltage for proper regulation. Depending on the output voltage and load at the output, the NCV891x34 may lose regulation and run in drop−out mode before reaching the UVLO threshold: refer to the Minimum Vin calculation tool for details. When the input voltage drops low enough that the part cannot regulate because it reaches its maximum duty cycle, the switching frequency is divided down by up to 4 (with a minimum frequency of 500 kHz). This helps lower the minimum voltage at which the regulator loses regulation.

While the NCV891x34 can withstand input voltages up to 45 V, an overvoltage monitoring circuit automatically terminates switching if the input voltage exceeds V_{OVSTP} (see Figure 4).

To avoid skipping switching pulses and entering an uncontrolled mode of operation, the switching frequency is reduced by a factor of 2 when the input voltage exceeds the V_{IN} Frequency Foldback threshold (see Figure 4). Frequency reduction is automatically terminated when the input voltage drops back below the V_{IN} Frequency Foldback threshold. This also helps to limit the power lost in switching and generating the drive voltage for the Power Switch.

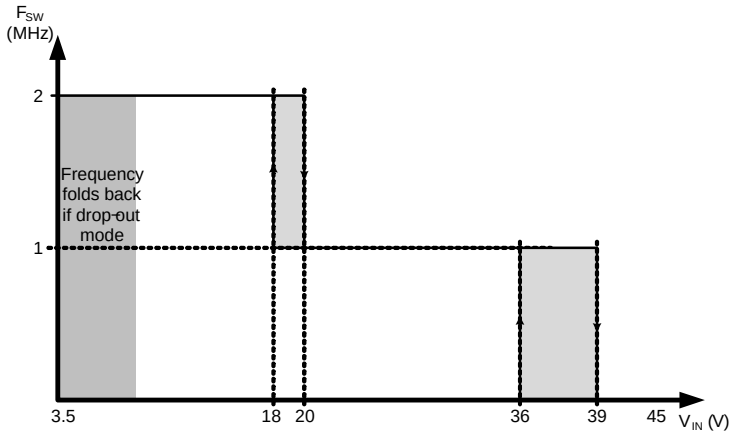


Figure 4. NCV891x34 Switching Frequency Profile vs. Input Voltage

Soft−Start

Once the NCV891x34 is enabled or is released from a fault condition, the DRV voltage will be established and the part will enter soft−start. A soft−start circuit ramps the switching regulator error amplifier reference voltage to the final valuewithin the soft−start completion time, $t_{(ss)}$. During soft−start, the average switching frequency is lower until the output voltage approaches regulation.

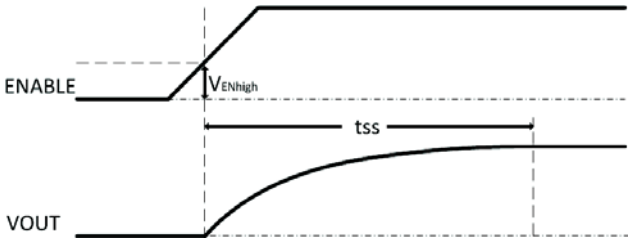


Figure 5. NCV891x34 Soft−start

Slope Compensation

A fixed slope compensation signal is generated internally and added to the sensed current to avoid increased output voltage ripple due to bifurcation of inductor ripple current at duty cycles above 50%. The fixed amplitude of the slope compensation signal requires the inductor to be greater than a minimum value, depending on output voltage, in order to avoid sub−harmonic oscillations. The recommended inductor values are 2.2 or 3.3 μH, although higher values are possible.

Current Limiting

Due to the ripple on the inductor current, the average output current of a buck converter is lower than the peak current setpoint of the regulator. Figure 6 shows – for a 2.2 μH inductor – how the variation of inductor peak current with input voltage affects the maximum DC current the NCV891x34 can deliver to a load.

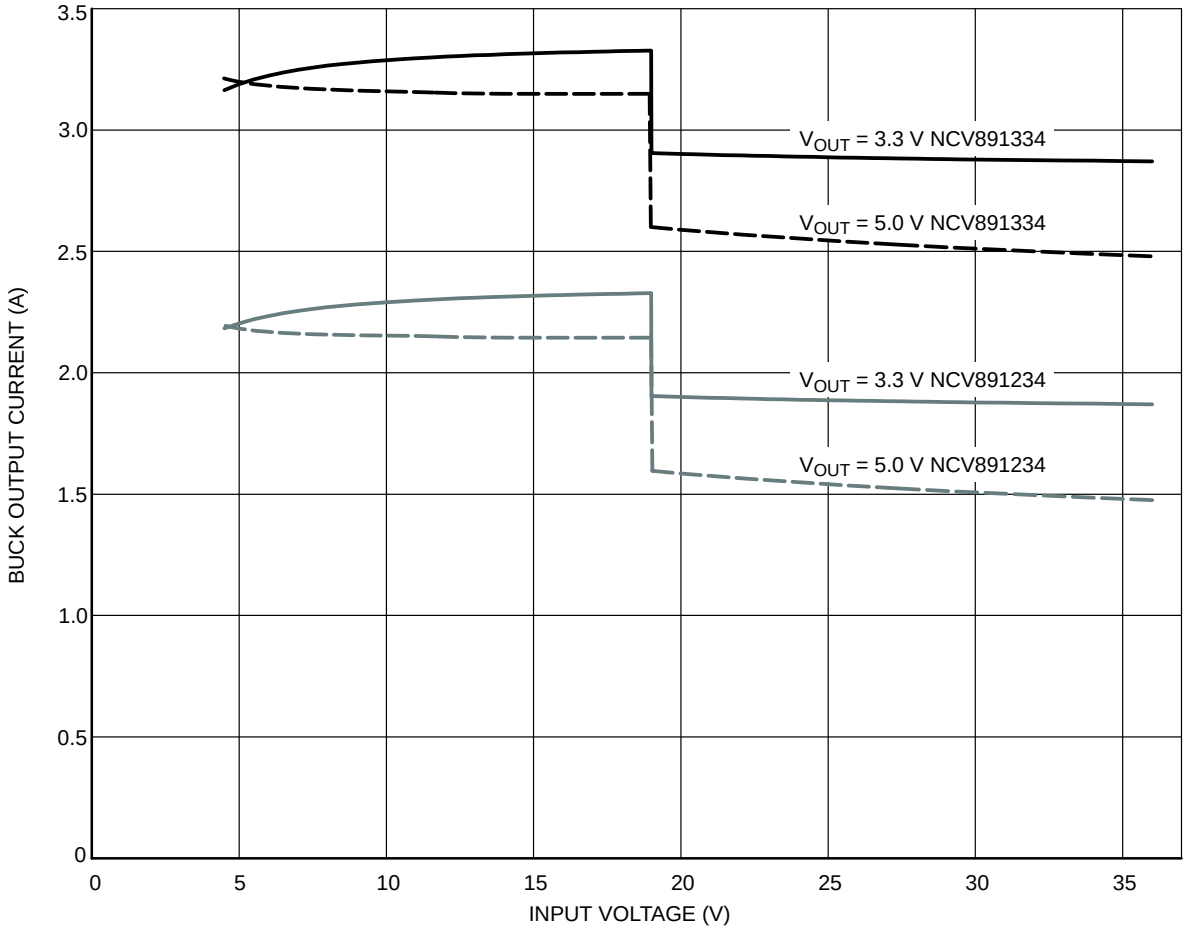


Figure 6. Worst Case NCV891x34 Load Current Capability with a 2.2 μH Inductor

Short Circuit Protection

During severe output overloads or short circuits, the NCV891x34 automatically reduces its switching frequency to F_{SWAF} under normal operating conditions and to F_{SWAFHV} during foldback. This creates duty cycles small enough to limit the peak current in the power components, while maintaining the ability to automatically reestablish the output voltage if the overload is removed.

In more severe short−circuit conditions where the inductor current is still too high after the switching frequency has fully folded back, the regulator enters a hiccup mode that further reduces the power dissipation and protects the system. In hiccup mode, the frequency is further reduced to F_{SWHIC}.

RESET function

The RSTB pin is pulled low when the output voltage falls below 7.5% of the nominal regulation level, and floats when the output is properly regulated. A pull−up resistor tied to the output is needed to generate a logic high signal on this open drain pin. The pin can be left unconnected when not used.

When the output voltage drops out of regulation, the pin goes low after a short noise−filtering delay (t_{filter}). It stays low for a 16 ms delay time after the output goes back to regulation, simplifying the connection to a micro−controller.

The RSTB pin is also pulled low immediately in case of VIN overvoltage, Thermal shutdown, VIN UVLO or DRV UVLO.

Feedback Loop

All components of the feedback loop (output voltage sensing, error amplifier and compensation) are integrated inside the NCV891x34, and are optimized to ensure regulation and sufficient phase and gain margin for the recommended conditions of operation.

Recommended conditions and components:

- Input: car battery
- Output: 3.3 V or 5 V, with output current up to 3 A
- Output capacitor: one to three parallel ceramic 10 μF capacitors
- Inductor: 2.2 μH to 3.3 μH

With these operating conditions and components, the open loop transfer function has a phase margin greater than 50°.

Bootstrap

At the DRV pin an internal regulator provides a ground−referenced voltage to an external capacitor (C_{DRV}), to allow fast recharge of the external bootstrap capacitor (C_{BST}) used to supply power to the power switch gate driver. If the voltage at the DRV pin goes below the DRV UVLO Threshold V_{DRVSTP}, switching is inhibited and the Soft−start circuit is reset, until the DRV pin voltage goes back up above V_{DRVSTT}.

The NCV891x34 monitors the bootstrap capacitor, and always ensures it stays charged no matter what the operating conditions are. As a result, the additional charging current for the bootstrap capacitor may prevent the regulator from entering Low−Iq mode at low input voltage. Practically, the 5 V output version does not enter Low−Iq mode for input voltages below 8 V.

Enable

The NCV891x34 is designed to accept either a logic level signal or battery voltage as an Enable signal. However if voltages above 40 V are expected, EN should be tied to VIN through a 10 kΩ resistor in order to limit the current flowing into the overvoltage protection of the pin.

EN low induces a shutdown mode which shuts off the regulator and minimizes its supply current to 9 μA typical by disabling all functions.

Upon enabling, voltage is established at the DRV pin, followed by a soft−start of the switching regulator output.

Synchronization

Two NCV891x34 can be synchronized out−of−phase to one another by connecting the SYNCO pin of one to the SYNCI pin of the other. Any number of NCV891x34 can also be synchronized to an external clock.

If a part does not have its switching frequency controlled by the SYNCI input, it drives the SYNCO pin low when it turns on the power switch, and drives it high half a switching period later.

When the switching frequency is controlled by the SYNCI input, the SYNCO pin is held low.

Synchronization starts within 2.5 ms of the RSTB Low−to−High transition. A rising edge at the SYNCI pin causes an NCV891x34 to immediately turn on the power switch. If another rising edge does not arrive at the SYNCI pin within the Master Reassertion Time, the NCV891x34 controls its own switching frequency, allowing uninterrupted operation in the event that the clock is turned off.

If internal conditions or excessive input voltage cause an NCV891x34 to fold back its switching frequency, the main oscillator switching frequency is no longer derived from the frequency received at the SYNCI pin. Under these conditions, the SYNCO pin is held low.

An external pulldown resistor is not required at the SYNCI pin if it is unused.

The SYNCO pin is a buffered output (no pull−up resistor needed), and must be left unconnected when not used.

FLTB Function

The FLTB pin is pulled low when one of the following conditions is detected:

- Low Input Voltage (below the LVI threshold, see parametric table)
- High Temperature (above the TWARN threshold, see parametric table)

A pull−up resistor tied to the output is needed to generate a logic high signal on this open drain pin. The pin can be left unconnected when not used.

There is a short noise−filtering delay (t_{filter}) to avoid false reporting.

Thermal Shutdown

A thermal shutdown circuit inhibits switching, resets the Soft−start circuit, and removes DRV voltage if internal temperature exceeds a safe level. Switching is automatically restored when temperature returns to a safe level.

Exposed Pad

The exposed pad (EPAD) on the back of the package must be electrically connected to the electrical ground (GND pin) for proper, noise−free operation.

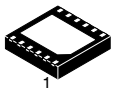
ORDERING INFORMATION

Device	Output	Package	Shipping†
NCV891234MW50R2G	5.0 V	DFN−12 With wettable flanks	3000 / Tape & Reel
NCV891234MW33R2G	3.3 V		
NCV891334MW50R2G	5.0 V		
NCV891334MW33R2G	3.3 V		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

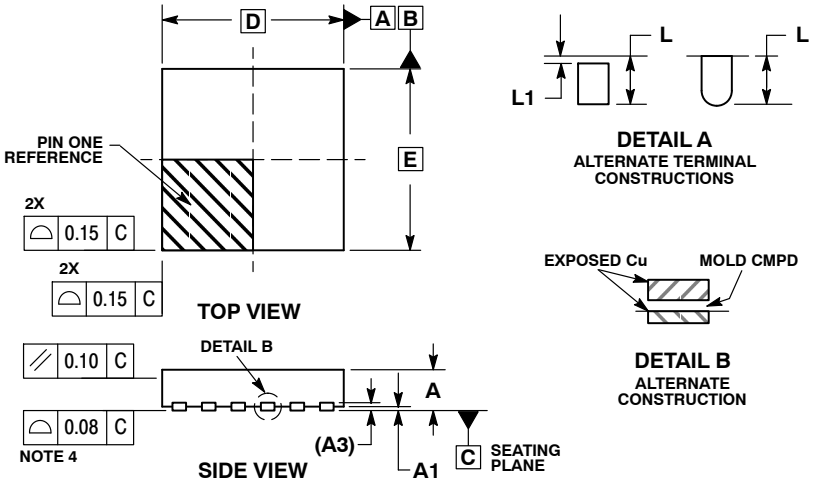
ON Semiconductor®



SCALE 2:1

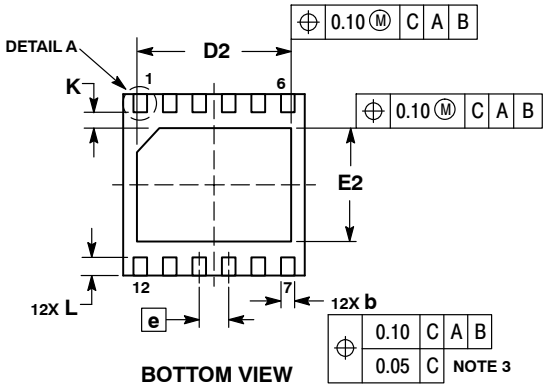
DFN12, 4x4, 0.65P
CASE 506CE
ISSUE O

DATE 23 FEB 2012

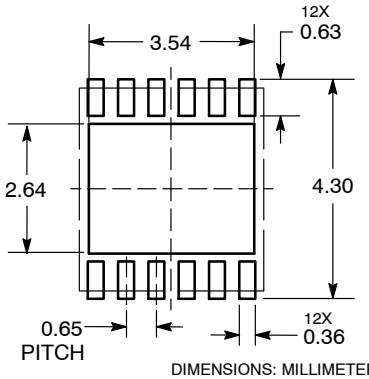


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	3.30	3.50
E	4.00 BSC	
E2	2.40	2.60
e	0.65 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



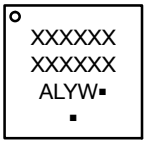
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX= Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**12 PIN DFN, 4X4, 0.65P**		**PAGE 1 OF 1**

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