

## Quad High-Voltage Amplifier Array

### Features

- Four Independent High-Voltage Amplifiers
- 215V Output Swing
- 9V/ $\mu$ s Typical Output Slew Rate
- 66.7V/V Fixed Gain
- High-Value Internal Feedback Resistors
- Very Low Operating Current

### Applications

- Tunable Laser
- Microelectromechanical Systems (MEMS) Driver
- Test Equipment
- Piezoelectric Transducer Driver
- Braille Driver

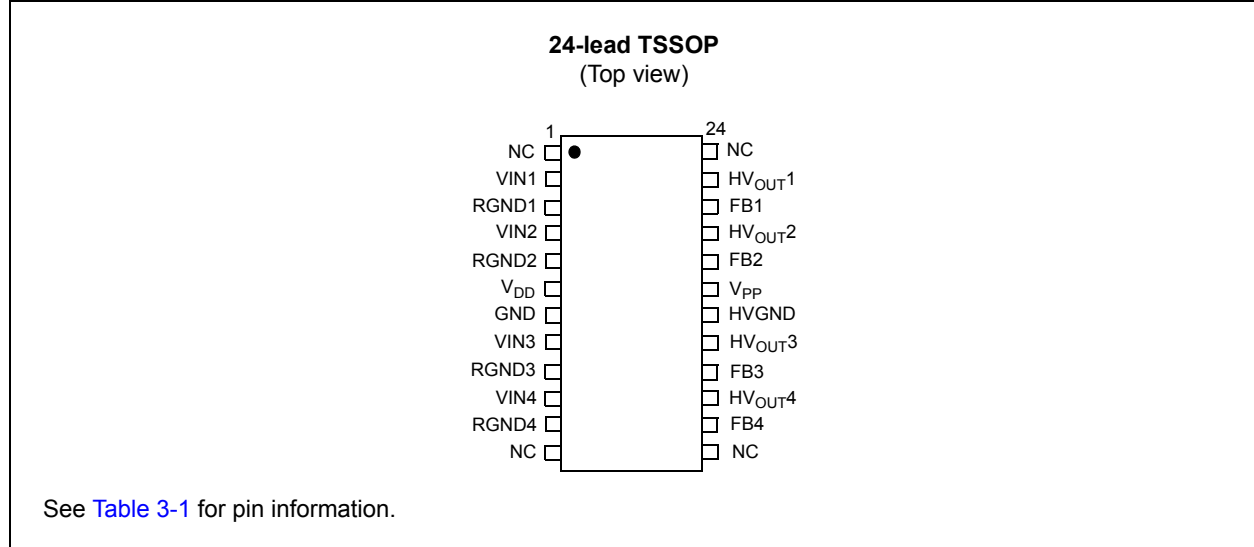
### General Description

The HV264 is a quad high-voltage amplifier array integrated circuit. It operates on a 225V high-voltage supply and a 5V low-voltage supply. Each channel has its own input and output.

When both  $V_{OUT}$  and FB pins are connected together and RGND is set at 0V, a non-inverting amplifier is formed with a closed-loop gain of 66.7V/V. High-value internal feedback resistors are used to minimize power dissipation. The input voltage  $V_{IN}$  is designed for a range of 0.05V to 3.22V. The output can swing from 1V to  $V_{PP}-10V$ . A 3.22V input will cause the output to swing to 215V.

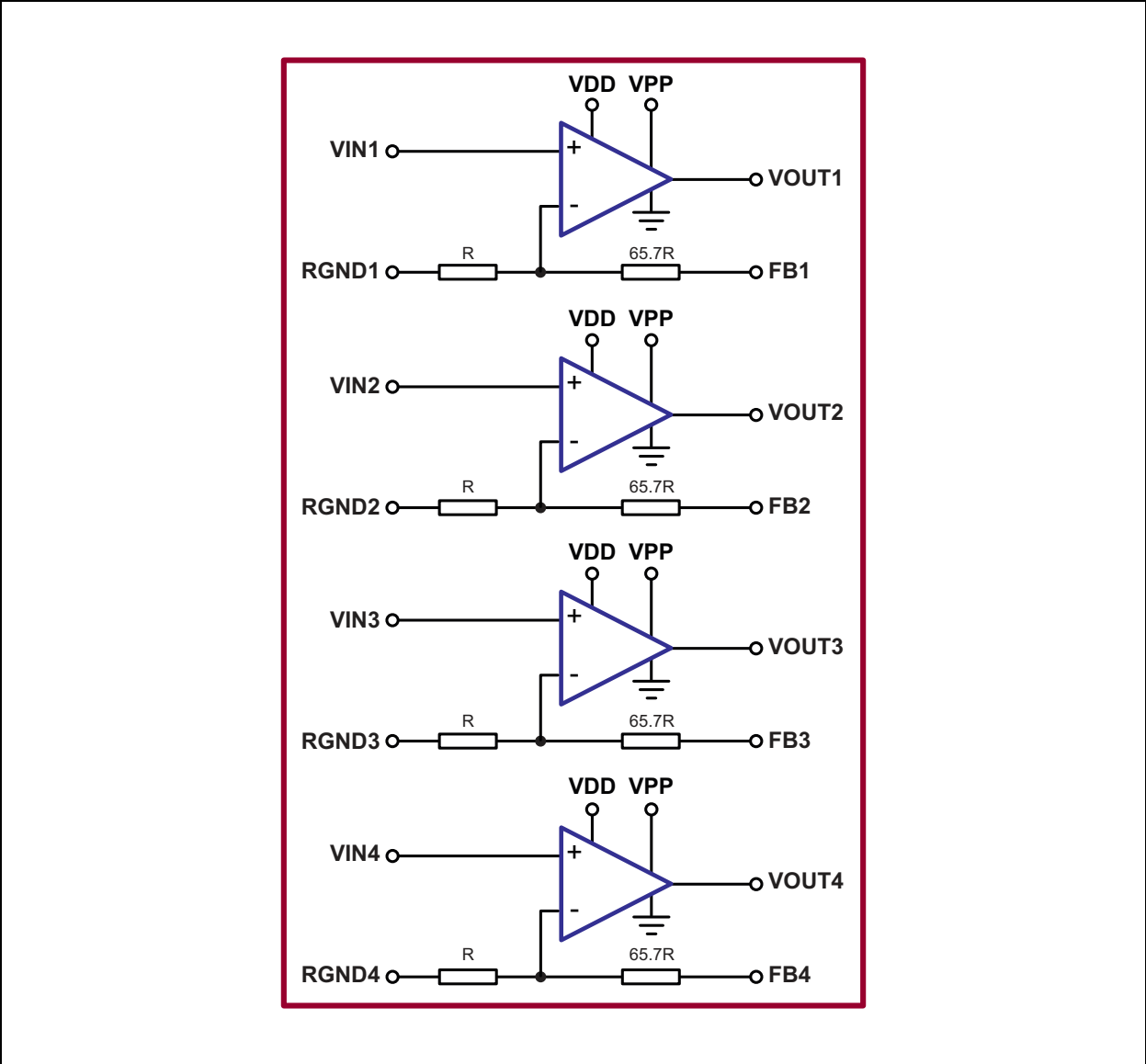
The HV264 is designed for maximum performance with minimal high-voltage current. The high-voltage current for each channel is less than 75  $\mu$ A. The typical output slew rate performance is 9V/ $\mu$ s.

### Package Type

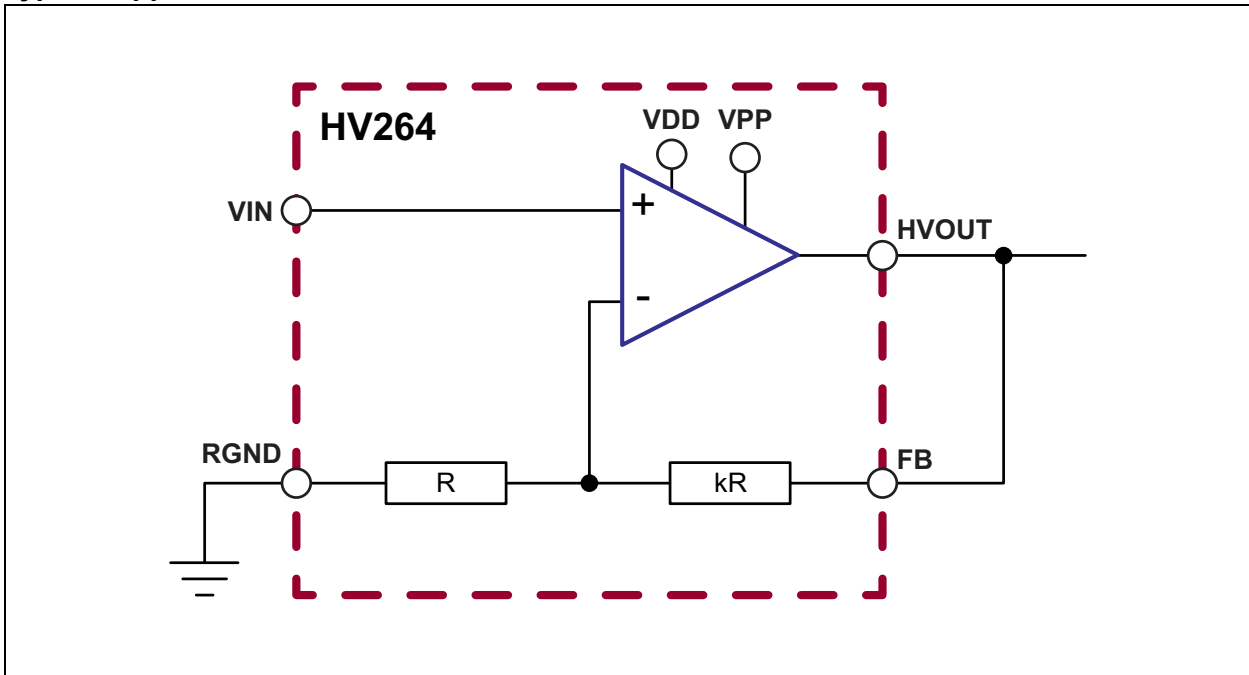


# HV264

## Functional Block Diagram



## Typical Application Circuit



# HV264

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

High-Voltage Supply, $V_{PP}$ .....	250V
Low-Voltage Supply, $V_{DD}$ .....	6.5V
Output Voltage, $HV_{OUT}$ .....	0V to $V_{PP}$
Analog Input Signal, $V_{IN}$ .....	0V to $V_{DD}$
Maximum Junction Temperature, $T_J$ .....	+150°C
Storage Temperature, $T_S$ .....	-65°C to +150°C
ESD Rating ( <b>Note 1</b> ) .....	ESD Sensitive

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:** Device is ESD sensitive. Handling precautions are recommended.

### RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
High-Voltage Positive Supply	$V_{PP}$	50	—	225	V	
Low-Voltage Positive Supply	$V_{DD}$	4.5	5	5.5	V	
Input Ground Range	$R_{GND}$	0	0	$V_{DD}$	V	
$V_{PP}$ Supply Current	$I_{PP}$	—	—	300	$\mu$ A	$V_{PP} = 200V$ , all inputs at 0V
$V_{DD}$ Supply Current	$I_{DD}$	—	—	5	mA	$V_{DD} = 5.5V$
Operating Ambient Temperature	$T_A$	-40	—	+125	°C	
Operating Junction Temperature	$T_J$	-40	—	+125	°C	

## DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating conditions unless otherwise noted, $T_J = +25^\circ\text{C}$ .						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
HV <sub>OUT</sub> Voltage Swing	HV <sub>OUT</sub>	1	—	V <sub>PP</sub> -10	V	No load
HV <sub>OUT</sub> Sink Current	I <sub>SINK</sub>	3	—	—	mA	
HV <sub>OUT</sub> Source Current	I <sub>SOURCE</sub>	3	—	—	mA	
Input Voltage Range	V <sub>IN</sub>	0	—	V <sub>DD</sub> -1.5	V	
V <sub>IN</sub> Input Current	I <sub>IN</sub>	—	—	50	nA	
HV <sub>OUT</sub> DC Offset	HV <sub>OS</sub>	—	—	±1	V	V <sub>IN</sub> = 0.2V

## AC ELECTRICAL CHARACTERISTICS

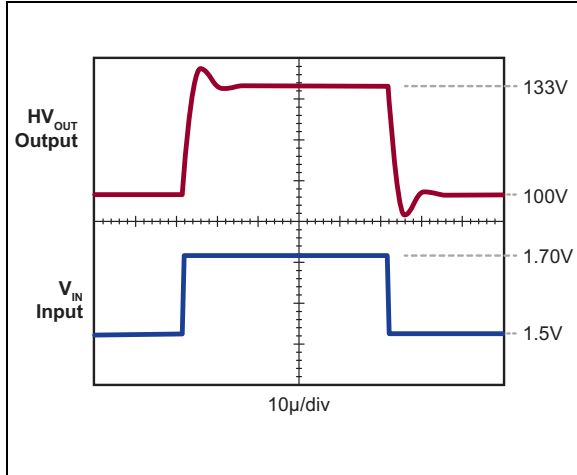
Electrical Specifications: Over operating conditions unless otherwise noted, $T_J = 25^\circ\text{C}$ .						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
HV <sub>OUT</sub> Slew Rate—Rising Edge	SR	5	9	30	V/μs	V <sub>PP</sub> = 200V, Load = 15 pF, measured between 10% to 90% of HV <sub>OUT</sub>
HV <sub>OUT</sub> Slew Rate—Falling Edge		—	9	—	V/μs	
Feedback Impedance, R <sub>f</sub> + R <sub>i</sub>	R <sub>FB</sub>	3.5	5.3	—	MΩ	
Closed-Loop Gain	A <sub>V</sub>	63.4	66.7	70	V/V	
HV <sub>OUT</sub> -3 dB Channel Bandwidth	BW	25	—	—	kHz	V <sub>PP</sub> = 200V, Load = 15 pF
HV <sub>OUT</sub> Capacitive Load	C <sub>LOAD</sub>	0	—	15	pF	
Output Referred Noise	V <sub>N</sub>	—	—	10	mV <sub>RMS</sub>	Measured at HV <sub>OUT</sub> , 0 kHz to 1 kHz single pole, V <sub>IN</sub> = 0.2V
V <sub>DD</sub> Power Supply Rejection Ratio	PSRR1	55	—	—	dB	V <sub>DD</sub> = 4.5V to 5.5V V <sub>PP</sub> = 200V, V <sub>IN</sub> = 0.1V
V <sub>PP</sub> Power Supply Rejection Ratio	PSRR2	60	—	—	dB	V <sub>DD</sub> = 5V, V <sub>PP</sub> = 50V to 200V, V <sub>IN</sub> = 0.1V
Crosstalk	Xtalk	—	—	-80	dB	Output referred

## TEMPERATURE SPECIFICATIONS

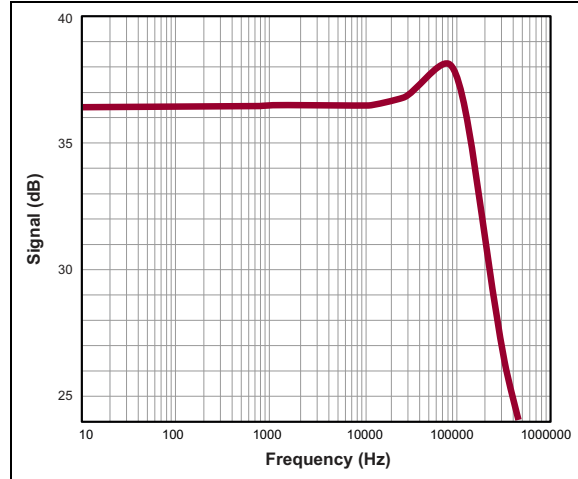
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>Temperature Range</b>						
Operating Ambient Temperature	T <sub>A</sub>	-40	—	+125	°C	
Operating Junction Temperature	T <sub>J</sub>	-40	—	+125	°C	
Storage Temperature	T <sub>S</sub>	-65	—	+150	°C	
<b>Package Thermal Resistance</b>						
24-lead TSSOP	θ <sub>JA</sub>	—	+72	—	°C/W	

## 2.0 TYPICAL PERFORMANCE CURVES

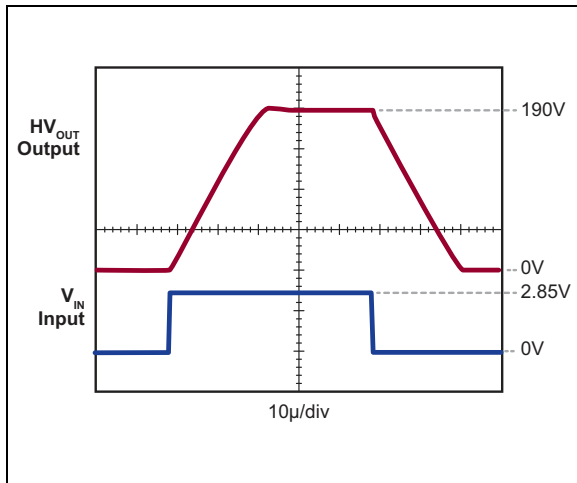
**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.



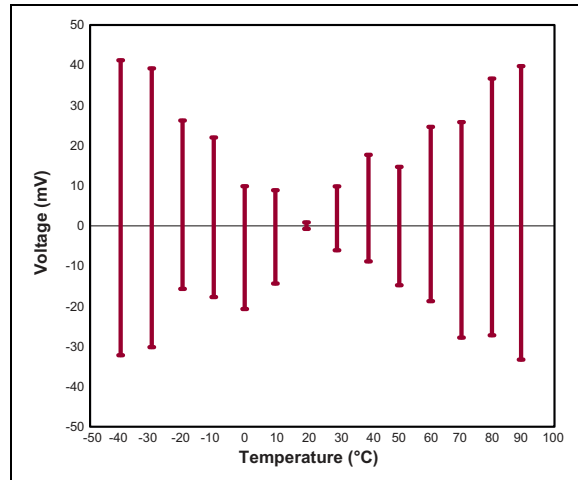
**FIGURE 2-1:** Typical Small-Signal Pulse Response.



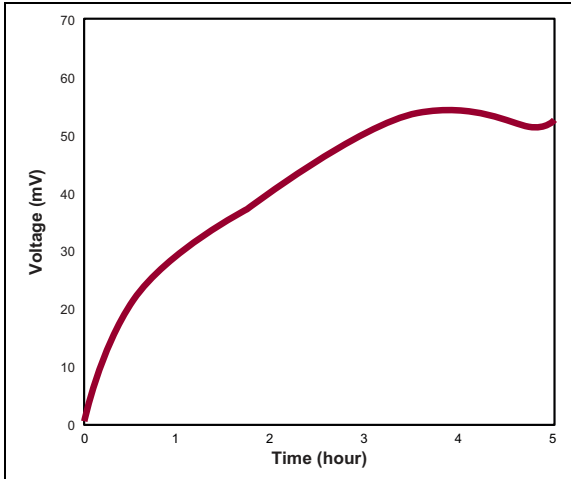
**FIGURE 2-3:** Typical Bode Plot of Small-Signal Gain ( $V_{IN} = 0.2 V_{P-P}$ ,  $V_{DC} = 1.5V$ ,  $V_{DD} = 5V$  and  $V_{PP} = 200V$ ).



**FIGURE 2-2:** Typical Large-Signal Pulse Response.



**FIGURE 2-4:** Distribution of Typical  $HV_{OUT}$  Deviation over Temperature ( $V_{IN} = 0.1 V_{DC}$ ,  $1.6 V_{DC}$ ,  $3.3 V_{DC}$ , in Reference to  $+20^{\circ}C$ ).



**FIGURE 2-5:** Typical  $HV_{OUT}$  Drift Over Time ( $V_{PP} = 200V$ ,  $V_{DD} = 5.5V$ ,  $V_{IN} = 0.2V$ , Room Temperature and 50 pF Output Loading).

## 3.0 PIN DESCRIPTION

The pin details are listed in [Table 3-1](#). Refer to [Section “Package Type”](#) for the location of the pins.

**TABLE 3-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	NC	No connection
2	VIN1	Amplifier Input 1
3	RGND1	Resistor ground for Channel 1. Typically grounded. Can be connected to a voltage source to create a DC offset.
4	VIN2	Amplifier Input 2
5	RGND2	Resistor ground for Channel 2. Typically grounded. Can be connected to a voltage source to create a DC offset.
6	V <sub>DD</sub>	Low-Voltage positive supply
7	GND	Device ground
8	VIN3	Amplifier Input 3
9	RGND3	Resistor ground for Channel 3. Typically grounded. Can be connected to a voltage source to create a DC offset.
10	VIN4	Amplifier Input 4
11	RGND4	Resistor ground for Channel 4. Typically grounded. Can be connected to a voltage source to create a DC offset.
12	NC	No connection
13	NC	No connection
14	FB4	Feedback Input 4
15	HVOUT4	Amplifier Output 4
16	FB3	Feedback Input 3
17	HVOUT3	Amplifier Output 3
18	HVGND	Device high-voltage supply ground
19	V <sub>PP</sub>	High-Voltage positive supply
20	FB2	Feedback Input 2
21	HVOUT2	Amplifier Output 2
22	FB1	Feedback Input 1
23	HVOUT1	Amplifier Output 1
24	NC	No connection



## 4.0 FUNCTIONAL DESCRIPTION

### 4.1 Power-Up/Power-Down Sequence

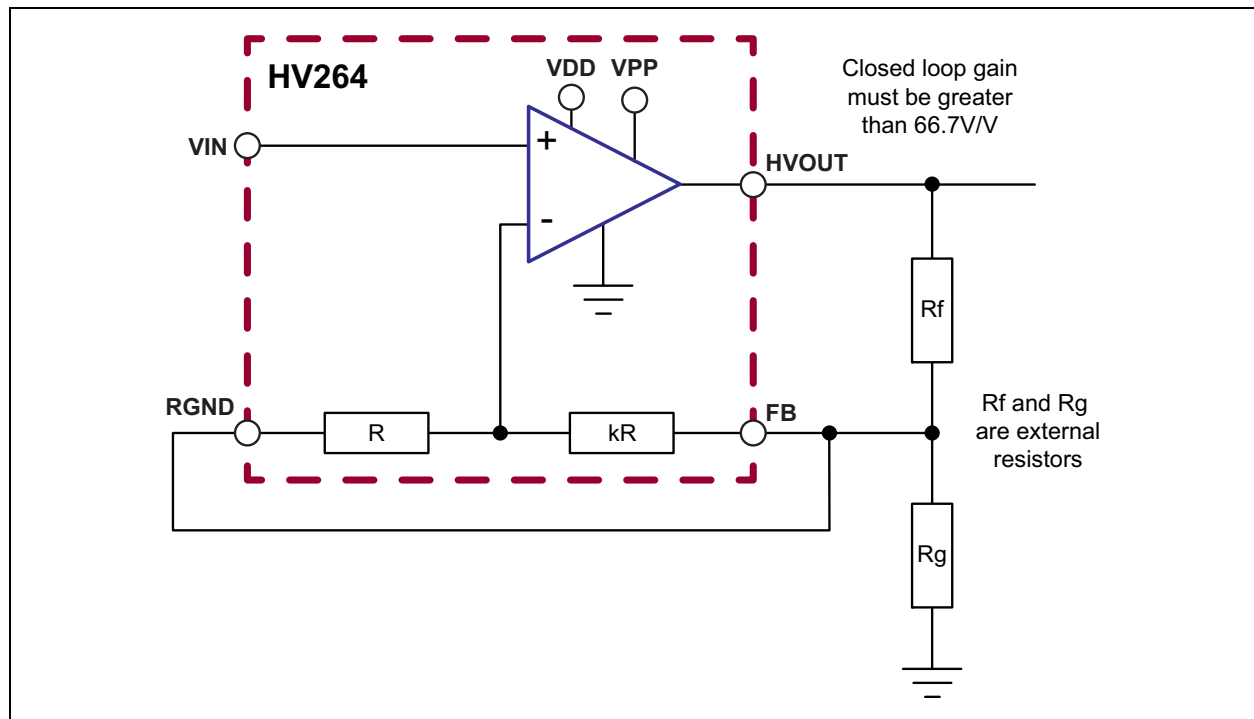
The device can be damaged due to an improper power-up/power-down sequence. To avoid this, please follow the acceptable power-up and power-down sequences in [Table 4-1](#) and [Table 4-2](#) and add an external diode across  $V_{PP}$  and  $V_{DD}$  where the anode of the diode is connected to  $V_{DD}$  and the cathode of the diode is connected to  $V_{PP}$ . Any low-current high-voltage diode such as a 1N4004 will be adequate.

**TABLE 4-1: ACCEPTABLE POWER-UP SEQUENCES**

Option 1		Option 2	
Step	Description	Step	Description
1	$V_{DD}$	1	$V_{DD}$
2	$V_{PP}$	2	Inputs
3	Inputs	3	$V_{PP}$

**TABLE 4-2: ACCEPTABLE POWER-DOWN SEQUENCES**

Option 1		Option 2	
Step	Description	Step	Description
1	Inputs	1	$V_{PP}$
2	$V_{PP}$	2	Inputs
3	$V_{DD}$	3	$V_{DD}$

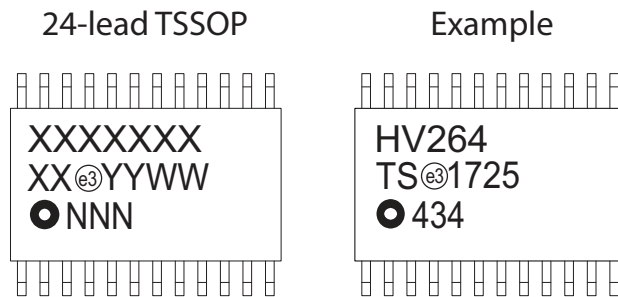


**FIGURE 4-1:** Application Circuit with External Gain Setting Resistors.

# HV264

## 5.0 PACKAGE MARKING INFORMATION

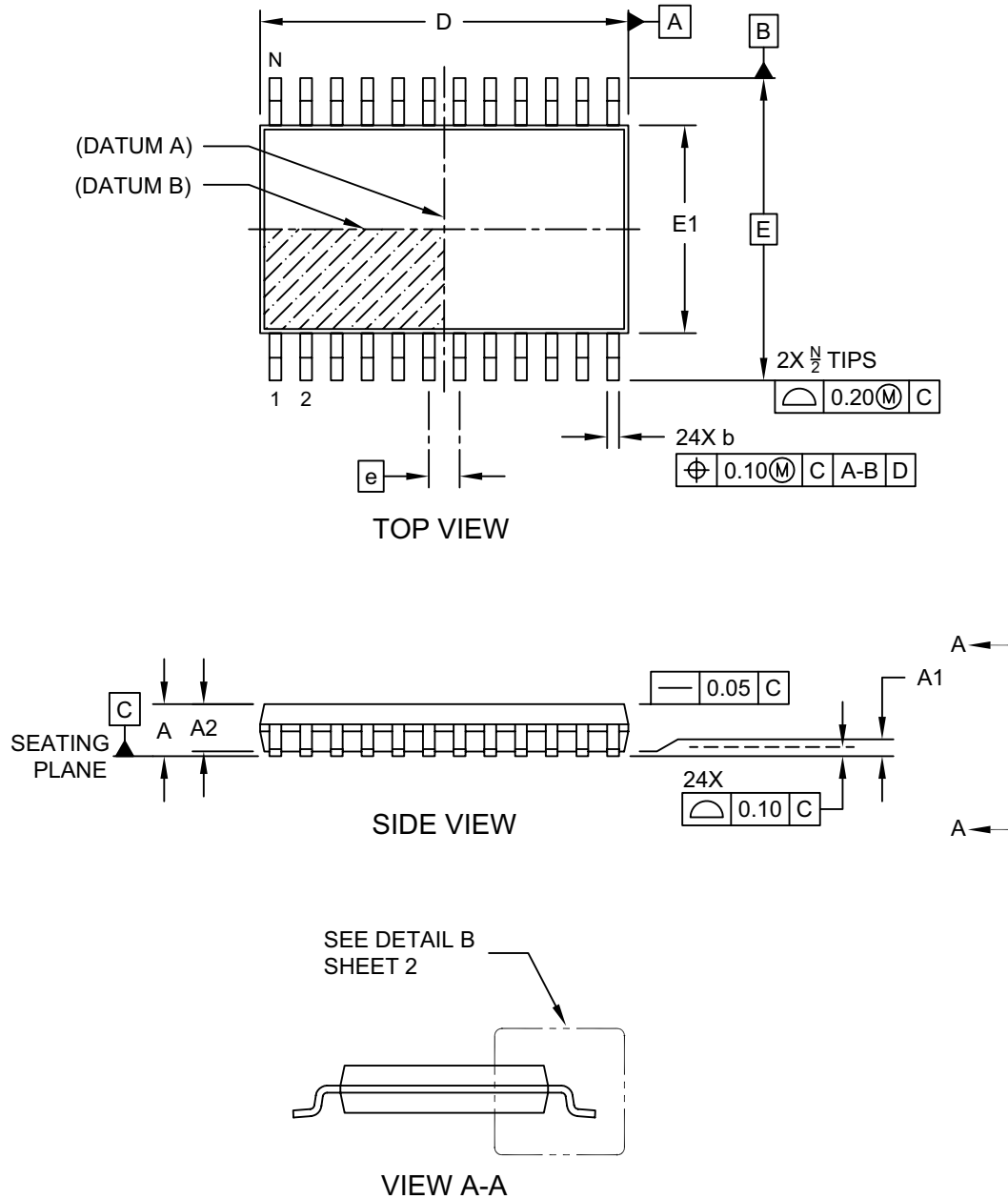
### 5.1 Packaging Information



<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	ⓔ3	Pb-free JEDEC <sup>®</sup> designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package.
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

## 24-Lead Thin Shrink Small Outline Package (QE) - 4.40 mm Body [TSSOP] Supertex Legacy & Micrel Legacy Package

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

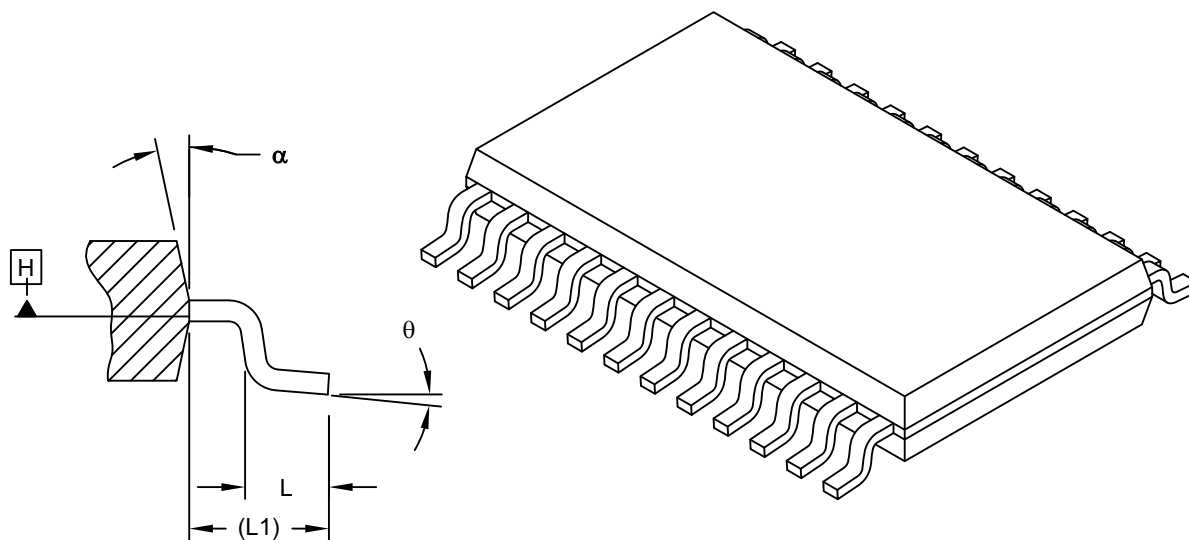


Microchip Technology Drawing C04-284A Sheet 1 of 2

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## 24-Lead Thin Shrink Small Outline Package (QE) - 4.40 mm Body [TSSOP] Supertex Legacy & Micrel Legacy Package

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



DETAIL B

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Leads	N	24		
Lead Pitch	e	0.65 BSC		
Overall Height	A	0.85	-	1.20
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	0.80	1.00	1.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	θ	0°	4°	8°
Overall Width	E	6.40 BSC		
Overall Length	D	7.70	7.80	7.90
Molded Package Width	E1	4.30	4.40	4.50
Lead Width	b	0.19	-	0.30
Mold Draft Angle Top	α	12° REF		

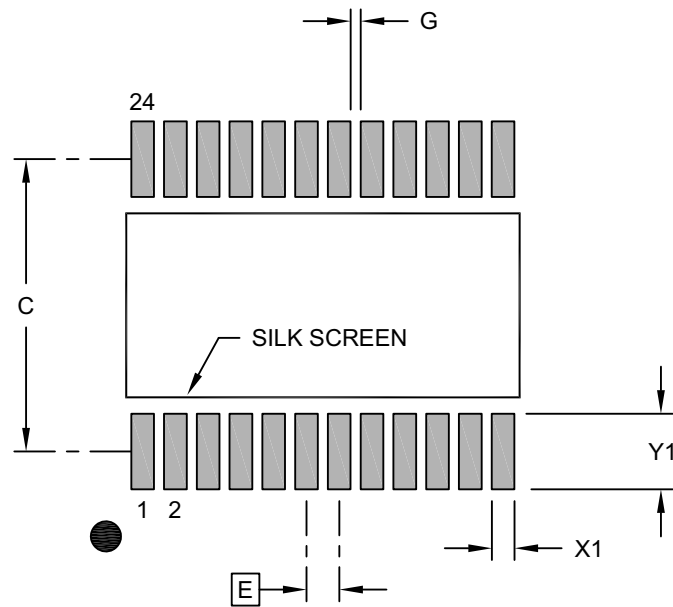
**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-284A Sheet 2 of 2

## 24-Lead Thin Shrink Small Outline Package (QE) - 4.40 mm Body [TSSOP] Supertex Legacy & Micrel Legacy Package

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.80	
Contact Pad Width (X24)	X1			0.45
Contact Pad Length (X24)	Y1			1.50
Contact Pad to Center Pad (X20)	G1	0.20		

**Notes:**

- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2284A

# HV264

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NOTES:

## APPENDIX A: REVISION HISTORY

### Revision B (February 2019)

- Updated [Section “Features”](#)
- Updated [Section “General Description”](#)
- Updated [Section 1.0 “Electrical Characteristics”](#)
- Updated [Section 5.0 “Package Marking Information”](#)
- Minor typographical edits

### Revision A (August 2017)

- Converted Supertex Doc# DSFP-HV264 to Microchip DS20005832B
- Changed the part marking format
- Made minor text changes throughout the document

# HV264

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NOTES:



## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
<b>Device:</b>	HV264	=	Quad High-Voltage Amplifier Array		
<b>Package:</b>	TS	=	24-lead TSSOP		
<b>Environmental:</b>	G	=	Lead (Pb)-free/RoHS-compliant Package		
<b>Media Type:</b>	(blank)	=	2500/Reel for a TS Package		

**Example:**

a) HV264TS-G: Quad High-Voltage Amplifier Array, 24-lead TSSOP, 2500/Reel

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NOTES:

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