

BGT24LTR11N16

Silicon Germanium 24GHz Radar  
Transceiver MMIC

Data Sheet

Revision: 1.3

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**Data Sheet**

**Revision History: 2018-05-08**

**Previous Revision: Datasheet Rev. 1.1**

<b>Page</b>	<b>Subjects (major changes since last revision)</b>
8,9	Reference to matching structures and footprint according to AN472
8	Specification of Harmonic Suppression is limited to second harmonic only
8	Note is added to TX_ON low /high level input voltage specification

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Last Trademarks Update 2011-02-24

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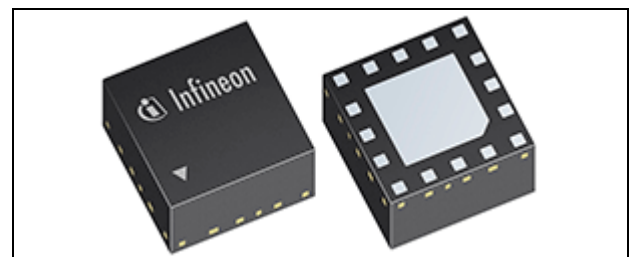
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# 1 Introduction



## 1.1 Features

- 24GHz transceiver MMIC
- Fully integrated low phase noise VCO
- Built in temperature compensation circuit for VCO stabilization
- Homodyne quadrature receiver
- Frequency divider
- Low power consumption
- Fully ESD protected device
- Single ended RF and IF terminals
- 200 GHz bipolar SiGe:C technology b7hf200
- Single supply voltage 3.3V
- TSNP-16-9 plastic package
- Pb-free (RoHS compliant) package



**Figure 1** BGT24LTR11N16 in TSNP-16-9

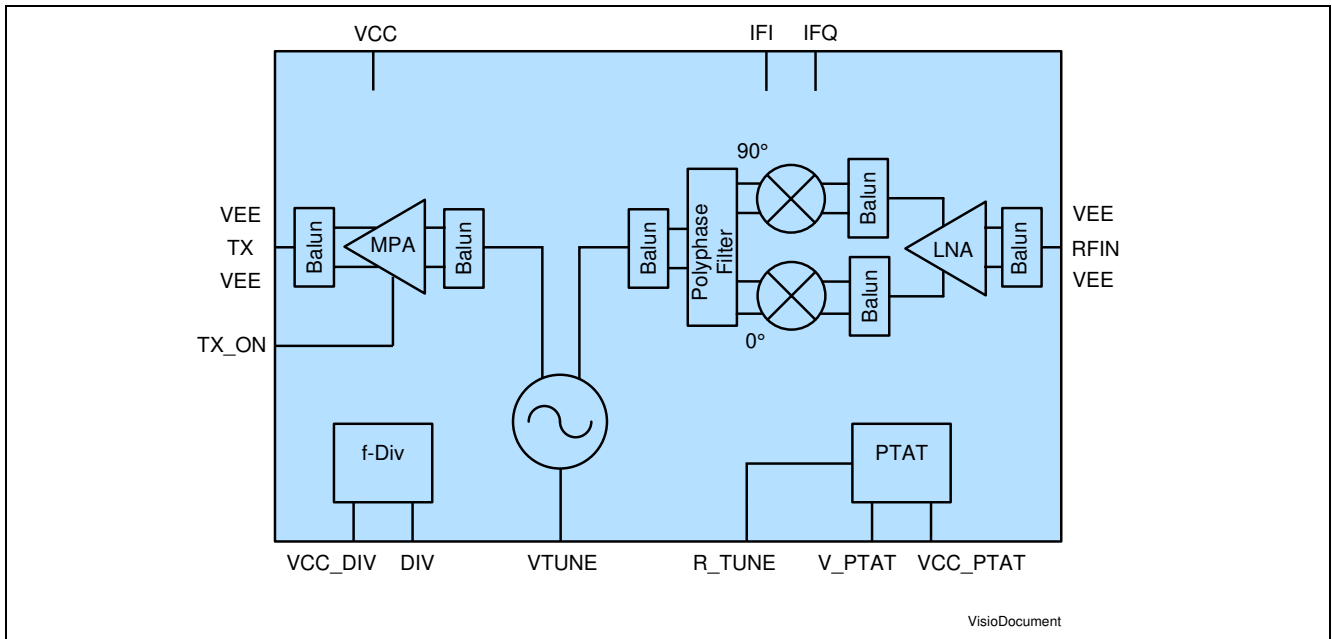
### Description

The BGT24LTR11 is a Silicon Germanium Transceiver MMIC operating from 24.0 GHz up to 24.25 GHz. It is based on a 24 GHz fundamental voltage controlled oscillator (VCO). A built in voltage source delivers a VCO tuning voltage ( $V_{PTAT}$ ) which is proportional to absolute temperature. When connected to the VCO tuning pin ( $V_{TUNE}$ ) it compensates for the inherent frequency drift of the VCO over temperature thus stabilizing the VCO within the ISM band eliminating the need for a PLL/Microcontroller. An integrated 1:16 frequency divider also allows for external phase lock loop VCO frequency stabilization.

The receiver section uses a low noise amplifier (LNA) in front of a quadrature homodyne down conversion mixer in order to provide excellent receiver sensitivity. Derived from the internal VCO signal, a RC polyphase filter (PPF) generates quadrature LO signals for the quadrature mixer. The I/Q IF outputs are available through a single ended terminal respectively.

The device is manufactured in a 0.18 $\mu$ m SiGe:C technology offering a cutoff frequency of 200 GHz. It is packaged in a 16 pin leadless RoHS compliant TSNP package.

Product Name	Package	Chip	Marking
BGT24LTR11N16	TSNP-16-9	T1811	LTR11



**Figure 2 BGT24LTR11N16 block diagram**

## 2 Electrical Characteristics

### 2.1 Absolute Maximum Ratings

Table 1 Absolute maximum ratings:  $T_A = -40\text{ °C} \dots 85\text{ °C}$ ; all voltages with respect to ground

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{CC}$	-0.3		3.6	V	
Supply voltage divider	$V_{CC\_DIV}$	-0.3		3.6	V	
Supply voltage PTAT voltage source	$V_{CC\_PTAT}$	-0.3		3.6	V	
DC voltage at RF pins	$V_{DC\_RF}$			0		MMIC provides short circuit to GND for RF_IN and TX_OUT
Voltage applied to none-RF I/O pins	$V_{DC\_I/O}$	-0.3		$V_{CC} + 0.3$	V	
Total power dissipation	$P$			300	mW	
Ambient temperature range	$T_A$	-40		85	°C	
Storage temperature range	$T_{STG}$	-50		125	°C	

**Attention: Stresses exceeding the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.**

### 2.2 ESD Integrity

Table 2 ESD integrity

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
ESD robustness HBM <sup>1</sup>	$V_{ESD-HBM}$	-1		1	kV	
ESD robustness CDM <sup>2</sup>	$V_{ESD-CDM}$	-500		500	V	

1) According to ANSI/ESDA/JEDEC JS-001 (R = 1.5kOhm, C = 100pF) for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM)-Component Level

2) According to JEDEC JESD22-C101 Field-Induced Charged Device Model (CDM), Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

Please note that this result is subject to:

- lot variations within the manufacturing process as specified by Infineon
- changes in the specific test setup

### 2.3 Power Supply

Table 3 Power supply characteristics:  $T_A = -40\text{ °C} \dots 85\text{ °C}$

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{CC}$	3.2	3.3	3.4	V	

**Table 3 Power supply characteristics:  $T_A = -40\text{ °C} \dots 85\text{ °C}$** 

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Supply current	$I_{CC}$		45	55	mA	
Duty cycle		1 : 1000		1		
Pulse duration	$t_P$	1			$\mu\text{s}$	

## 2.4 TX Section

**Table 4 TX characteristics:  $T_A = -40\text{ °C} \dots 85\text{ °C}$ ; all parameters specified including a TX port matching structure and package footprint provided by Infineon in AN472**

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
VCO frequency range	$f_{VCO}$	24.050		24.250	GHz	$V_{PTAT}$ connected to VTUNE; 16 kOhm resistor connected from R_TUNE to GND
VCO phase noise	$P_N$			-55 -80	dBc/ Hz	@ 10 kHz offset @ 100 kHz offset
VCO AM noise	$P_{AM}$			-135	dBc/ Hz	@ 100 kHz offset
Tuning voltage to cover VCO frequency range	$VTUNE$	0.7		2.5	V	
VCO tuning sensitivity within VCO frequency range			720	2000	MHz/V	
Second Harmonic Suppression		25			dBc	
Non-harmonic suppression		62			dBc	$f > 10\text{ GHz}$ ; $D_{DIV} = 16$
Non-harmonic suppression		45			dBc	$f \leq 10\text{ GHz}$ ; $D_{DIV} = 16$
TX output power	$P_{TX}$	2	6	10	dBm	
TX load impedance	$Z_{TXOUT}$		50		$\Omega$	Including TX port matching structure according to AN472
TX_ON low level input voltage (TX=OFF)	$V_{TX\_ON\_low}$			0.8	V	TX_ON pin is chip internally pulled up to $V_{CC}$ via typ. 98 kOhm resistor
TX_ON high level input voltage (TX=ON)	$V_{TX\_ON\_high}$	2			V	TX_ON pin is chip internally pulled up to $V_{CC}$ via typ. 98 kOhm resistor
TX_ON input voltage hysteresis	$V_{TX\_ON\_hys}$	50			mV	
TX_ON input current	$I_{TX\_ON}$	-100		100	$\mu\text{A}$	
TX_ON switching time	$t_{TX\_ON}$			2	ns	
Power up TX settling time	$t_{TX\_Power\_up}$			100ns		Defines the time TX section requires to settle after VCC supply voltage is within specified range



## 2.5 RX Section (Measured with TX\_ON=0V)

**Table 5** RX characteristics:  $T_A = -40\text{ °C} \dots 85\text{ °C}$ ; all parameters specified including RX port matching structure and package footprint provided by Infineon in AN472

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
RX frequency range	$f_{RX}$	24.0		24.25	GHz	
RX input impedance	$Z_{RXIN}$		50		$\Omega$	Including RX port matching structure according to AN472
Voltage conversion gain	$G_C$	15.5	20	26.5	dB	
SSB noise figure	$NF_{SSB}$		10	18	dB	Single sideband @ $f_{IF} = 100\text{ kHz}$
Input compression point	$IP_{1dB}$	-28			dBm	
Quadrat. phase imbalance	$\varepsilon_P$	0		24	deg	
Quadrat. amplitude imbalance	$\varepsilon_A$	-1		1	dB	
IF output impedance	$Z_{IF}$			1	k $\Omega$	Single ended

## 2.6 Frequency Divider

**Table 6** Frequency divider characteristics:  $T_A = -40\text{ °C} \dots 85\text{ °C}$

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Prescaler division ratio	$D_{DIV}$	16		8192	-	16 if $V_{CC\_PTAT} = 0\text{ V}$ , 8192 if $V_{CC\_PTAT} = 3.3\text{ V}$
Prescaler output voltage for division ratio 16	$V_{DIV16}$	60	120	350	mV	Peak to Peak voltage when DIV_OUT is terminated with 50 Ohm and $D_{DIV}=16$
Prescaler output "high" voltage for division ratio 8192	$V_{DIV8192H}$	2.4			V	DIV_OUT is loaded with 1M $\Omega$ , 13 pF
Prescaler output "low" voltage for division ratio 8192	$V_{DIV8192L}$			0.8	V	DIV_OUT is loaded with 1M $\Omega$ , 13 pF
Prescaler supply voltage	$V_{CC\_DIV}$	3.2	3.3	3.4	V	
Prescaler supply current	$I_{CC\_DIV}$	13	19	25	mA	

## 2.7 Proportional to absolute temperature (PTAT) voltage source

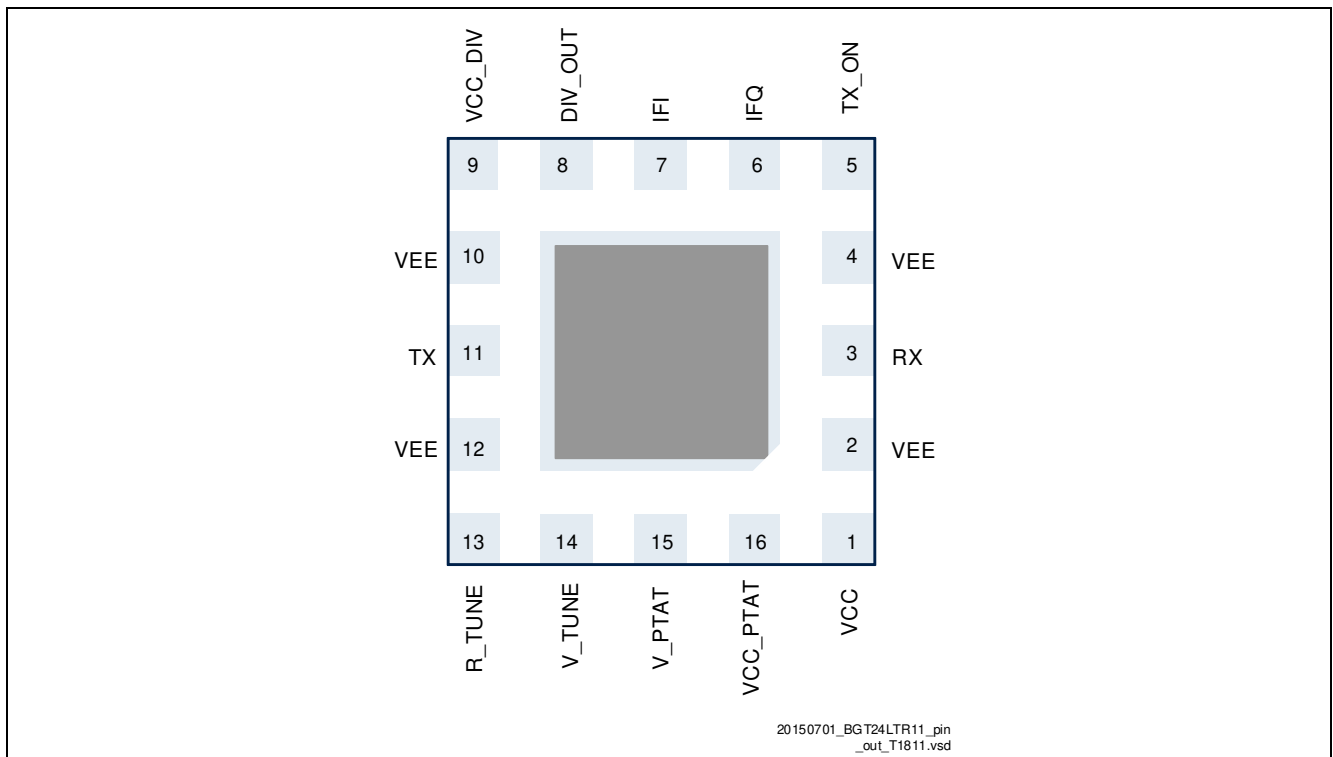
**Table 7** PTAT voltage source characteristics:  $T_A = -40\text{ °C} \dots 85\text{ °C}$

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Supply voltage	$V_{CC\_PTAT}$	3.2	3.3	3.4	V	
Supply current	$I_{CC\_PTAT}$		1.5	2.5	mA	

**Table 7** PTAT voltage source characteristics:  $T_A = -40\text{ °C} \dots 85\text{ °C}$

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Output voltage	$V_{OUT\_PTAT}$	0.7	1.3	2	V	

### 3 Pin description



**Figure 3** Pin-out (top view)

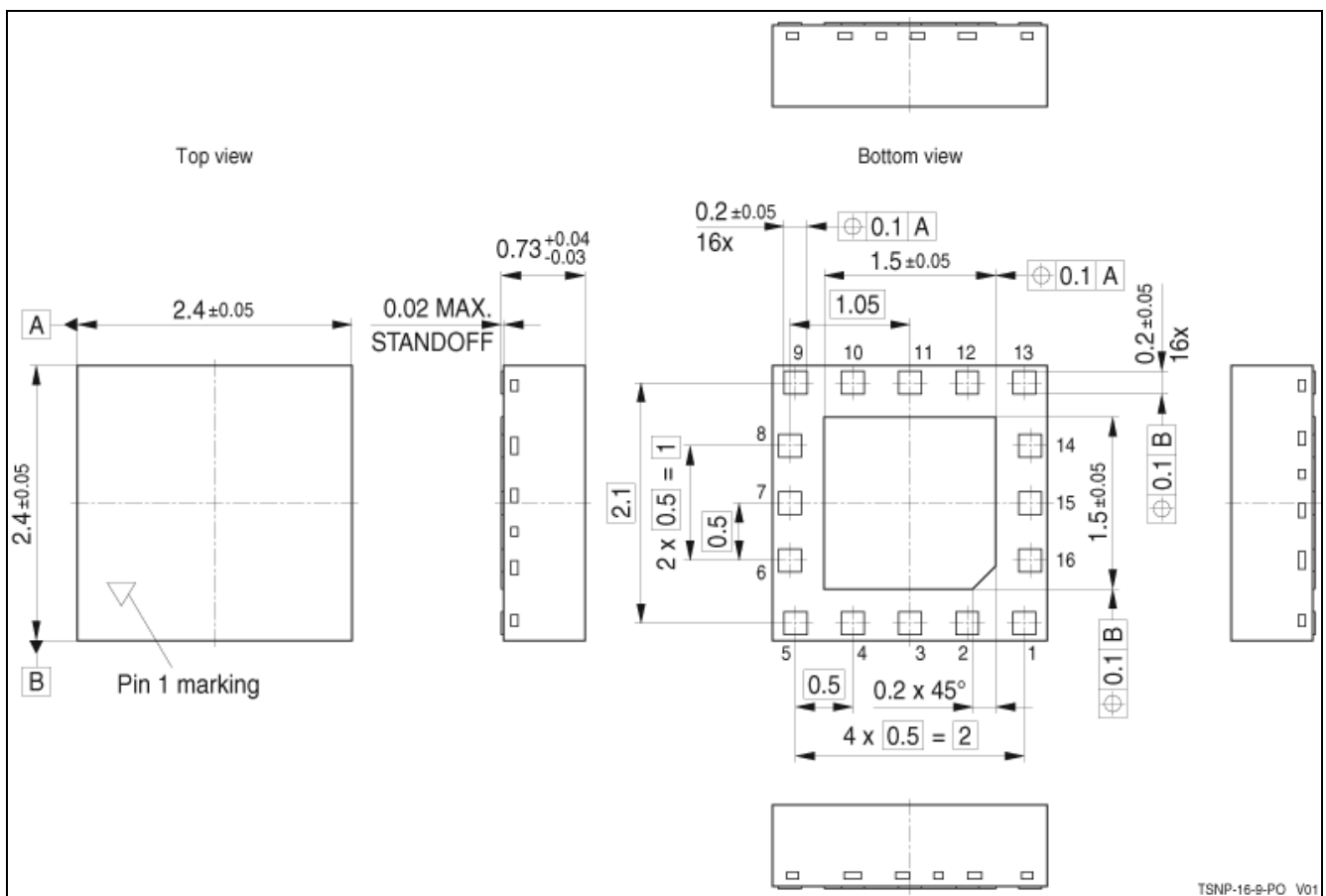
**Table 8** Pin definition and function

Pin Number	Name	Function
1	VCC	Supply voltage
2	VEE	Ground
3	RX	Receiver RF input
4	VEE	GND
5	TX_EN	Output power enable
6	IFQ	Quadrature phase down converter IF output
7	IFI	In phase down converter IF output
8	DIV_OUT	Frequency divider output
9	VCC_DIV	Supply voltage of prescaler
10	VEE	Ground
11	TX	Tranmitter RF output
12	VEE	Ground

**Table 8 Pin definition and function**

Pin Number	Name	Function
13	R_TUNE	VCO operating frequency band select
14	V_TUNE	VCO frequency tuning input
15	V_PTAT	PTAT voltage source output
16	VCC_PTAT	PTAT voltage source power supply

## 4 Physical Dimension



**Figure 4 Package Outline (top, side and bottom view) of TSNP-16-9**

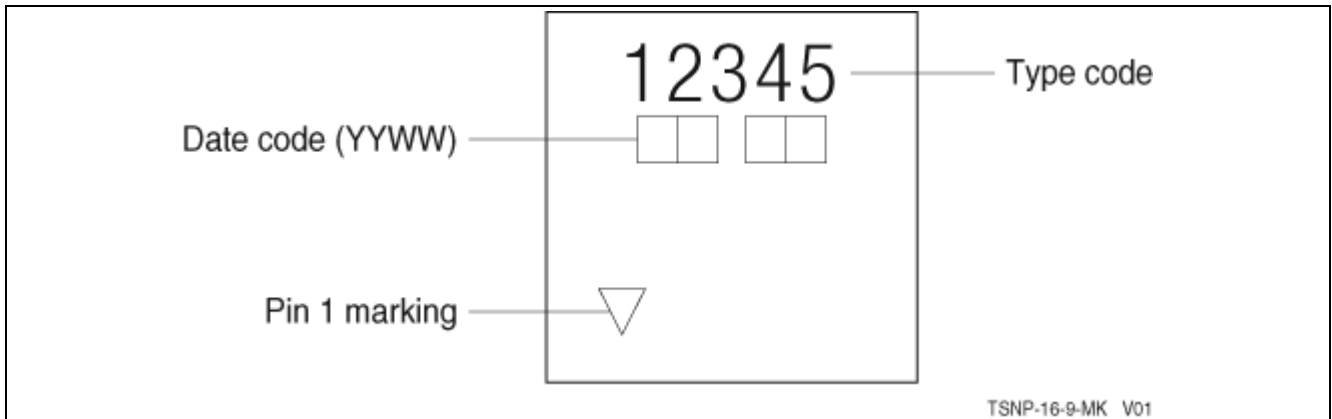


Figure 5 Marking Layout of TSNP-16-9 (example)

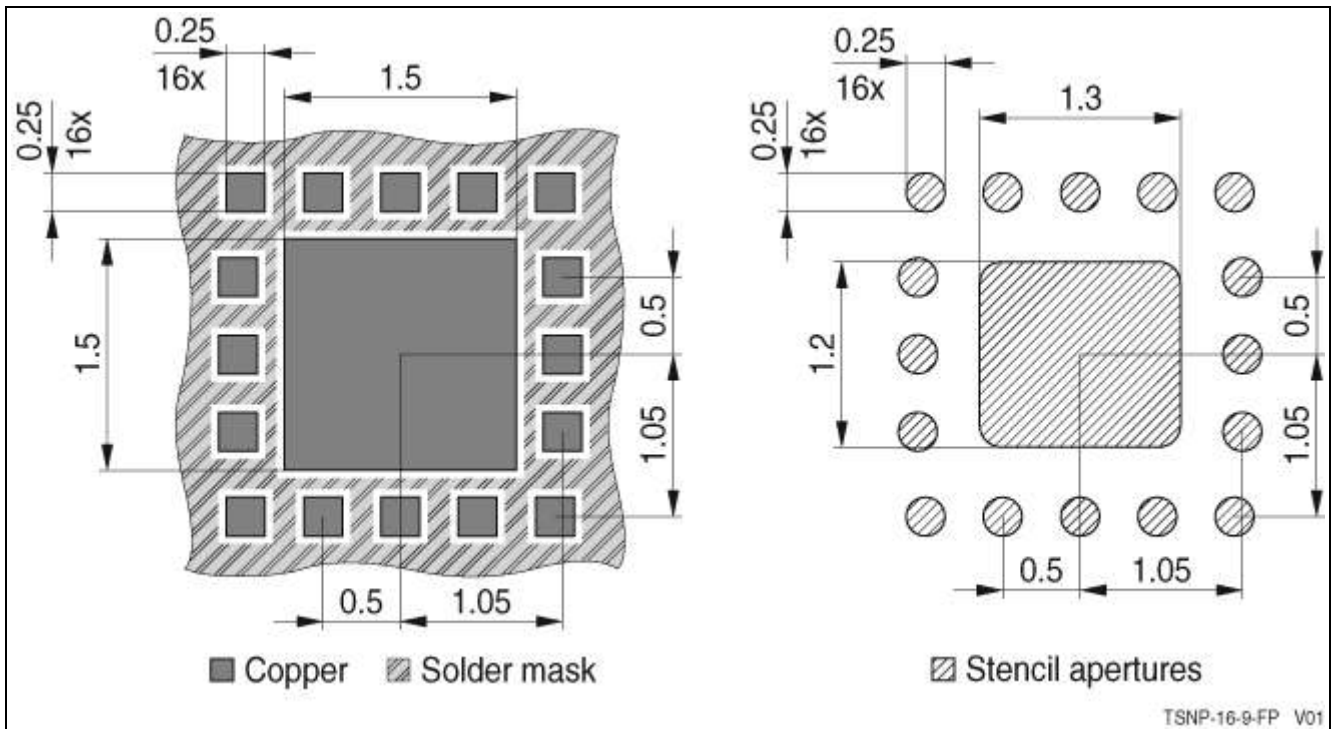
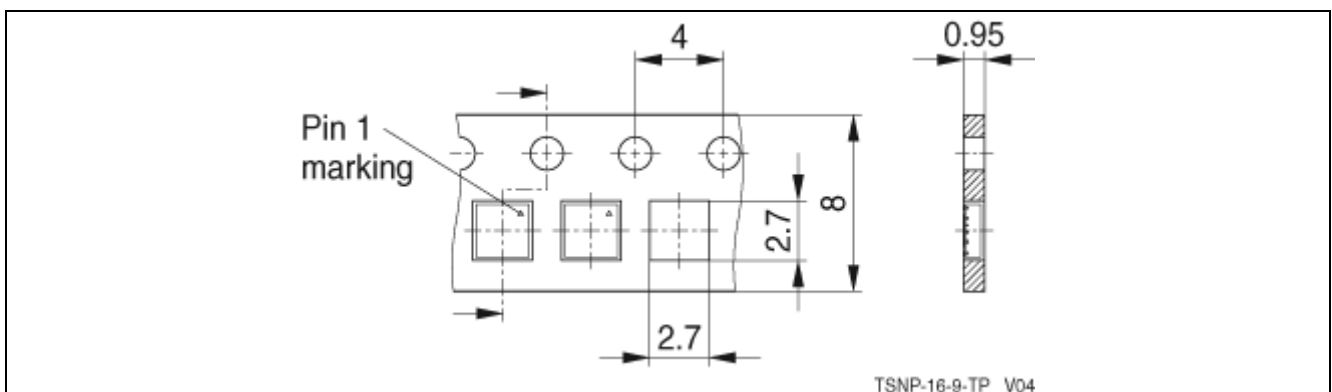


Figure 6 Soldering Footprint of TSNP-16-9



**Figure 7    Packing Description of TSNP-16-9; Ø Reel: 180 mm, Pieces / Reel: 3000, Reels / Box: 1**

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