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# MOSFET - Power, Single N-Channel, Shielded Gate, PowerTrench®

150 V, 31 mΩ, 27 A



ON Semiconductor®

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## NTTFS034N15MC

### Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Capable of 175°C Tj Max Rating

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

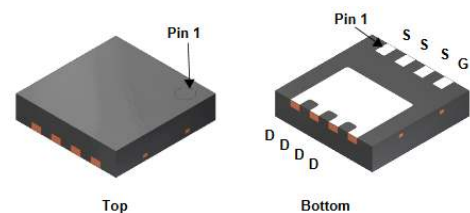
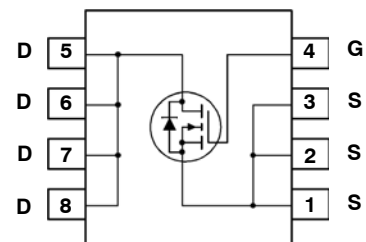
Parameter	Symbol	Value	Unit		
Drain-to-Source Voltage	V <sub>DSS</sub>	150	V		
Gate-to-Source Voltage	V <sub>GS</sub>	±20	V		
Continuous Drain Current R <sub>θJC</sub> (Note 5)	Steady State	T <sub>C</sub> = 25°C	I <sub>D</sub>	27	A
		T <sub>C</sub> = 25°C	P <sub>D</sub>	53.6	W
		T <sub>A</sub> = 25°C	I <sub>D</sub>	6.2	A
		T <sub>A</sub> = 25°C	P <sub>D</sub>	2.8	W
		T <sub>A</sub> = 25°C	P <sub>D</sub>	1.2	W
Pulsed Drain Current (Note 3)	T <sub>C</sub> = 25°C	I <sub>DM</sub>	110	A	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C		
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L(pk)</sub> = 6 A) (Note 4)	E <sub>AS</sub>	54	mJ		
Maximum Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T <sub>L</sub>	260	°C		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on a FR-4 board using 1 in<sup>2</sup> pad of 2 oz copper.
2. Surface mounted on a FR-4 board using the minimum recommended pad of 2 oz copper.
3. Pulsed ID please refer to Figure 12 SOA graph for more details
4. E<sub>AS</sub> of 54 mJ is based on starting T<sub>J</sub> = 25°C; L = 3 mH, I<sub>AS</sub> = 6 A, V<sub>DD</sub> = 150 V, V<sub>GS</sub> = 10 V.
5. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

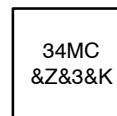
V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX
150 V	31 mΩ @ 10 V	27 A

### N-CHANNEL MOSFET



WDFN8  
CASE 483AW

### MARKING DIAGRAM



34MC = Specific Device Code  
&Z = Assembly Location  
&3 = 3-Digit Date Code  
&K = Lot Traceability

### ORDERING INFORMATION

Device	Package	Shipping†
NTTFS034N15MC	WDFN8 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTTFS034N15MC

## THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-to-Case – Steady State (Note 5)	$R_{\theta JC}$	2.8	$^{\circ}C/W$
Thermal Resistance Junction-to-Ambient – Steady State (Notes 1, 5)	$R_{\theta JA}$	53	$^{\circ}C/W$
Thermal Resistance Junction-to-Ambient – Steady State (Notes 2, 5)	$R_{\theta JA}$	125	$^{\circ}C/W$

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 V, I_D = 250 \mu A$	150			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250 \mu A$ , referenced to $25^{\circ}C$		77		$mV/^{\circ}C$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0 V, V_{DS} = 120 V, T_J = 25^{\circ}C$			1	$\mu A$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20 V, V_{DS} = 0 V$			$\pm 100$	nA

### ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 70 \mu A$	2.5		4.5	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 70 \mu A$ , referenced to $25^{\circ}C$		-8.1		$mV/^{\circ}C$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10 V, I_D = 13 A$		26	31	$m\Omega$
		$V_{GS} = 8 V, I_D = 6 A$		28.3	36.3	$m\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 10 V, I_D = 13 A$		29		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0 V, f = 1 MHz$ $V_{DS} = 75 V$		905		pF
Output Capacitance	$C_{OSS}$			270		
Reverse Transfer Capacitance	$C_{RSS}$			5		
Gate-Resistance	$R_G$			0.6	1.2	$\Omega$
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10 V, V_{DS} = 75 V, I_D = 13 A$		12		nC
Threshold Gate Charge	$Q_{G(TH)}$			3.1		
Gate-to-Source Charge	$Q_{GS}$			4.8		
Gate-to-Drain Charge	$Q_{GD}$			1.8		
Plateau Voltage	$V_{GP}$			5.4		
Output Charge	$Q_{OSS}$	$V_{GS} = 0 V, V_{DD} = 75 V$		32		nC

### RESISTIVE SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10 V, V_{DS} = 75 V,$ $I_D = 13 A, R_G = 6 \Omega$		12		ns
Rise Time	$t_r$			2.2		
Turn-Off Delay Time	$t_{d(off)}$			14		
Fall Time	$t_f$			2.5		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0 V, I_S = 13 A, T_J = 25^{\circ}C$		0.87	1.2	V
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0 V, V_{DD} = 75 V$ $di_S/dt = 300 A/\mu s, I_S = 13 A$		41		ns
Reverse Recovery Charge	$Q_{RR}$			126		nC
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0 V, V_{DD} = 75 V$ $di_S/dt = 1000 A/\mu s, I_S = 13 A$		22		ns
Reverse Recovery Charge	$Q_{RR}$			164		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Switching characteristics are independent of operating junction temperature

TYPICAL CHARACTERISTICS

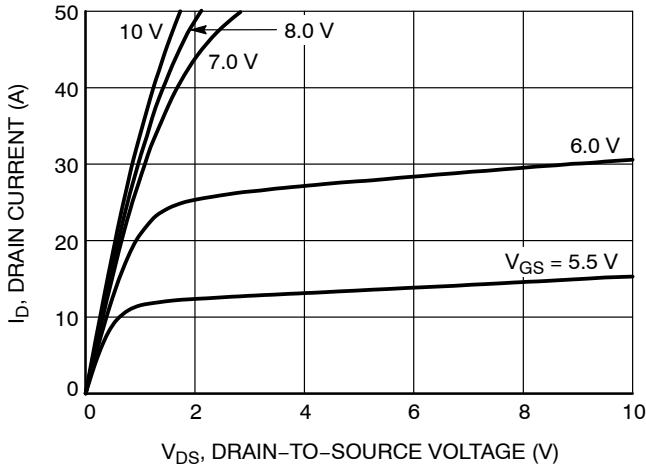


Figure 1. On-Region Characteristics

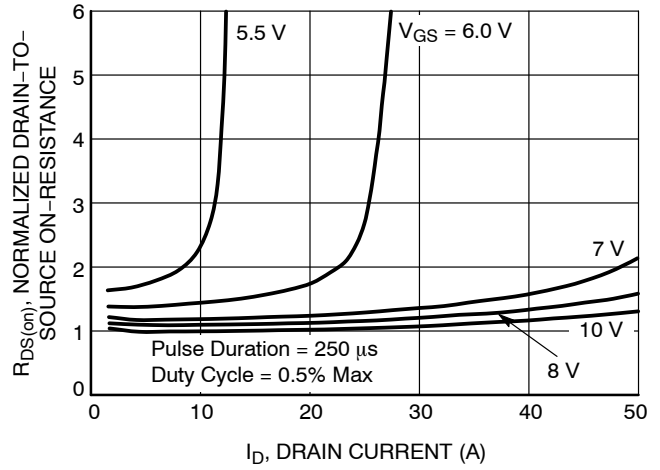


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

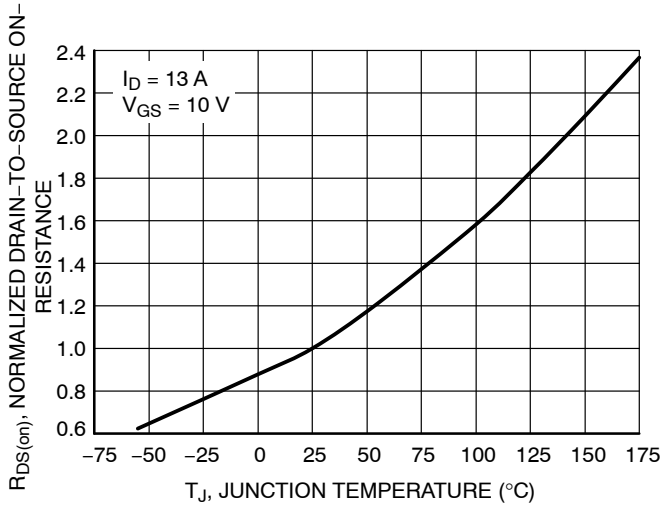


Figure 3. Normalized On-Resistance vs. Junction Temperature

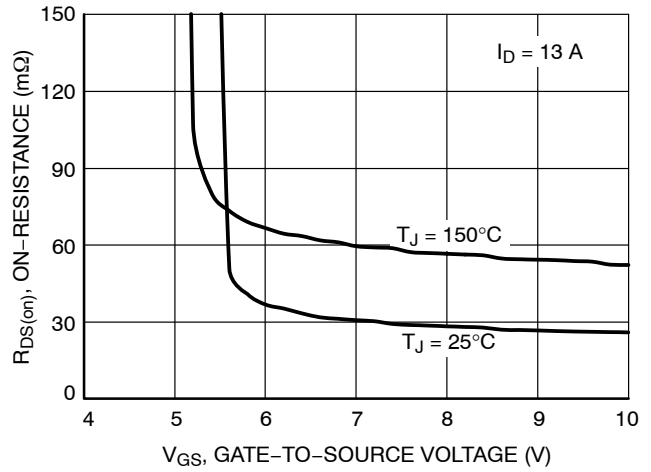


Figure 4. On-Resistance vs. Gate-to-Source Voltage

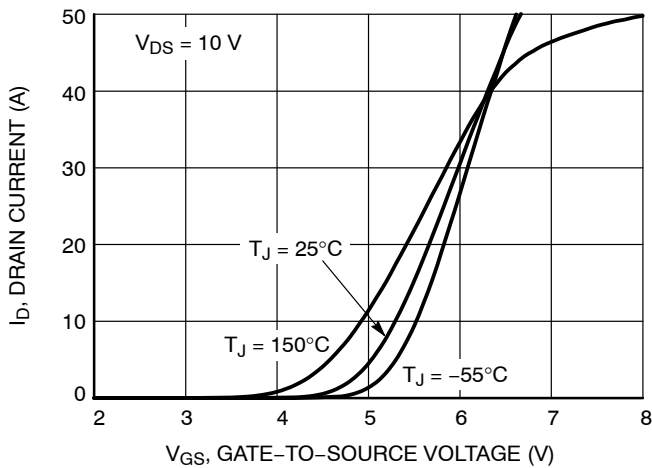


Figure 5. Transfer Characteristics

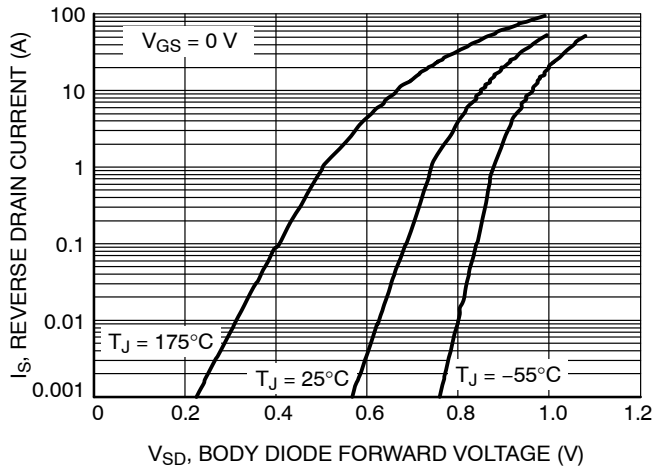


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

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## TYPICAL CHARACTERISTICS

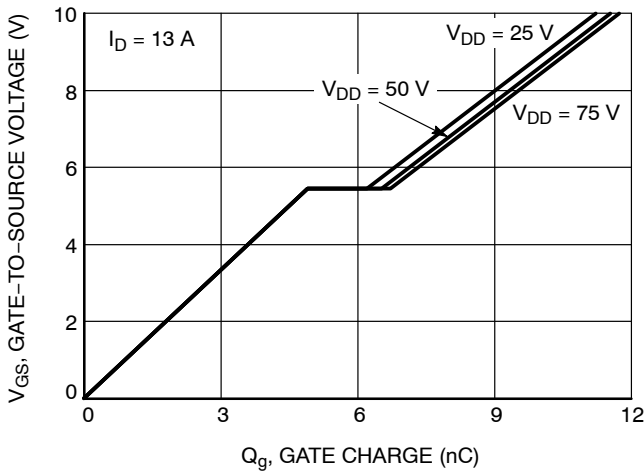


Figure 7. Gate Charge Characteristics

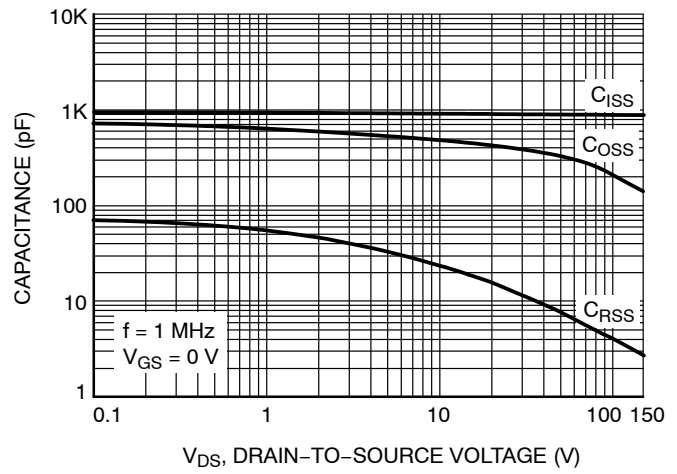


Figure 8. Capacitance vs. Drain-to-Source Voltage

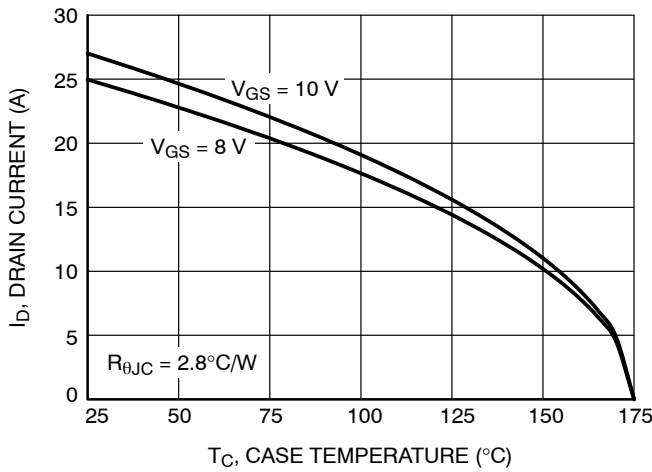


Figure 9. Drain Current vs. Case Temperature

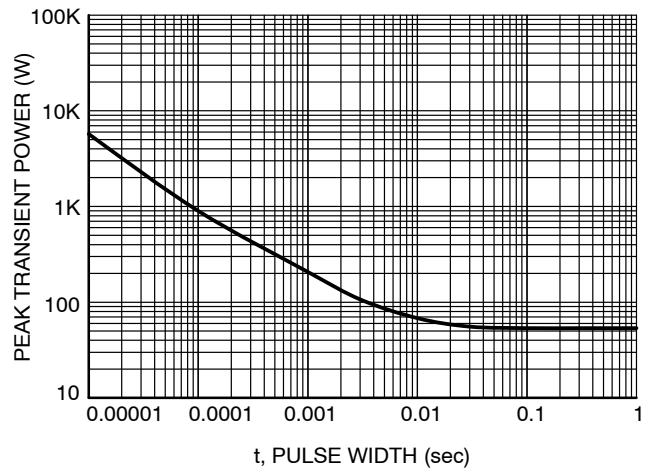


Figure 10. Peak Power

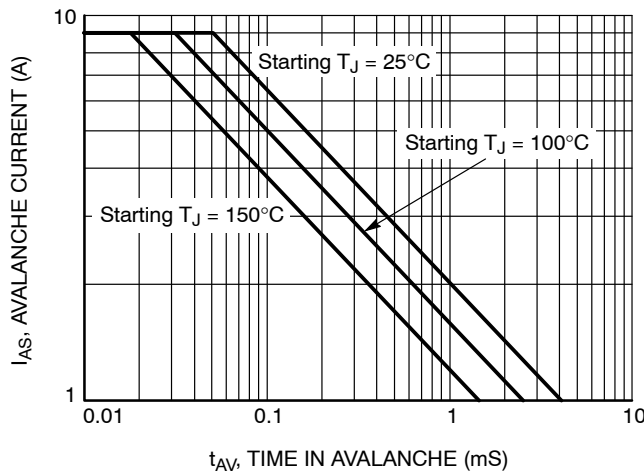


Figure 11. Unclamped Inductive Switching Capability

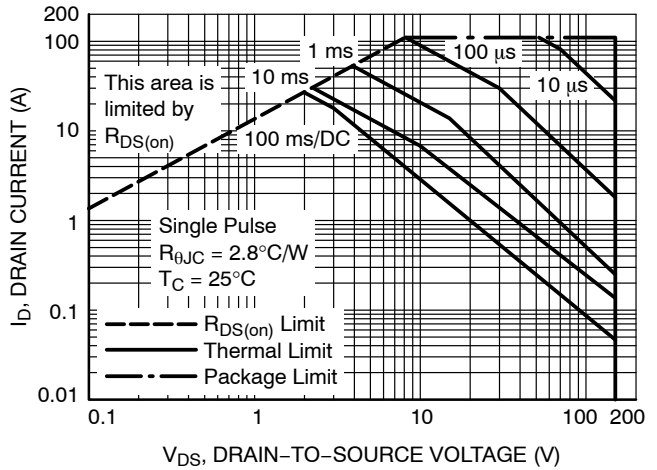


Figure 12. Forward Bias Safe Operating Area

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## TYPICAL CHARACTERISTICS

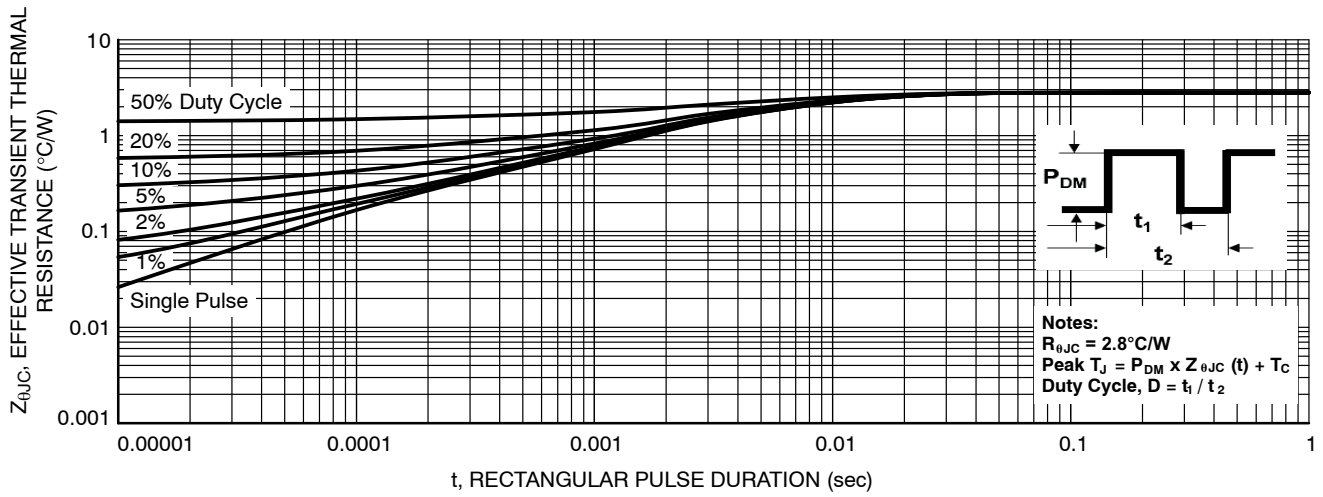
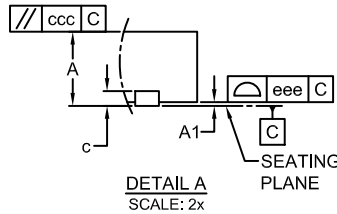
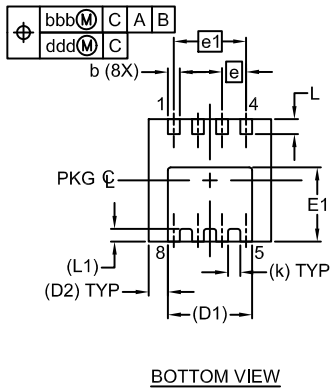
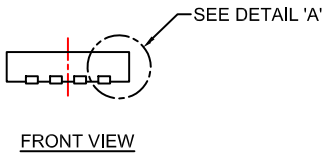
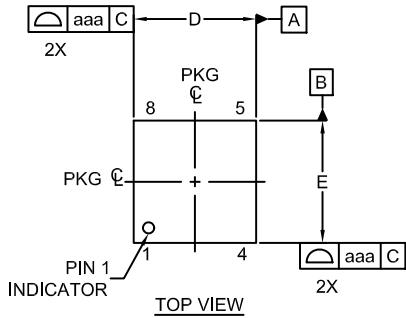


Figure 13. Transient Thermal Impedance

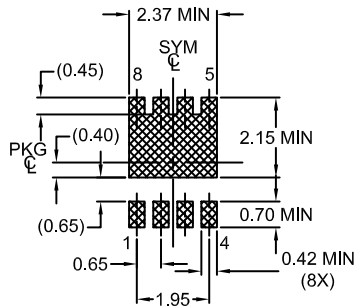
# NTTFS034N15MC

## PACKAGE DIMENSIONS

**WDFN8 3.3X3.3, 0.65P**  
**CASE 483AW**  
**ISSUE A**



### LAND PATTERN RECOMMENDATION\*



### NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	-	0.05
b	0.27	0.32	0.37
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.27 REF		
D2	0.52 REF		
E	3.20	3.30	3.40
E1	1.85	1.95	2.05
e	0.65 BSC		
e1	1.95 BSC		
k	0.33 REF		
L	0.30	0.40	0.50
L1	0.34 REF		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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