MACH 1 and 2 CPLD Families

High-Performance EE CMOS Programmable Logic

FEATURES

- **High-performance electrically-erasable CMOS PLD families**
- **32 to 128 macrocells**
- **44 to 100 pins in cost-effective PLCC, PQFP and TQFP packages**
- **SpeedLocking™ – guaranteed fixed timing up to 16 product terms**
- **Commercial 5/5.5/6/7.5/10/12/15-ns t_{PD} and Industrial 7.5/10/12/14/18-ns t_{PD}**
- **Configurable macrocells**
  - — Programmable polarity
  - — Registered or combinatorial outputs
  - — Internal and I/O feedback paths
  - — D-type or T-type flip-flops
  - — Output Enables
  - — Choice of clocks for each flip-flop
  - — Input registers for MACH 2 family
- **JTAG (IEEE 1149.1)-compatible, 5-V in-system programming available**
- **Peripheral component interconnect (PCI) compliant at 5/5.5/6/7.5/10/12 ns**
- **Safe for mixed supply voltage system designs**
- **Bus-Friendly™ inputs and I/Os reduce risk of unwanted oscillatory outputs**
- **Programmable power-down mode results in power savings of up to 75%**
- **Supported by Vantis DesignDirect™ software for rapid logic development**
  - — Supports HDL design methodologies with results optimized for Vantis
  - — Flexibility to adapt to user requirements
  - — Software partnerships that ensure customer success
- **Lattice/Vantis and third-party hardware programming support**
  - — Lattice/VantisPRO™ (formerly known as MACHPRO®) software for in-system programmability support on PCs and Automated Test Equipment
  - — Programming support on all major programmers including Data I/O, BP Microsystems, Advin, and System General

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Table 1. MACH 1 and 2 Family Device Features [1]

Feature	MACH111 (SP)	MACH131 (SP)	MACH211 (SP)	MACH221 (SP)	MACH231 (SP)
Macrocells	32	64	64	96	128
Maximum user I/O pins	32	64	32	48	64
t_{PD} (ns)	5.0	5.5	7.5 (6.0)	7.5	6.0 (10)
t_S (ns)	3.5	3.0	5.5 (5)	5.5	5 (6.5)
t_{CO} (ns)	3.5	4	4.5 (4)	5	4 (6.5)
f_{CNT} (MHz)	182	182	133 (166)	133	166 (100)

Note:

1. Values in parentheses ( ) are for the SP version.

GENERAL DESCRIPTION

The MACH® 1 & 2 families from Lattice/Vantis offer high-performance, low cost Complex Programmable Logic Devices (CPLDs), addressing the growing need for speed in networking, telecommunications and computing. MACH 1 & 2 devices are available in speeds as fast as 5.0-ns t_{PD} and in densities ranging from 32 to 128 macrocells (Tables 1 and 2). The overall benefits for users include guaranteed high performance for entry-to-mid-level logic needs at a low cost.

Table 2. MACH 1 and 2 Family Speed Grades[1]

Device	-5	-6	-7	-10	-12	-14	-15	-18
MACH111	C (Note 2)		C, I	C, I	C, I	I	C	I
MACH111SP	C (Note 2)		C, I	C, I	C, I	I	C	I
MACH131	C (Note 3)		C, I	C, I	C, I	I	C	I
MACH131SP	C (Note 3)		C, I	C, I	C, I	I	C	I
MACH211			C	C, I	C, I	I	C	I
MACH211SP		C	C	C, I	C, I	I	C	I
MACH221			C	C, I	C, I	I	C	I
MACH221SP			C	C, I	C, I	I	C	I
MACH231		C	C	C	C, I	I	C	I
MACH231SP				C	C, I	I	C	I

Notes:

1. C = Commercial, I = Industrial

2. -5 speed grade for MACH111 (SP) = 5.0 ns t_{PD}

3. -5 speed grade for MACH131(SP) = 5.5 ns t_{PD}

The MACH 1 & 2 families consist of ten devices—five base options, each with a counterpart that includes JTAG-compatible in-system programming (ISP). These devices offer five different density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), and Plastic Leaded Chip Carrier (PLCC) packages from 44 to 100 pins (Table 3). Each MACH 1 & 2 device is PCI compliant and includes other features such as SpeedLocking architecture for guaranteed fixed timing, Bus-Friendly inputs and I/Os, and programmable power-down mode for extra power savings.

Table 3. MACH 1 and 2 Family Package and I/O Options

Device	44-pin PLCC	44-pin TQFP	68-pin PLCC	84-pin PLCC	100-pin TQFP	100-pin PQFP
MACH111	X	X				
MACH111SP	X	X				
MACH131				X		
MACH131SP					X	X
MACH211	X	X				
MACH211SP	X	X				
MACH221			X			
MACH221SP						X
MACH231				X		
MACH231SP					X	X

Note:

1. *The MACH110, MACH120, MACH130, MACH210, MACHLV210, MACH215, MACH220 and MACH230 are not listed above and not recommended for new designs. However, they are still supported by Lattice/Vantis. For technical or sales support, please call your local Lattice/Vantis sales office or visit our Web site at www.vantis.com for more information.*

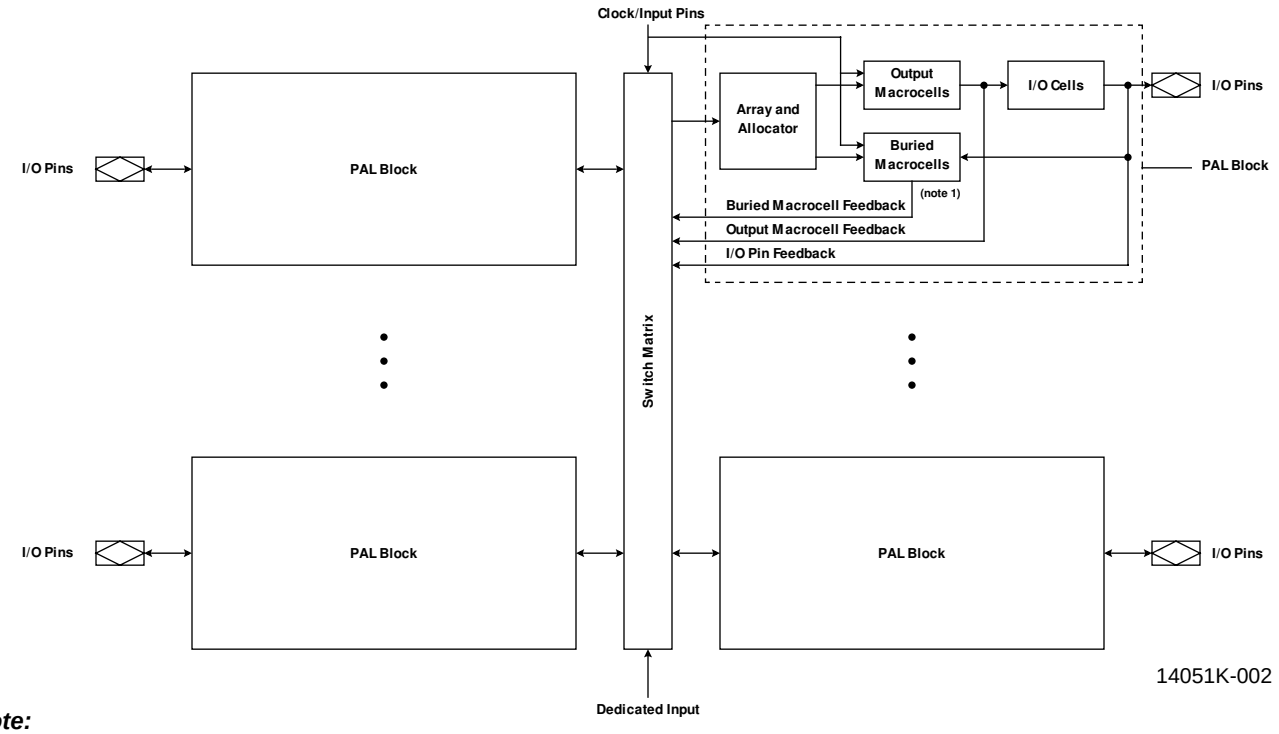
Lattice/Vantis offers software design support for MACH devices in both the MACHXL® and DesignDirect development systems. The DesignDirect development system is the Lattice/Vantis implementation software that includes support for all Lattice/Vantis CPLD, FPGA, and SPLD devices. This system is supported under Windows '95, '98 and NT as well as Sun Solaris and HPUX.

DesignDirect software is designed for use with design entry, simulation and verification software from leading-edge tool vendors such as Cadence, Exemplar Logic, Mentor Graphics, Model Technology, Synopsys, Synplicity, Viewlogic and others. It accepts EDIF 2 0 0 input netlists, generates JEDEC files for Lattice/Vantis PLDs and creates industry-standard EDIF, Verilog, VITAL compliant VHDL and SDF simulation netlists for design verification.

DesignDirect software is also available in product configurations that include VHDL and Verilog synthesis from Exemplar Logic and VHDL, Verilog RTL and gate level timing simulation from Model Technology. Schematic capture and ABEL entry, as well as functional simulation, are also provided.

FUNCTIONAL DESCRIPTION

Each MACH 1 and 2 device consists of multiple, optimized PAL® blocks interconnected by a switch matrix. The switch matrix allows communication between PAL blocks, and routes inputs to the PAL blocks. Together, the PAL blocks and switch matrix allow the logic designer to create large designs in a single device instead of using multiple devices.



Note:

1. There are no buried macrocells in MACH 1 devices. All macrocells are output macrocells.

Device	PAL Blocks	Macrocells per Block	I/Os per Block	Product Terms per Block
MACH111(SP)	2	16	16	70
MACH131(SP)	4	16	16	70
MACH211(SP)	4	16	8	68
MACH221(SP)	8	12	6	52
MACH231(SP)	8	16	8	68

Figure 1. Overall Architecture of MACH 1 & 2 Devices

The switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that return to the same PAL block still must go through the switch matrix. This mechanism ensures that PAL blocks in MACH devices communicate with each other with guaranteed fixed timing (SpeedLocking).

The switch matrix makes a MACH device more advanced than simply several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

Each PAL block consists of the following elements:

- Product-term array
- Logic Allocator
- Macrocells
- I/O cells

Each PAL block additionally contains an asynchronous reset product term and an asynchronous preset product term. This allows the flip-flops within a single PAL block to be initialized as a bank. There are also output enable product terms that provide tri-state control for the I/O cells.

Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the switch matrix (Table 4), and are provided in both true and complement forms for efficient logic implementation.

Because the number of product terms available for a given function is not fixed, the full sum of products is not realized in the array. The product terms drive the logic allocator, which allocates the appropriate number of product terms to generate the function.

Table 4. PAL Block Inputs

Device	Number of Inputs to PAL Block	Device	Number of Inputs to PAL Block
MACH111	26	MACH211SP	26
MACH111SP	26	MACH221	26
MACH131	26	MACH221SP	26
MACH131SP	26	MACH231	32
MACH211	26	MACH231SP	32

Logic Allocator

The logic allocator (Figure 2) is a block within which different product terms are allocated to the appropriate macrocells in groups of four product terms called “product term clusters”. The availability and distribution of product term clusters is automatically considered by the software as it fits functions within the PAL block. The size of the product term clusters has been designed to provide high utilization of product terms. Complex functions using many product terms are possible, and when few product terms are used, there will be a minimal number of unused, or wasted, product terms left over.

The product term clusters do not “wrap” around the logic block. This means that the macrocells at the ends of the block have fewer product terms available (Tables 5, 6, 7, 8).

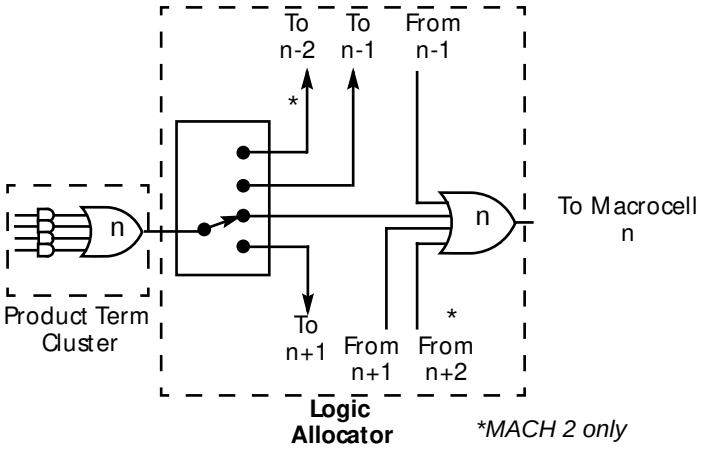


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Figure 2. Product Term Clusters and the Logic Allocator

Table 5. Logic Allocation for MACH111(SP)

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M_0	C_0, C_1	M_8	C_8, C_9
M_1	C_0, C_1, C_2	M_9	C_8, C_9, C_{10}
M_2	C_1, C_2, C_3	M_{10}	C_9, C_{10}, C_{11}
M_3	C_2, C_3, C_4	M_{11}	C_{10}, C_{11}, C_{12}
M_4	C_3, C_4, C_5	M_{12}	C_{11}, C_{12}, C_{13}
M_5	C_4, C_5, C_6	M_{13}	C_{12}, C_{13}, C_{14}
M_6	C_5, C_6, C_7	M_{14}	C_{13}, C_{14}, C_{15}
M_7	C_6, C_7	M_{15}	C_{14}, C_{15}

Table 6. Logic Allocation for MACH131(SP)

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M_0	C_0, C_1	M_8	C_7, C_8, C_9
M_1	C_0, C_1, C_2	M_9	C_8, C_9, C_{10}
M_2	C_1, C_2, C_3	M_{10}	C_9, C_{10}, C_{11}
M_3	C_2, C_3, C_4	M_{11}	C_{10}, C_{11}, C_{12}
M_4	C_3, C_4, C_5	M_{12}	C_{11}, C_{12}, C_{13}
M_5	C_4, C_5, C_6	M_{13}	C_{12}, C_{13}, C_{14}
M_6	C_5, C_6, C_7	M_{14}	C_{13}, C_{14}, C_{15}
M_7	C_6, C_7, C_8	M_{15}	C_{14}, C_{15}

Table 7. Logic Allocation for MACH211(SP) and MACH231(SP)

Macrocell			Macrocell		
Output	Buried	Available Clusters	Output	Buried	Available Clusters
M_0		C_0, C_1, C_2	M_8		C_7, C_8, C_9, C_{10}
	M_1	C_0, C_1, C_2, C_3		M_9	C_8, C_9, C_{10}, C_{11}
M_2		C_1, C_2, C_3, C_4	M_{10}		$C_9, C_{10}, C_{11}, C_{12}$
	M_3	C_2, C_3, C_4, C_5		M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_4		C_3, C_4, C_5, C_6	M_{12}		$C_{11}, C_{12}, C_{13}, C_{14}$
	M_5	C_4, C_5, C_6, C_7		M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_6		C_5, C_6, C_7, C_8	M_{14}		C_{13}, C_{14}, C_{15}
	M_7	C_6, C_7, C_8, C_9		M_{15}	C_{14}, C_{15}

Table 8. Logic Allocation for MACH221(SP)

Macrocell			Macrocell		
Output	Buried	Available Clusters	Output	Buried	Available Clusters
M_0		C_0, C_1, C_2	M_6		C_5, C_6, C_7, C_8
	M_1	C_0, C_1, C_2, C_3		M_7	C_6, C_7, C_8, C_9
M_2		C_1, C_2, C_3, C_4	M_8		C_7, C_8, C_9, C_{10}
	M_3	C_2, C_3, C_4, C_5		M_9	C_8, C_9, C_{10}, C_{11}
M_4		C_3, C_4, C_5, C_6	M_{10}		C_9, C_{10}, C_{11}
	M_5	C_4, C_5, C_6, C_7		M_{11}	C_{10}, C_{11}

Macrocell

There are two fundamental types of macrocell: the output macrocell and the buried macrocell. The buried macrocell is only found in MACH 2 devices. The use of buried macrocells effectively doubles the number of macrocells available without increasing the pin count.

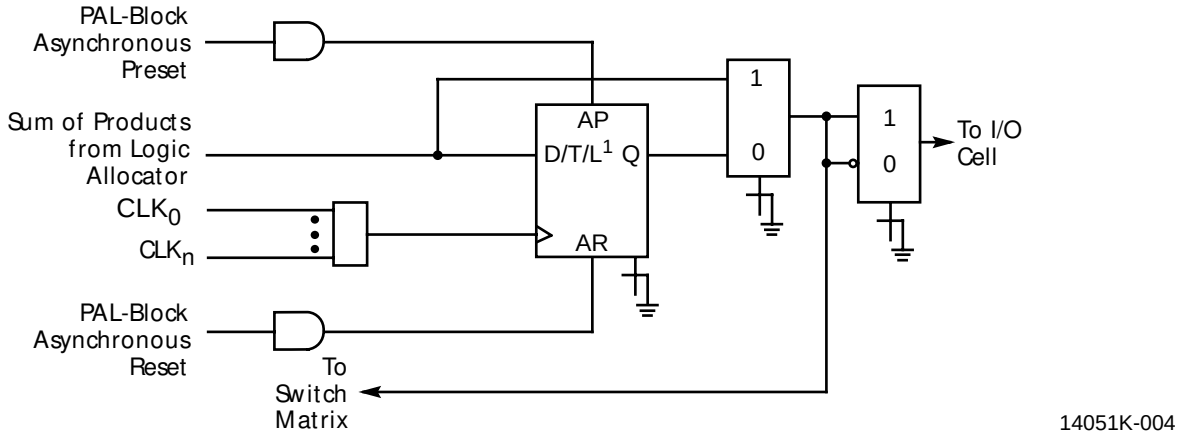
Both macrocell types can generate registered or combinatorial outputs. For the MACH 2 series, a transparent-low latch configuration is provided. If the register is used, it can be configured as a T-type or a D-type flip-flop. Register and latch functionality is defined in Table 9. Programmable polarity (for output macrocells) and the T-type flip-flop both give the software a way to minimize the number of product terms needed. These choices can be made automatically by the software when it fits the design into the device.

Table 9. Register/Latch Operation

Configuration	D/T	CLK/LE	Q+
D-Register	X	0,1,↓	Q
	0	↑	0
	1	↑	1
T-Register	X	0,1,↓	Q
	0	↑	Q
	1	↑	$\overline{Q}$
Latch	X	1	Q
	0	0	0
	1	0	1

The output macrocell (Figure 3) sends its output back to the switch matrix, via internal feedback, and to the I/O cell. The feedback is always available regardless of the configuration of the I/O cell. This allows for buried combinatorial or registered functions, freeing up the I/O pins for use as inputs if not needed as outputs. The basic output macrocell configurations are shown in Figure 4.

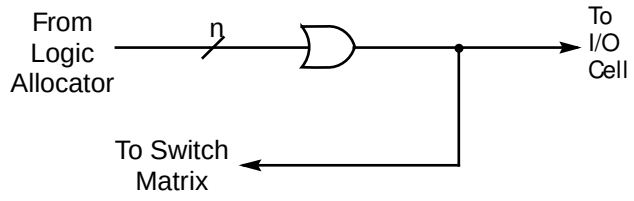
The buried macrocell (Figure 5) does not send its output to an I/O cell. The output of a buried macrocell is provided only as an internal feedback signal which feeds the switch matrix. This allows the designer to generate additional logic without requiring additional pins. The buried macrocell can also be used to register or latch inputs. The input register is a D-type flip-flop; the input latch is a transparent-low D-type latch. Once configured as a registered or latched input, the buried macrocell cannot generate logic from the product-term array. The basic buried macrocell configurations are shown in Figure 6.



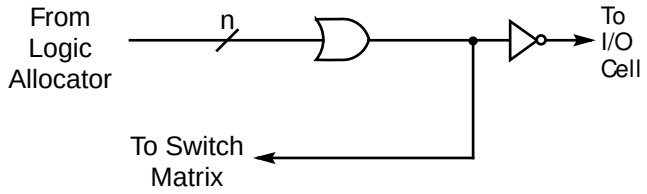
Note:

1. Latch option available on MACH 2 devices only.

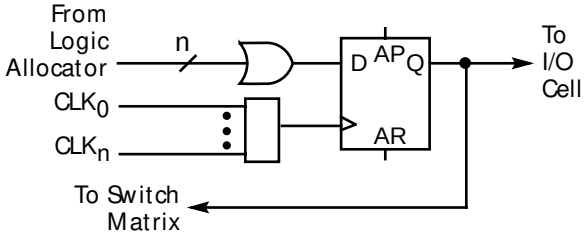
Figure 3. Output Macrocell



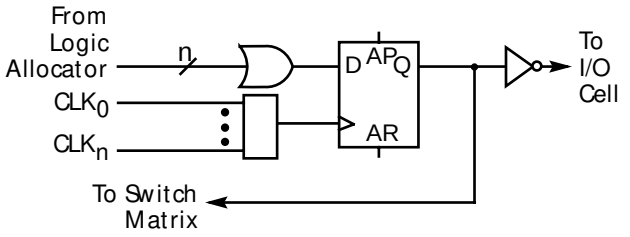
a. Combinatorial, active high



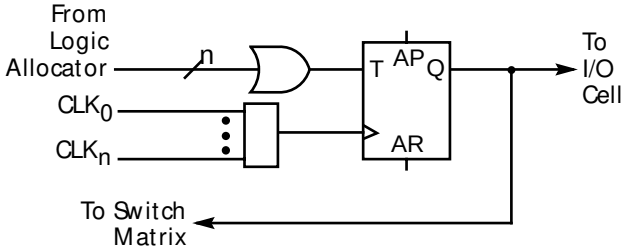
b. Combinatorial, active low



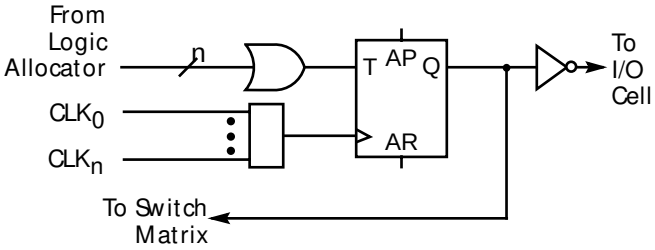
c. D-type register, active high



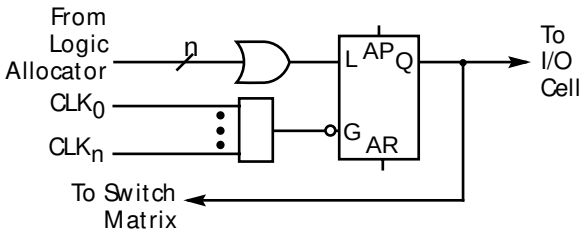
d. D-type register, active low



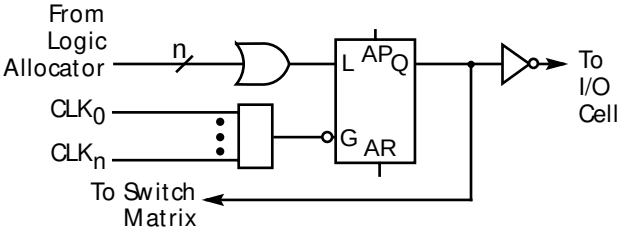
e. T-type register, active high



f. T-type register, active low



g. Latch, active high (MACH 2 only)



h. Latch, active low (MACH 2 only)

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Figure 4. Output Macrocell Configurations

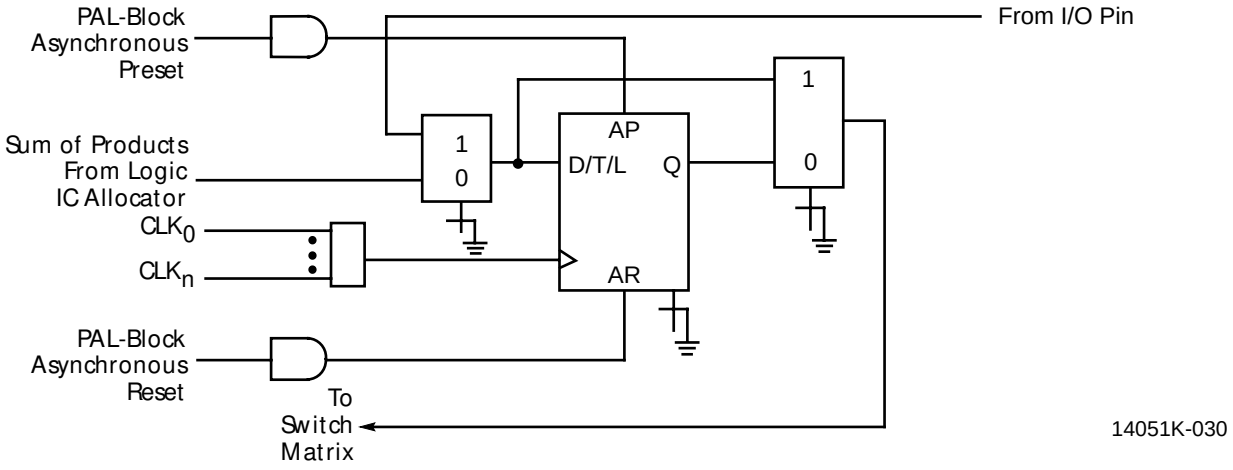


Figure 5. Buried Macrocell (MACH 2 only)

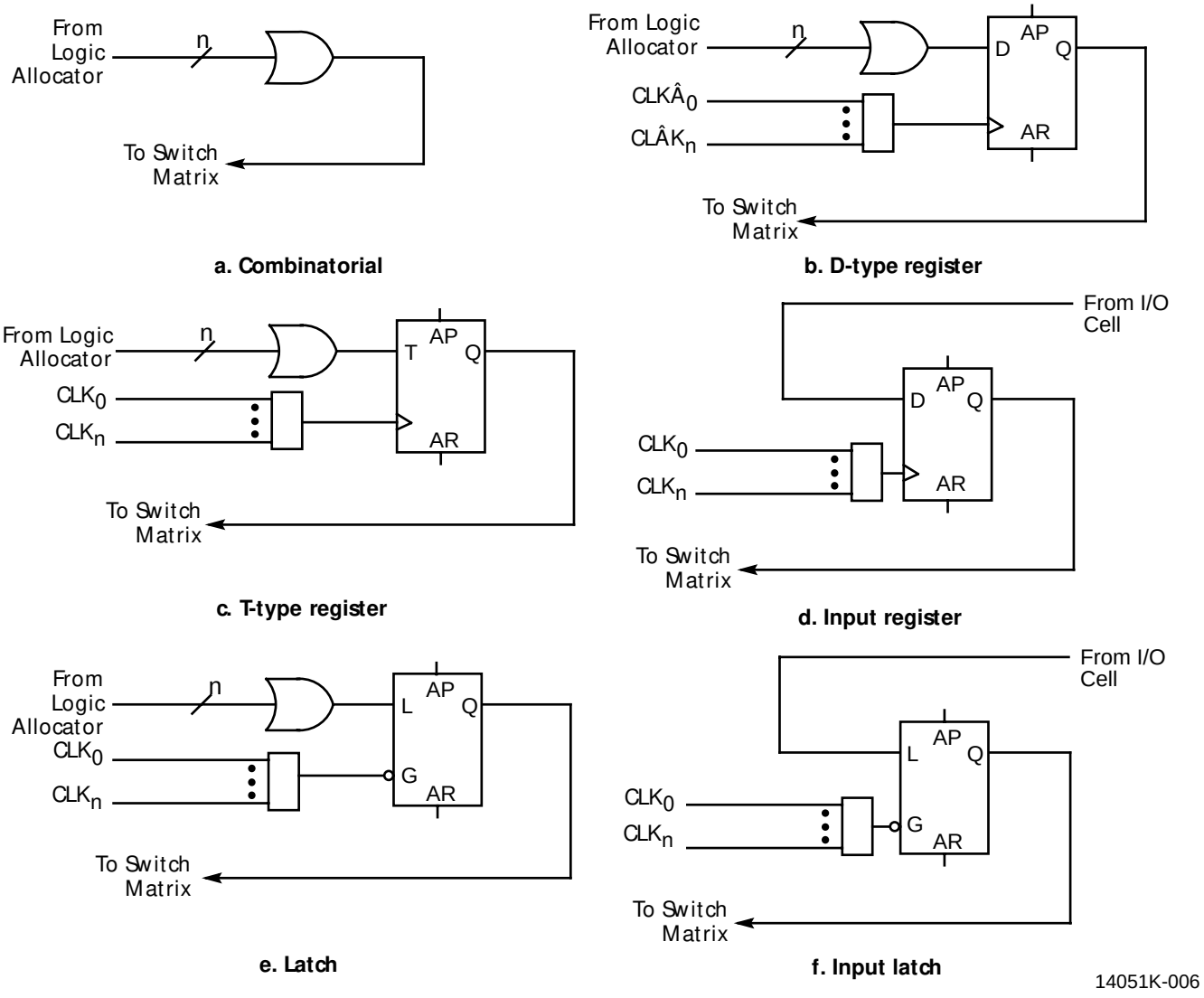


Figure 6. Buried Macrocell Configurations (MACH 2 only)

The flip-flops in either macrocell type can be clocked by one of several clock pins (Table 10). Registers are clocked on the rising edge of the clock input. Latches hold their data when the gate input is HIGH. Clock pins are also available as inputs, although care must be taken when a signal acts as both clock and input to the same device.

Table 10. Macrocell Clocks

Device	Number of Clocks Available	Device	Number of Clocks Available
MACH111	4	MACH211SP	2
MACH111SP	2	MACH221	4
MACH131	4	MACH221SP	4
MACH131SP	4	MACH231	4
MACH211	4	MACH231SP	4

All flip-flops have asynchronous reset and preset. This is controlled by the common product terms that control all flip-flops within a PAL block. For a single PAL block, all flip-flops, whether in an output or a buried macrocell, are initialized together. The initialization functionality of the flip-flops is illustrated in Table 11.

Table 11. Asynchronous Reset/Preset Operation

Configuration	AR	AP	CLK/LE	Q+
Register	0	0	X	See Table 9
	0	1	X	1
	1	0	X	0
	1	1	X	0
Latch	0	0	X	See Table 9
	0	1	0	Illegal
	0	1	1	1
	1	0	0	Illegal
	1	0	1	0
	1	1	0	Illegal
	1	1	1	0

I/O Cells

The I/O cells (Figure 7) provide a three-state output buffer. The three-state buffer can be left permanently enabled for use only as an output, permanently disabled for use as an input, or it can be controlled by one of two product terms for bi-directional signals and bus connections. The two product terms provided are common to a bank of I/O cells.

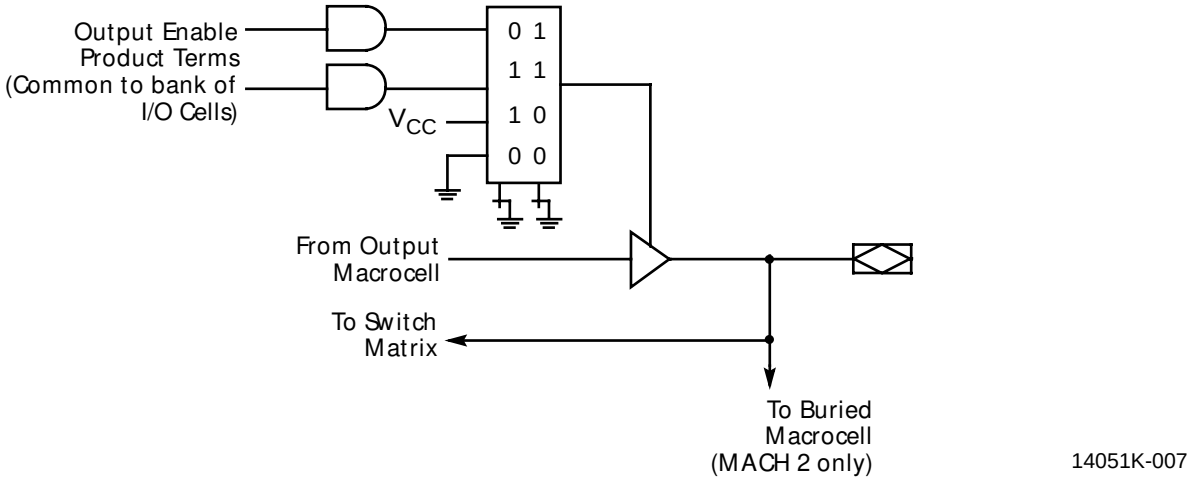


Figure 7. I/O Cell

SPEEDLOCKING FOR GUARANTEED FIXED TIMING

The unique MACH 1 & 2 architecture is designed for high performance—a metric that is met in both raw speed, and even more importantly, **guaranteed fixed speed**. The design of the switch matrix and PAL blocks guarantee a fixed pin-to-pin delay that is independent of the logic required by the design. Other non-Lattice/Vantis CPLDs incur serious timing delays as product terms expand beyond their typical 4 or 5 product term limits (Figure 8). Speed *and* SpeedLocking combine to give designers easy access to the performance required in today's designs.

14051K-001

Figure 8. Timing in MACH 1 & 2 vs. Non-MACH Devices

JTAG IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACHxxxSP devices provide in-system programming (ISP) capability through their JTAG ports. This capability has been implemented in a manner that insures that the JTAG port remains compliant to the IEEE 1149.1 standard. By using JTAG as the communication interface through which ISP is achieved, customers benefit from a standard, well-defined interface.

MACHxxxSP devices can be programmed across the commercial temperature and voltage range. These devices tristate the outputs during programming. Lattice/Vantis provides its free PC-based Lattice/VantisPRO software to facilitate in-system programming. Lattice/VantisPRO software takes the JEDEC file output produced by Vantis' design implementation software, along with information about the JTAG chain, and creates a set of vectors that are used to drive the JTAG chain. Lattice/VantisPRO software can use these vectors to drive a JTAG chain via the parallel port of a PC. Alternatively, Lattice/VantisPRO software can output files in formats understood by common automated test equipment. This equipment can then be used to program MACHxxxSP devices during the testing of a circuit board. For more information about in-system programming, refer to the separate document entitled *MACH ISP Manual*.

BUS-FRIENDLY INPUTS AND I/Os

The MACH 1 & 2 inputs and I/Os include two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. For the circuit diagram, please refer to the *Input/Output Equivalent Schematics (page 393)* in the General Information Section of the Vantis 1999 Data Book.

PCI COMPLIANT

The MACH 1 & 2 families in -5/-6/-7/-10/-12 speed grades are fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The MACH 1 & 2 families' predictable timing ensures compliance with the PCI AC specifications independent of the design.

POWER-DOWN MODE

The MACH 1 & 2 families feature a programmable low-power mode in which individual signal paths can be programmed for low power. These low-power speed paths will be slower than the non-low-power paths. This feature allows speed critical paths to run at maximum frequency while the rest of the paths operate in the low-power mode, resulting in power savings of up to 75%. If all of the signals in a PAL block are in low-power mode, then the total power is reduced even further.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS

All MACHxxxSP and most of the MACH 1 & 2 devices are safe for mixed supply voltage system designs. These 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they can accept inputs from other 3.3-V devices. The MACH 1 & 2 families provide easy-to-use mixed-voltage design compatibility. For more information, refer to the Technical Note entitled *Mixed Supply Design with MACH 1 & 2 SP Devices*.

POWER-UP RESET

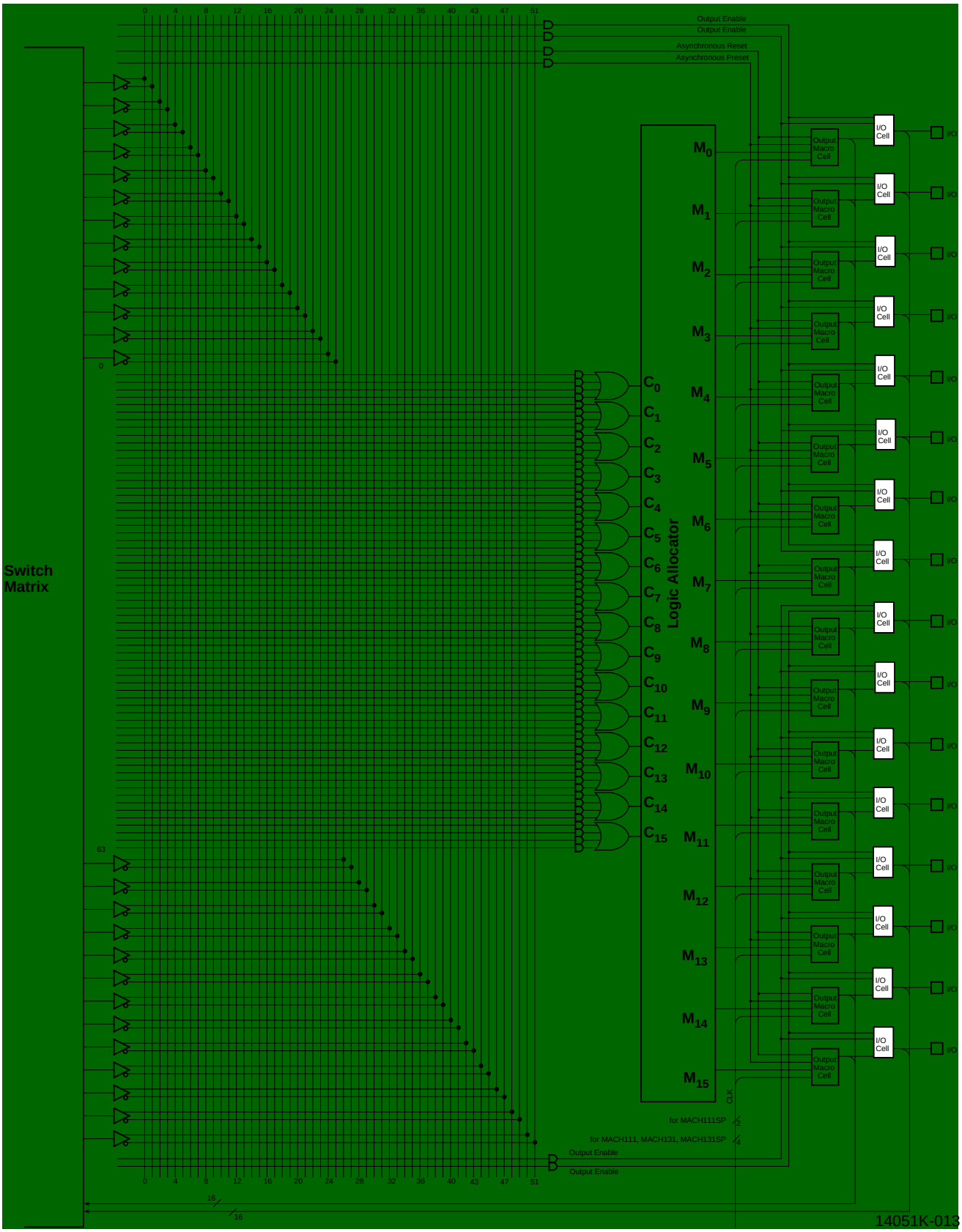
All flip-flops power-up to a logic LOW for predictable system initialization. The actual values of the outputs of the MACH devices will depend on the configuration of the macrocell. To guarantee

initialization values, the V_{CC} rise must be monotonic and the clock must be inactive until the reset delay time has elapsed.

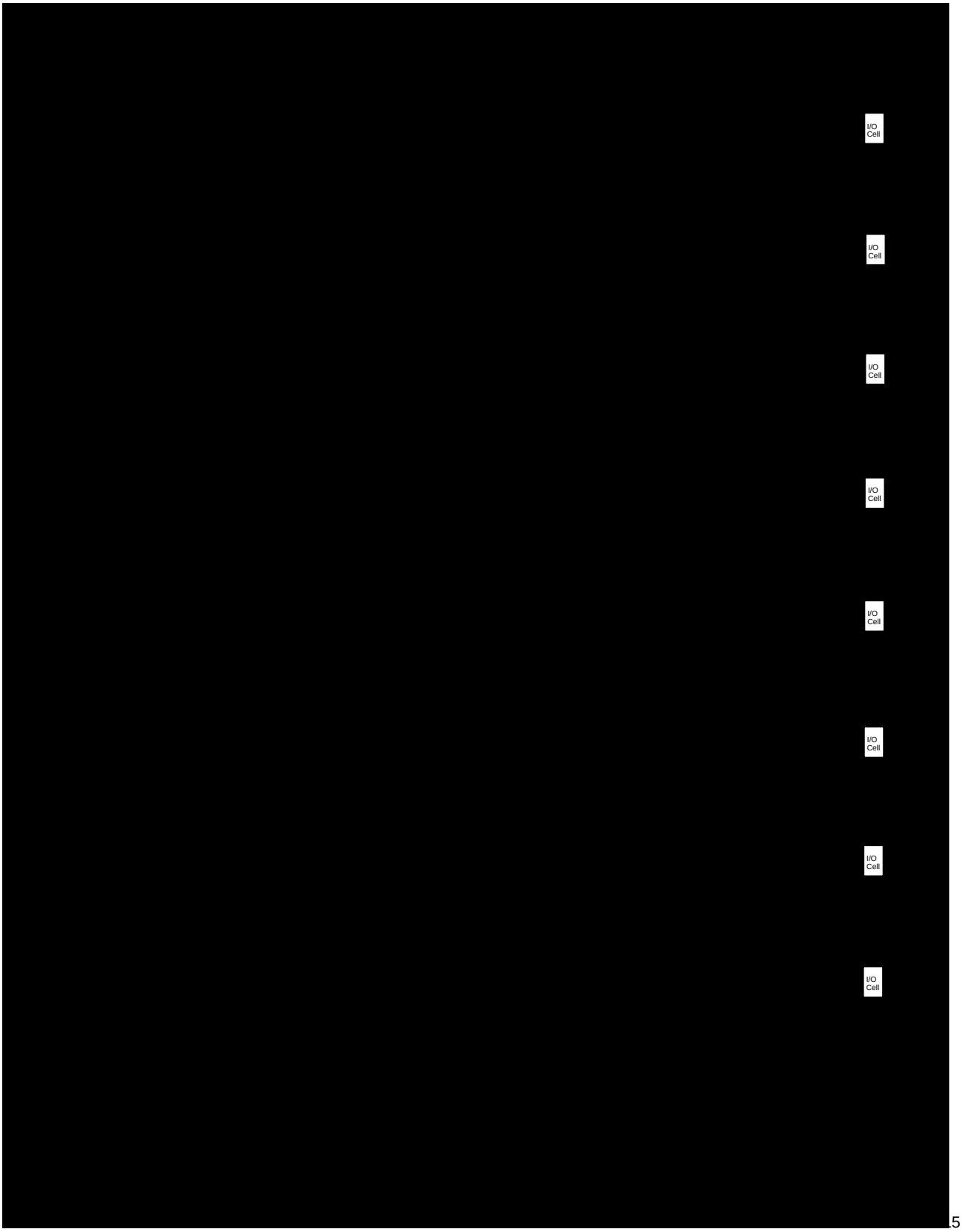
SECURITY BIT

A security bit is provided on the MACH devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

MACH111(SP) AND MACH131(SP) PAL BLOCK

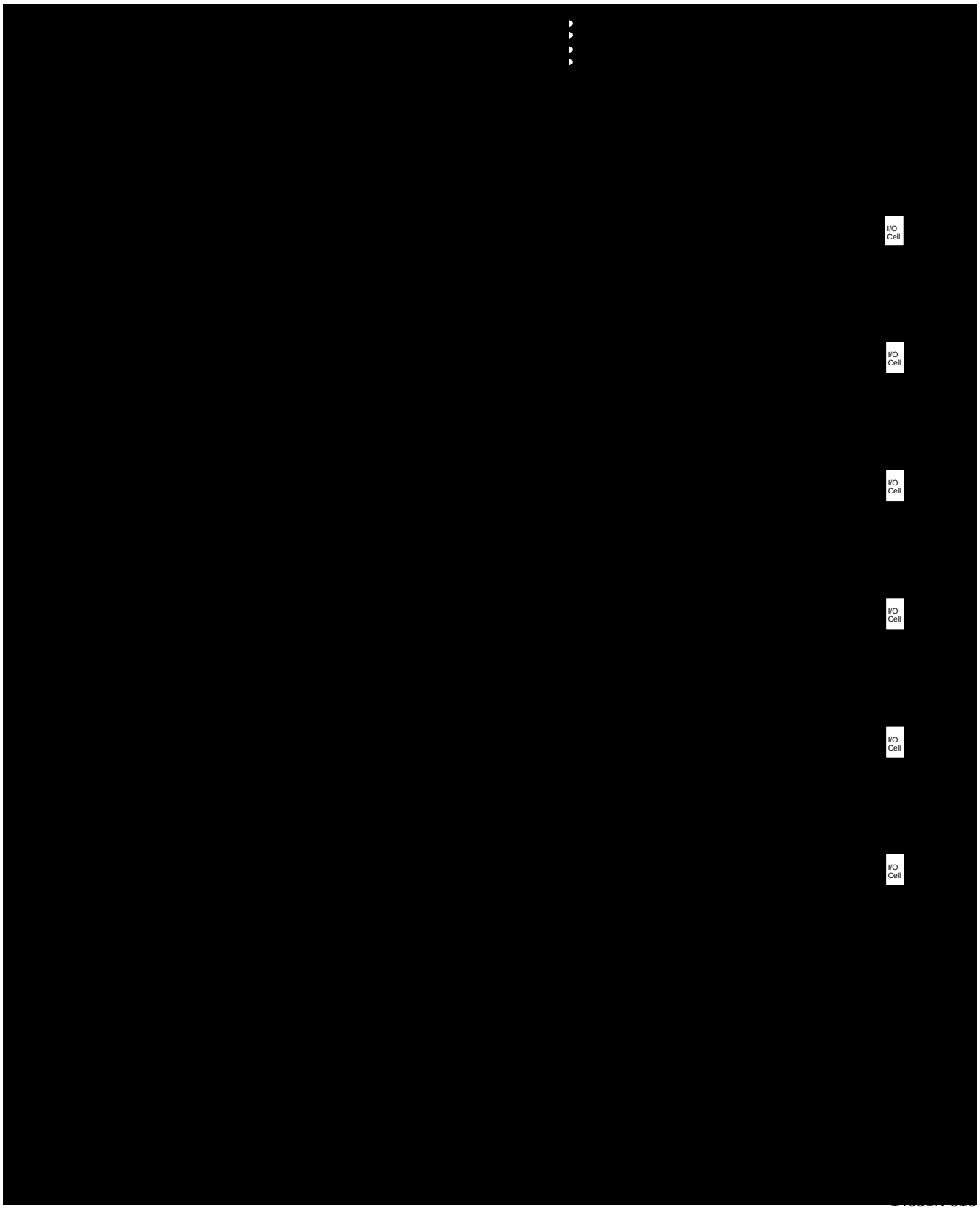


MACH211(SP) PAL BLOCK

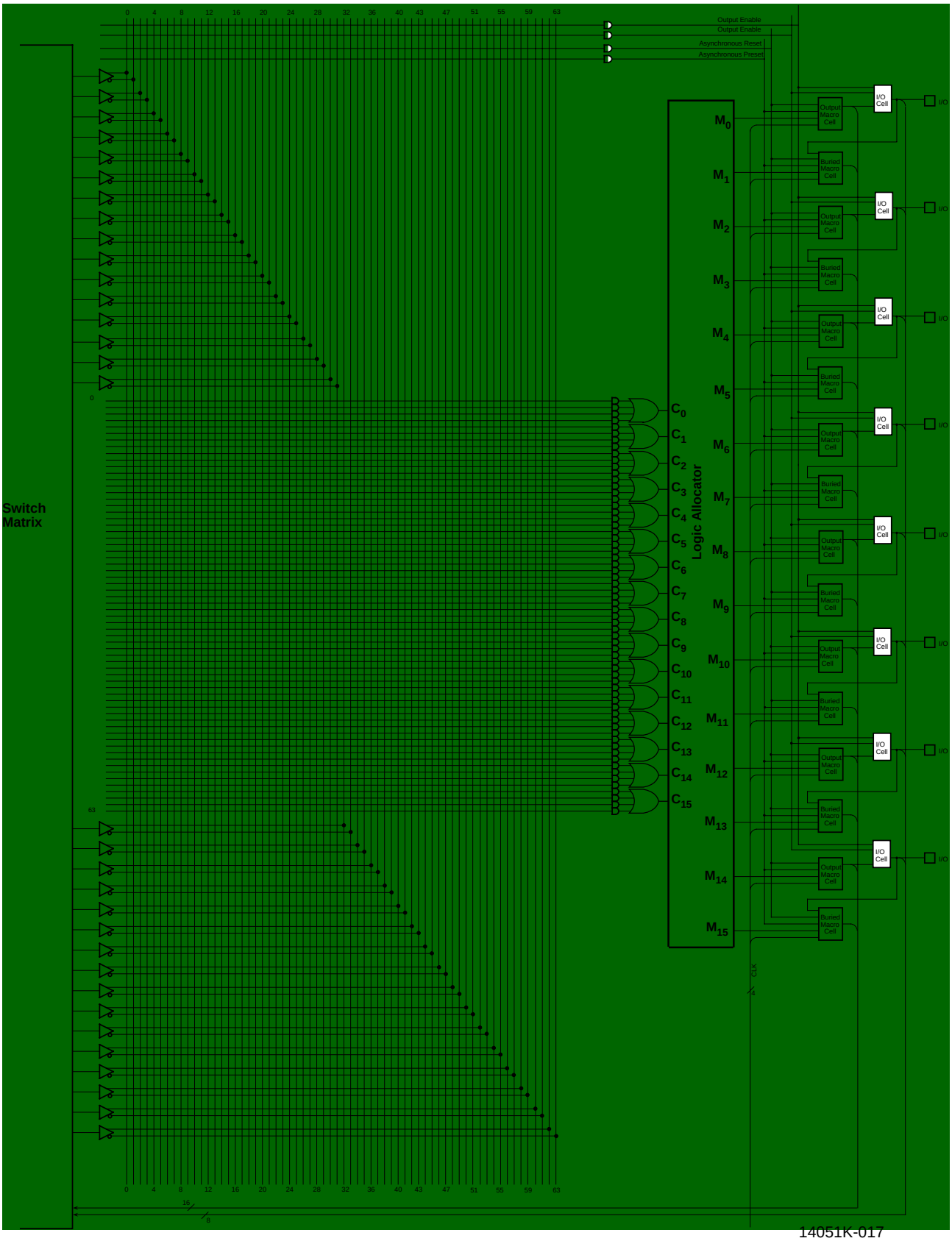


5

MACH221(SP) PAL BLOCK

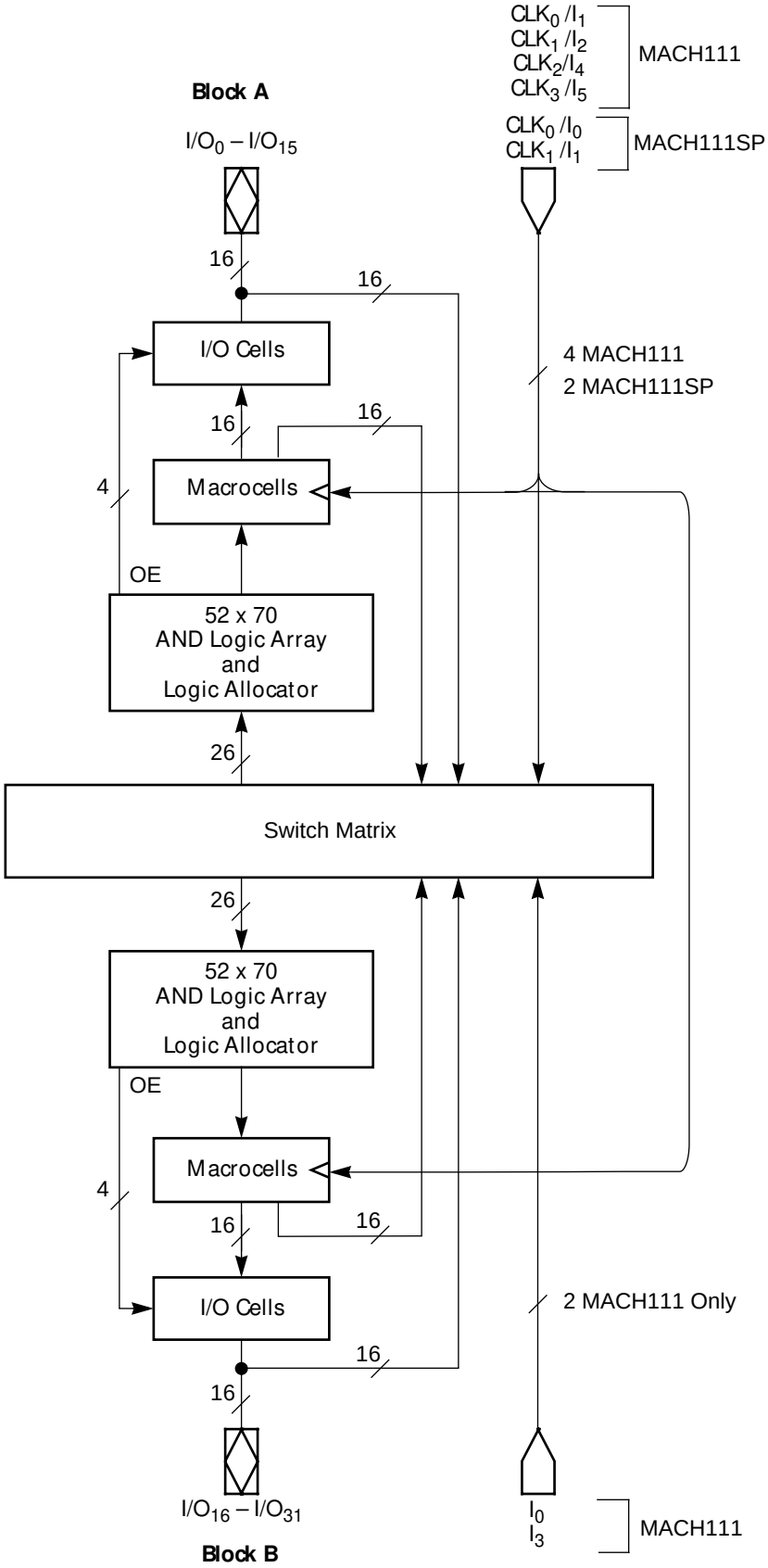


MACH231(SP) PAL BLOCK

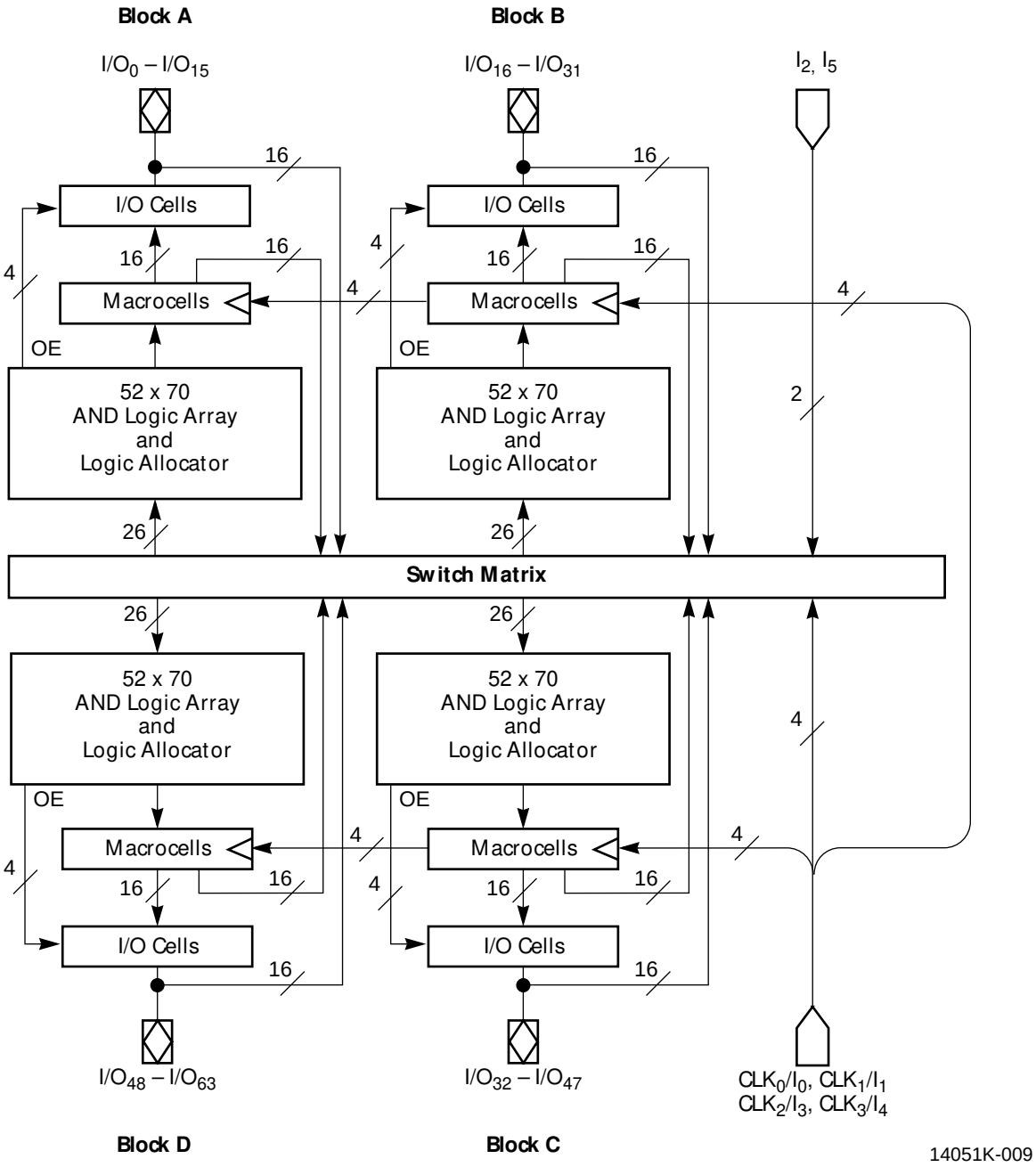


14051K-017

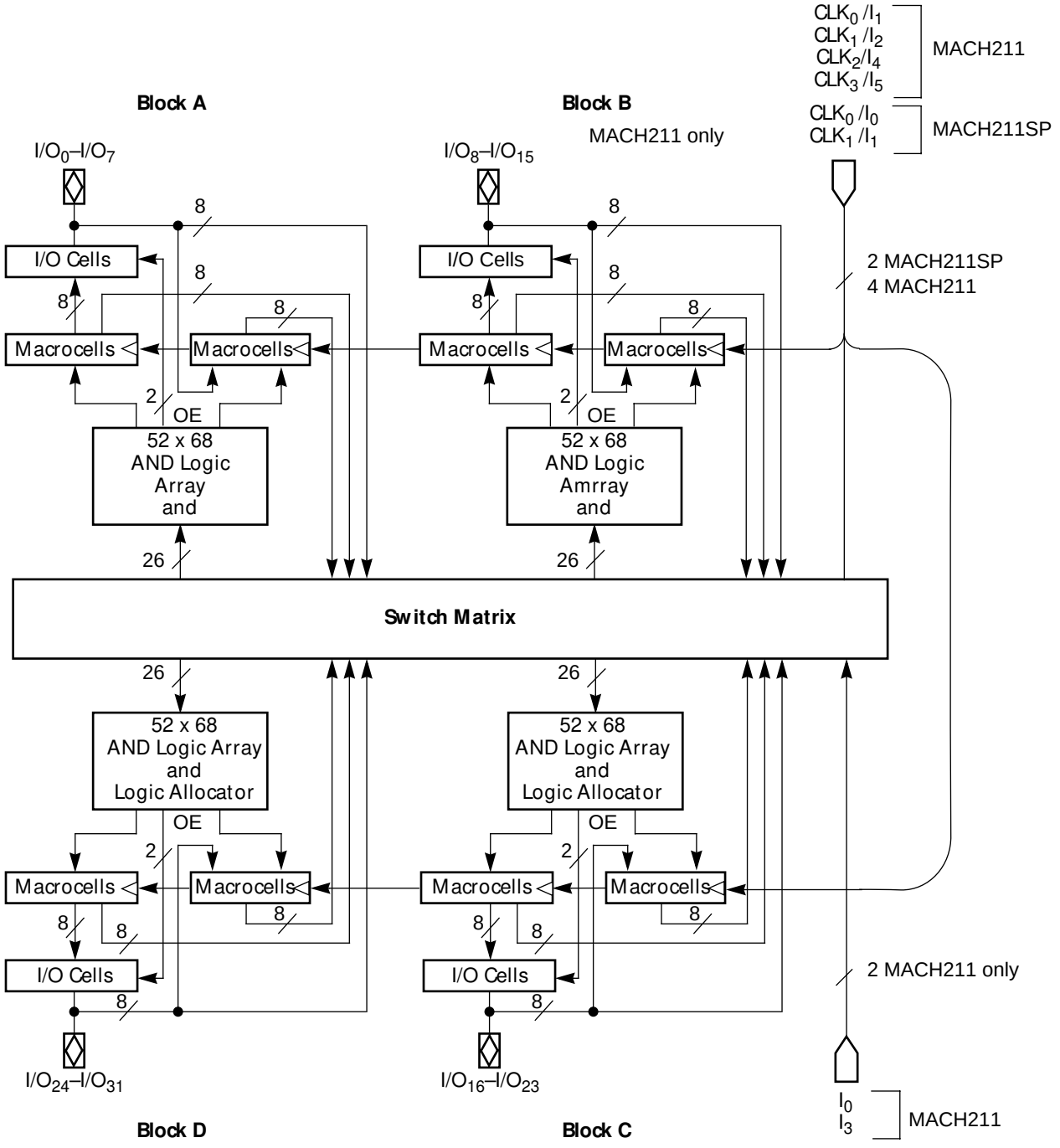
BLOCK DIAGRAM (MACH111, MACH111SP)



BLOCK DIAGRAM (MACH131, MACH131SP)

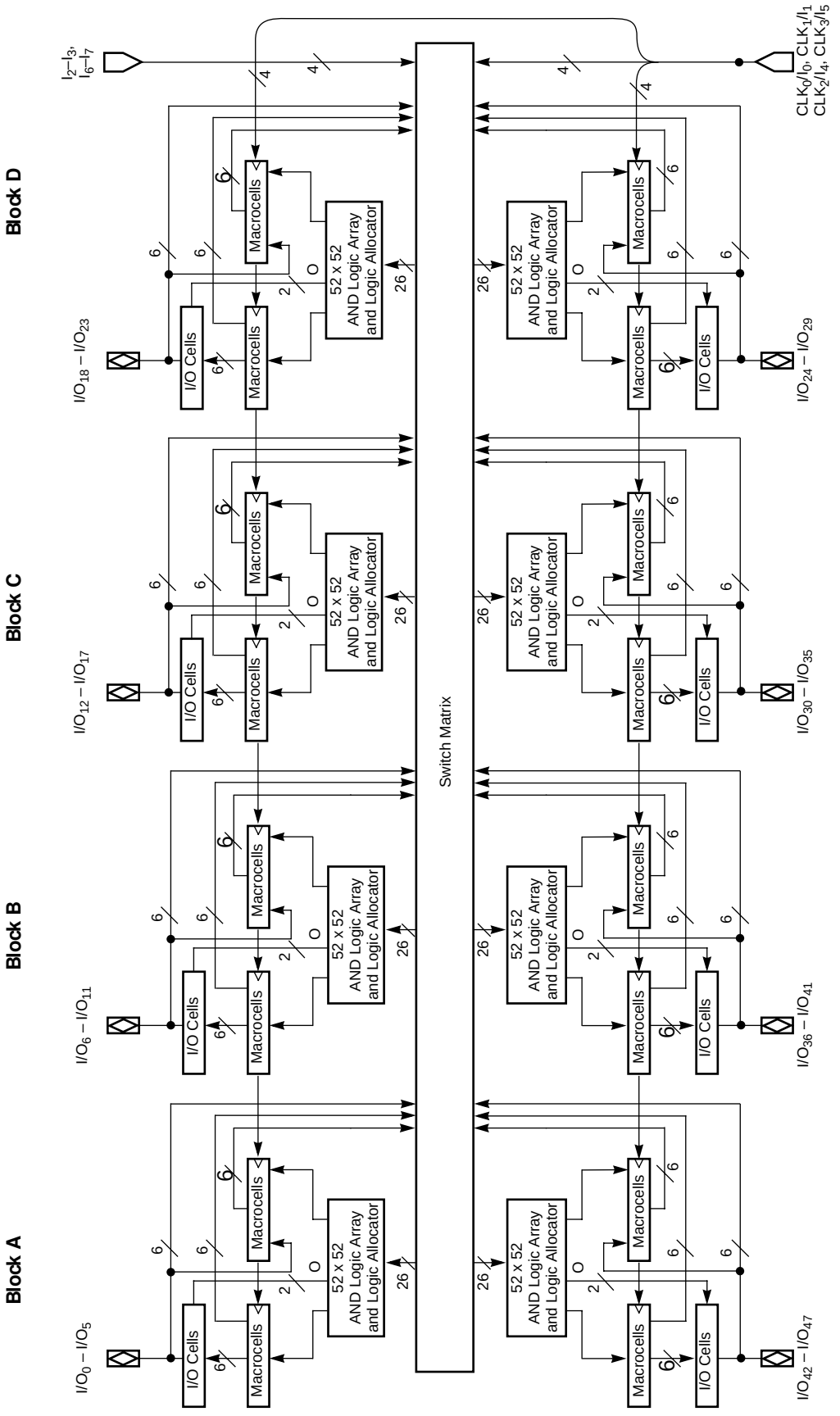


BLOCK DIAGRAM (MACH211, MACH211SP)

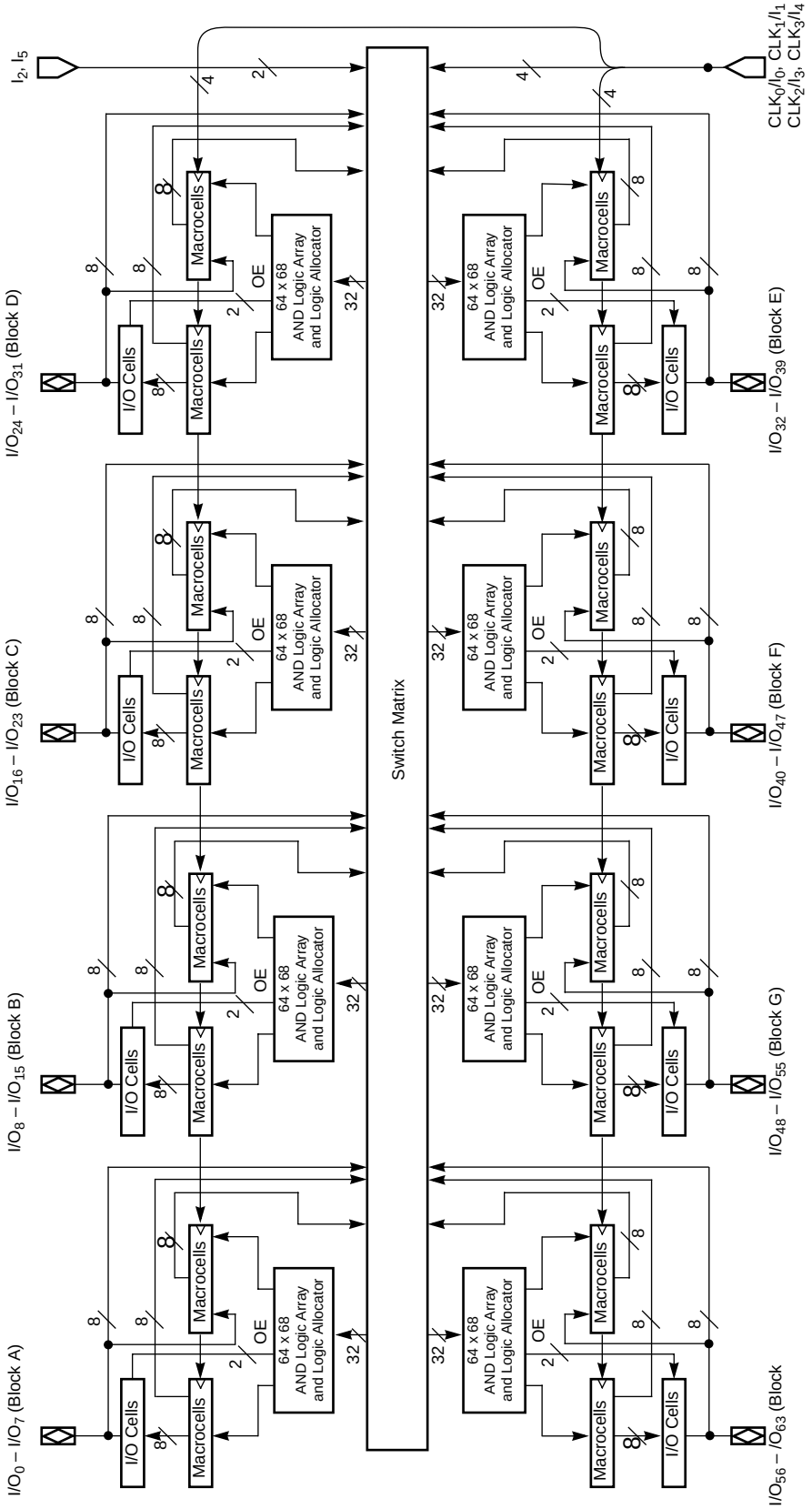


14051K-010

BLOCK DIAGRAM (MACH221, MACH221SP)



BLOCK DIAGRAM (MACH231, MACH231SP)



14051K-012

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
With Power Applied . . . . . -55°C to +125°C

Device Junction Temperature . . . . . +150°C

Supply Voltage with
Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} +0.5 V

DC Output or I/O Pin Voltage . . -0.5 V to V_{CC} +0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = -40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4			V
		I_{OH} = –300 µA, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 1)			3.5	V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} (Note 2)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V V_{CC} = Max (Note 4)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 4)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max (Note 5)	–30		–130 (Note 6), –160	mA

Notes:

1. *This applies to MACH111SP, MACH131SP, and die code "B" or later for MACH211(SP) and MACH231(SP). This does not apply to MACH111, MACH131, MACH221(SP), and die code "A" for MACH211(SP) and MACH231(SP).*
2. *Total I_{OL} for one PAL block should not exceed 64 mA.*
3. *These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
5. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
6. *For commercial temperature range only.*

MACH111 AND MACH111SP
SWITCHING CHARACTERISTICS OVER OPERATING RANGES[1]

Parameter Symbol	Parameter Description				-5		-7		-10		-12		-14		-15		-18		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output					5		7.5		10		12		14		15		18	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	3.5		5.5		6.5		7		8.5		10		12		ns
				T-type	4		6.5		7.5		8		10		11		13.5		ns
t_H	Register Data Hold Time				0		0		0		0		0		0		0		ns
t_{CO}	Clock to Output					3.5		5		6		8		10		10		12	ns
t_{WL}	Clock Width			LOW	2.5		3		5		6		6		6		7.5		ns
t_{WH}				HIGH	2.5		3		5		6		6		6		7.5		ns
f_{MAX}	Maximum Frequency	External Feedback	$1/(t_S + t_{CO})$	D-type	143		95		80		66.7		54		50		42		MHz
				T-type	133		87		74		62.5		50		47.6		39		MHz
		Internal Feedback (f_{CNT})		D-type	182		133		100		76.9		69		66.6		53		MHz
				T-type	167		125		91		71.4		57		55.5		44		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		200		167		100		83.3		83.3		83.3		66.7		MHz
t_{AR}	Asynchronous Reset to Registered Output					7.5		9.5		11		16		19.5		20		24	ns
t_{ARW}	Asynchronous Reset Width (Note 2)				4.5		5		7.5		12		14.5		15		18		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)				4.5		5		7.5		8		10		10		12		ns
t_{AP}	Asynchronous Preset to Registered Output					7.5		9.5		11		16		19.5		20		24	ns
t_{APW}	Asynchronous Preset Width (Note 2)				4.5		5		7.5		12		14.5		15		18		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)				4.5		5		7.5		8		10		10		12		ns
t_{EA}	Input, I/O, or Feedback to Output Enable					7.5		9.5		10		12		14.5		15		18	ns
t_{ER}	Input, I/O, or Feedback to Output Disable					7.5		9.5		10		12		14.5		15		18	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)					10		10		10		10		10		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)					7		7		7		7		7		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)					3		3		3		3		3		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)					10		10		10		10		10		10		10	ns

Notes:

1. *See "Switching Test Circuit" in the General Information Section of the Vantis 1999 Data Book.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where this parameter may be affected.*
3. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*

MACH131 AND MACH131SP
SWITCHING CHARACTERISTICS OVER OPERATING RANGES[1]

Parameter Symbol	Parameter Description				-5		-7		-10		-12		-14		-15		-18		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output					5.5		7.5		10		12		14		15		18	ns
t_S	Setup Time from Input, I/O, or Feedback			D-type	3.0		5.5		6.5		7		8.5		10		12		ns
				T-type	3.5		6.5		7.5		8		10		11		13.5		ns
t_H	Hold Time				0		0		0		0		0		0		0		ns
t_{CO}	Clock to Output					4		5		6		8		10		10		12	ns
t_{WL}	Clock Width			LOW	2.5		3		4		6		6		6		7.5		ns
t_{WH}				HIGH	2.5		3		4		6		6		6		7.5		ns
f_{MAX}	Maximum Frequency	External Feedback	$1/(t_S + t_{CO})$	D-type	143		95		80		66.7		54		50		42		MHz
				T-type	133		87		74		62.5		50		47.6		39		MHz
		Internal Feedback (f_{CNT})		D-type	182		133		100		76.9		69		66.6		53		MHz
				T-type	167		125		91		71.4		57		55.5		44		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		200		167		125		83.3		83.3		83.3		66.7		MHz
t_{AR}	Asynchronous Reset to Registered Output					8.5		9.5		11		16		19.5		20		24	ns
t_{ARW}	Asynchronous Reset Width (Note 2)				4.5		5		7.5		12		14.5		15		18		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)				4.5		5		7.5		8		10		10		12		ns
t_{AP}	Asynchronous Preset to Registered Output					8.5		9.5		11		16		19.5		20		24	ns
t_{APW}	Asynchronous Preset Width (Note 2)				4.5		5		7.5		12		14.5		15		18		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)				4.5		5		7.5		8		10		10		12		ns
t_{EA}	Input, I/O, or Feedback to Output Enable					7.5		9.5		10		12		14.5		15		18	ns
t_{ER}	Input, I/O, or Feedback to Output Disable					7.5		9.5		10		12		14.5		15		18	ns
t_{LP}	t_{PD} Increase for Powered-Down Macrocell (Note 3)					10		10		10		10		10		10		10	ns
t_{LPS}	t_S Increase for Powered-Down Macrocell (Note 3)					7		7		7		7		7		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-Down Macrocell (Note 3)					3		3		3		3		3		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-Down Macrocell (Note 3)					10		10		10		10		10		10		10	ns

Notes:

1. *See "Switching Test Circuit" in the General Information Section of the Vantis 1999 Data Book..*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where this parameter may be affected.*
3. *If a signal is powered down, this parameter must be added to its respective high-speed parameter.*

MACH211 AND MACH211SP
SWITCHING CHARACTERISTICS OVER OPERATING RANGES [1]

Parameter Symbol	Parameter Description				-6		-7		-10		-12		-14		-15		-18		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output					6		7.5		10		12		14		15		18	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	5		5.5		6.5		7		8.5		10		12		ns
				T-type	5.5		6.5		7.5		8		10		11		13.5		ns
t_H	Register Data Hold Time				0		0		0		0		0		0		0		ns
t_{CO}	Clock to Output					4		4.5		6		8		10		10		12	ns
t_{WL}	Clock Width			LOW	2.5		3		5		6		6		6		7.5		ns
t_{WH}				HIGH	2.5		3		5		6		6		6		7.5		ns
f_{MAX}	Maximum Frequency	External Feedback	$1/(t_S + t_{CO})$	D-type	111		100		80		66.7		54		50		42		MHz
				T-type	105		91		74		62.5		50		47.6		39		MHz
		Internal Feedback (f_{CNT})		D-type	166		133		100		83.3		69		66.6		55.6		MHz
				T-type	150		125		91		76.9		62.5		62.5		51.3		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		200		167		100		83.3		83.3		83.3		66.7		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				5		5.5		6.5		7		8.5		10		12		ns
t_{HL}	Latch Data Hold Time				0		0		0		0		0		0		0		ns
t_{GO}	Gate to Output					7		7 7.5 (note 4)		7 8 (note 5)		10		11		11		13 (note 6) 13.5	ns
t_{GWL}	Gate Width LOW				2.5		3		5		6		6		6		7.5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					9		9.5		12		14		17		17		20 (note 6) 20.5	ns
t_{SIR}	Input Register Setup Time				1.5		2		2		2		2		2		2.5		ns
t_{HIR}	Input Register Hold Time				1.5		2		2		2		2.5		2.5		3.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					10		11		13		15		18		18		20 (note 6) 22	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	8		9		10		12		14.5		15		18		ns
				T-type	9		10		11		13		16		16		19.5		ns
t_{WICL}	Input Register Clock Width			LOW	2.5		3		5		6		6		6		7.5		ns
t_{WICH}				HIGH	2.5		3		5		6		6		6		7.5		ns
f_{MAXIR}	Maximum Input Register Frequency		$1/(t_{WICL} + t_{WICH})$		200		167		100		83.3		83.3		83.3		66.7		MHz
t_{SIL}	Input Latch Setup Time				1.5		2		2		2		2		2		2.5		ns
t_{HIL}	Input Latch Hold Time				1.5		2		2		2		2.5		2.5		3.5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					12		12		14		17		20		20		24	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					13		14		16		19		22		22		26.5	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				7		7.5		8.5		9		11		12		14.5		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				9		10		11		13		16		16		19.5		ns
t_{WIGL}	Input Latch Gate Width LOW				2.5		3		5		6		6		6		7.5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches					12		12.5		14		16		19		19		23	ns

MACH211 AND MACH211SP (CONTINUED)
SWITCHING CHARACTERISTICS OVER OPERATING RANGES [1]

Parameter Symbol	Parameter Description	-6		-7		-10		-12		-14		-15		-18		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{AR}	Asynchronous Reset to Registered or Latched Output		9		9.5		15		16		19.5		20		24	ns
t_{ARW}	Asynchronous Reset Width (Note 2)	4		5		10		12		14.5		15		18		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)	4		5		10		10		10		10		12		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		9		9.5		15		16		19.5		20		24	ns
t_{APW}	Asynchronous Preset Width (Note 2)	4		5		10		12		14.5		15		18		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)	4		5		10		10		10		10		12		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		9		9.5		10		12		14		15		18	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		9		9.5		10		12		14		15		18	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)		10		10		10		10		10		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		10		10		10		10		10		10		10	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		0		0		0		0		0		0		0	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		10		10		10		10		10		10		10	ns

Notes:

1. *See "Switching Test Circuit" in the General Information Section of the Vantis 1999 Data Book.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where this parameter may be affected.*
3. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*
4. *MACH211 t_{GO} = 7 ns. MACH211SP t_{GO} = 7.5 ns.*
5. *MACH211, commercial t_{GO} = 7 ns.*
6. *The faster -18 t_{GO}, t_{PDL}, t_{ICO}, apply to MACH211 only, not MACH211SP.*

MACH221 and MACH221SP
SWITCHING CHARACTERISTICS OVER OPERATING RANGES [1]

Parameter Symbol	Parameter Description				-7		-10		-12		-14		-15		-18		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output					7.5		10		12		14		15		18	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	5.5		6.5		7		8.5		10		12		ns
				T-type	6.5		7.5		8		10		11		13.5		ns
t_H	Register Data Hold Time				0		0		0		0		0		0		ns
t_{CO}	Clock to Output					5		6		8		10		10		12	ns
t_{WL}	Clock Width			LOW	3		5		6		6		6		7.5		ns
t_{WH}				HIGH	3		5		6		6		6		7.5		ns
f_{MAX}	Maximum Frequency	External Feedback	$1/(t_S + t_{CO})$	D-type	95		80		66.7		54		50		42		MHz
				T-type	87		74		62.5		50		47.6		39		MHz
		Internal Feedback (f_{CNT})		D-type	133		100		83.3		69		66.6		55.6		MHz
				T-type	125		91		76.9		62.5		62.5		51.3		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		167		100		83.3		83.3		83.3		66.7		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				5.5		6.5		7		8.5		10		12		ns
t_{HL}	Latch Data Hold Time				0		0		0		0		0		0		ns
t_{GO}	Gate to Output					7		7 (note 2)		10		11		11		13.5	ns
t_{GWL}	Gate Width LOW				3		5		6		6		6		7.5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					9.5		12		14		17		17		20.5	ns
t_{SIR}	Input Register Setup Time				2		2		2		2		2		2.5		ns
t_{HIR}	Input Register Hold Time				2		2		2		2.5		2.5		3.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					11		13		15		18		18		22	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	9		10		12		14.5		15		18		ns
				T-type	10		11		13		16		16		19.5		ns
t_{WICL}	Input Register			LOW	3		5		6		6		6		7.5		ns
t_{WICH}	Clock Width			HIGH	3		5		6		6		6		7.5		ns
f_{MAXIR}	Maximum Input Register Frequency		$1/(t_{WICL} + t_{WICH})$		167		100		83.3		83.3		83.3		66.7		MHz
t_{SIL}	Input Latch Setup Time				2		2		2		2		2		2.5		ns
t_{HIL}	Input Latch Hold Time				2		2		2		2.5		2.5		3.5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					12		14		17		20		20		24	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					14		16		19		22		22		26.5	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				7.5		8.5		9		11		12		14.5		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				10		11		13		16		16		19.5		ns
t_{WIGL}	Input Latch Gate Width LOW				3		5		6		6		6		7.5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches					11.5		14		16		19		19		23	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output					9.5		15		16		19.5		20		24	ns
t_{ARW}	Asynchronous Reset Width (Note 3)				5		10		12		14.5		15		18		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)				5		8		10		10		10		12		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output					9.5		15		16		19.5		20		24	ns

MACH221 and MACH221SP (CONTINUED)
SWITCHING CHARACTERISTICS OVER OPERATING RANGES [1]

Parameter Symbol	Parameter Description	-7		-10		-12		-14		-15		-18		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{APW}	Asynchronous Preset Width (Note 3)	5		10		12		14.5		15		18		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)	5		8		10		10		10		12		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		9.5		12		12		14		15		18	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		9.5		12		12		14		15		18	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 4)		10		10		10		10		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 4)		10		10		10		10		10		10	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 4)		0		0		0		0		0		0	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 4)		10		10		10		10		10		10	ns

Notes:

1. *See "Switching Test Circuits" in the General Information section of the Vantis 1999 Data Book.*
2. *MACH221 t_{GO} = 7 ns. MACH221SP t_{GO} = 8 ns.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where this parameter may be affected.*
4. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*

MACH231 AND MACH231SP
SWITCHING CHARACTERISTICS OVER OPERATING RANGES [1]

Parameter Symbol	Parameter Description				-6		-7		-10		-12		-14		-15		-18		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output					6		7.5		10		12		14		15		18	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	5		5.5		6.5		7		8.5		10		12		ns
				T-type	6		6.5		7.5		8		10		11		13.5		ns
t_H	Register Data Hold Time				0		0		0		0		0		0		0		ns
t_{CO}	Clock to Output					4		5		6.5		8		10		10		12	ns
t_{WL}	Clock Width			LOW	2.5		3		4		6		6		6		7.5		ns
t_{WH}				HIGH	2.5		3		4		6		6		6		7.5		ns
f_{MAX}	Maximum Frequency	External Feedback	$1/(t_S + t_{CO})$	D-type	111		95		77		66.7		54		50		42		MHz
				T-type	100		87		72		62.5		50		47.6		39		MHz
		Internal Feedback (f_{CNT})		D-type	166		133		100		83.3		69		66.6		55.6		MHz
				T-type	150		125		91		76.9		62.5		62.5		51.3		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		200		167		125		83.3		83.3		83.3		66.7		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				5		5.5		6.5		7		8.5		10		12		ns
t_{HL}	Latch Data Hold Time				0		0		0		0		0		0		0		ns
t_{GO}	Gate to Output					5		6		7.5		8.5		11		11		13.5	ns
t_{GWL}	Gate Width LOW				2		3		4		6		6		6		7.5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					9		9.5		14		14.5		17		17		20.5	ns
t_{SIR}	Input Register Setup Time				1.5		2		2		2		2		2		2.5		ns
t_{HIR}	Input Register Hold Time				1.5		2		2.5		2.5		2.5		2.5		3.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					10		11		15.5		16		18		18		22	ns
t_{ICS}	Input Register Clock to output Register Setup			D-type	8		9		11		12		14.5		15		18		ns
				T-type	9		10		12		13		16		16		19.5		ns
t_{WICL}	Input Register Clock Width			LOW	2.5		3		4		6		6		6		7.5		ns
t_{WICH}				HIGH	2.5		3		4		6		6		6		7.5		ns
f_{MAXIR}	Maximum Input Register Frequency				200		167		125		83.3		83.3		83.3		66.7		MHz
t_{SIL}	Input Latch Setup Time				1.5		2		2		2.5		2.5		2.5		2.5		ns
t_{HIL}	Input Latch Hold Time				1.5		2		2.5		3		3		3		3.5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					11		12		17		17		20		20		24	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					13		14		18		19.5		22		22		26.5	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				7		7.5		10		10.5		11		12		14.5		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				9		10		11		13.5		16		16		19.5		ns

MACH231 AND MACH231SP (CONTINUED)
SWITCHING CHARACTERISTICS OVER OPERATING RANGES [1]

Parameter Symbol	Parameter Description	-6		-7		-10		-12		-14		-15		-18		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	2		3		4		6		6		6		7.5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		11		12.5		16		17		19		19		23	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		9		9.5		13		16		19.5		20		24	ns
t_{ARW}	Asynchronous Reset Width (Note 2)	4		5		10		12		14.5		15		18		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)	4		5		7.5		8		10		10		12		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		9		9.5		13		16		19.5		20		24	ns
t_{APW}	Asynchronous Preset Width (Note 2)	4		5		10		12		14.5		15		18		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)	4		5		7.5		8		10		10		12		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		9		9.5		10		12		15		15		18	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		9		9.5		10		12		15		15		18	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)		9		10		10		10		10		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		6		7		7		7		7		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		0		0		0		0		0		0		0	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		9		10		10		10		10		10		10	ns

Notes:

1. *See "Switching Test Circuit" in the General Information section of the Vantis 1999 Data Book.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where this parameter may be affected.*
3. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V	V_{CC} = 5.0V, T_A = 25°C f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V		8	pF

Note:

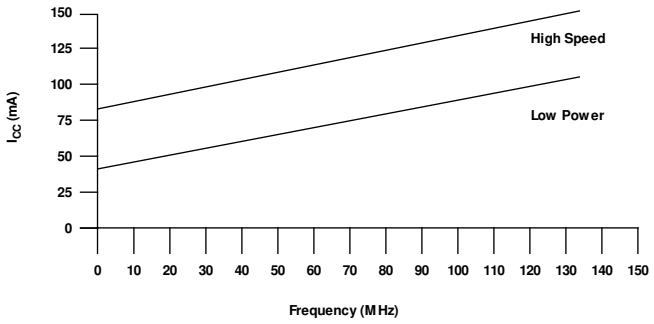
1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where these parameters may be affected.*

I_{CC} vs. FREQUENCY

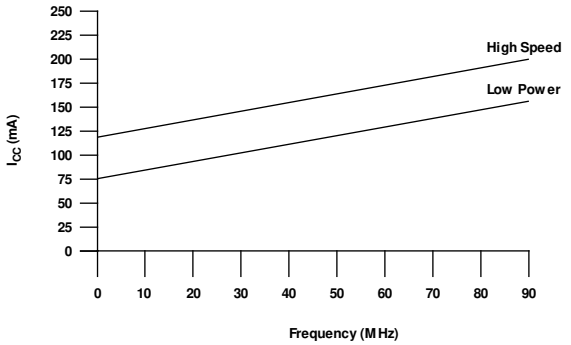
These curves represent the typical power consumption for a particular device at system frequency. The selected "typical" pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register.

T_A = 25°C, V_{CC} =5V

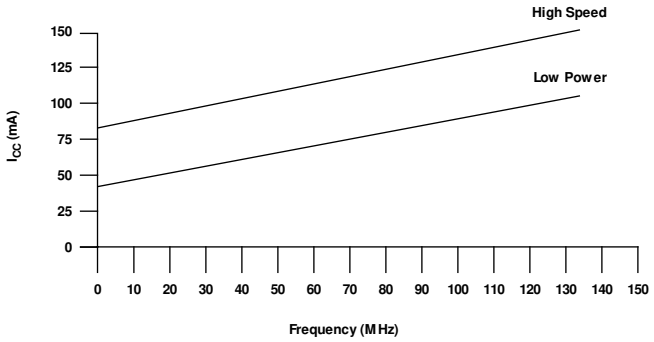
MACH111(SP)



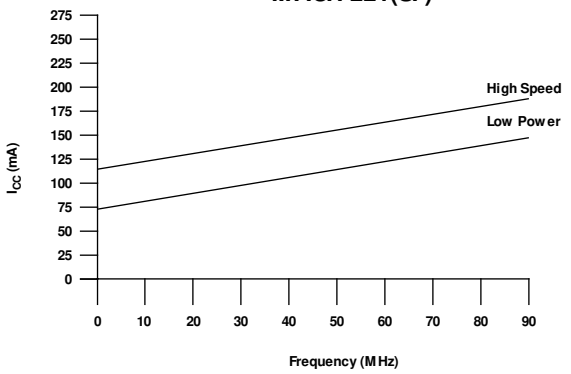
MACH131(SP)



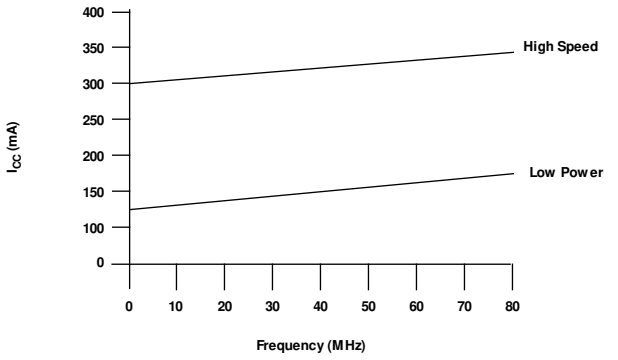
MACH211(SP)



MACH 221(SP)



MACH231



MACH231SP

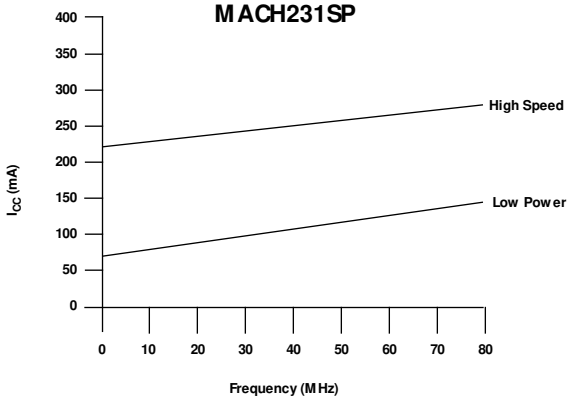


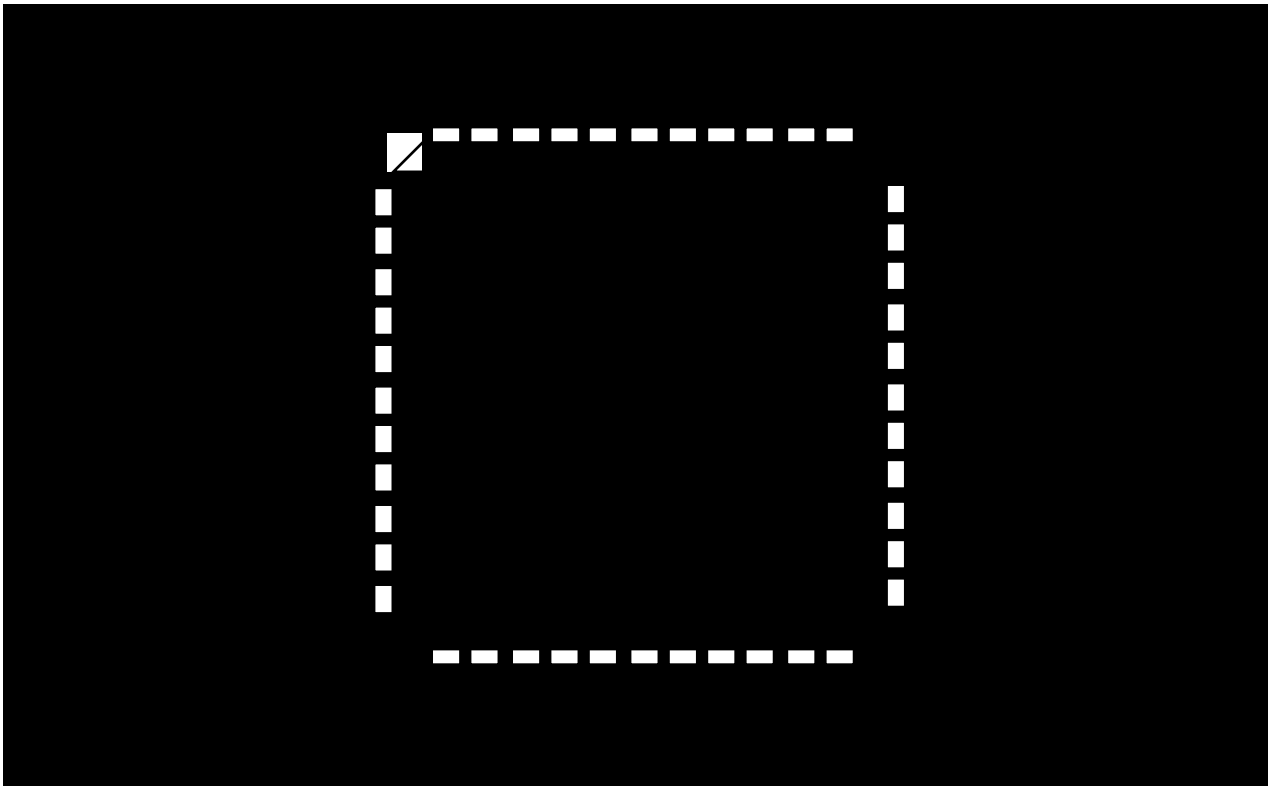
Table 12. I_{CC}

Device	Parameter Symbol	Parameter Description	Test Description	Typ	Unit
MACH111(SP) MACH211(SP)	I_{CC}	Supply Current (Static)	V_{CC} = 5V, T_A = 25°C, f = 0 MHz	40	mA
MACH221(SP)				70	
MACH131(SP)				75	
MACH231SP				80	
MACH231				135	
MACH111(SP) MACH211(SP)		Supply Current (Active)	V_{CC} = 5V, T_A = 25°C, f = 1 MHz	45	
MACH221(SP)				75	
MACH131(SP)				80	
MACH231SP				100	
MACH231				150	

44- PIN PLCC CONNECTION DIAGRAM (MACH111-5/7/10/12/15 AND MACH111SP-5/7/10/12/15)

Top View

44-Pin PLCC



14051K-018

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

Note:

1. Pin designators in parentheses ( ) apply to the MACH111SP

44-PIN TQFP CONNECTION DIAGRAM (MACH111-5/7/10/12/15 AND MACH111SP-5/7/10/12/15)

Top View

44-Pin TQFP

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

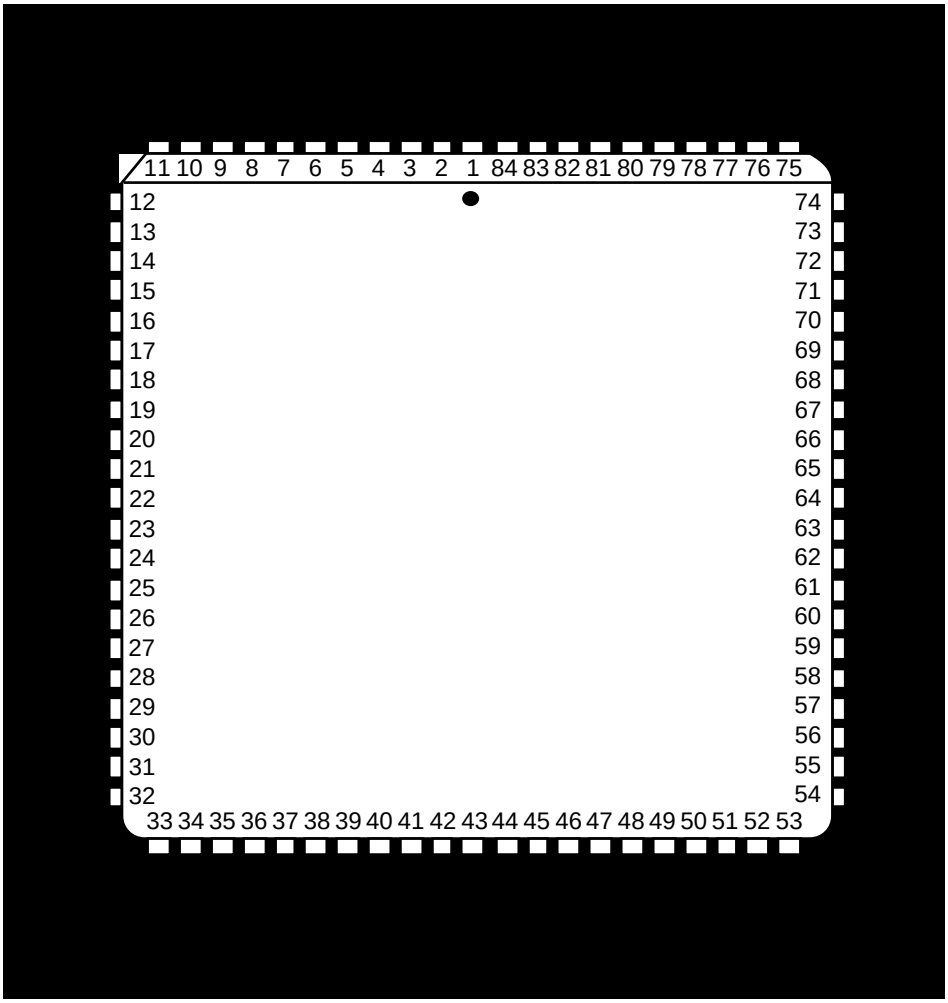
Note:

1. Pin designators in parentheses ( ) apply to the MACH111SP

84-PIN PLCC CONNECTION DIAGRAM (MACH131-5/7/10/12/15)

Top View

84-Pin PLCC



14051K-020

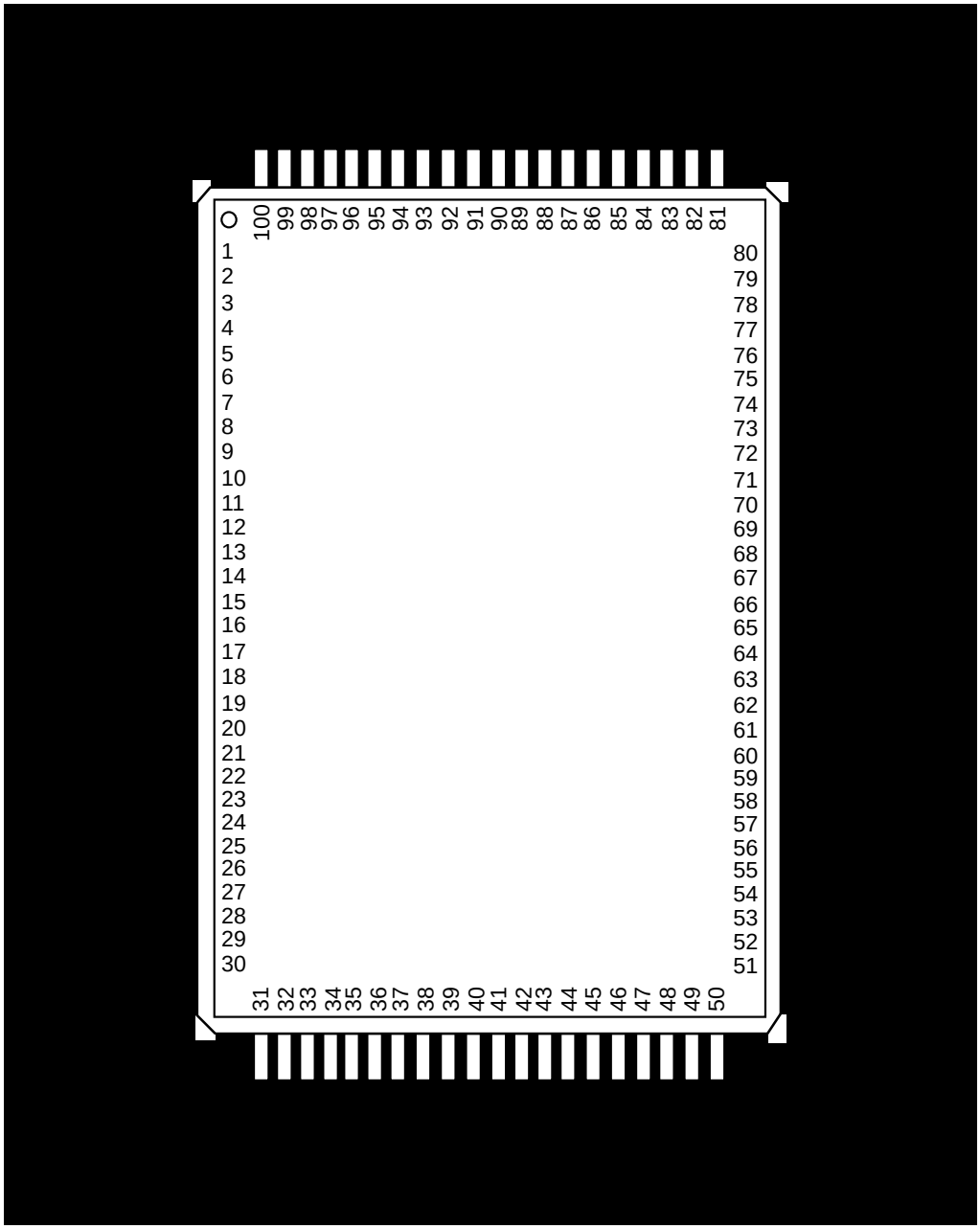
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

100-PIN PQFP CONNECTION DIAGRAM (MACH131SP-5/7/10/12/15)

Top View

100-Pin PQFP



14051K-021

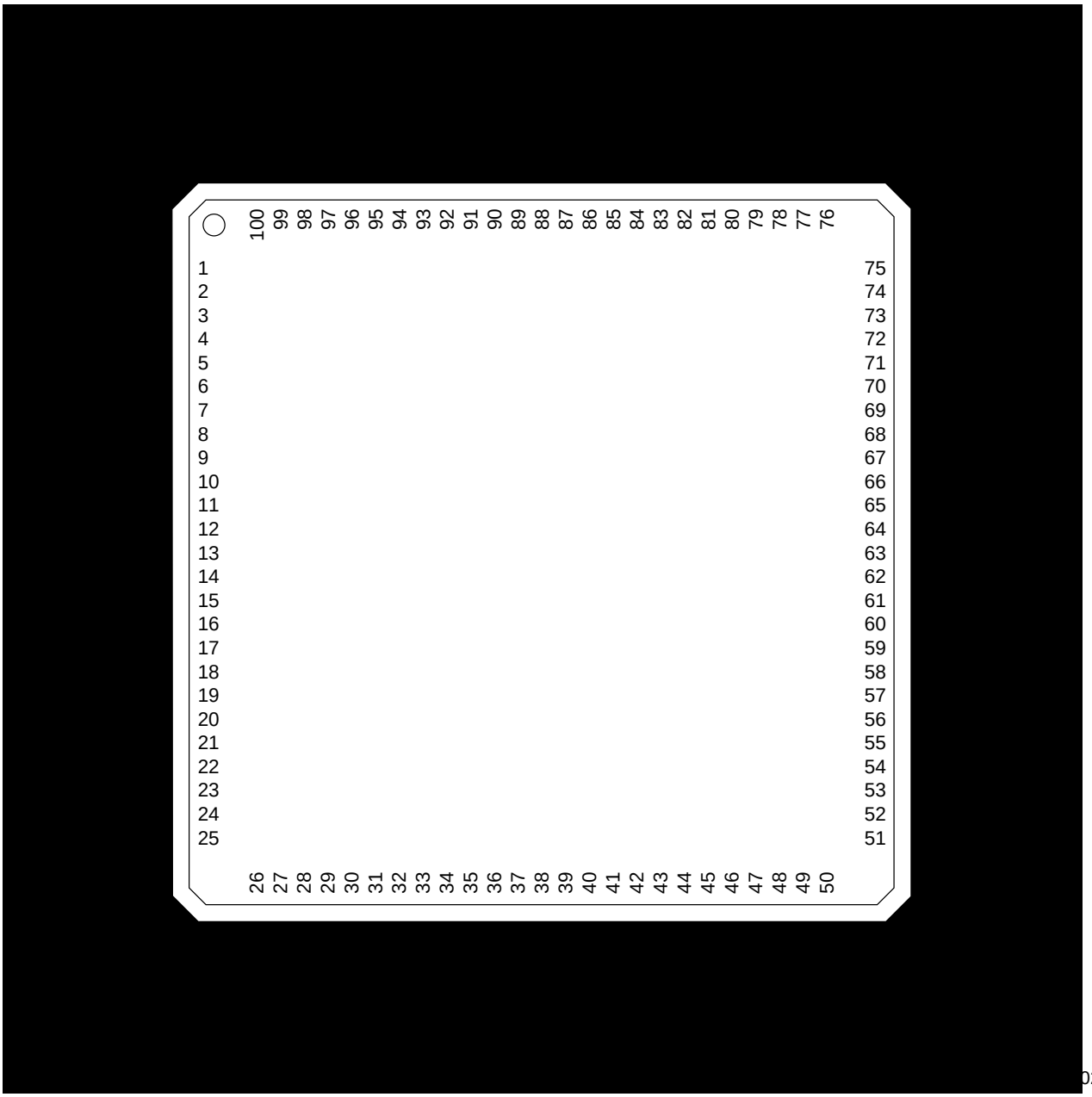
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

100-PIN TQFP CONNECTION DIAGRAM (MACH131SP-5/7/10/12/15)

Top View

100-Pin TQFP



022

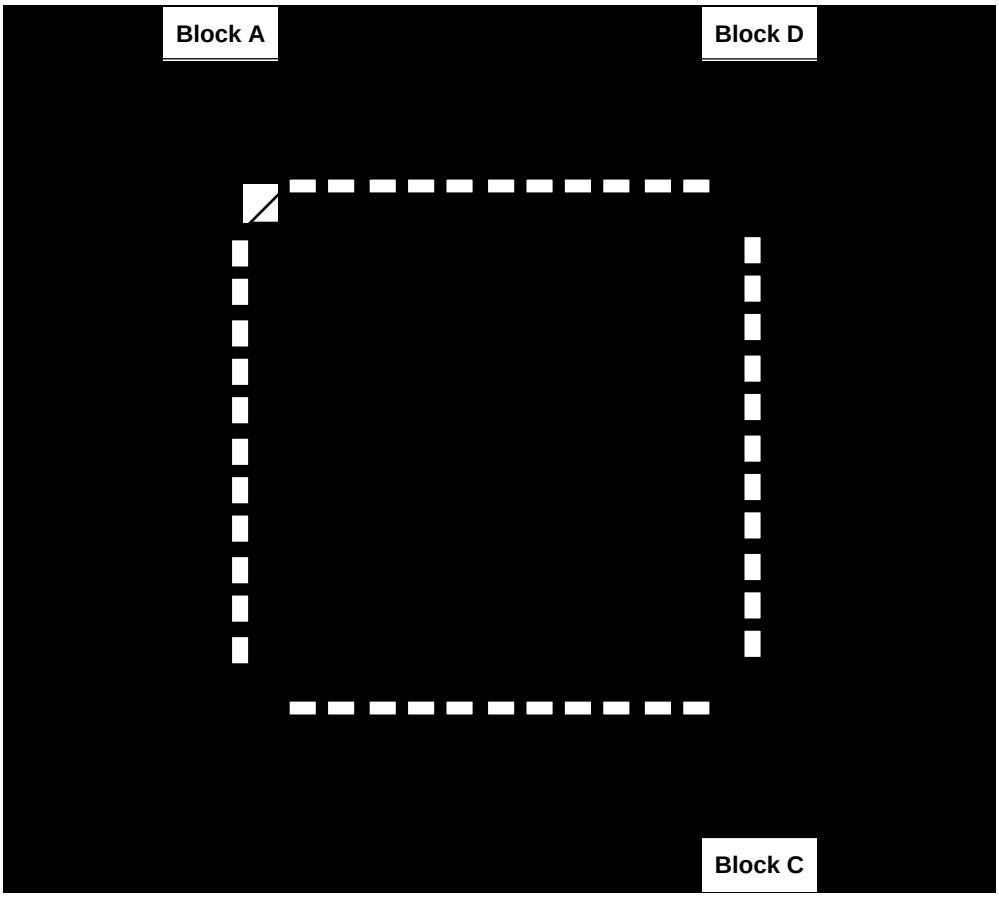
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

44-PIN PLCC CONNECTION DIAGRAM (MACH211-7/10/12/15 AND MACH211SP-6/7/10/12/15)

Top View

44-Pin PLCC



14051K-023

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

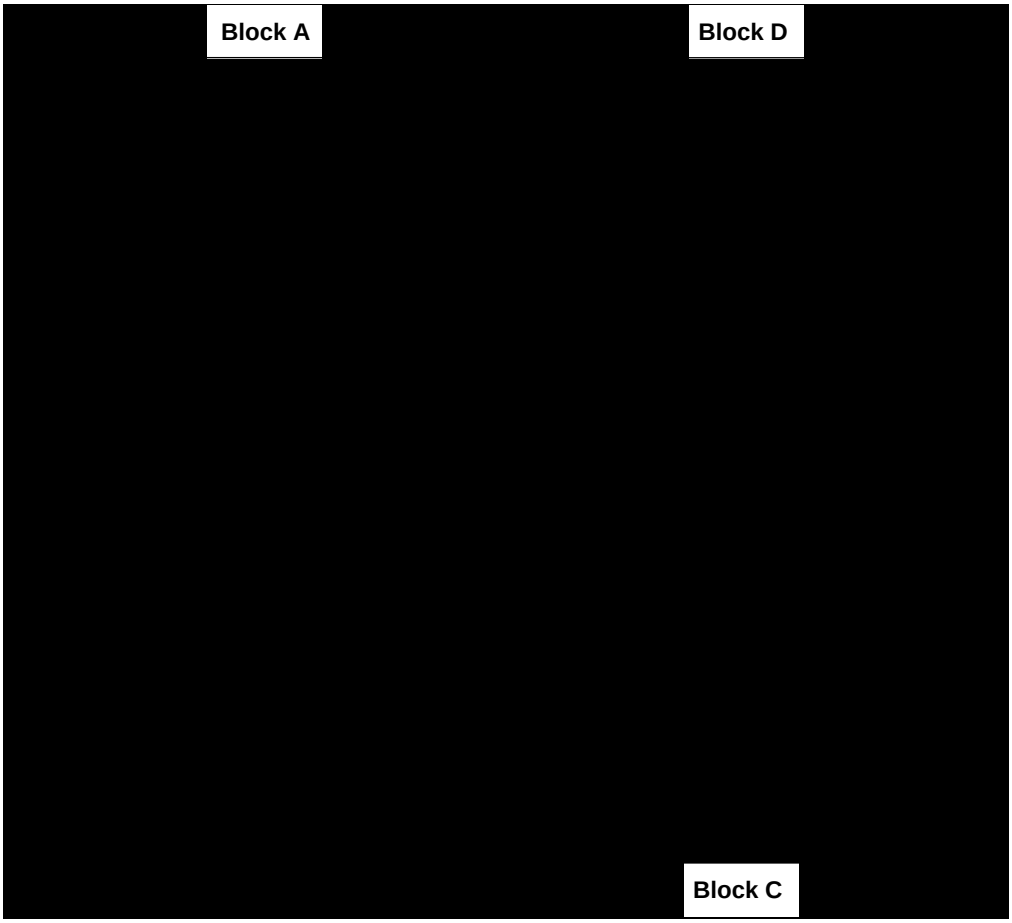
Note:

1. Pin designators in parentheses ( ) apply to the MACH211SP

44-PIN TQFP CONNECTION DIAGRAM (MACH211-7/10/12/15 AND MACH211SP-6/7/10/12/15)

Top View

44-Pin TQFP



14051K-024

PIN DESIGNATIONS

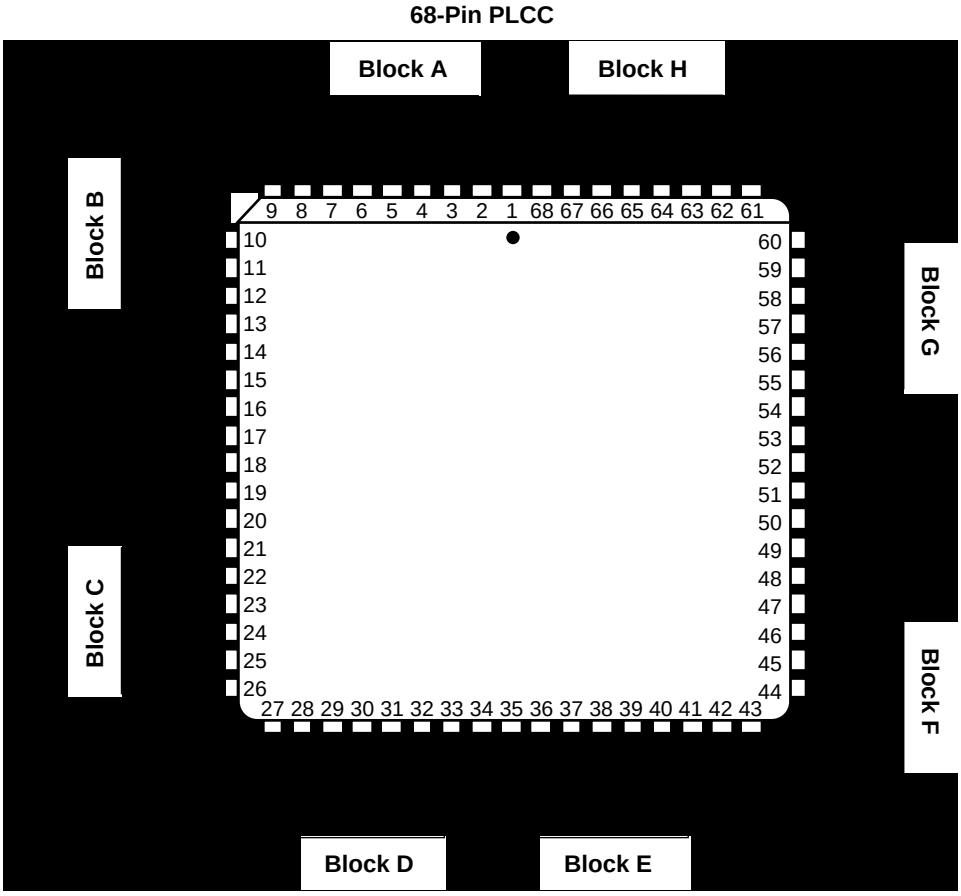
CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

Note:

1. Pin designators in parentheses ( ) apply to the MACH211SP

68-PIN PLCC CONNECTION DIAGRAM (MACH221-7/10/12/15)

Top View



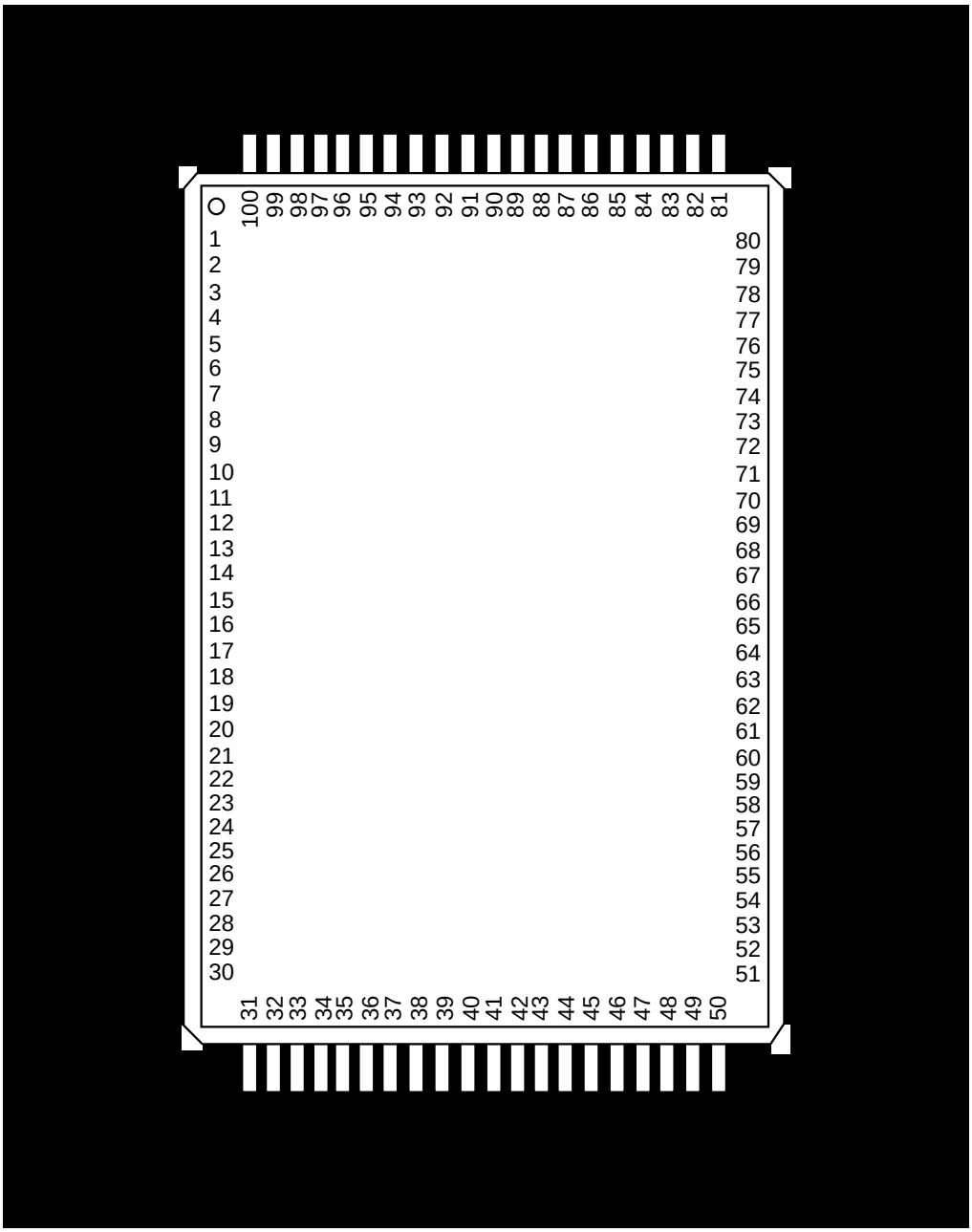
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

100-PIN PQFP CONNECTION DIAGRAM (MACH221SP-7/10/12/15)

Top View

100-Pin PQFP



14051K-026

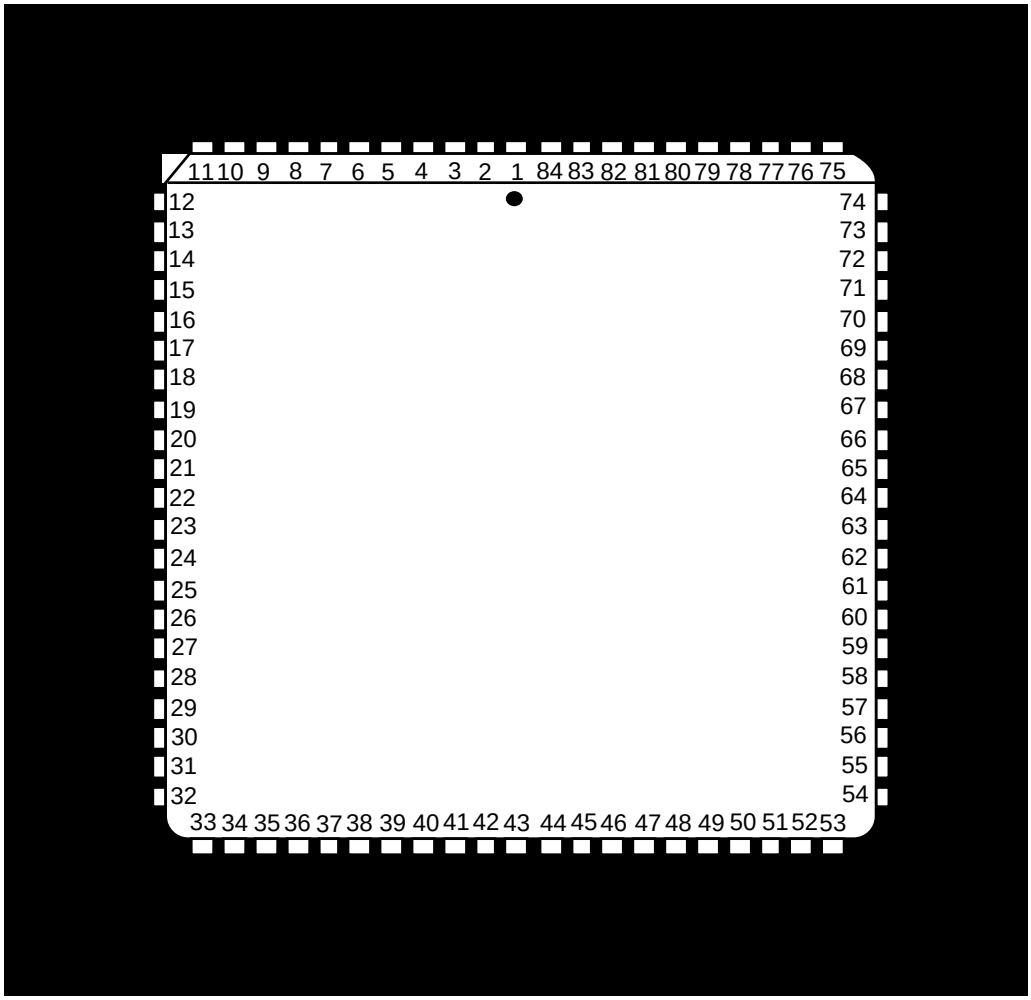
PIN DESIGNATIONS

I/CLK = Input or Clock
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

84-PIN PLCC CONNECTION DIAGRAM (MACH231-6/7/10/12/15)

Top View

84-Pin PLCC



14051K-027

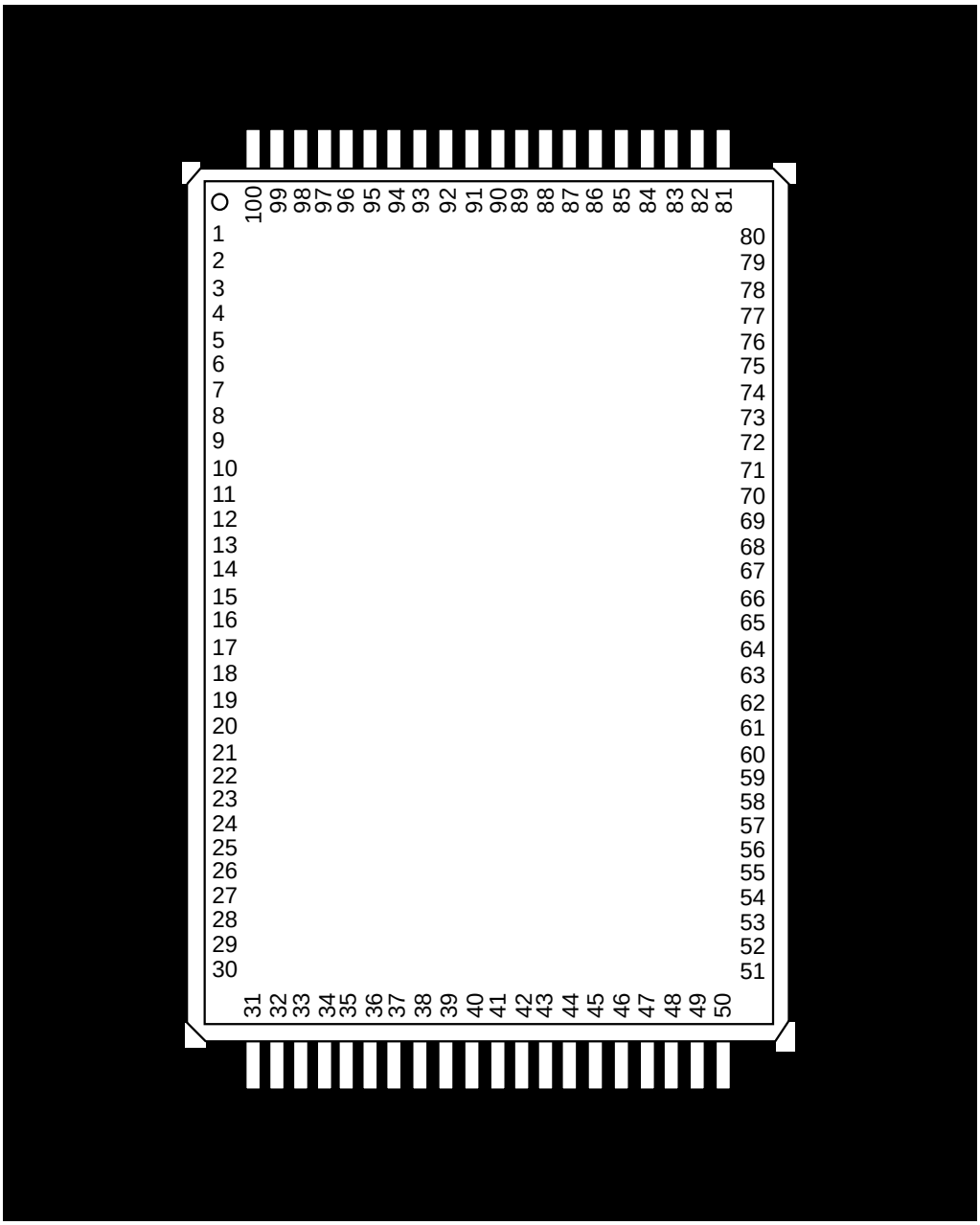
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

100-PIN PQFP CONNECTION DIAGRAM (MACH231SP-10/12/15)

Top View

100-Pin PQFP



14051K-028

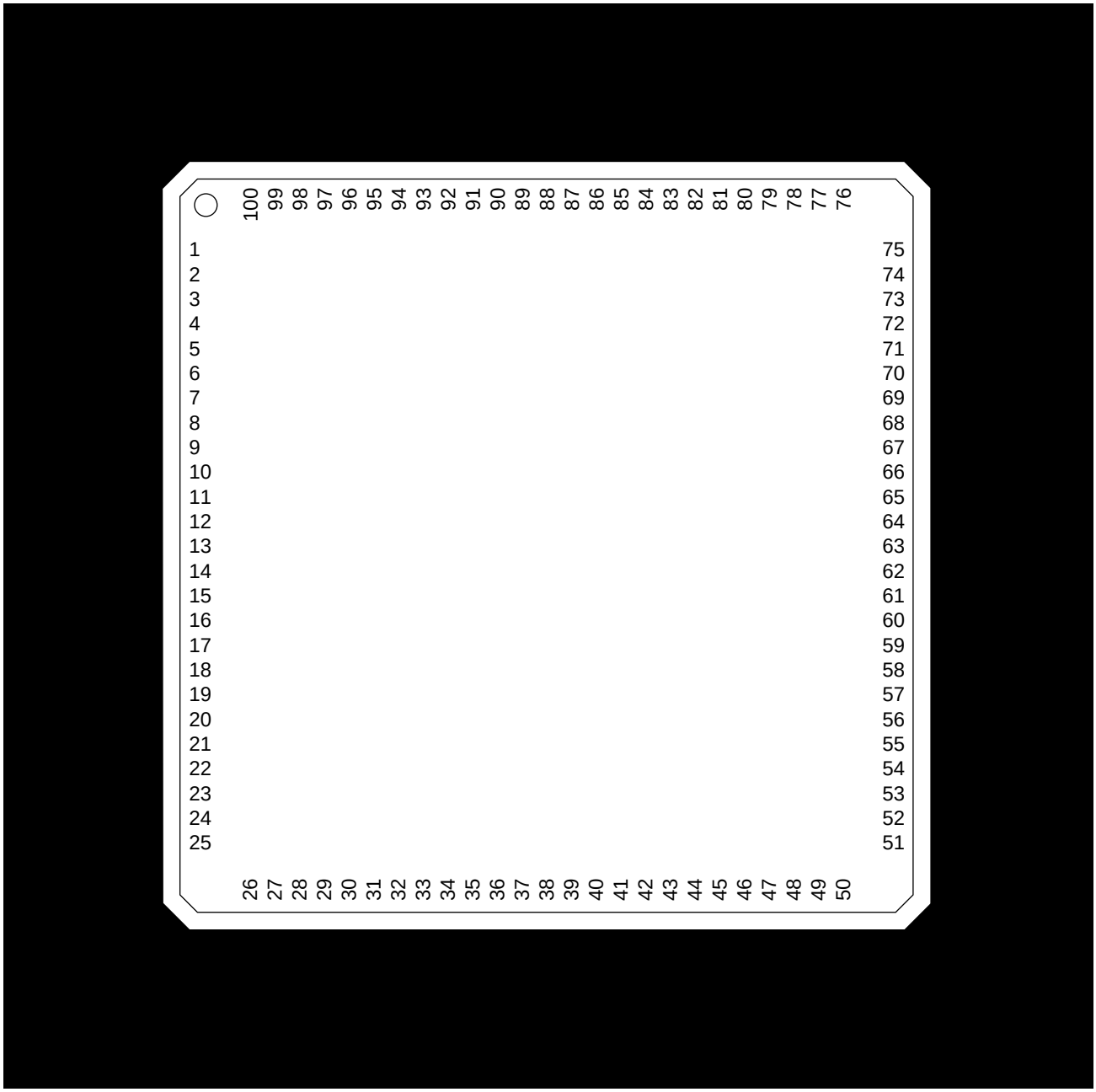
PIN DESIGNATIONS

I/CLK = Input or Clock
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

100-PIN TQFP CONNECTION DIAGRAM (MACH231SP-10/12/15)

Top View

100-Pin TQFP

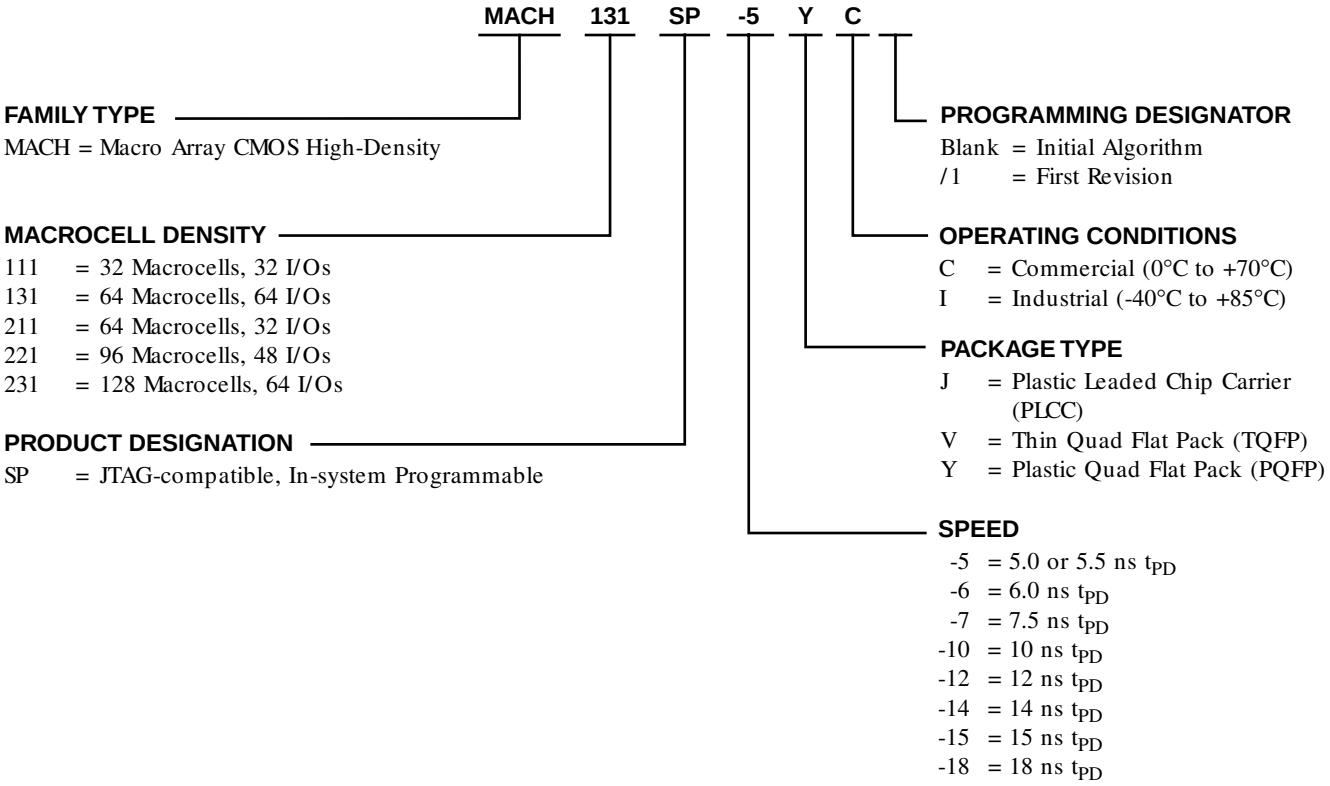


PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

ORDERING INFORMATION

Lattice/Vantis programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations – Commercial		
MACH111	-5, -7, -10, -12, -15	JC, VC
MACH111SP	-5, -7, -10, -12, -15	JC, VC
MACH131	-5, -7, -10, -12, -15	JC/1
MACH131SP	-5, -7, -10, -12, -15	VC, YC
MACH211	-7, -10, -12, -15	JC, VC
MACH211SP	-6, -7, -10, -12, -15	JC, VC
MACH221	-7, -10, -12, -15	JC
MACH221SP	-7, -10, -12, -15	YC
MACH231	-6, -7	JC
	-10, -12, -15	JC/1
MACH231SP	-10, -12, -15	VC, YC

Valid Combinations – Industrial		
MACH111	-7, -10, -12, -14, -18	JI
MACH111SP	-7, -10, -12, -14, -18	JI
MACH131	-7, -10, -12, -14, -18	JI/1
MACH131SP	-7, -10, -12, -14, -18	YI
MACH211	-10, -12, -14, -18	JI
MACH211SP	-10, -12, -14, -18	JI
MACH221	-10, -12, -14, -18	JI
MACH221SP	-10, -12, -14, -18	YI
MACH231	-12, -14, -18	JI/1
MACH231SP	-12, -14, -18	YI

Valid Combinations

The Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice/Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note:

1. *All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e. MACH131SP-5YC-7YI*