

### Analog Peripherals

- **10-Bit ADC**
- 500 ksp/s
- 16 external inputs
- VREF from on-chip VREF, external pin, Internal Regulator or V<sub>DD</sub>
- Internal or external start of conversion source
- Built-in temperature sensor
- **10-Bit Current Output DAC**
- **Comparator**
  - Programmable hysteresis and response time
  - Configurable as interrupt or reset source
  - Low current (<0.5  $\mu$ A)

### On-Chip Debug

- C8051F336 can be used as code development platform; Complete development kit available
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug
- Provides breakpoints, single stepping, inspect/modify memory and registers

### Supply Voltage 1.8 to 3.6 V

- On-chip LDO for internal core supply
- Built-in voltage supply monitor

**Temperature Range: -40 to +85 °C**

### High-Speed 8051 $\mu$ C Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

### Memory

- 768 Bytes RAM
- 8 kB byte-programmable EPROM code memory

### Digital Peripherals

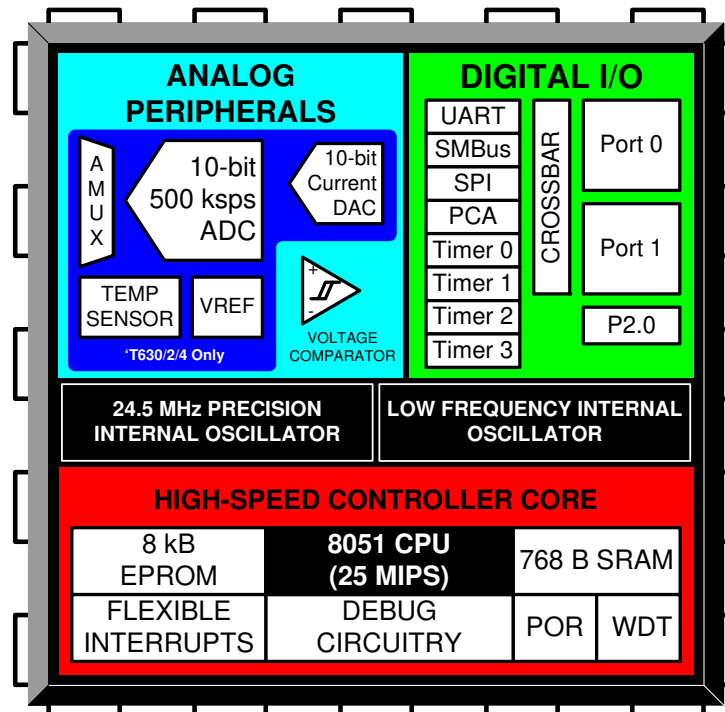
- 17 Port I/O with high sink current capability
- Hardware enhanced UART, SMBus™, and enhanced SPI™ serial ports
- Four general purpose 16-bit counter/timers
  - Timer 3 supports real-time clock using external clock source
- 16-Bit programmable counter array (PCA) with three capture/compare modules and enhanced PWM functionality

### Clock Sources

- Two internal oscillators:
  - 24.5 MHz with  $\pm$ 2% accuracy supports crystal-less UART operation and low-power suspend mode with fast wake time
  - 80/40/20/10 kHz low frequency, low power operation
- External oscillator: RC, C, or CMOS Clock
- Switch between clock sources on-the-fly; useful in power saving modes

### Full Technical Data Sheet

- C8051T630/1/2/3/4/5



# C8051T630-GDI

## 1. Ordering Information

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	EPROM Memory (Bytes)	RAM (Bytes)	Calibrated Internal 24.5 MHz Oscillator	Internal 80 kHz Oscillator	SMBus/I <sup>2</sup> C	Enhanced SPI	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 500ksps ADC	10-bit Current Output DAC	Internal Voltage Reference	Temperature Sensor	Analog Comparator	Package
C8051T630-GDI	25	8k*	768	Y	Y	Y	Y	Y	4	Y	17	Y	Y	Y	Y	Y	Tested Die in Wafer Form
*Note: 512 bytes reserved for factory use																	

## 2. Pin Definitions

Table 2.1 lists the pin definitions for the C8051T630-GDI. For a complete description of the operation of each pin, refer to technical data sheet C8051T630/1/2/3/4/5.

**Table 2.1. Pin Definitions for the C8051T630-GDI**

Name	Physical Pad Number	Type	Description
V <sub>DD</sub>	3	Pin	Power Supply Voltage.
GND	2	G	Ground.
$\overline{\text{RST}}$	4	D I/O	Device Reset. Open-drain output of internal POR or V <sub>DD</sub> monitor. An external source can initiate a system reset by driving this pin low for at least 10 $\mu\text{s}$ .
C2CK		D I/O	Clock signal for the C2 Debug Interface.
P2.0/	5	D I/O	Port 2.0.
C2D		D I/O	Bi-directional data signal for the C2 Debug Interface.
P0.0/	1	D I/O or A In	Port 0.0.
VREF		A In	External VREF input.
P0.1	21	D I/O or A In	Port 0.1.
IDA0		AOut	IDA0 Output.
P0.2/	20	D I/O or A In	Port 0.2.
V <sub>PP</sub>	19	A In	V <sub>PP</sub> Programming Supply Voltage
P0.3/	18	D I/O or A In	Port 0.3.
EXTCLK		A I/O or D In	External Clock Pin. This pin can be used as the external clock input for CMOS, capacitor, or RC oscillator configurations.
P0.4	17	D I/O or A In	Port 0.4.
P0.5	16	D I/O or A In	Port 0.5.

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Table 2.1. Pin Definitions for the C8051T630-GDI (Continued)

Name	Physical Pad Number	Type	Description
P0.6/ CNVSTR	15	D I/O or A In  D In	Port 0.6.  ADC0 External Convert Start or IDA0 Update Source Input.
P0.7	14	D I/O or A In	Port 0.7.
P1.0	13	D I/O or A In	Port 1.0.
P1.1	12	D I/O or A In	Port 1.1.
P1.2	11	D I/O or A In	Port 1.2.
P1.3	10	D I/O or A In	Port 1.3.
P1.4	9	D I/O or A In	Port 1.4.
P1.5	8	D I/O or A In	Port 1.5.
P1.6	7	D I/O or A In	Port 1.6.
P1.7	6	D I/O or A In	Port 1.7.

## 3. Bonding Instructions

**Table 3.1. Bond Pad Coordinates (Relative to Center of Die)**

Physical Pad Number	Example Package Pin Number (QFN-20)	Package Pin Name	Physical Pad X (μm)	Physical Pad Y (μm)
1	1	P0.0	-689	451
2	2	GND	-689	-53
3	3	VDD	-689	-152
4	4	RESET_B	-689	-282
5	5	P2.0	-689	-459
6	6	P1.7	-493	-655
7	7	P1.6	-336	-655
8	8	P1.5	-194	-655
9	9	P1.4	337	-655
10	10	P1.3	494	-655
11	11	P1.2	689	-167
12	12	P1.1	689	-11
13	13	P1.0	689	132
14	14	P0.7	689	309
15	15	P0.6	689	451
16	16	P0.5	466	654
17	17	P0.4	324	654
18	18	P0.3	167	654
19	19	VPP	-193	654
20	19	P0.2	-343	654
21	20	P0.1	-486	654

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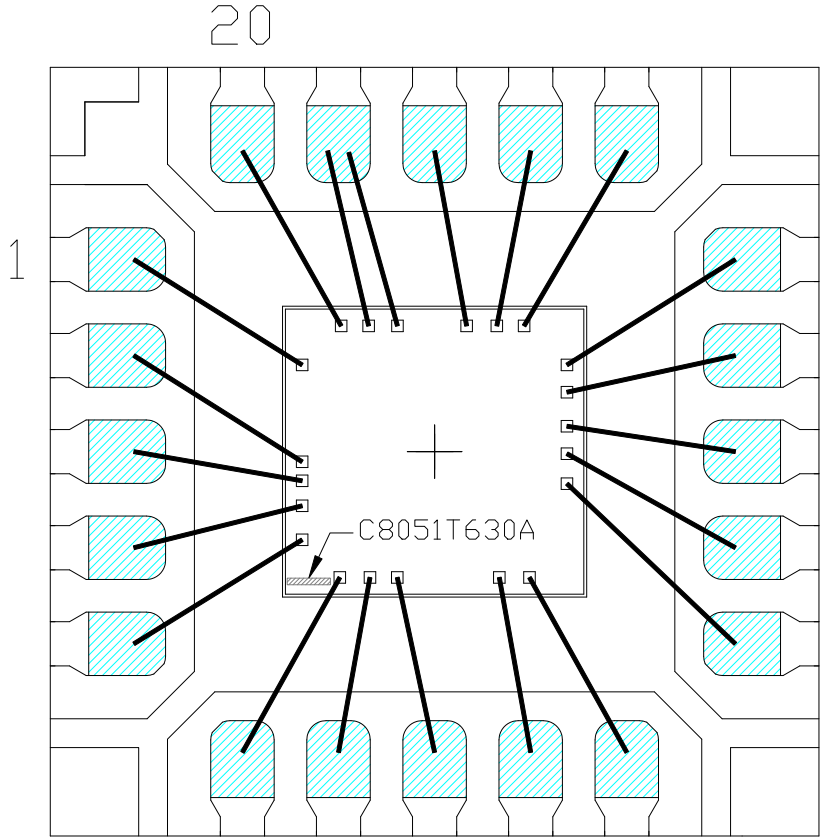


Figure 3.1. Die Bonding (QFN-20)

**Table 3.2. Wafer and Die Information**

<b>Wafer ID</b>	C8051T630A
<b>Wafer Dimensions</b>	8 in.
<b>Die Dimensions</b>	1.58 mm x 1.51 mm
<b>Wafer Thickness</b>	12 mil $\pm$ 0.6 mil
<b>Wafer Identification</b>	Notch
<b>Scribe Line Width</b>	80u
<b>Die per Wafer*</b>	Contact Sales for info
<b>Passivation</b>	Standard
<b>Wafer Packaging Detail</b>	Wafer Jar
<b>Bond Pad Dimensions</b>	60 $\mu$ m x 60 $\mu$ m
<b>Maximum Processing Temperature</b>	250 °C
<b>Electronic Die Map Format</b>	.txt
<b>Bond Pad Pitch Minimum</b>	99 $\mu$ m
<b>*Note:</b> This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).	

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## 4. Wafer Storage Guidelines

It is necessary to conform to appropriate wafer storage practices to avoid product degradation or contamination.

- Wafers may be stored for up to 18 months in the original packaging supplied by Silicon Labs.
- Wafers must be stored at a temperature of 18–24 °C.
- Wafers must be stored in a humidity-controlled environment with a relative humidity of <30%.
- Wafers should be stored in a clean, dry, inert atmosphere (e.g. nitrogen or clean, dry air).



## DOCUMENT CHANGE LIST

### Revision 1.0 to Revision 1.1

- Changed Wafer Packaging Detail to “Wafer Jar” in Table 3.2 on page 7.

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