MC1600 Series (-30°C to +85°C)

The requirement for digital systems with ever higher performance has increased the need for high-speed integrated circuits. The industry has recognized that the only economical way to obtain high operating system speed is through the use of emitter-coupled logic. Motorola offers a state-of-the-art, emitter-coupled logic family with sub-nanosecond propagation delays – MECL III.

MECL III circuit design is similar to that used in the popular MECL 10,000 family. In the MECL III line, as well as MECL 10,000, advanced processing techniques are employed and the capability for driving low-impedance terminated lines is provided. MECL III is recommended for new designs.

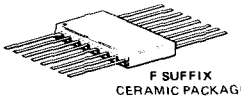
2

GENERAL FEATURES

- Gate Switching Speeds of 1.0 ns typical
- Capability of Driving Terminated Lines with Impedance as Low as 50 Ohms
- Flip-Flop Toggle Rate Greater Than 500 MHz
- Operation with Unused Inputs Left Open
- Multilayer Metalization for economy
- New Packages with Improved Electrical and Thermal Characteristics
- Compatibility with MECL 10,000 Series
- Counting Speeds to above 1 GHz

P SUFFIX
PLASTIC PACKAGE
CASE 646

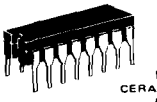
L SUFFIX
CERAMIC PACKAGE
CASE 632



F SUFFIX
CERAMIC PACKAGE
CASE 650

P SUFFIX
PLASTIC PACKAGE
CASE 648

F SUFFIX
CERAMIC PACKAGE
CASE 607



L SUFFIX
CERAMIC PACKAGE
CASE 620

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C unless otherwise noted.)

Function	Type ① -30° to +85°C	Loading Factor # Each Output	Propagation Delay 50-ohm Load ns typ	Power Dissipation (No Load) mW typ/pkg	Case
Voltage Controlled Oscillator	MC1648	–	*225 MHz typ	150	607,632,646
Dual A/D Comparator	MC1650	70	3.5	275	620,650
Dual A/D Comparator	MC1651	70	3.0	275	620,650
Binary Counter	MC1654	70	*325 MHz typ	750 ⌐⌐⌐	620
Voltage-Controlled Multivibrator	MC1658	70	*150 MHz typ	125	620,648,650
Dual 4-Input OR/NOR Gate	MC1660	70	1.1	120	620,650
Quad 2-Input NOR Gate	MC1662	70	1.1	240	620,650
Quad 2-Input OR Gate	MC1664	70	1.1	240	620,650
Dual Clocked R-S Flip-Flop	MC1666	70	1.8	220	620,650
Dual Clocked Latch	MC1668	70	1.8	220	620,650
Master-Slave Type D Flip-Flop	MC1670	70	*350 MHz typ	220	620,650
Triple 2-Input Exclusive OR Gate	MC1672	70	1.3	220	620,650
Triple 2-Input Exclusive NOR Gate	MC1674	70	1.3	220	620,650
Bi-Quinary Counter	MC1678	70	*350 MHz typ	750 ⌐⌐⌐	620
Dual 4-5-Input OR/NOR Gate	MC1688	70	0.8	125	650
UHF Prescaler Type D Flip-Flop	MC1690	70	*500 MHz min	200	620,650
Quad Line Receiver	MC1692	70	1.1	220	620,650
4-Bit Shift Register	MC1694	70	*325 MHz typ	750 ⌐⌐⌐	620
1 GHz Divide-By-Ten Counter	MC1696	–	*1 GHz min	650	650

① L suffix denotes Dual In-Line Ceramic Package, F suffix denotes Ceramic Flat Package, P suffix denotes Dual In-Line Plastic Package. (i.e., MC1600L = Ceramic Dual In-Line Package, MC1600F = Ceramic Flat Package, MC1600P = Plastic Dual In-Line Package).

⌐⌐⌐ Requires Heat Sink – IERC-LIC-214A2WCB or equivalent.

*Toggle Frequency

#DC Loading Factors are based on:

1. Full load output current, I_L = -25 mAdc max
2. Maximum input current, I_{in} = 350 μAdc

Numbers at ends of terminals denote pin numbers for L package (Case 620 unless noted as Case 632) and P package (Case 646 unless noted as Case 648).

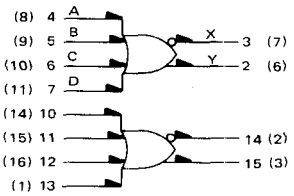
Numbers in parenthesis denote pin numbers for F package (Case 650 unless noted as Case 607).

CASE	V_{CC}	V_{EE}
	Pin No.	Pin No.
650	4,5	12
620	1, 16	8

See individual drawing for devices with other Cases.

GATES

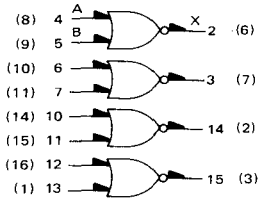
MC1660
Dual 4-Input OR/NOR Gate



$X = \overline{A+B+C+D}$
$Y = A+B+C+D$

t_{pd} = 0.9 ns typ (510-ohm load)
1.1 ns typ (50-ohm load)
P_D = 120 mW typ/pkg (no load)

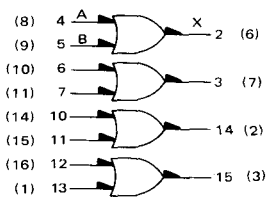
MC1662
Quad 2-Input NOR Gate



$X = \overline{A+B}$

t_{pd} = 0.9 ns typ (510-ohm load)
1.1 ns typ (50-ohm load)
P_D = 240 mW typ/pkg (no load)

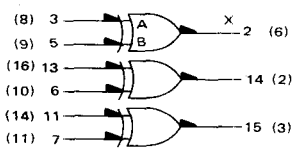
MC1664
Quad 2-Input OR Gate



$X = A+B$

t_{pd} = 0.9 ns typ (510-ohm load)
1.1 ns typ (50-ohm load)
P_D = 240 mW typ/pkg (no load)

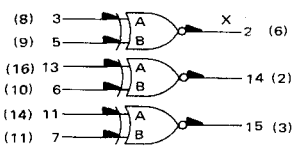
MC1672
Triple 2-Input Exclusive OR Gate



$X = A \bullet \bar{B} + \bar{A} \bullet B$

t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns typ (50-ohm load)
P_D = 220 mW typ/pkg

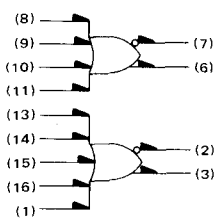
MC1674
Triple 2-Input Exclusive NOR Gate



$X = A \bullet B + \bar{A} \bullet \bar{B}$

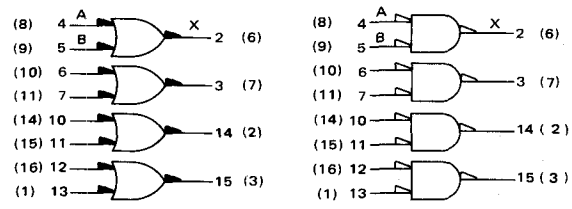
t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns type (50-ohm load)
P_D = 220 mW typ/pkg

MC1688
Dual 4-5-Input OR/NOR Gate



t_{pd} = 0.8 ns typ
P_D = 125 mW typ/pkg (No Load)

MC1664



X = A + B X = A • B

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

Number at end of terminals denotes pin number of L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

Four 2-input OR or AND gating functions in a single package. An internal bias reference voltage insures that the threshold point remains in the center of the transition region over the temperature range -30 to +85°C.

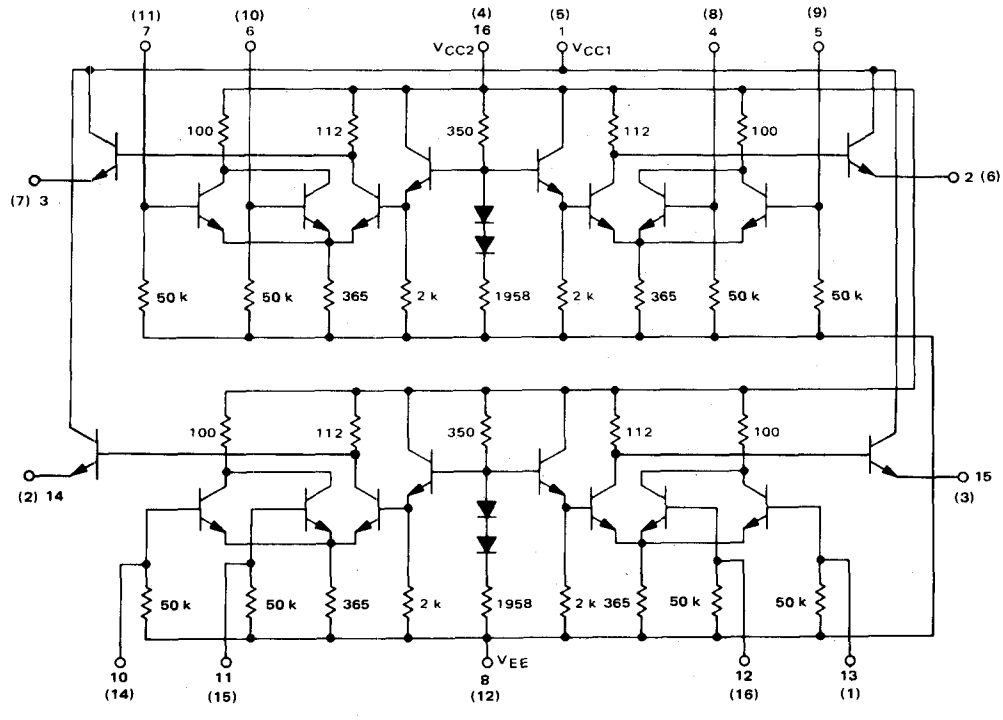
Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

4

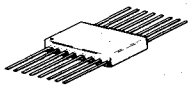
CIRCUIT SCHEMATIC



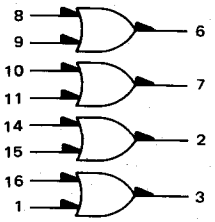
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. Air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



F SUFFIX
CERAMIC PACKAGE
CASE 650



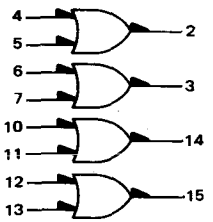
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

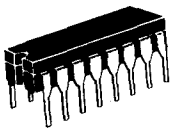
Characteristic	Symbol	Pin Under Test	MC1664F Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	–	–	56	–	–	mAdc	–	–	–	–	12	4,5
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μAdc	*	–	–	–	12	4,5
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	8	–	–	–	12	4,5
		6	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	8	–	–	12	4,5
		6	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	9	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	8	–	12	4,5
		6	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	9	–	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	6	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	8	12	4,5
		6	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	9	12	4,5
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{8+6+}	6	–	1.6	–	1.5	–	1.7	ns	8	6	–	–	12	4,5
	t_{8-6-}	6	–	1.8	–	1.7	–	1.9	ns	8	6	–	–	12	4,5
Rise Time	t_{6+}	6	–	2.2	–	2.1	–	2.3	ns	8	6	–	–	12	4,5
Fall Time	t_{6-}	6	–	2.2	–	2.1	–	2.3	ns	8	6	–	–	12	4,5

*Individually test each input applying V_{IH} or V_{IL} to input under test.

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





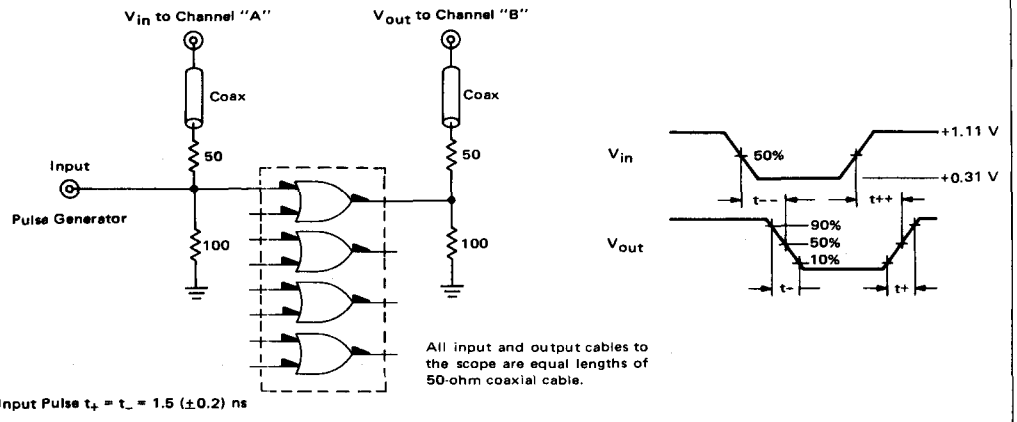
L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	MC1664L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	56	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	4	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	5	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	4	–	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	4	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	5	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	–	1.6	–	1.5	–	1.7	ns	4	2	–	–	8	1,16
	t_{4-2-}	2	–	1.8	–	1.7	–	1.9	ns	4	2	–	–	8	1,16
Rise Time	t_{2+}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{2-}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Input Pulse $t_+ = t_- = 1.5\ (\pm 0.2)$ ns

Unused outputs connected to a 50-ohm resistor to ground.

4