

**SN5412, SN54LS12
SN7412, SN74LS12**

SDLS040 TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

DECEMBER 1983—REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

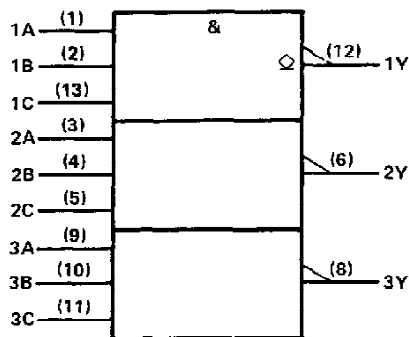
These devices contain three independent 3-input NAND gates with open-collector outputs. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN5412 and SN54LS12 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7412 and SN74LS12 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol†

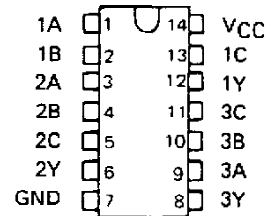


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

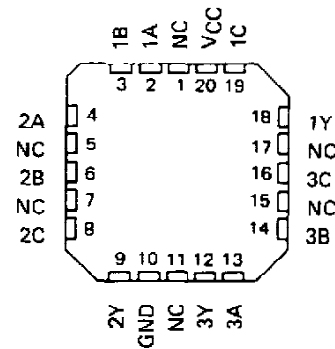
SN5412, SN54LS12 . . . J OR W PACKAGE
SN7412 . . . N PACKAGE
SN74LS12 . . . D OR N PACKAGE

(TOP VIEW)



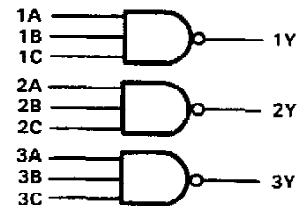
SN54LS12 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



$$Y = \overline{A \cdot B \cdot C} \text{ or}$$

$$Y = \overline{A} + \overline{B} + \overline{C}$$

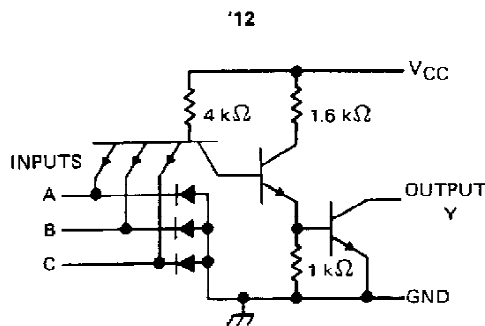
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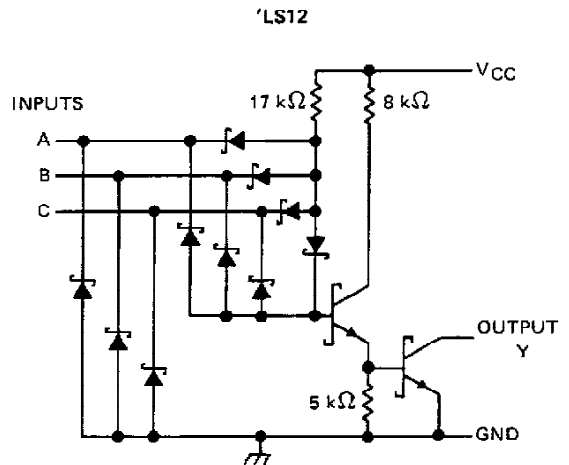
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SN5412, SN54LS12
SN7412, SN74LS12
TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

schematics (each gate)



Resistor values shown are nominal.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '12	5.5 V
'LS12	7 V
Off-state output voltage	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SN5412, SN5412

TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN5412			SN7412			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
V _{OH} High-level output voltage			5.5			5.5	V
I _{OL} Low-level output current			16			16	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5412			SN7412			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IK}	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V	
I _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, V _{OH} = 5.5 V						0.25	mA	
	V _{CC} = MIN, V _{IL} = 0.7 V, V _{OH} = 5.5 V			0.25					
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA			0.2	0.4		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA	
I _{IH}	V _{CC} = MAX, V _I = 2.4 V			40			40	μA	
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-1.6			-1.6	mA	
I _{CCH}	V _{CC} = MAX, V _I = 0			3	6		3	6	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V			9	16.5		9	16.5	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	A, B or C	Y	R _L = 4 kΩ,	C _L = 15 pF		35	45	ns
t _{PHL}			R _L = 400 Ω,	C _L = 15 pF		8	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.


TEXAS INSTRUMENTS

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SN54LS12, SN74LS12

TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	SN54LS12			SN74LS12			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
V _{OH} High-level output voltage			5.5			5.5	V
I _{OL} Low-level output current			4			8	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS12			SN74LS12			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA		-1.5			-1.5	V	
I _{OH}	V _{CC} = MIN, V _{IL} = MAX, V _{OH} = 5.5 V		0.1			0.1	mA	
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 8 mA					0.35	0.5	
I _I	V _{CC} = MAX, V _I = 7 V		0.1			0.1	mA	
I _{IH}	V _{CC} = MAX, V _I = 2.7 V		20			20	μA	
I _{IL}	V _{CC} = MAX, V _I = 0.4 V		-0.4			-0.4	mA	
I _{CCCH}	V _{CC} = MAX, V _I = 0		0.7	1.4		0.7	1.4	mA
I _{CCCL}	V _{CC} = MAX, V _I = 4.5 V		1.8	3.3		1.8	3.3	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A, B or C	Y	R _L = 2 kΩ, C _L = 15 pF		17	32	ns
t _{PHL}					15	28	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TEXAS
INSTRUMENTS

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN5412J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SN7412N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN7412N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS12D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		
SN74LS12D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		
SN74LS12DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		
SN74LS12DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		
SN74LS12N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS12N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS12N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS12N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SNJ5412J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SNJ5412J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SNJ5412W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	-55 to 125		
SNJ5412W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN5412, SN7412 :

- Catalog: [SN7412](#)
- Military: [SN5412](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

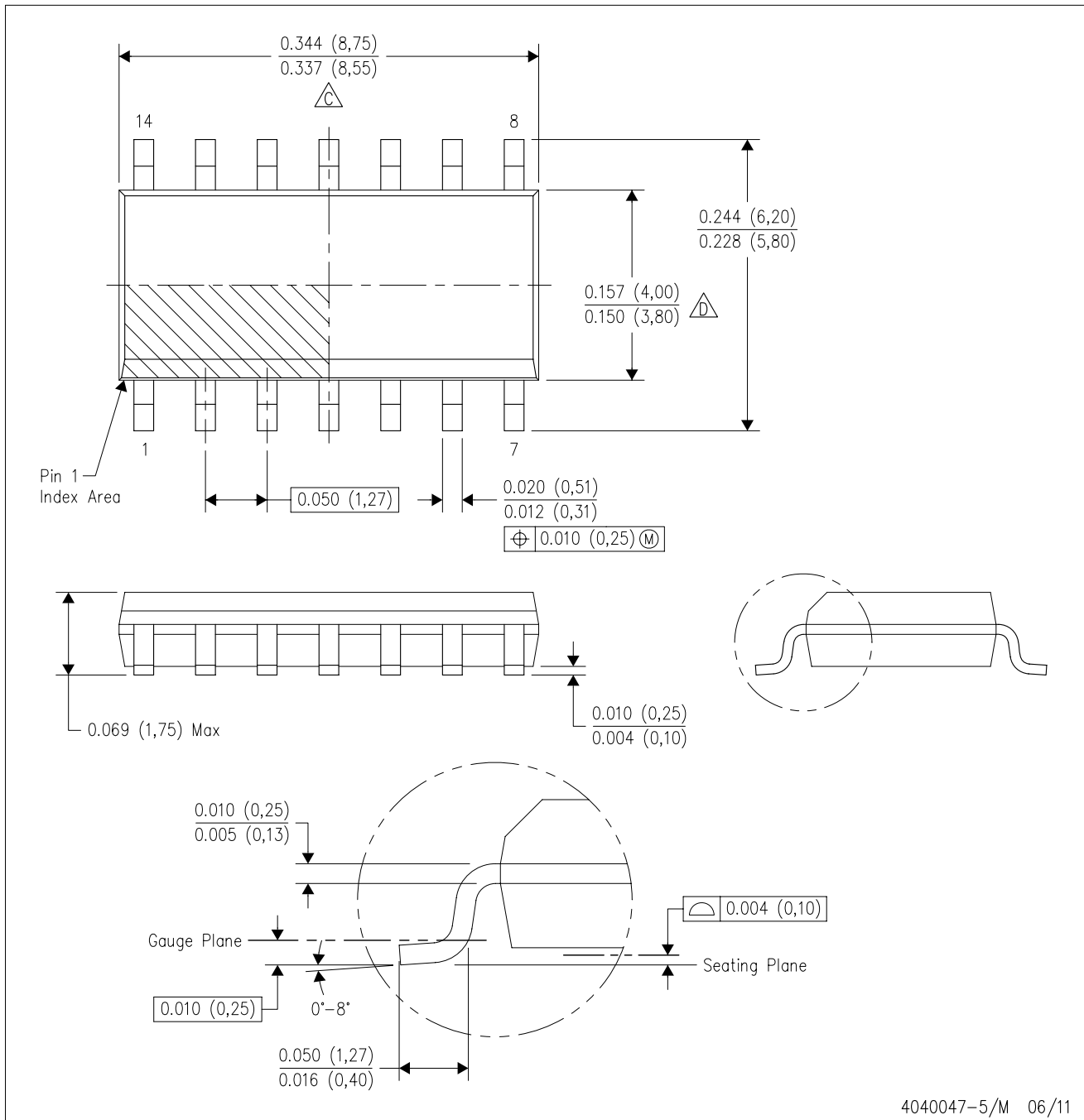


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

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