16 W ultra-wide input range auxiliary power supply for metering using ICE5BR3995CZ

REF_5BR3995CZ_16W1

About this document

Scope and purpose

This document is a reference design for a 16 W auxiliary power supply for single-phase electric meter with the latest fifth-generation Infineon fixed-frequency (FF) CoolSET™ ICE5BR3995CZ. The power supply is designed with ultra-wide input compatible with most geographic regions and three isolated outputs (12 V/1 A, 5 V/0.2 A, 5 V/0.2 A).

Highlights of the auxiliary power supply for smart metering are:

- Tightly regulated output voltages, high efficiency under light load and low standby power
- Comprehensive protection for a robust system
- 950 V rated MOSFET for ultra-wide input range
- Input line overvoltage protection (OVP)

Intended audience

This document is intended for power supply design engineers who are designing auxiliary power supplies for a single-phase electric meter or ultra-wide input range flyback converter.

Table of contents

1 System introduction

With the advancement of technology, the energy meter had also been undergoing continuous development to improve accuracy, power consumption, communication interfaces, measuring parameters, anti-tempering features, etc. These requirements are driving the demand for more innovative power supply designs to power electric meters. Infineon has introduced the latest fifth-generation FF CoolSET™ to address this need in an efficient and cost-effective manner.

An auxiliary SMPS is needed to power the various modules, which typically operate from a stable DC voltage source. The Infineon CoolSET™ (as shown in **Figure 1**) forms the heart of the system, providing the necessary protection and AC-DC conversion from the mains to multiple regulated DC voltages to power the various blocks.

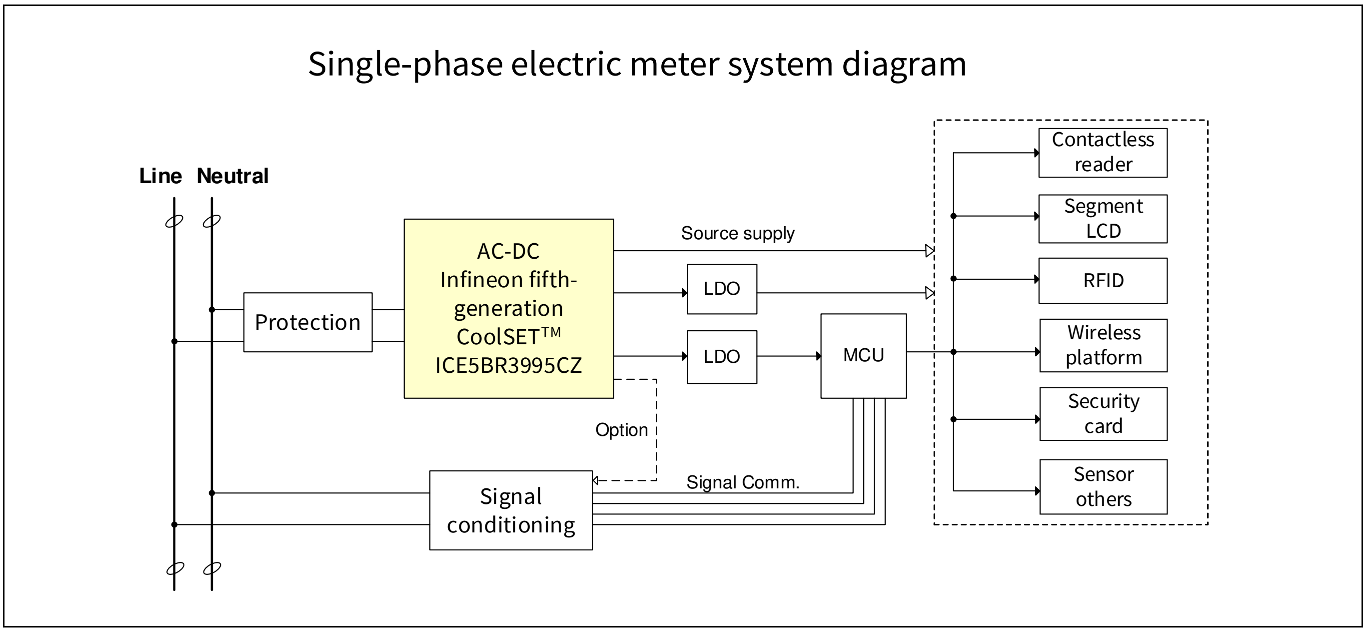


Figure 1 Simplified electric meter system diagram

Table 1 lists the system requirements for an auxiliary power supply for an electric meter, and the corresponding Infineon solution is shown in the right-hand column.

Table 1 System requirements and Infineon solutions

	System requirement for electric meter	Infineon solution – ICE5BR3995CZ
1	High efficiency under light load and low standby power	Digital frequency reduction and active burst mode (ABM)
2	Robust system and protection features	Comprehensive CoolSET™ protection feature in DIP-7 package
3	Line voltage fluctuation	950 V rated CoolMOS™ integrated for ultra-wide input voltage

1.1 High efficiency under light load and low standby power

Low power consumption of the meter is a key operating criterion. Smart meters in the field are consuming energy, which is a cost that must be paid by the end user. And in most cases, the system will reside in an idle state, in which the loading toward the auxiliary power supply is low. It is crucial that the auxiliary power supply operates as efficiently as possible, because it will be in this particular state for most of the time. Under light-load conditions, losses incurred with the power switch are usually dominated by the switching operation. The choice of switching scheme and frequency plays a crucial role in ensuring high conversion efficiency.

In this reference design, ICE5BR3995CZ was primarily chosen due to its frequency reduction switching scheme. Compared with a traditional FF flyback, the CoolSET™ reduces its switching frequency from medium to light load, thereby minimizing switching losses. Therefore, an efficiency of more than 80 percent is achievable under 25 percent loading conditions and nominal input voltages.

1.2 Simplified circuitry with good integration of power and protection features

To relieve the designer of the complexity of PCB layout and circuit design, CoolSET™ is a highly integrated device with both a controller and a 950 V MOSFET integrated into a single, space-saving DIP-7 package. These certainly help the designer to reduce component count as well as simplifying the layout into a simple PCB design for ease of manufacturing.

1.3 Auto-restart protection scheme to minimize interruption to enhance end-user experience

For a commercial electric meter unit, it would be annoying to both the end user and the manufacturer if the system were to halt and latch after protection. To minimize interruption, the CoolSET™ implements auto-restart mode for all protections.

2 Reference board design

This document provides complete design details including specifications, schematics, bill of materials (BOM), PCB layout and transformer design. Performance results pertaining to line/load regulation, efficiency, transient load, thermal conditions, conducted EMI scans and so on are also included.

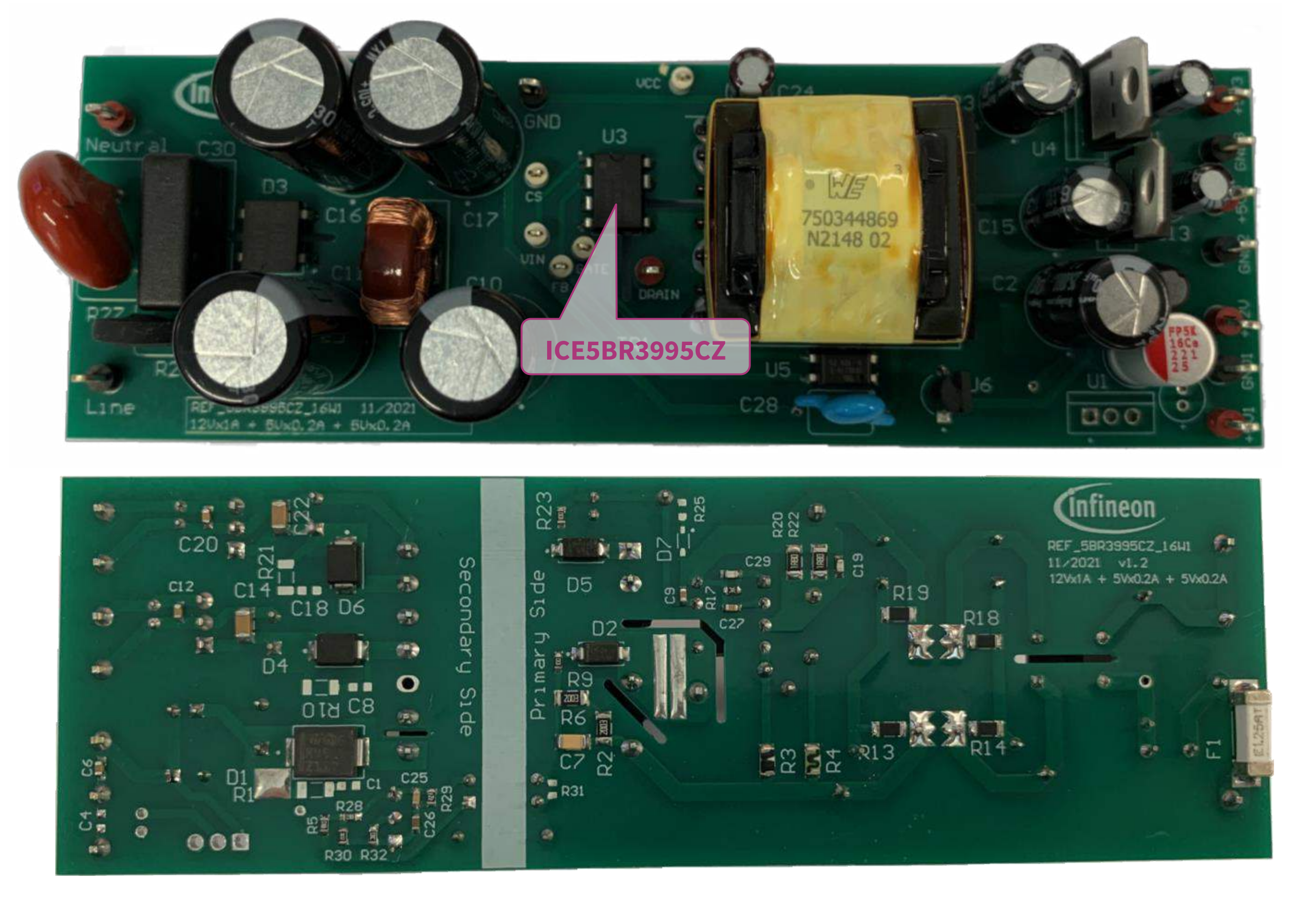


Figure 2 REF_5BR3995CZ_16W1

3 Power supply specifications

The table below shows the minimum acceptable performance of the design at 25°C ambient temperature. Actual performance is listed in the measurements section.

Table 2 Specifications of REF_5BR3995CZ_16W1

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
Input						
Voltage	V_{IN}	85	–	460	V AC	2 wires (no P.E.)
Frequency	f_{LINE}	47	50/60	63	Hz	
Output						
Output voltage 1	V_{O1}	–	12	–	V	
Output current 1	I_{O1}	–	–	1.0	A	
Output voltage ripple 1	$V_{RIPPLE1}$	–	–	120	mV	±1 percent
Output voltage 2	V_{O2}	–	5	–	V	
Output current 2	I_{O2}	–	–	0.2	A	±1 percent, tapped from 8 V output via LDO
Output voltage ripple 2	$V_{RIPPLE2}$	–	–	50	mV	
Output voltage 3	V_{O3}	–	5		V	
Output current 3	I_{O3}	–	–	0.2	A	±1 percent, tapped from 8 V output via LDO
Output voltage ripple 3	$V_{RIPPLE3}$	–	–	50	mV	
Output power	P_{OUT_Nom}		14	–	W	
Overcurrent protection (12 V)	I_{OCP}		1.2	–	A	
Start-up time	t_{start_up}		–	350	ms	With full load on other outputs
Environmental						
Conducted EMI			10		dB	Margin, CISPR 22 class B
ESD						EN 61000-4-2
Contact discharge			±6		kV	
Air discharge			±8		kV	
Surge immunity						EN 61000-4-5
Differential mode			±2		kV	
Common mode			±6		kV	
PCBA dimension			140 x 45 x 35		mm^2	L x W x H

4 Circuit diagram

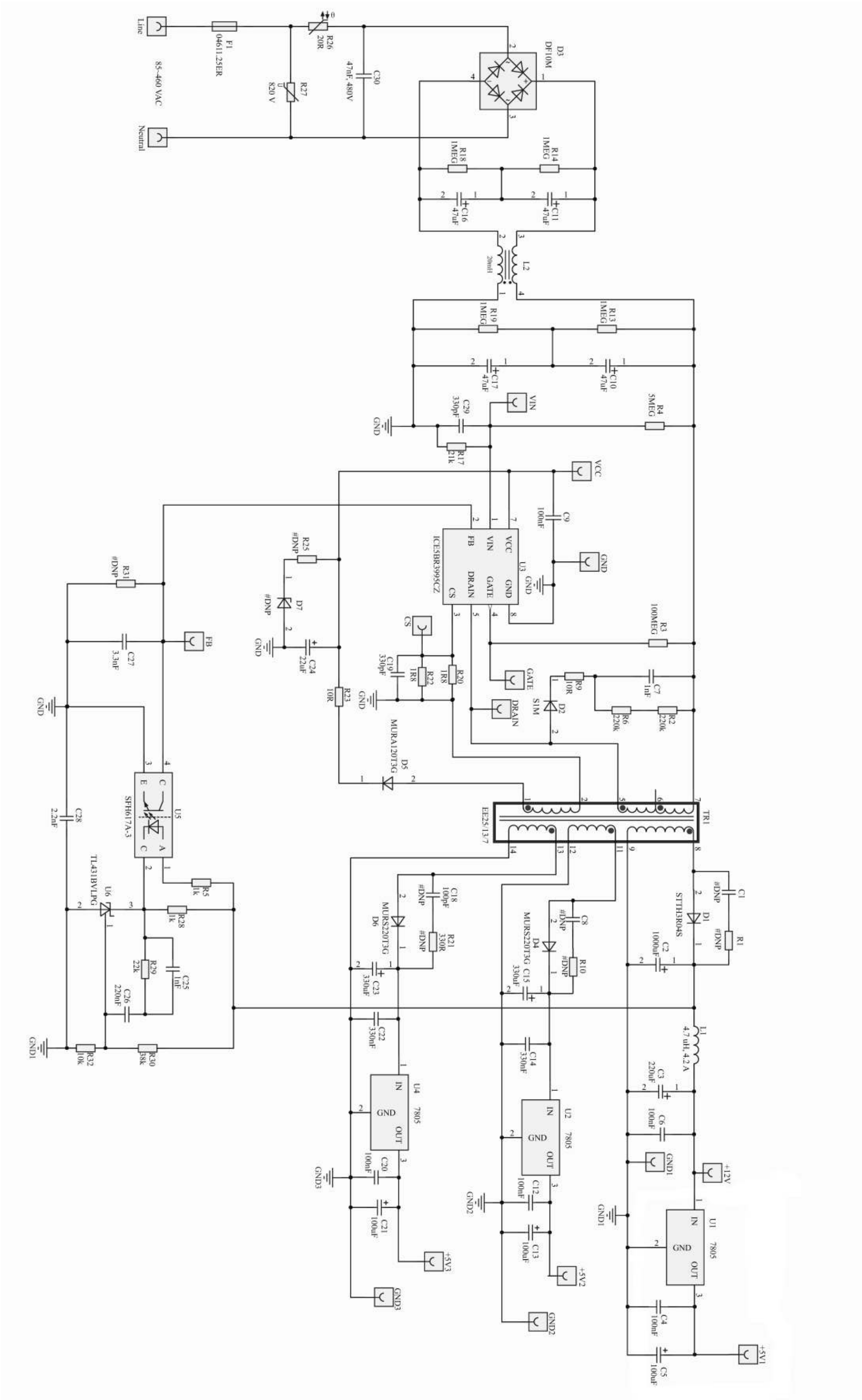


Figure 3 Schematic of REF_5BR3995CZ_16W1

5 Circuit description

In this section, the design circuit for the SMPS unit will be briefly described by the different functional blocks. For details of the design procedure and component selection for the flyback circuitry please refer to the IC design guide [2] and calculation tool [3] .

5.1 EMI filtering and line rectification

The input of the power supply unit is in the range of 85 V AC ~ 460 V AC. The fuse F1 is directly connected to the input line to protect the system in case of excess current entering the system circuit due to any fault. Following is the varistor R27, which is connected across the input to absorb excess energy during line-surge transient. Thermistor R26 is placed to reduce inrush current during the turning-on period. The X-capacitor C30 reduces EMI noise. The bridge rectifier D3 rectifies the AC input into DC voltage, filtered by the Pi circuit, which reduces the EMI noise.

5.2 Flyback converter power stage

The flyback converter power stage consists of transformer TR1, CoolSET™, secondary rectification diodes D1, D4 and D6, and secondary output capacitors C2, C15 and C23.

When the primary HV MOSFET turns on, energy is stored in the transformer. When it turns off, the stored energy is discharged to the output capacitors and into the output load.

For the output rectification, lower forward voltage and ultrafast recovery diodes can improve efficiency. There are two separate 5 V outputs from low dropout (LDO) regulator (U2, U4), and these outputs are not affected by cross-regulation. However, their inputs should be maintained within the operating range of the LDO.

5.3 Control of flyback converter through fifth-generation FF CoolSET™ ICE5BR3995CZ

5.3.1 Current sensing

The ICE5BR3995CZ is a current mode controller. The primary peak current is controlled cycle-by-cycle through the current sense (CS) resistors R20 and R22 in the CS pin (pin 3). Transformer saturation can be avoided through peak-current limitation (PCL); therefore, the system is more protected and reliable.

5.3.2 Feedback and compensation network

Resistor dividers R30 and R32 are used to sense the V_{OUT} and send the reference voltage to the feedback (FB) pin (pin 2) via error amplifier TL431(U6) and optocoupler (U5). A Type II compensation network (C25, C26 and R29) is implemented to stabilize the system.

The FB pin of ICE5BR3995CZ is a multifunction pin, which is used to select the entry burst power level (there are three levels available) through the resistor at the FB pin (R31) and also the burst-on/burst-off sense input during ABM. Here R31 is not placed for default ABM configuration.

5.4 Unique features of the fifth-generation FF CoolSET™ ICE5BR3995CZ

5.4.1 Fast self-start-up and sustaining of V_{CC}

The IC uses a cascode structure to fast-charge the V_{CC} capacitor. Pull-up resistor R3 connected to the GATE pin (pin 4) is used to initiate the start-up phase. At first, $I_{VCC\_Charge1}$ is used to charge the V_{CC} capacitor from 0 V to V_{CC_SCP}. This is a protection which reduces the power dissipation of the power MOSFET during V_{CC} short-to-GND condition. Thereafter, a much higher charging current of $I_{VCC\_Charge2}$ will charge the V_{CC} capacitor until the V_{CC_ON} is reached.

After start-up, the IC V_{CC} supply is usually sustained by the auxiliary winding of the transformer, which needs to support the V_{CC} to be above undervoltage lockout (UVLO) voltage (10 V typ.).

5.4.2 CCM, DCM operation with frequency reduction

ICE5BR3995CZ can be operated in either discontinuous conduction mode (DCM) or continuous conduction mode (CCM) with frequency-reduction features. This reference board is designed to operate in DCM at operating input voltage and load conditions. When the system is operating at high output load, the controller will switch at 65 kHz FF. In order to achieve a better efficiency between light load and medium load, frequency reduction is implemented as a function of V_{FB}, as shown in **Figure 4**. Switching frequency will not reduce further once the minimum switching frequency of 28 kHz is reached.

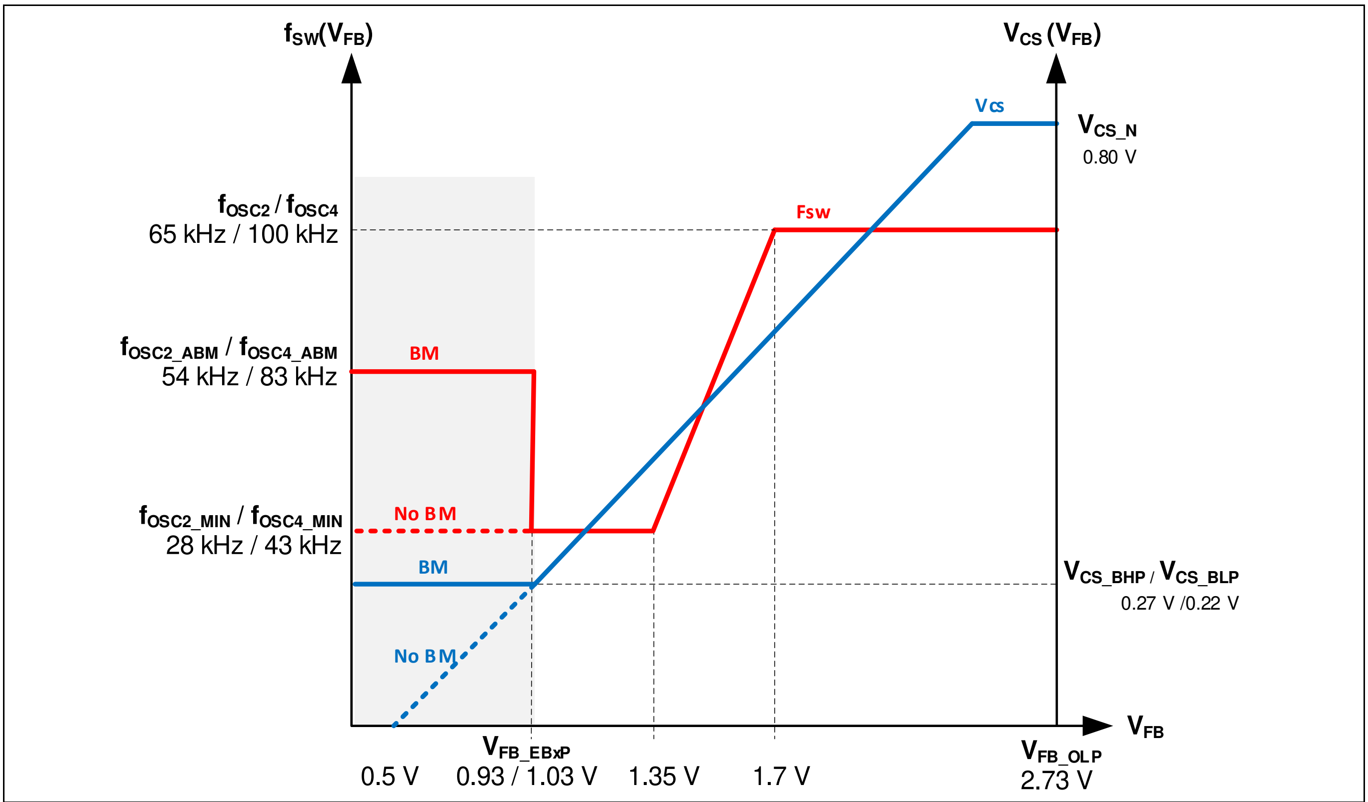


Figure 4 **Frequency reduction curve**

5.4.3 Frequency jittering with modulated gate drive

The ICE5BR3995CZ has a frequency jittering feature with modulated gate drive to reduce the EMI noise. The jitter frequency is internally set at 65 kHz (±4 percent), and the jitter period is 4 ms.

5.4.4 System robustness and reliability through protection features

Protection is one of the major factors in determining whether the system is safe and robust – therefore sufficient protection is necessary. ICE5BR3995CZ provides comprehensive protection to ensure the system is operating safely. This includes line overvoltage protection (LOVP), V_{CC} OV and undervoltage (UV), overload, overtemperature and V_{CC} short-to-GND. When those faults are found, the system will enter protection mode. Once the fault is removed, the system resumes normal operation. A list of protections and failure conditions is shown in the table below.

Table 3 Protection functions of ICE5BR3995CZ

Protection function	Failure condition	Protection mode
V_{IN} LOVP	V_{VIN} greater than V_{VIN_LOVP}	Non-switch auto-restart
V_{CC} OV	V_{VCC} greater than V_{VCC_OVP}	Odd-skip auto-restart
V_{CC} UV	V_{VCC} less than V_{VCCoff}	Auto-restart
Overload	V_{FB} greater than V_{FB_OLP} and lasts for $t_{FB\_OLP\_B}$	Odd-skip auto-restart
Overtemperature	T_J greater than 140°C (40°C hysteresis)	Non-switch auto-restart
V_{CC} short-to-GND (V_{VCC} = 0 V, $R_{start\text{-}up}$ = 50 MΩ, V_{DRAIN} = 90 V)	V_{VCC} less than V_{CC_SCP}, $I_{VCC\_Charge1}$ ≈ -0.2 mA	Cannot start up

5.5 Clamper circuit

A clamper network (D2, C7, R2, R6, R9) is used to reduce the switching voltage spikes across the DRAIN pin of the integrated HV MOSFET of the CoolSET™, which are generated by the leakage inductance of the transformer TR1. This is a dissipative circuit; therefore, the value of clamper devices need to be fine-tuned depending on the voltage derating factor and efficiency requirement.

5.6 PCB design tips

For a good PCB design layout, there are several points to note.

- The switching power loop needs to be as small as possible (see **Figure 5**). There are four power loops in the reference design; one on the HV side and three on the output side. The HV side loop starts from the bulk capacitor (C10) positive terminal, primary transformer winding (pin 7 and pin 5 of TR1), CoolSET™, CS resistors and back to the C17 negative terminal. The first output side loop (12 V output) starts at the transformer winding (pin 8 of TR1), output diode D1, output capacitor C2 and back to pin 9 of TR1. The second output side loop (8 V output) starts at the transformer winding (pin 11 of TR1), output diode D4, output capacitor C15 and back to pin 12 of TR1. The third output side loop (8 V output) starts at the transformer winding (pin 13 of TR1), output diode D6, output capacitor C23 and back to pin 14 of TR1.

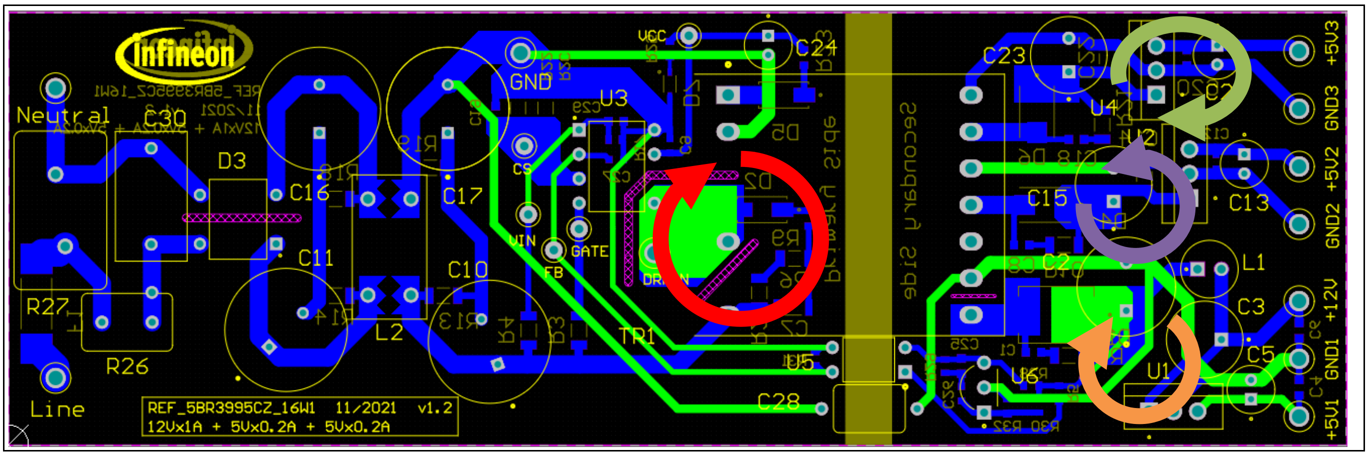


Figure 5 PCB layout tips

- Star-ground connection should be used to reduce high-frequency (HF) noise coupling that can affect the functional operation. The ground of the small-signal components should connect directly to the IC ground (pin 8 of U3).
- Separating the HV components and LV components, e.g., clamper circuit, main switching circuit can help to reduce spark-over chance of the high energy surge during a lightning surge test.
- Make the PCB copper pour on the DRAIN pin of the MOSFET act as a heatsink.

5.7 EMI reduction tips

EMI compliance is always a challenge for the power supply designer. There are several critical points to consider in order to achieve a satisfactory EMI performance.

- A proper transformer design can significantly reduce EMI. Low leakage inductance can incur a low switching spike and HF noise. Interlaced winding technique is the most common practice to reduce leakage inductance. Winding shield, core shield and whole transformer shield are also some of the techniques used to reduce EMI.
- Input CMC greatly reduces EMI, but this is costly and impractical especially for low-power applications.
- Short-switching power-loop design in the PCB (as described in section 5.6) can reduce radiated EMI due to the antenna effect.
- An output diode snubber circuit can reduce HF noise.
- Ferrite beads can reduce HF noise, especially on critical nodes such as the DRAIN pin, clamper diode and output diode terminals. There is no ferrite bead used in this design, as this can reduce the efficiency due to additional losses, especially on high-current terminals.

6 PCB layout

6.1 Top side

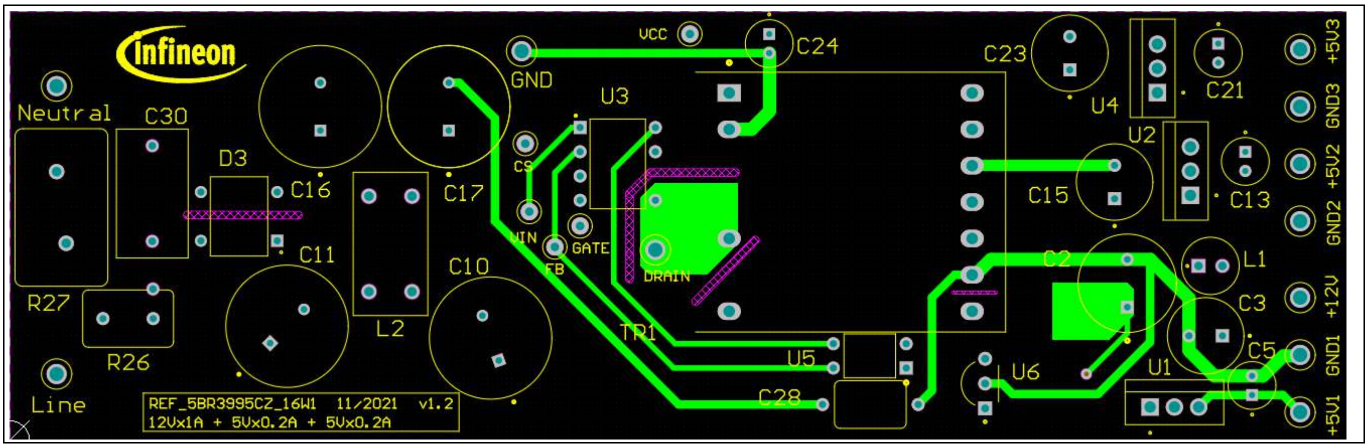


Figure 6 Top-side component legend

6.2 Bottom side

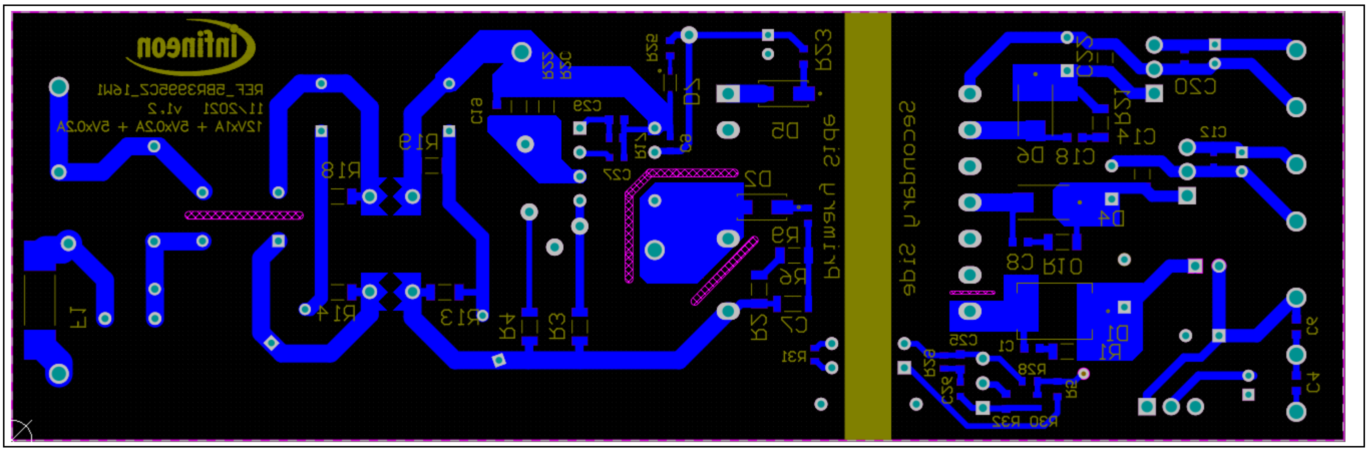


Figure 7 Bottom-side component legend

7 Bill of materials

Table 4 BOM

No.	Designator	Description	Part number	Manufacturer	Quantity
1	C19, C29	Ceramic capacitor 330 pF 50 V C0G/NP0 0603			2
2	C2	Aluminum capacitor 1000 µF 20% 25 V radial	25PX1000MEFCT810 X16	Rubycon	1
3	C3	Aluminum capacitor 220 µF 20% 25 V radial	UHD1E221MPD1TD	Nichicon	1
4	C13, C21	Capacitor 100 µF 20% 10 V	10YXF100MEFCT15X 11	Rubycon	2
5	C7	Ceramic capacitor 1206 1 nF 500 V X7R 10%	12067C102KAT2A	AVX	1
6	C4, C6, C9, C12, C20	Ceramic capacitor 100 nF 50 V X7R 0603			5
7	C10, C11, C16, C17	Aluminum capacitor 47 µF 20% 400 V	EPAG401ELL470MK3 0S	United Chemi-Con	4
8	C14, C22	Ceramic capacitor 1206 330 nF 50 V X7R			2
9	C15, C23	Aluminum capacitor 330 µF 20% 16 V	16YXF330MEFC8X11. 5	Rubycon	2
10	C24	Capacitor 22 µF 20% 35 V	UPW1H220MDD1TD	Nichicon	1
11	C25	Ceramic capacitor 1000 pF 50 V X7R 0603			1
12	C26	Ceramic capacitor 220 nF 50 V X7R 0603			1
13	C27	Ceramic capacitor 3300 pF 50 V X7R 0603			1
14	C28	Ceramic capacitor 2200 pF 440 V AC radial	DE1E3RA222MN4AN 01F	Murata	1
15	C30	Capacitor, SUP, X1, 0.047 µF, 480 V AC		Keya	1
16	D1	Ultrafast diode 400 V 3 A SMC	STTH3R04S	STMicroelectron ics	1
17	D2	General-purpose diode 1 kV 1 A DO214AC	S1M	ON Semiconductor	1
18	D3	Bridge rectifier 1-phase 1 kV 1.5 A 4-DIP	DF10M	ON Semiconductor	1
19	D4, D6	General-purpose diode 200 V 2 A SMB	MURS220T3G	ON Semiconductor	2
20	D5	General-purpose diode 200 V 1 A SMA	MURA120T3G	ON Semiconductor	1
21	F1	Surge-resistant TeleLink fuse	04611.25ER	Littelfuse	1
22	L1	Fixed inductor 4.7µH 4.2 A 30 mΩ TH			1
23	L2	CMC 20 mH 500 mA 2LN TH	744821120	Würth Elektronik	1
24	R2, R6	SMD resistor 200 kΩ 1% 1/4 W 1206			2
25	R3	SMD resistor 100 MΩ 1% 300 mW 1206	CRHA1206AF100MFK EF	Vishay	1
26	R4	SMD resistor 5 MΩ 1% 300 mW 1206	CRHV1206AF5M00FK FT	Vishay	1
27	R13, R14, R18, R19	SMD resistor 0.25 W 1 MΩ 1% 100 ppm	RCV12061M00FKEA	Vishay	4
28	R9, R23	SMD resistor 10 Ω 1% 1/10 W 0603			2
29	R17	SMD resistor 20.5 kΩ 1% 1/10 W 0603			1
30	R20, R22	SMD resistor 1.8 Ω 1% 1/4 W 1206			2
31	R5, R28	SMD resistor 1 kΩ 1% 1/10 W 0603			2
32	R29	SMD resistor 22 kΩ 1% 1/10 W 0603			1
33	R30	SMD resistor 38 kΩ 1% 1/10 W 0603			1
34	R32	SMD resistor 10 kΩ 1% 1/10 W 0603			1

35	R26	ICL 25 Ω 20% 2.5 A 11.5 mm	B57236S0250M051	TDK	1
36	R27	Varistor 820 V 6.5 kA disk 14 mm	V14H510AUTO	Littelfuse	1
37	TR1	Transfomer EE25/13/7	750344869(rev.02)	Würth Elektronik	1
38	U2, U4	IC linear regulator 5 V 1.5 A TO-220AB	L7805ABV	STMicroelectronics	2
39	U3	FF 950 V CoolSET™	ICE5BR3995CZ	Infineon	1
40	U5	Opto-isolator 5.3 kV transistor 4-DIP	SFH617A-3	Vishay	1
41	U6	IC V_{REF} shunt 36 V 0.4% TO92-3	TL431BVLPG	ON Semiconductor	1
42	+5 V1, +5 V2, +5 V3, +12 V, DRAIN, neutral	Test point THT, red	5010	Keystone	6
43	GND, GND1, line, GND2, GND3	Test point THT, black	5011	Keystone	5
44	CS, FB, GATE, V_{CC}, V_{IN}	Test point THT, white	5002	Keystone	5

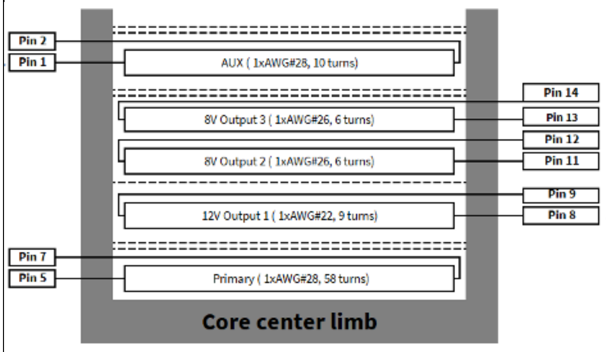
8 Transformer specification

Refer to Appendix A for transformer design.

Core name and material: EE25/13/7, TP4A (TDG)

Primary inductance: L_P = 730 µH (±10 percent), measured between pin 5 and pin 7

Manufacturer and part number: Würth Elektronik Midcom (750344869) Rev. 02



Wire size requirement :

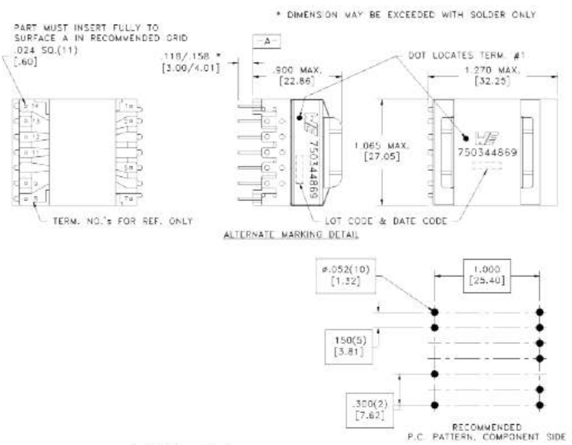
Start	Stop	No. of turns	Wire size	Layer
5	7	58	1 x AWG#28	Primary
8	9	9	1 x AWG#22	O/P_1 Secondary
11	12	6	1 x AWG#26	O/P_2 Secondary
13	14	6	1 x AWG#26	O/P_3 Secondary
1	2	11	1 x AWG#28	AUX

Horizontal and vertical external shields are added and tied to pin 2

CUSTOMER TERMINAL	RoHS	LEAD(Pb)–FREE
Sn 96%, Ag 4%	Yes	Yes

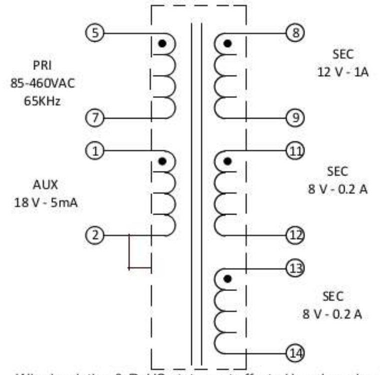
more than you expect

WÜRTH ELEKTRONIK



ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	1-2	@20°C	0.17 ohms max.
D.C. RESISTANCE	5-7	@20°C	0.60 ohms max.
D.C. RESISTANCE	8-9	@20°C	0.05 ohms max.
D.C. RESISTANCE	11-12	@20°C	0.08 ohms max.
D.C. RESISTANCE	13-14	@20°C	0.08 ohms max.
INDUCTANCE	5-7	10kHz, 100mV, Ls	730.00µH ±10%
SATURATION CURRENT	5-7	20% rolloff from initial	1A
LEAKAGE INDUCTANCE	5-7	tie(8+9+11+12+13+14),100kHz, 100mV, Ls	35µH max.
DIELECTRIC	7-8	tie(2+5,8+9+11+12+13+14), 5000VAC, 1 second	4000VAC, 1 minute
DIELECTRIC	1-7	625VAC, 1 second	
TURNS RATIO		(5-7):(1-2)	5.27:1
TURNS RATIO		(5-7):(8-9)	6.44:1
TURNS RATIO		(5-7):(11-12)	9.67:1
TURNS RATIO		(5-7):(13-14)	9.67:1



GENERAL SPECIFICATIONS:

OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.

Designed to comply with the following requirements as defined by IEC62368-1, EN62368-1, UL62368-1/CSA62368-1 and AS/NZS62368.1:
- Reinforced insulation for a primary circuit at a working voltage of 460Vrms, 650Vpeak, OVC II, Pollution Degree 2.

Designed to meet 6kV (1.2x50µsec, 3± repetitions) surge test between PRI and SEC.

Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability. Marking detail font and color may vary on preproduction samples.

DFM		Packaging Specifications Method: Tray PKG-0737	CONVENTION PLACEMENT	Tolerances unless otherwise specified: Angles: ±1° Decimals: ±.005 [.13] Fractions: ±1/64 Footprint: ± .001 [.03]	DRAWING TITLE TRANSFORMER	PART NO. 750344869
DATE						
ENG	NWU					
REV.	02			This drawing is dual dimensioned. Dimensions in brackets are in millimeters.		
DATE	2021/6/24	www.we-online.com/midcom				SPECIFICATION SHEET 1 OF 1

Figure 8 Transformer structure

9 Measurement data and graphs

Table 5 Efficiency and standby performance

Input (V AC/Hz)	P_{IN} (W)	V_{O1} (V)	I_{O1} (A)	V_{O2} (V)	I_{O2} (A)	V_{O3} (V)	I_{O3} (A)	P_{OUT} (W)	Efficiency (%)
85 V AC/60 Hz	0.226	12.015	0.000	5.010	0.005	4.980	0.005	0.050	
	19.490	12.000	0.996	4.985	0.198	4.968	0.198	13.918	71.41
115 V AC/60 Hz	0.245	12.015	0.000	5.010	0.005	4.980	0.005	0.050	
	18.926	12.000	0.996	4.985	0.198	4.968	0.198	13.918	73.54
230 V AC/50 Hz	0.361	12.015	0.000	5.010	0.005	4.980	0.005	0.050	
	18.720	12.000	0.996	4.992	0.198	4.968	0.198	13.919	74.36
264 V AC/50 Hz	0.455	12.015	0.000	5.010	0.005	4.980	0.005	0.050	
	18.689	12.000	0.996	4.992	0.198	4.968	0.198	13.919	74.48
300 V AC/50 Hz	0.447	12.015	0.000	5.010	0.005	4.980	0.005	0.050	
	18.753	12.000	0.996	4.992	0.198	4.968	0.198	13.919	74.22
460 V AC/50 Hz	0.805	12.015	0.000	5.010	0.005	4.980	0.005	0.050	
	19.650	12.000	0.996	4.992	0.198	4.968	0.198	13.919	70.84

Minimum-load condition: 12 V/0 mA, 5 V/5 mA, 5 V/5 mA;

Full-load condition: 12 V/1.0 A, 5 V/200 mA, 5 V/200 mA;

Minimum-load current for LDO regulation is 5 mA.

Table 6 Efficiency and standby performance with a single-output configuration

Input (V AC/Hz)	P_{IN} (W)	V_{O1} (V)	I_{O1} (A)	P_{OUT} (W)	Efficiency
85 V AC/60 Hz	0.052	12.078	0.000	0.000	
	15.570	12.046	0.996	11.998	77.06%
115 V AC/60 Hz	0.067	11.984	0.000	0.000	
	15.190	12.046	0.996	11.998	78.98%
230 V AC/50 Hz	0.164	12.078	0.000	0.000	
	15.100	12.046	0.996	11.998	79.46%
264 V AC/50 Hz	0.206	12.078	0.000	0.000	
	15.150	12.046	0.996	11.998	79.19%
300 V AC/50 Hz	0.256	12.078	0.000	0.000	
	15.220	12.046	0.996	11.998	78.83%
460 V AC/50 Hz	0.563	12.780	0.000	0.000	
	16.070	12.046	0.996	11.998	74.66%

Note: Single-output (+12 V) configuration efficiency measurement was done by removing two LDO outputs; the actual board comes with LDO circuits. The overall circuit is not optimized for single-output configuration; the above efficiency data is for illustration only.

9.1 Efficiency curve

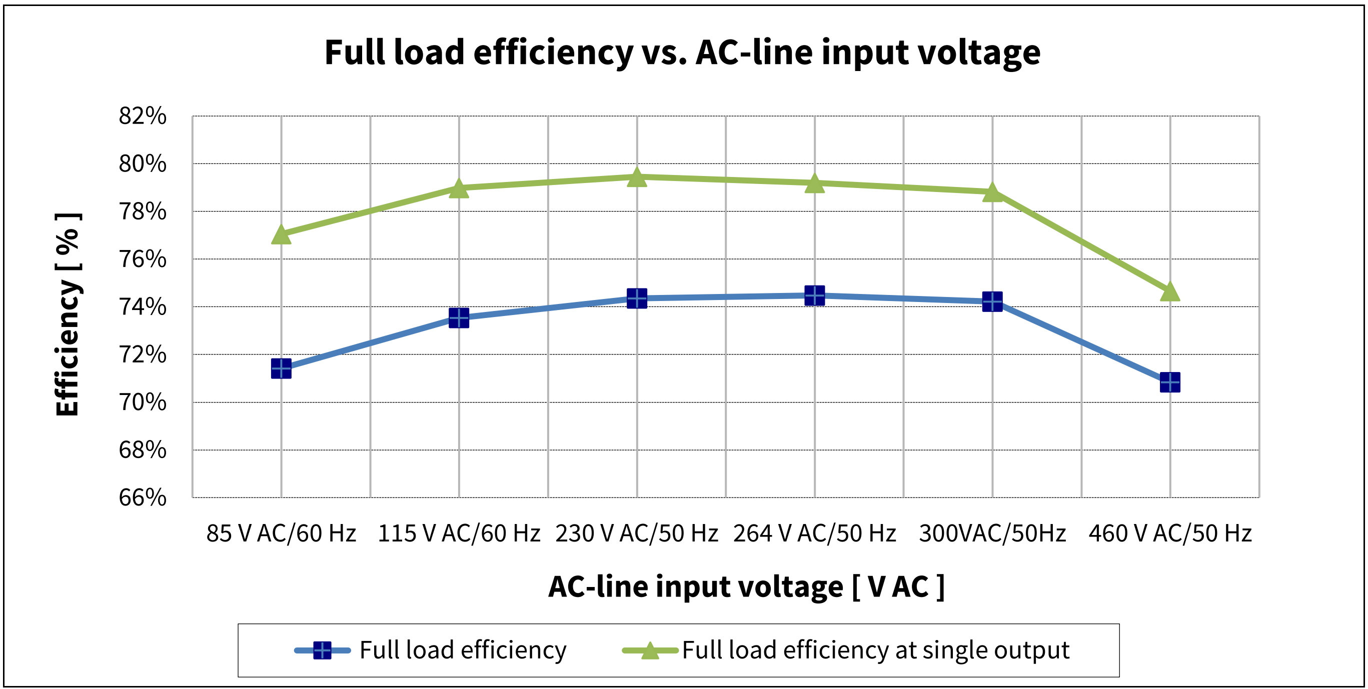


Figure 9 **Efficiency vs. input line voltage**

9.2 Standby power

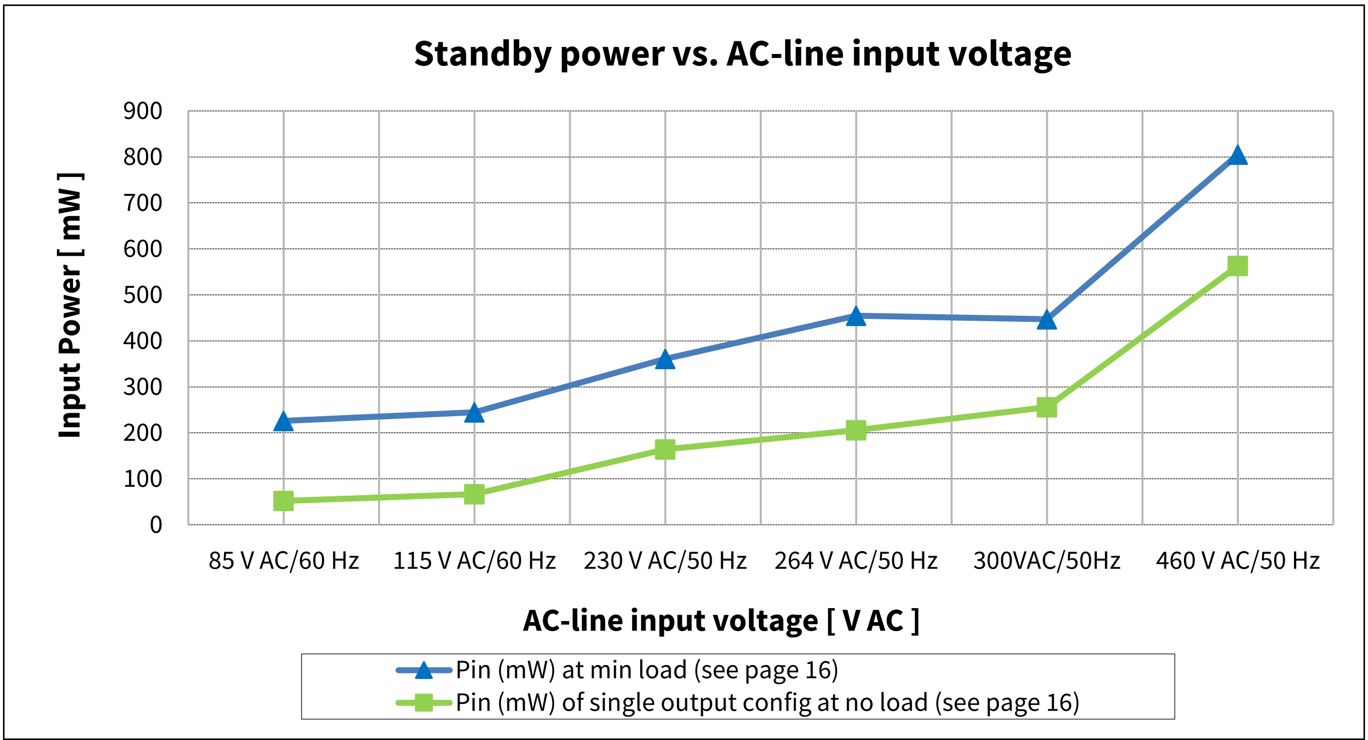


Figure 10 **Standby power vs. input line voltage**

9.3 Output voltage regulation

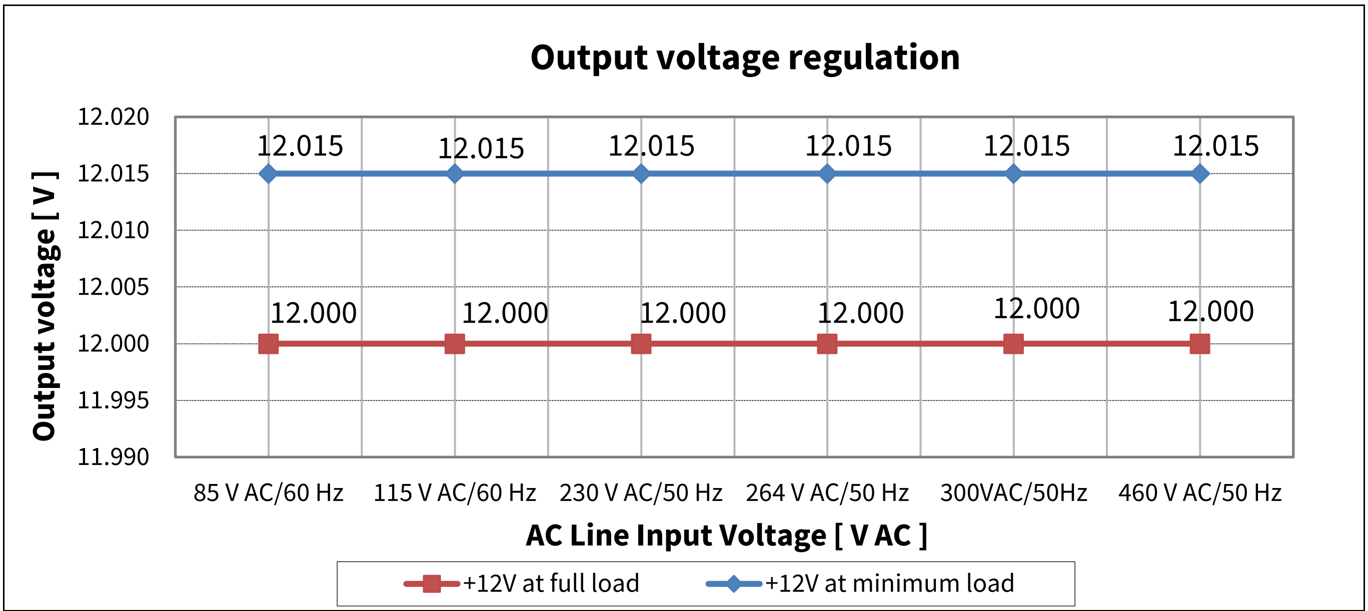


Figure 11 Output voltage regulation

9.4 ESD immunity (EN 61000-4-2)

This system was subjected to ESD testing according to EN 61000-4-2 for both contact and air discharge. A test failure was defined as non-recoverable.

- Air discharge: pass ±8 kV; contact discharge: pass ± 6 kV.

Table 7 System ESD test result

Description	ESD test	Level	Number of strikes		Test result
			V_{O1}	GND	
115/230 V AC	Contact	±6 kV	10	10	Pass
	Air	±8 kV	10	10	Pass

9.5 Surge immunity (EN 61000-4-5)

The reference board was subjected to a surge immunity test (±2 kV DM and ±6 kV CM) according to EN 61000-4-5. It was tested at full load (resistive load). A test failure was defined as non-recoverable.

Table 8 System surge immunity test result

Description	Test	Level	Number of strikes				Test result
			0°	90°	180°	270°	
115/230 V AC	DM	±2 kV	3	3	3	3	Pass
	CM	±6 kV	3	3	3	3	Pass

9.6 Conducted emissions (EN 55022 class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) class B. The reference board was tested at full load (resistive load) at an input voltage of 115 V AC and 230 V AC.

- 115 V AC: pass with greater than 10 dB margin for quasi-peak measurement
- 230 V AC: pass with greater than 10 dB margin for quasi-peak measurement

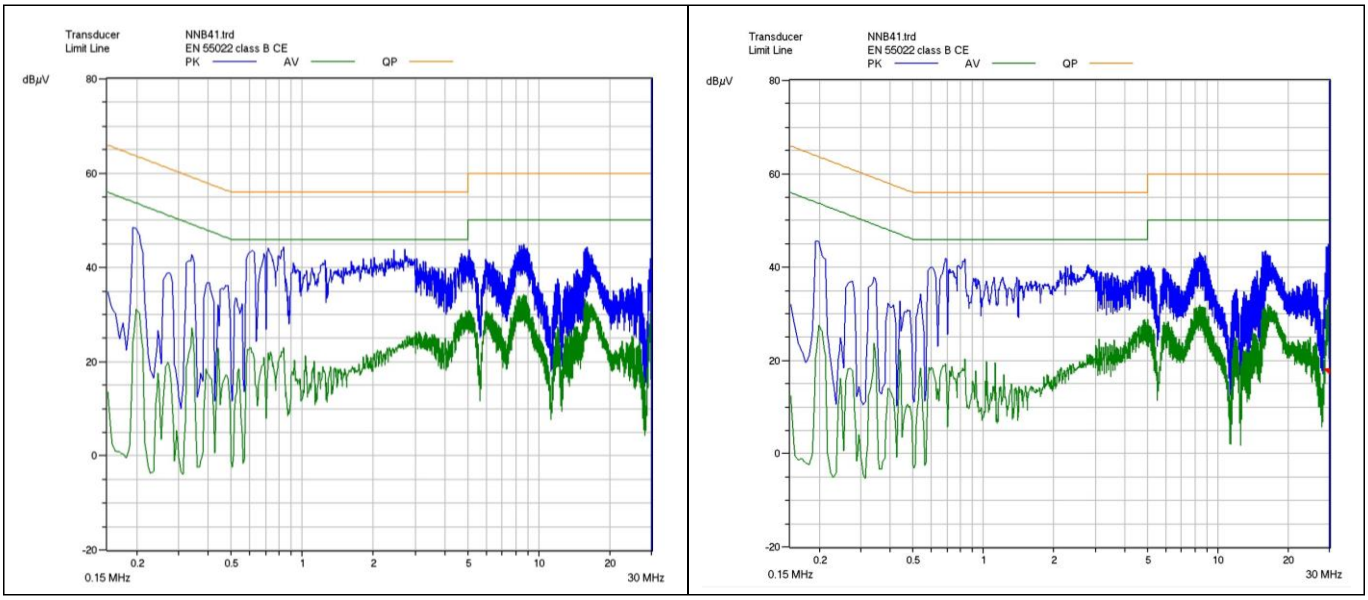
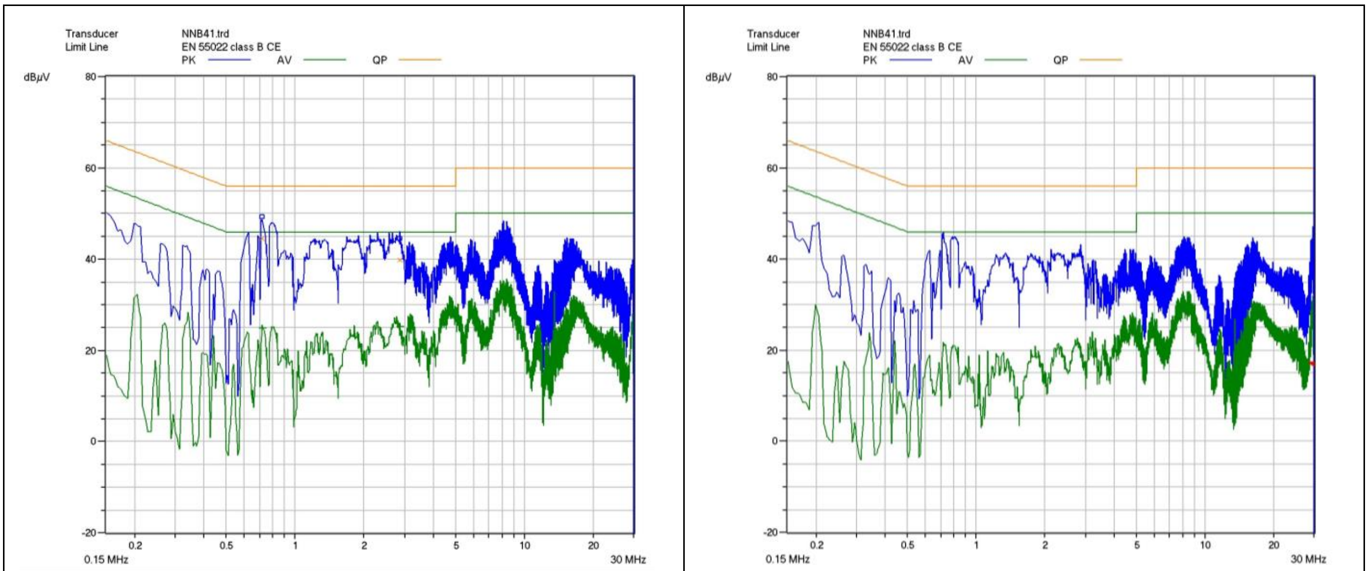


Figure 12 Conducted emissions at 115 V AC and full load on line (left) and neutral (right)



Final Measurement Results: * = Limit exceeded

Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Notes
0.7140	L	49.2	L	24.9	L	44.5	46.0	56.0	
2.8500	L	44.5	L	25.3	L	39.9	46.0	56.0	

Figure 13 Conducted emissions at 230 V AC and full load on line (left) and neutral (right)

9.7 Thermal measurement

Thermal measurement was done using an infrared thermography camera (FLIR-T62101) at an ambient temperature of 25°C taken after one hour running at full load. The temperature of the components was taken in an open-frame set-up.

Table 9 Thermal measurement of components (open-frame)

No.	Components	Temperature at 85 V AC (°C)	Temperature at 460 V AC (°C)
1	U3 (ICE5BR3995CZ)	68.3	83.1
2	D3 (bridge diode)	55.5	37.4
3	TR1 (transformer)	56.6	65.5
4	D1 (output 1 diode)	97.2	97.8
5	D4 (output 2 diode)	68.6	69.8
6	D6 (output 3 diode)	64.7	65.6

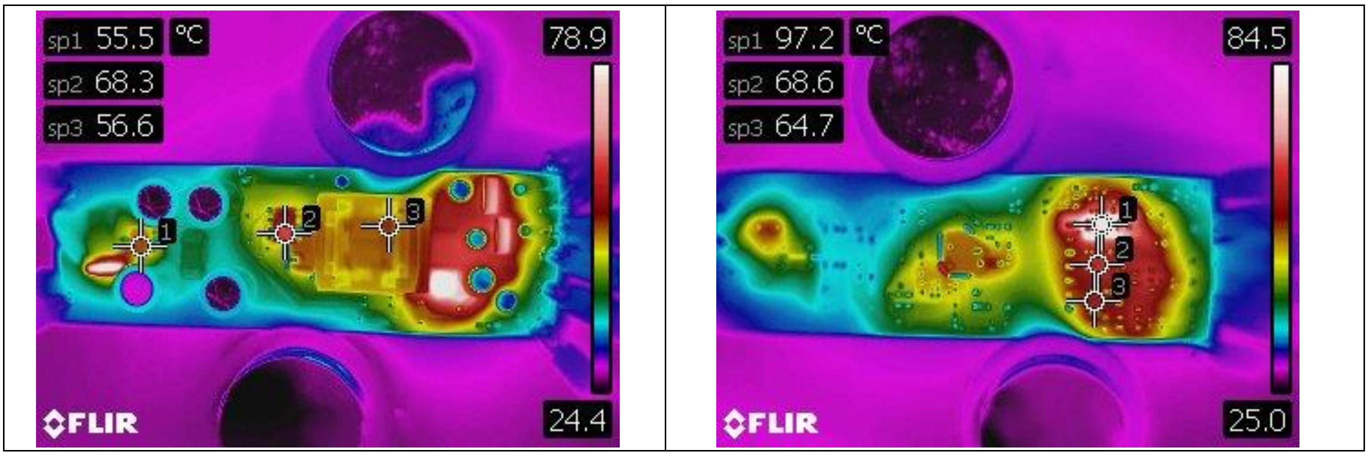


Figure 14 Top-layer (left) and bottom-layer (right) thermal image at 85 V AC input voltage

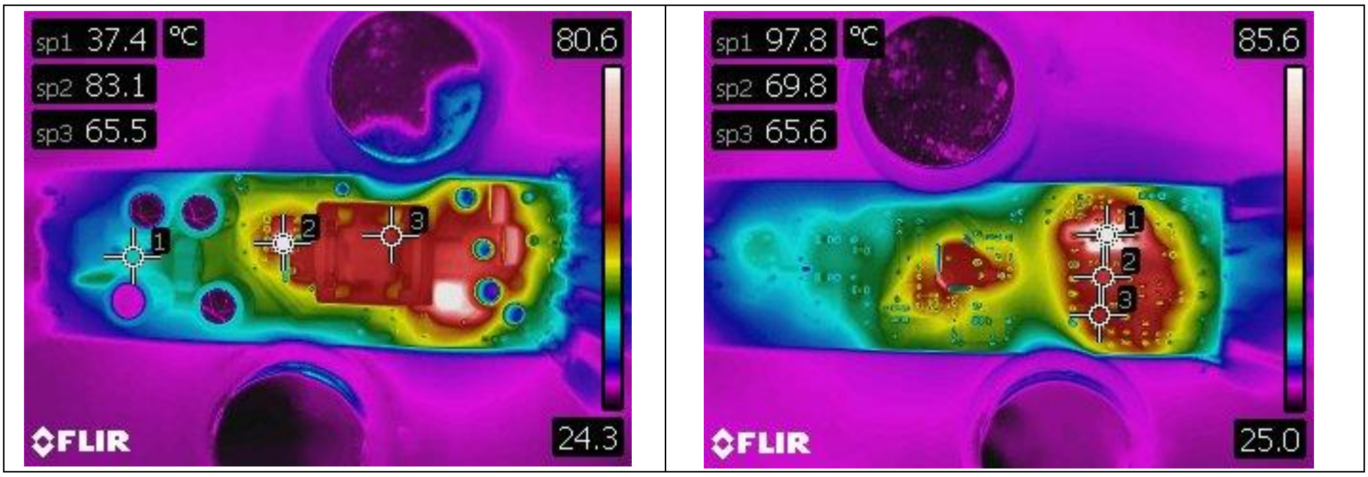


Figure 15 Top-layer (left) and bottom-layer (right) thermal image at 460 V AC input voltage

10 Waveforms and oscilloscope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy HDO4034 oscilloscope.

10.1 Start-up at full load

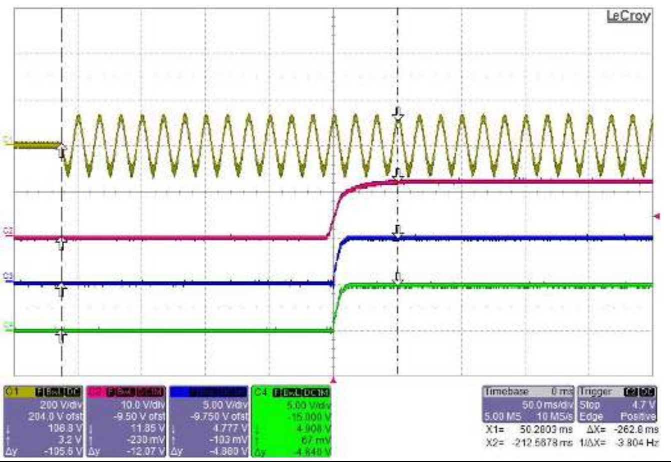
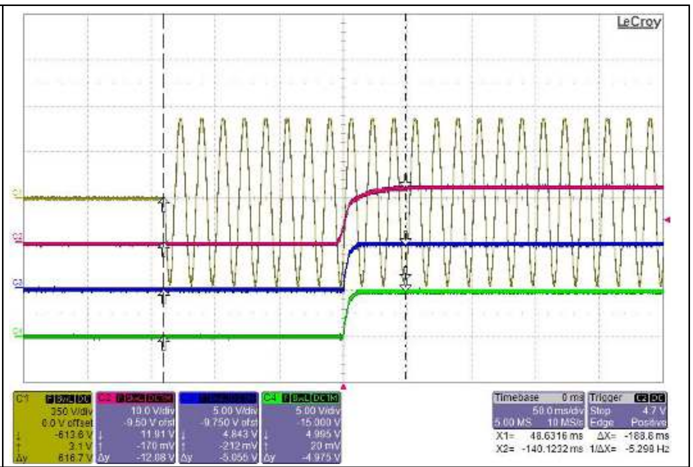
	
C1 (yellow) : AC-line voltage C2 (purple) : +12 V output voltage C3 (blue) : +5 V2 output voltage C4 (green) : +5 V3 output voltage	C1 (yellow) : AC-line voltage C2 (purple) : +12 V output voltage C3 (blue) : +5 V2 output voltage C4 (green) : +5 V3 output voltage
85 V AC start-up time at full load is around 262 ms	460 V AC start-up time at full load is around 188 ms

Figure 16 **Start-up**

10.2 Soft-start at full load

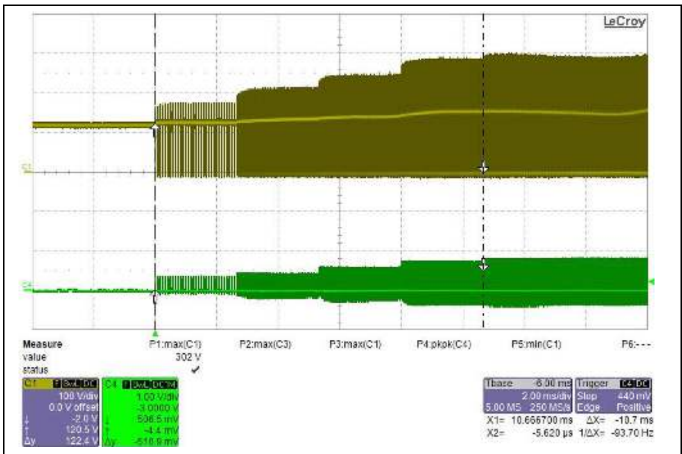
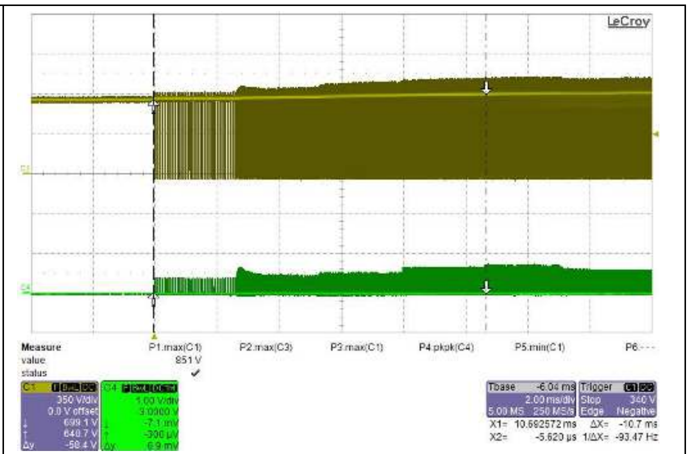
	
C1 (yellow) : Drain voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C4 (green) : CS voltage
85 V AC soft-start at full load within ~12 ms	460 V AC soft-start time at full load within ~12 ms

Figure 17 **Soft-start**

10.3 Drain and CS voltage at full load

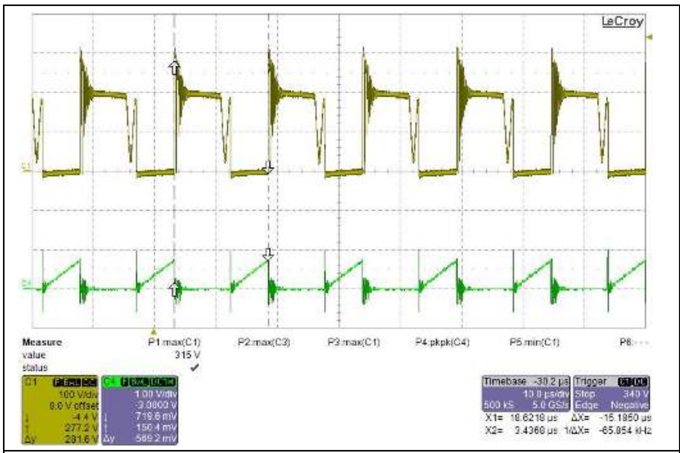
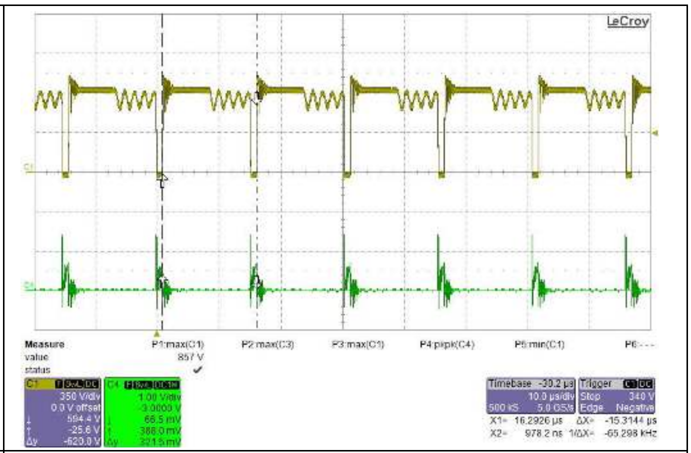
	
C1 (yellow) : Drain voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C4 (green) : CS voltage
85 V AC, maximum drain voltage at full load is ~315 V	460 V AC, maximum drain voltage at full load is ~857 V

Figure 18 Drain and CS voltage

10.4 Frequency jittering and modulated gate drive

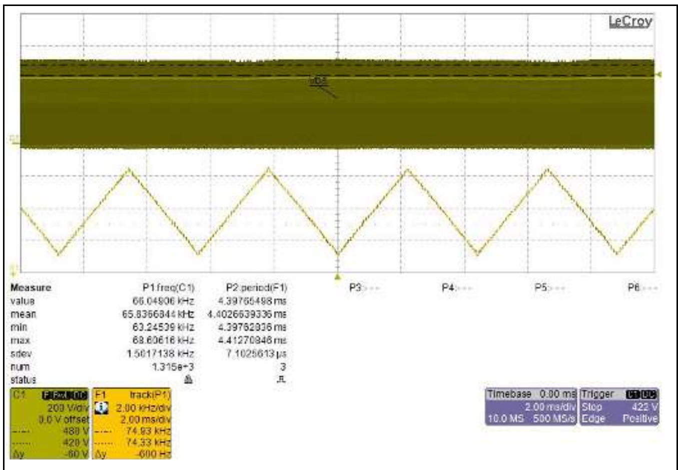
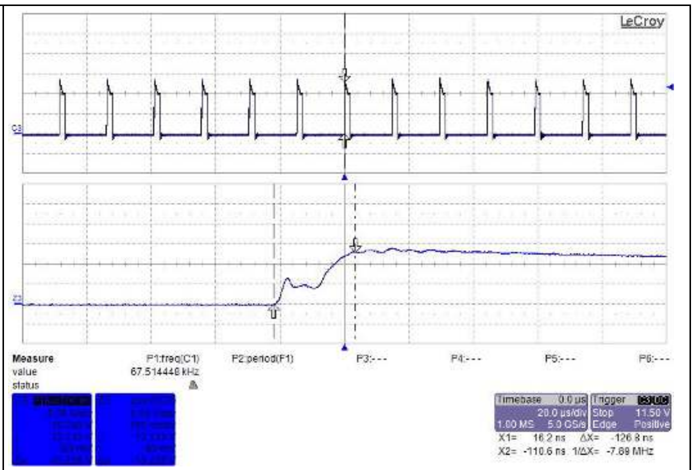
	
C1 (yellow) : Drain voltage F1 (yellow) : Frequency track of drain voltage	C3 (blue) : Gate voltage
Frequency jittering is from ~63 kHz to ~68 kHz with a jitter period of ~4 ms	Modulated gate drive at ~120 ns rise time

Figure 19 Frequency jittering and modulated gate drive

10.5 Load-transient response

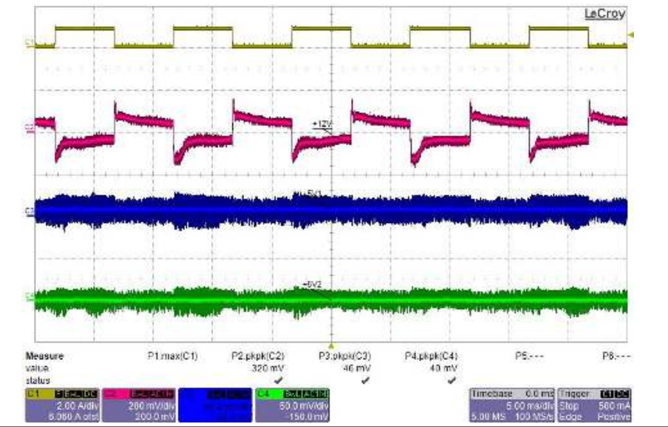
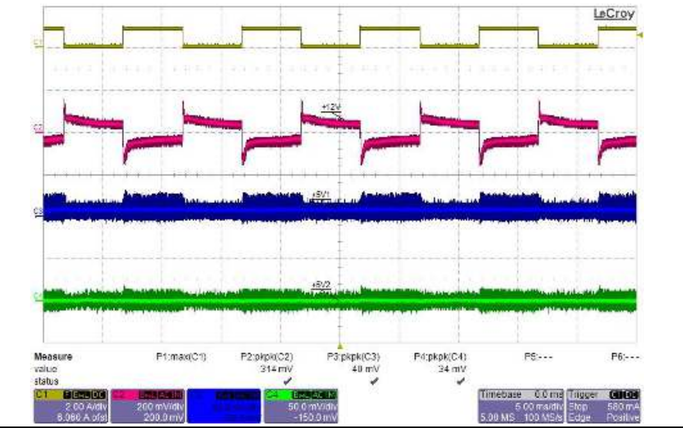
	
C2 (purple) : +12 V output voltage C3 (blue) : +5 V2 output voltage C4 (green) : +5 V3 output voltage	C2 (purple) : +12 V output voltage C3 (blue) : +5 V2 output voltage C4 (green) : +5 V3 output voltage
85 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~320 mV +5 V2 output voltage $V_{ripple\_pk\_pk}$ is ~46 mV +5 V3 output voltage $V_{ripple\_pk\_pk}$ is ~40 mV	460 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~314 mV +5 V2 output voltage $V_{ripple\_pk\_pk}$ is ~40 mV +5 V3 output voltage $V_{ripple\_pk\_pk}$ is ~34 mV

Figure 20 **Load-transient response with +12 V output load change from 10 percent load to 100 percent load at 0.4 A/μs slew rate, 100 Hz. +5 V2 and +5 V3 output load are fixed at 0.2 A. Probe terminals are decoupled with 10 μF electrolytic and 0.1 μF ceramic capacitors. Oscilloscope is bandwidth filter limited to 20 MHz**

10.6 Output ripple voltage at full load

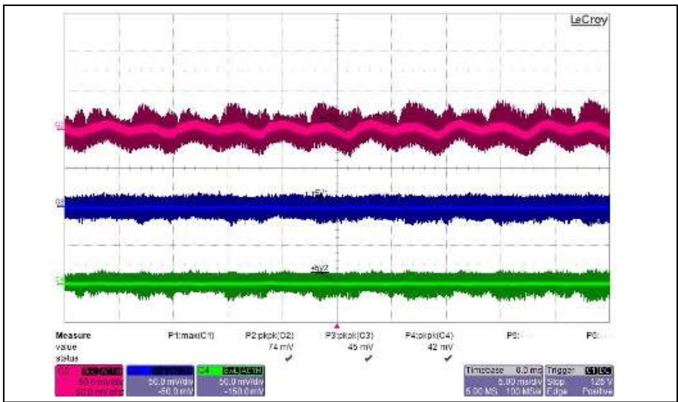
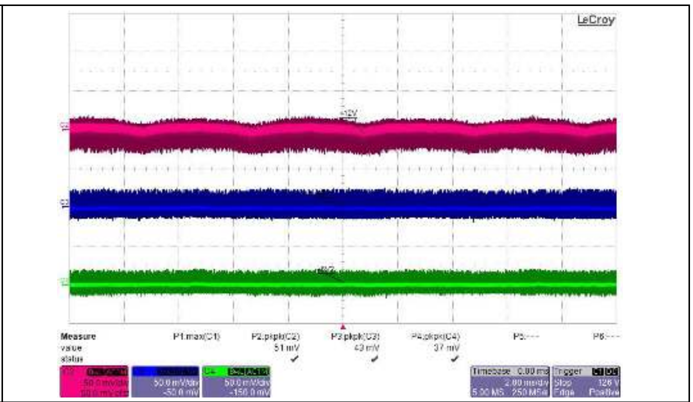
	
C2 (purple) : +12 V output voltage C3 (blue) : +5 V2 output voltage C4 (green) : +5 V3 output voltage	C2 (purple) : +12 V output voltage C3 (blue) : +5 V2 output voltage C4 (green) : +5 V3 output voltage
85 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~74 mV +5 V2 output voltage $V_{ripple\_pk\_pk}$ is ~45 mV +5 V3 output voltage $V_{ripple\_pk\_pk}$ is ~42 mV	460 V AC +12 V output voltage $V_{ripple\_pk\_pk}$ is ~51 mV +5 V2 output voltage $V_{ripple\_pk\_pk}$ is ~43 mV +5 V3 output voltage $V_{ripple\_pk\_pk}$ is ~37 mV

Figure 21 **Output ripple voltage at full load. Probe terminals are decoupled with 10 μF electrolytic and 0.1 μF ceramic capacitors. Oscilloscope is bandwidth filter limited to 20 MHz**

10.7 Output ripple voltage at ABM

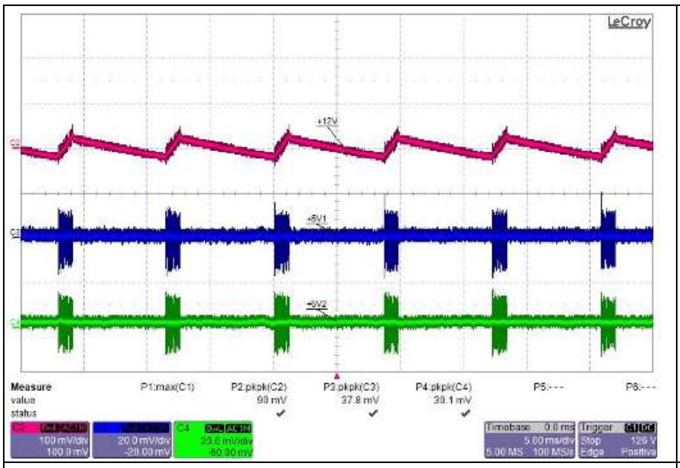
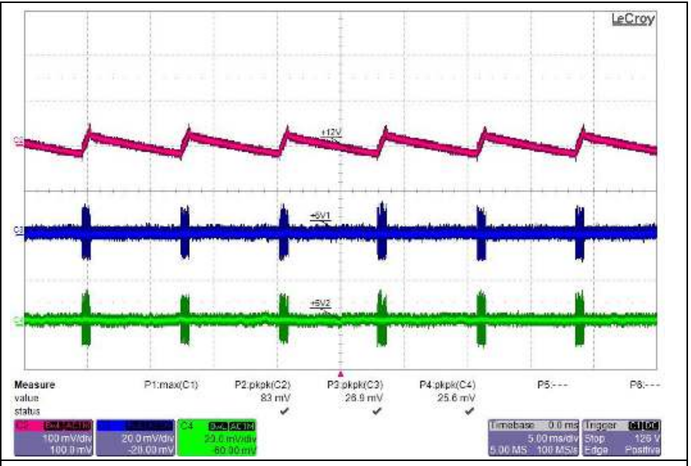
<table>
<tr><td>
</td><td>
</td></tr>
<tr><td>C2 (purple) : +12 V output voltage
C3 (blue) : +5 V2 output voltage
C4 (green) : +5 V3 output voltage</td><td>C2 (purple) : +12 V output voltage
C3 (blue) : +5 V2 output voltage
C4 (green) : +5 V3 output voltage</td></tr>
<tr><td>85 V AC
+12 V output voltage $V_{ripple\_pk\_pk}$ is ~90 mV
+5 V2 output voltage $V_{ripple\_pk\_pk}$ is ~37.8 mV
+5 V3 output voltage $V_{ripple\_pk\_pk}$ is ~30.1 mV</td><td>460 V AC
+12 V output voltage $V_{ripple\_pk\_pk}$ is ~83 mV
+5 V2 output voltage $V_{ripple\_pk\_pk}$ is ~26.9 mV
+5 V3 output voltage $V_{ripple\_pk\_pk}$ is ~25.6 mV</td></tr>
</table>

Figure 22 Output ripple voltage at minimum load. Probe terminals are decoupled with 10 µF electrolytic and 0.1 µF ceramic capacitors. Oscilloscope is bandwidth filter limited to 20 MHz

10.8 Entering ABM

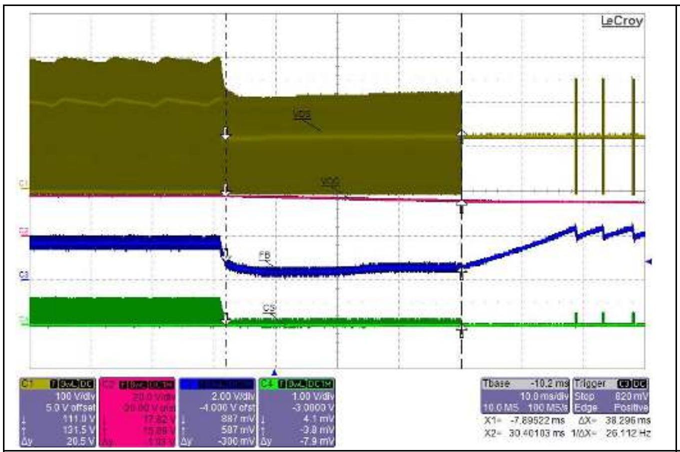
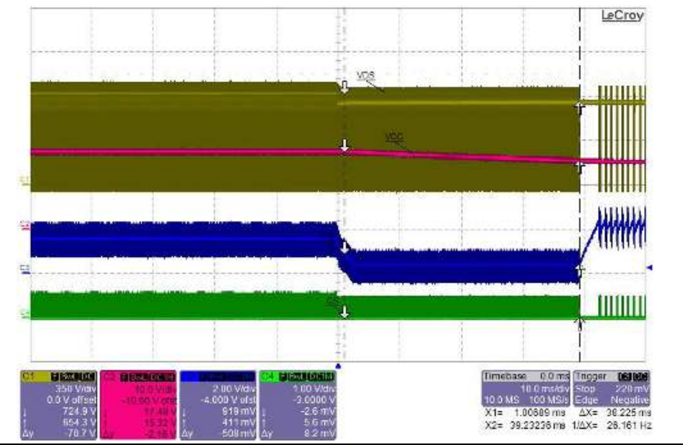
<table>
<tr><td>
</td><td>
</td></tr>
<tr><td>C1 (yellow) : Drain voltage
C2 (purple) : V_{CC} voltage
C3 (blue) : FB pin voltage
C4 (green) : CS voltage</td><td>C1 (yellow) : Drain voltage
C2 (purple) : V_{CC} voltage
C3 (blue) : FB pin voltage
C4 (green) : CS voltage</td></tr>
<tr><td>85 V AC enters ABM at FB pin voltage less than 1.03 V (V_{FB_EBLP}) for around 38 ms (t_{FB_BEB})</td><td>460 V AC enters ABM at FB pin voltage less than 1.03 V (V_{FB_EBLP}) for around 38 ms (t_{FB_BEB})</td></tr>
</table>

Figure 23 Entering ABM

10.9 During ABM

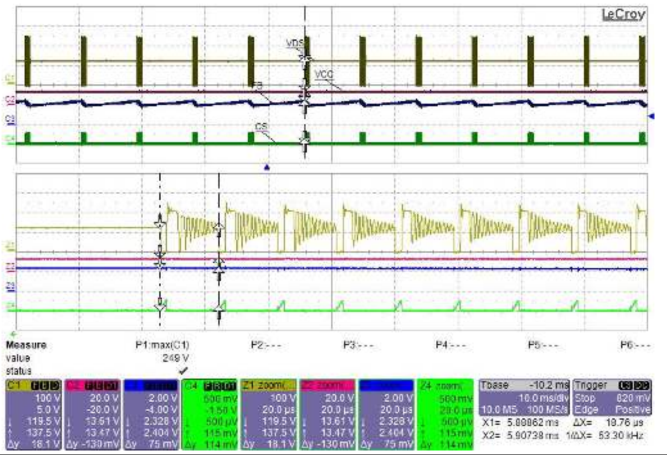
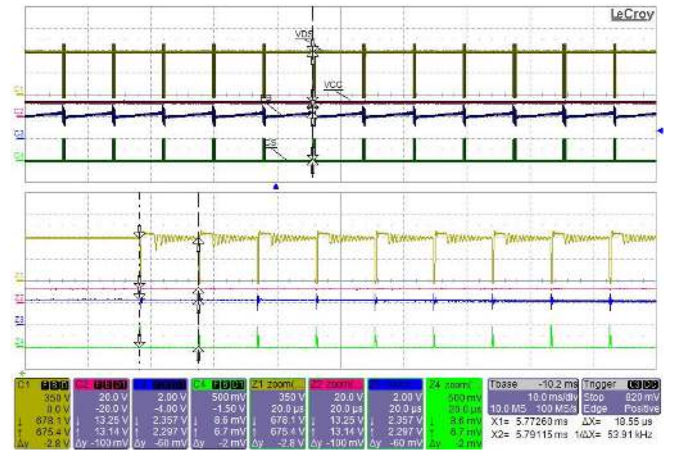
	
C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage
85 V AC ABM. Burst-on at FB voltage 2.35 V ($V_{FB\_Bon\_ISO}$) and burst-off at 2 V ($V_{FB\_Boff\_ISO}$). CS voltage at 0.27 V (V_{CS_BHP}). Switching frequency at 53 kHz (f_{OSC2_ABM}).	460 V AC ABM. Burst-on at FB voltage 2.35 V ($V_{FB\_Bon\_ISO}$) and burst-off at 2 V ($V_{FB\_Boff\_ISO}$). CS voltage at 0.27 V (V_{CS_BHP}). Switching frequency at 54 kHz (f_{OSC2_ABM}).

Figure 24 During ABM

10.10 Leaving ABM

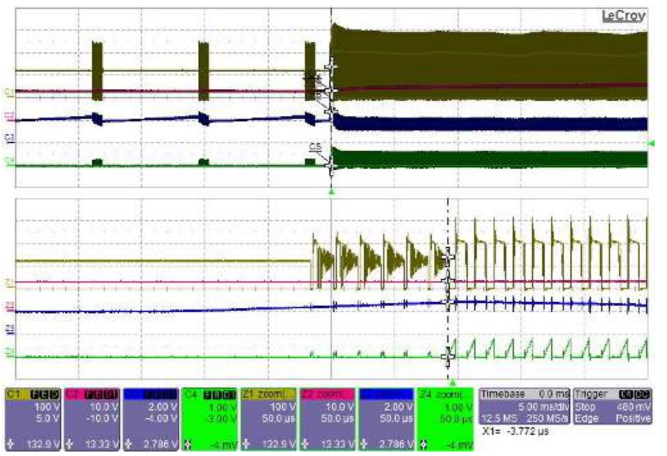
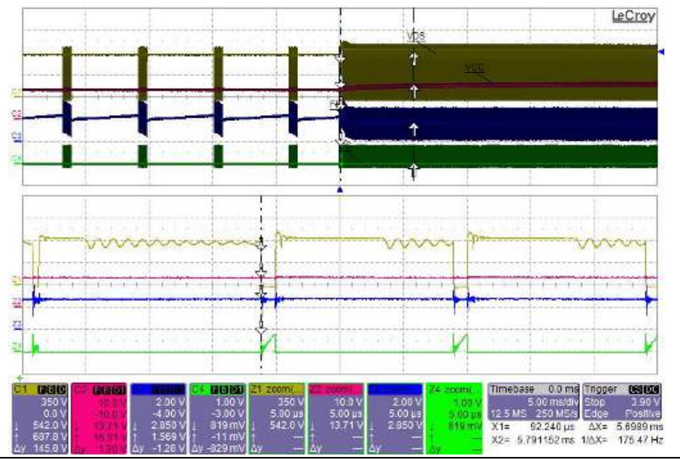
	
C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage
85 V AC Leaves ABM at FB voltage higher than 2.73 V (V_{FB_LB})	460 V AC Leaves ABM at FB voltage higher than 2.73 V (V_{FB_LB})

Figure 25 Leaving ABM

10.11 V_{CC} OV/UV protection

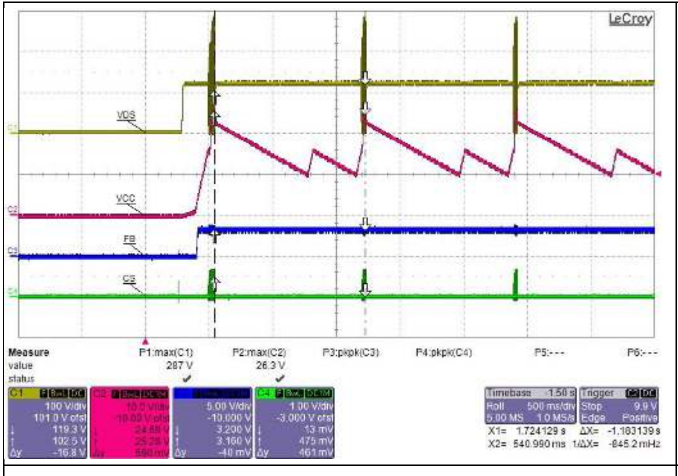
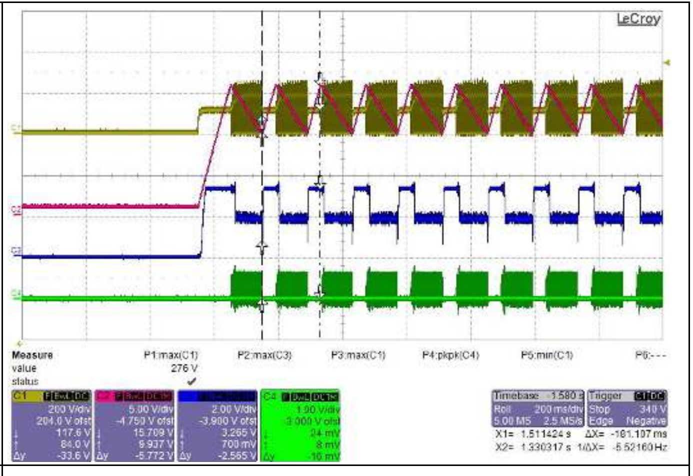
	
C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage
Trigger V_{CC} OVP at V_{CC} voltage greater than 25.5 V (V_{VCC_OVP}). Odd-skip auto-restart mode. Short R32.	Trigger V_{CC} UVP at V_{CC} voltage less than 10 V (V_{VCC_OFF}). Auto-restart mode. Open R23.

Figure 26 **V_{CC} OV/UV protection**

10.12 Overload protection

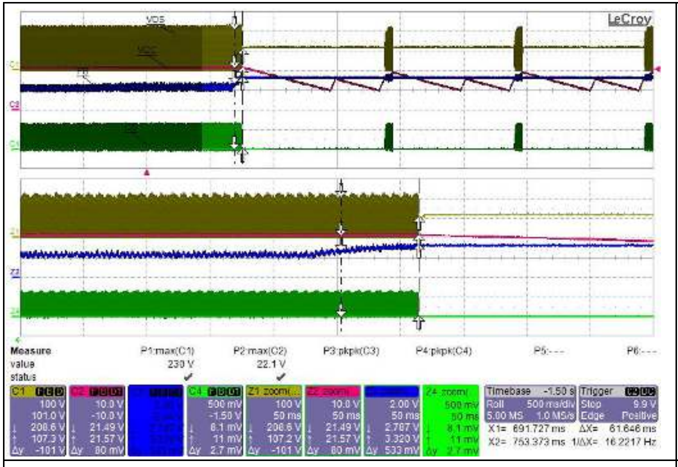
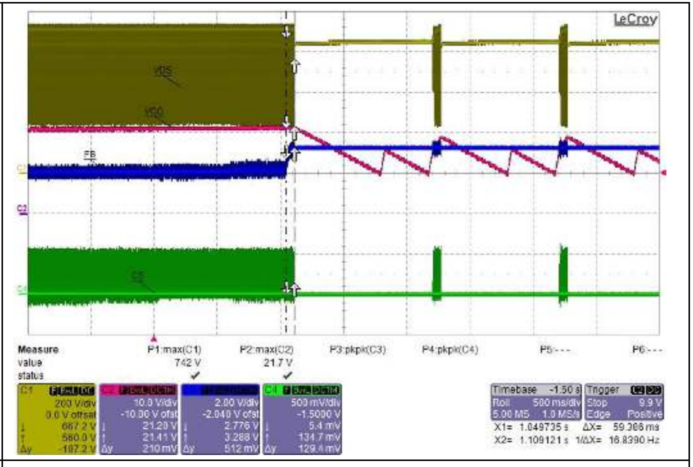
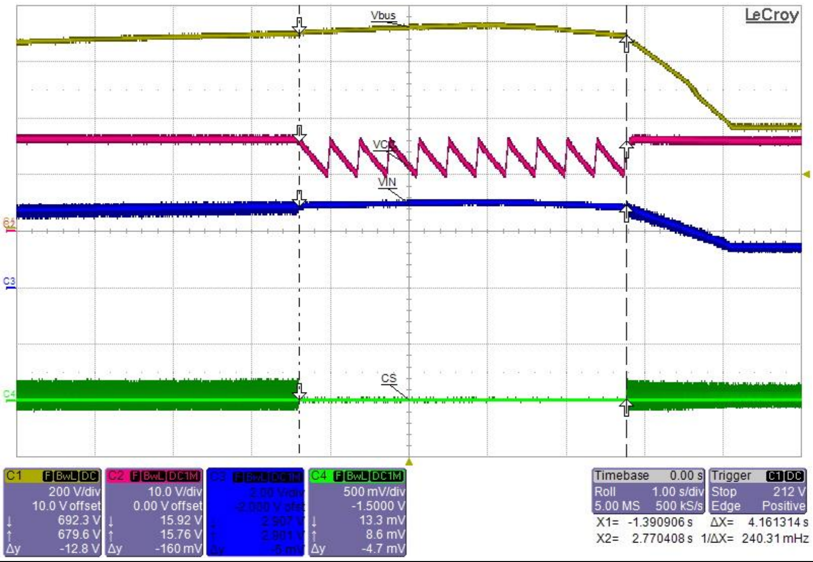
	
C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage
85 V AC at full load to overload. Trigger protection at FB pin voltage greater than 2.73 V (V_{FB_OLP}) for about 61 ms ($t_{FB\_OLP\_B}$). Odd-skip auto-restart mode.	460 V AC at full load to overload. Trigger protection at FB pin voltage greater than 2.73 V (V_{FB_OLP}) for about 59 ms ($t_{FB\_OLP\_B}$). Odd-skip auto-restart mode.

Figure 27 **Overload protection**

10.13 Line overvoltage protection



C1 (yellow) : Bus voltage
C2 (purple) : V_{CC} voltage
C3 (blue) : VIN pin voltage
C4 (green) : CS voltage

Trigger LOVP at (692 V bus voltage/490 V AC), VIN pin voltage is greater than 2.85 V (V_{VIN_LOVP}).
Non-switch auto-restart mode.
Resume switching when VIN pin voltage is lower than 2.85 V (V_{VIN_LOVP}).

Figure 28 Line overvoltage protection

11 Appendix A: Transformer design and spreadsheet

Calculation tool for FF flyback converter using fifth-generation CoolSET™ (Version 1.1)

Project:	REF_5BR3995CZ_16W1
Application:	Aux for metering
CoolSET™:	ICE5BR3995CZ
Date:	30 June 2021
Revision:	Version 1.1

Notes:

Enter design variables in orange-colored cells

Read design results in green-colored cells

Equation numbers are according to the design guide

Component designators refer to the calculation tool

Select component values based on standard values available

Voltage/current rating does not include design margin, voltage spikes and transient currents

In “Output regulation”, only fill in either isolated or non-isolated, whichever is applicable

	Description	Eq. #	Parameter	Unit	Value
Input, output, CoolSET™ specs					
Line input					
Input	Minimum AC input voltage		V_{ACMin}	[V]	85
Input	Maximum AC input voltage		V_{ACMax}	[V]	460
Input	Line frequency		f_{AC}	[Hz]	60
Input	Bus capacitor DC ripple voltage		$V_{DCRipple}$	[V]	30
Output 1 specs					
Input	Output voltage 1		V_{Out1}	[V]	12
Input	Output current 1		I_{Out1}	[A]	1
Input	Forward voltage of output diode 1		V_{FOut1}	[V]	0.6
Input	Output ripple voltage 1		$V_{OutRipple1}$	[V]	0.2
Result	Output power 1	Eq. 001	P_{Out1}	[W]	12
Result	Output load weight 1	Eq. 004	K_{L1}		0.79
Output 2 and 3 specs					
Input	Output voltage 2		V_{Out2}	[V]	8
Input	Output current 2		I_{Out2}	[A]	0.2
Input	Forward voltage of output diode 2		V_{FOut2}	[V]	0.2
Input	Output ripple voltage 2		$V_{OutRipple2}$	[V]	0.2
Result	Output power 2	Eq. 002	P_{Out2}	[W]	1.6
Result	Output load weight 2	Eq. 005	K_{L2}		0.11
Input	Output voltage 3		V_{Out2}	[V]	8
Input	Output current 3		I_{Out2}	[A]	0.2
Input	Forward voltage of output diode 3		V_{FOut2}	[V]	0.2
Input	Output ripple voltage 3		$V_{OutRipple2}$	[V]	0.2
Result	Output power 3	Eq. 002	P_{Out2}	[W]	1.6
Result	Output load weight 3	Eq. 005	K_{L2}		0.11
Auxiliary					
Input	V_{CC} voltage		V_{Vcc}	[V]	15
Input	Forward voltage of V_{CC} diode (D2)		$V_{F\ Vcc}$	[V]	0.6
Power					
Input	Efficiency		η		0.83
Result	Nominal output power	Eq. 003	P_{OutNom}	[W]	15.2

Input	Maximum output power for overload protection		P_{OutMax}	[W]	17
Result	Maximum input power for overload protection	Eq. 006	P_{InMax}	[W]	19.88
Input	Minimum output power		P_{OutMin}	[W]	0.2

Controller/CoolSET™

	Controller/CoolSET™				ICE5BR3995CZ
Input	Switching frequency		f_S	[Hz]	65000
Input	Targeted max. drain source voltage		V_{DSMax}	[V]	850
Input	Max. ambient temperature		T_{amax}	[°C]	50

Diode bridge and input capacitor

Diode bridge

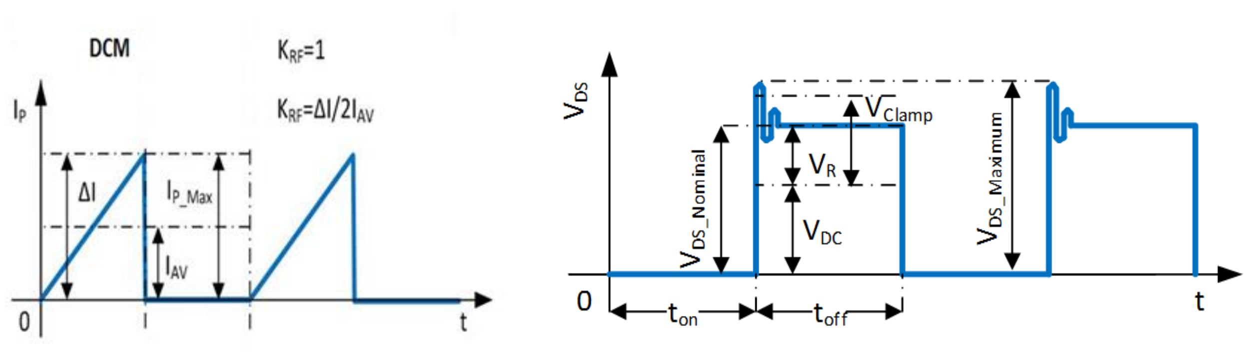
Input	Power factor		cosφ		0.6
Result	Maximum AC input current	Eq. 007	I_{ACRMS}	[A]	0.39
Result	Peak voltage at V_{ACMax}	Eq. 008	$V_{DCMaxPk}$	[V]	650.54

Input capacitor

Result	Peak voltage at V_{ACMin}	Eq. 009	$V_{DCMinPk}$	[V]	120.21
Result	Selected minimum DC input voltage	Eq. 010	$V_{DCMinSet}$	[V]	90.21
Result	Discharging time at each half-line cycle	Eq. 011	T_D	[ms]	6.42
Result	Required energy at discharging time of input capacitor	Eq. 012	W_{In}	[Ws]	0.13
Result	Calculated input capacitor	Eq. 013	C_{INCal}	[µF]	40.42
Input	Select input capacitor (C1)		C_{in}	[µF]	47
Result	Calculated minimum DC input voltage	Eq. 015	V_{DCMin}	[V]	94.98

Transformer design

Drain voltage and current waveform



Primary inductance and winding currents

Input	Reflection voltage		V_{RSET}	[V]	80
Result	Maximum duty cycle	Eq. 016	D_{Max}		0.46
Input	Select current ripple factor		K_{RF}		1
Result	Primary inductance	Eq. 017	L_P	[H]	7.30E-04
Result	Primary turn-on average current	Eq. 018	I_{AV}	[A]	0.46
Result	Primary peak-to-peak current	Eq. 019	ΔI	[A]	0.92
Result	Primary peak current	Eq. 020	I_{PMax}	[A]	0.92
Result	Primary valley current	Eq. 021	I_{Valley}	[A]	0.00
Result	Primary RMS current	Eq. 022	I_{PRMS}	[A]	0.357

Select core type

Input	Select core type				2

Result	Core type				E25/13/7
Result	Core material				N87
Result	Maximum flux density		B_{Max}	[T]	0.3
Result	Cross-sectional area		A_e	[mm²]	52
Result	Bobbin width		BW	[mm]	15.6
Result	Winding cross-section		A_N	[mm²]	61
Result	Average length of turn		l_N	[mm]	50

Winding calculation

Result	Calculated minimum number of primary turns	Eq. 023	N_{PCal}	Turns	42.82
Input	Select number of primary turns		N_P	Turns	58
Result	Calculated number of secondary 1 turns	Eq. 024	N_{S1Cal}	Turns	9.14
Input	Select number of secondary 1 turns		N_{S1}	Turns	9
Result	Calculated number of secondary 2 turns	Eq. 025	N_{S2Cal}	Turns	5.95
Input	Select number of secondary 2 turns		N_{S2}	Turns	6
Result	Calculated number of auxiliary turns	Eq. 026	N_{VccCal}	Turns	11.14
Input	Select number of auxiliary turns		N_{Vcc}	Turns	10
Result	Calculated V_{CC} voltage	Eq. 027	V_{VccCal}	[V]	13.40

Post calculation

Result	Primary to secondary 1 turns ratio	Eq. 028	N_{PS1}		6.44
Result	Primary to secondary 2 turns ratio	Eq. 029	N_{PS2}		9.67
Result	Post-calculated reflected voltage	Eq. 030	V_{RPost}	[V]	81.20
Result	Post-calculated maximum duty cycle	Eq. 031	$D_{MaxPost}$		0.46
Result	Duty cycle prime	Eq. 032	D_{Max}'		0.53
Result	Actual flux density	Eq. 033	B_{MaxAct}	[T]	0.222
Result	Maximum DC input voltage for CCM operation	Eq. 034	$V_{DCmaxCCM}$	[V]	93.34

Transformer winding design

Input	Margin according to safety standard		M	[mm]	0
Input	Copper space factor		f_{Cu}		0.4
Result	Effective bobbin window	Eq. 035	BW_E	[mm]	15.6
Result	Effective winding cross-section	Eq. 036	A_{Ne}	[mm²]	61.0
Input	Primary winding area factor		AF_{NP}		0.45
Input	Secondary 1 winding area factor		AF_{NS1}		0.25
Input	Secondary 2 winding area factor		AF_{NS2}		0.20
Input	Auxiliary winding area factor		AF_{NVcc}		0.10

Primary winding

Result	Calculated copper wire cross-sectional area	Eq. 037	A_{PCal}	[mm²]	0.1893
Result	Calculated maximum wire size	Eq. 038	AWG_{PCal}		24
Input	Select wire size		AWG_P		28
Input	Select number of parallel wire		nw_P		1
Result	Copper wire diameter	Eq. 039	d_P	[mm]	0.32
Result	Copper wire cross-sectional area	Eq. 040	A_P	[mm²]	0.0821
Result	Wire current density	Eq. 041	S_P	[A/mm²]	4.35
Input	Insulation thickness		INS_P	[mm]	0.01
Result	Turns per layer	Eq. 042	NL_P	Turns/layer	45
Result	Number of layers	Eq. 043	Ln_P	Layers	2

Secondary 1 winding

Result	Calculated copper wire cross-sectional area	Eq. 044	A_{NS1Cal}	[mm²]	0.6778
Result	Calculated maximum wire size	Eq. 045	AWG_{S1Cal}		19
Input	Select wire size		AWG_{S1}		22

Input	Select number of parallel wires		nw_{S1}		1
Result	Copper wire diameter	Eq. 046	d_{S1}	[mm]	0.6465
Result	Copper wire cross-sectional area	Eq. 047	A_{S1}	[mm^2]	0.3282
Result	Peak current	Eq. 048	I_{S1Max}	[A]	4.6537
Result	RMS current	Eq. 049	I_{S1RMS}	[A]	1.9648
Result	Wire current density	Eq. 050	S_{S1}	[A/mm^2]	5.99
Input	Insulation thickness		INS_{S1}	[mm]	0.02
Result	Turns per layer	Eq. 051	NL_{S1}	Turns/layer	9
Result	Number of layers	Eq. 052	Ln_{S1}	Layers	1

Secondary 2 winding

Result	Calculated copper wire cross-sectional area	Eq. 053	A_{NS2Cal}	[mm^2]	0.8133
Result	Calculated maximum wire size	Eq. 054	AWG_{S2Cal}		18
Input	Select wire size		AWG_{S2}		26
Input	Select number of parallel wires		nw_{S2}		1
Result	Copper wire diameter	Eq. 055	d_{S2}	[mm]	0.4073
Result	Copper wire cross-sectional area	Eq. 056	A_{S2}	[mm^2]	0.1303
Result	Peak current	Eq. 057	I_{S2Max}	[A]	0.9307
Result	RMS current	Eq. 058	I_{S2RMS}	[A]	0.3930
Result	Wire current density	Eq. 059	S_{S2}	[A/mm^2]	3.02
Input	Insulation thickness		INS_{S2}	[mm]	0.02
Result	Turns per layer	Eq. 060	NL_{S2}	Turns/layer	34
Result	Number of layers	Eq. 061	Ln_{S2}	Layers	1

RCD clamper and CS resistor

RCD clamper circuit

Input	Leakage inductance percentage		$L_{LK\%}$	[%]	1
Result	Leakage inductance	Eq. 062	L_{LK}	[H]	7.30E-06
Result	Clamping voltage	Eq. 063	V_{Clamp}	[V]	118.26
Result	Calculated clamping capacitor	Eq. 064	$C_{ClampCal}$	[nF]	0.26
Input	Select clamping capacitor value (C2)		C_{Clamp}	[nF]	1
Result	Calculated clamping resistor	Eq. 065	$R_{ClampCal}$	[kΩ]	167.0
Input	Select clamping resistor value (R4)		R_{Clamp}	[kΩ]	400

CS resistor

Input	CS threshold value from datasheet		V_{CS_N}	[V]	0.8
Result	Calculated current sense resistor (R8A, R8B)	Eq. 066	R_{sense}	[Ω]	0.87

Output rectifier

Secondary 1 output rectifier

Result	Diode reverse voltage	Eq. 067	$V_{RDiode1}$	[V]	112.95
Result	Diode RMS current		I_{S1RMS}	[A]	1.96
Input	Max. voltage undershoot at output capacitor		ΔV_{Out1}	[V]	0.3
Input	Number of clock periods		n_{cp1}		20
Result	Output capacitor ripple current	Eq. 068	$I_{Ripple1}$	[A]	1.69
Result	Calculated minimum output capacitor	Eq. 069	$C_{Out1Cal}$	[µF]	1026
Input	Select output capacitor value (C152)		C_{Out1}	[µF]	1000
Input	ESR (Z_{max}) value from datasheet at 100 kHz		R_{ESR1}	[Ω]	0.032
Input	Number of parallel capacitors		nc_{COut1}		1
Result	Zero frequency of output capacitor	Eq. 070	f_{ZCOut1}	[kHz]	4.97
Result	First-stage ripple voltage	Eq. 071	$V_{Ripple1}$	[V]	0.148919
Input	Select LC filter inductor value (L151)		L_{out1}	[µH]	4.7
Result	Calculated LC filter capacitor	Eq. 072	C_{LCCal1}	[µF]	217.9
Input	Select LC filter capacitor value (C153)		C_{LC1}	[µF]	220

Result	LC filter frequency	Eq. 073	f_{LC1}	[kHz]	4.95
Result	Second-stage ripple voltage	Eq. 074	$V_{2ndRipple1}$	[mV]	0.86

Secondary 2 output rectifier

Result	Diode reverse voltage	Eq. 075	$V_{RDiode2}$	[V]	75.30
Result	Diode RMS current		I_{S2RMS}	[A]	0.39
Input	Max. voltage undershoot at output capacitor		ΔV_{Out1}	[V]	0.15
Input	Number of clock periods		n_{cp2}		20
Result	Output capacitor ripple current	Eq. 076	$I_{Ripple2}$	[A]	0.34
Result	Calculated minimum output capacitor	Eq. 077	$C_{Out2Cal}$	[µF]	410
Input	Select output capacitor value (C152)		C_{Out2}	[µF]	330

V_{CC} diode and capacitor

V_{CC} diode and capacitor

Result	Auxiliary diode reverse voltage (D2)	Eq. 083	$V_{RDiodeVCC}$	[V]	125.56
Input	Soft-start time from datasheet		t_{ss}	[ms]	12
Input	$I_{VCC,Charge3}$ from datasheet		$I_{VCC\_Charge3}$	[mA]	2
Input	V_{CC} on-threshold		V_{VCC_ON}	[V]	16
Input	V_{CC} off-threshold		V_{VCC_OFF}	[V]	10
Result	Calculated V_{CC} capacitor	Eq. 084	C_{VCCCal}	[µF]	22.00
Input	Select V_{CC} capacitor (C3)		C_{VCC}	[µF]	22
Input	V_{CC} short threshold from datasheet		V_{VCC_SCP}	[V]	1.1
Input	$I_{VCC\_Charge1}$ from datasheet		$I_{VCC\_Charge1}$	[mA]	0.2
Result	Start-up time	Eq. 085	$t_{StartUp}$	[ms]	284.90

Calculation of losses

Input diode bridge

Input	Diode bridge forward voltage		V_{FBR}	[V]	1
Result	Diode bridge power loss	Eq. 086	P_{DIN}	[W]	0.78

Transformer copper

Result	Primary winding copper resistance	Eq. 087	R_{PCu}	[mΩ]	607.52
Result	Secondary 1 winding copper resistance	Eq. 088	R_{S1Cu}	[mΩ]	23.58
Result	Secondary 2 winding copper resistance	Eq. 089	R_{S2Cu}	[mΩ]	39.60
Result	Primary winding copper loss	Eq. 090	P_{PCu}	[mW]	77.62
Result	Secondary 1 winding copper loss	Eq. 091	P_{S1Cu}	[mW]	91.04
Result	Secondary 2 winding copper loss	Eq. 092	P_{S2Cu}	[mW]	6.12
Result	Total transformer copper loss	Eq. 093	P_{Cu}	[W]	0.1748

Output rectifier diode

Result	Secondary 1 diode loss	Eq. 094	P_{Diode1}	[W]	1.18
Result	Secondary 2 diode loss	Eq. 095	P_{Diode2}	[W]	0.08

RCD clamper circuit

Result	RCD clamper loss	Eq. 096	$P_{Clamper}$	[W]	0.34

Current sense resistor

Result	CS resistor loss	Eq. 097	P_{CS}	[W]	0.11

MOSFET

Input	$R_{DS(on)}$ from datasheet		$R_{DS(on)}$ at T_A = 125°C	[Ω]	7.69
Input	$C_{o(er)}$ from datasheet		$C_{o(er)}$	[pF]	5
Input	Total capacitance at drain pin (external)		C_{DS}	[pF]	25
Result	Switch-on loss at minimum AC input voltage	Eq. 098	$P_{SONMinAC}$	[W]	0.0303
Result	Conduction loss at minimum AC input voltage	Eq. 099	$P_{condMinAC}$	[W]	0.9825

Result	Total MOSFET loss at minimum AC input voltage	Eq. 100	$P_{MOSMinAC}$	[W]	1.0127
Result	Switch-on loss at maximum AC input voltage	Eq. 101	$P_{SONMaxAC}$	[W]	0.5221
Result	Conduction loss at maximum AC input voltage	Eq. 102	$P_{condMaxAC}$	[W]	0.1434
Result	Total MOSFET loss at maximum AC input voltage	Eq. 103	$P_{MOSMaxAC}$	[W]	0.6655
Result	Total MOSFET loss (from minimum or maximum AC)		P_{MOS}	[W]	1.0127

Controller

Input	Controller current consumption		$I_{VCC\_Normal2}$	[mA]	2
Result	Controller loss	Eq. 104	P_{Ctrl}	[W]	0.027

Efficiency after losses

Result	Total power loss	Eq. 105	P_{Losses}	[W]	3.70
Result	Post calculated efficiency	Eq. 106	η_{Post}	%	81.68%

CoolSET™/MOSFET temperature

CoolSET™/MOSFET temperature

Input	Enter thermal resistance junction-ambient (include copper pour)		R_{thJA_As}	[°K/W]	80
Result	Temperature rise	Eq. 107	ΔT	[°K]	81.1
Result	Junction temperature at T_{amax}	Eq. 108	Tjmax	°C	131.1

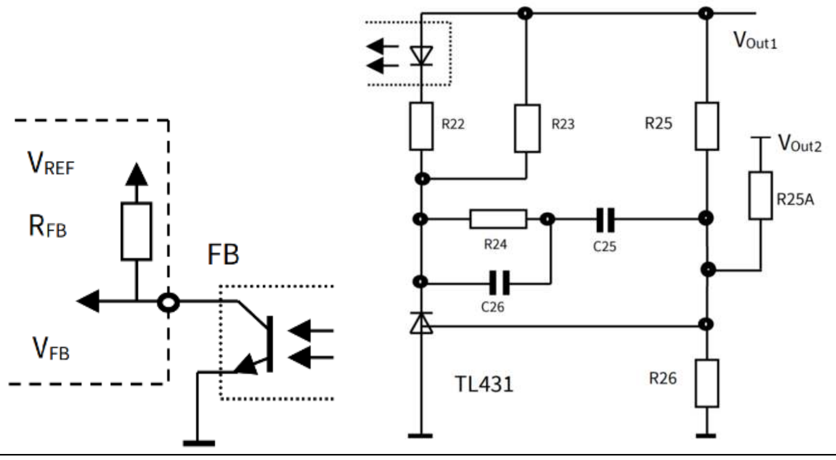
Line OVP

Line OVP

Input	Select AC input LOVP		V_{OVP_AC}	[V AC]	500
Input	High-side DC input voltage divider/resistor (R3A, R3B, R3C)		R_{I1}	[MΩ]	5
Input	Controller LOVP threshold		V_{VIN_LOVP}	[V]	2.85
Result	Low-side DC input voltage divider/resistor	Eq. 109	R_{I2Cal}	[kΩ]	20.23
Input	Select low-side DC input voltage divider/resistor (R7)		R_{I2}	[kΩ]	20.5
Result	Post-calculated LOVP	Eq. 110	V_{OVP_ACPost}	[V AC]	493.54

Output regulation (isolated using TL431 and optocoupler)

Isolated feedback circuit



Output regulation

Input	TL431 reference voltage		V_{REF_TL}	[V]	2.5
Input	Weighted regulation factor of V_{Out1}		W_1		1
Input	Current for voltage divider/resistor R26		I_{R26}	[mA]	0.25
Result	Calculated voltage divider/resistor	Eq. 111	$R26_{Cal}$	[kΩ]	10
Input	Select voltage divider/resistor value		R26	[kΩ]	10
Result	Calculated voltage divider/resistor	Eq. 112	$R25_{Cal}$	[kΩ]	38.00
Input	Select voltage divider/resistor value		R25	[kΩ]	38.0

Optocoupler and TL431 bias

Input	Current transfer ratio (CTR)		G_C	[Percent]	200%

Input	Optocoupler diode forward voltage		V_{FOpto}	[V]	1.25
Input	Maximum current for optocoupler diode		I_{Fmax}	[mA]	50
Input	Minimum current for TL431		I_{KAmin}	[mA]	1
Result	Calculated minimum optocoupler bias resistance	Eq. 114	$R22_{Cal}$	[kΩ]	0.1650
Input	Select optocoupler bias resistor		R22	[kΩ]	1
Input	FB pull-up reference voltage V_{REF} from datasheet		V_{REF}	[V]	3.3
Input	V_{FB_OLP} from datasheet		V_{FB_OLP}	[V]	2.75
Input	R_{FB} from datasheet		R_{FB}	[kΩ]	15
Result	Calculated maximum TL431 bias resistance	Eq. 115	$R23_{Cal}$	[kΩ]	1.27
Input	Selected TL431 bias resistor		R23	[kΩ]	1

Regulation loop

Result	FB transfer characteristic	Eq. 116	K_{FB}		30.00
Result	Gain of FB transfer characteristic	Eq. 117	G_{FB}	[db]	29.54
Result	Voltage divider transfer characteristic	Eq. 118	K_{VD}		0.208333
Result	Gain of voltage divider transfer characteristic	Eq. 119	G_{VD}	[db]	-13.62
Result	Resistance at maximum load pole	Eq. 120	R_{LH}	[Ω]	8.73
Result	Resistance at minimum load pole	Eq. 121	R_{LL}	[Ω]	48.00
Result	Poles of power stage at maximum load pole	Eq. 122	f_{OH}	[Hz]	36.47
Result	Poles of power stage at minimum load pole	Eq. 123	f_{OL}	[Hz]	6.63
Result	Zero frequency of the compensation network	Eq. 124	f_{OM}	[Hz]	15.55
Input	Zero dB crossover frequency		fg	[kHz]	5
Input	PWM-OP gain from datasheet		A_V		2.03
Result	Transient impedance	Eq. 117	Z_{PWM}	[V/A]	2.2
Result	Power stage at crossover frequency	Eq. 118	$\|F_{PWR}(fg)\|$		0.043
Result	Gain of power stage at crossover frequency	Eq. 119	$G_{PWR}(fg)$	[db]	-27.31
Result	Gain of the regulation loop at fg	Eq. 120	Gs(ω)	[db]	-11.389
Result	Separated components of the regulator	Eq. 121	Gr(ω)	[db]	11.389
Result	Calculated resistance value of compensation network	Eq. 122	$R24_{Cal}$	[kΩ]	29.38
Input	Select resistor value of compensation network		R24	[kΩ]	22
Result	Calculated capacitance value of compensation network	Eq. 123	$C26_{Cal}$	[nF]	1.447
Input	Select capacitor value of compensation network		C26	[nF]	1
Result	Calculated capacitance value of compensation network	Eq. 124	$C25_{Cal}$	[nF]	464.17
Input	Select capacitor value of compensation network		C25	[nF]	220

Final design

Electrical

Minimum AC voltage			[V]	85
Maximum AC voltage			[V]	460
Maximum input current			[A]	0.23
Minimum DC voltage			[V]	95
Maximum DC voltage			[V]	651
Maximum output power			[W]	16.5
Output voltage 1			[V]	12.0
Output ripple voltage 1			[mV]	0.9
Output voltage 1			[V]	8.0
Output ripple voltage 1			[mV]	0.0
Transformer peak current			[A]	0.92
Maximum duty cycle				0.46
Reflected voltage			[V]	81
Copper losses			[W]	0.17
MOSFET losses			[W]	1.01
Sum losses			[W]	3.70
Efficiency			[Percent]	81.68%

Transformer

Core type				E25/13/7

Core material				N87
Effective core area			[mm²]	52
Maximum flux density			[mT]	222
Inductance			[µH]	730
Margin			[mm]	0
Primary turns			Turns	58
Primary copper wire size			AWG	28
Number of primary copper wires in parallel				1
Primary layers			Layer	2
Secondary 1 turns (N_{S1})			Turns	9
Secondary 1 copper wire size			AWG	22
Number of secondary 1 copper wires in parallel				1
Secondary 1 layers			Layer	1
Secondary 2 turns (N_{S2})			Turns	6
Secondary 2 copper wire size			AWG	26
Number of secondary 2 copper wires in parallel				1
Secondary 2 layers			Layer	1
Auxiliary turns			Turns	10
Leakage inductance			[µH]	7.3

Components

Input capacitor (C1)			[µF]	47.0
Secondary 1 output capacitor (C152)			[µF]	1000.0
Secondary 1 output capacitor in parallel				1.0
Secondary 1 LC filter inductor (L151)			[µH]	4.7
Secondary 1 LC filter capacitor (C153)			[µF]	220.0
Secondary 2 output capacitor (C102)			[µF]	330.0
Secondary 2 output capacitor in parallel				1.0
V_{CC} capacitor (C3)			[µF]	22.0
Sense resistor (R8A, R8B)			[Ω]	0.87
Clamping resistor (R4)			[kΩ]	400.0
Clamping capacitor (C2)			[nF]	1
High-side DC input voltage divider/resistor (R3A, R3B, R3C)			[MΩ]	5000.0
Low-side DC input voltage divider/resistor (R7)			[kΩ]	20.5

Regulation components (isolated using TL431 and optocoupler)

Voltage divider		R26	[kΩ]	10.0
Voltage divider (V_{out1} sense)		R25	[kΩ]	38.0
Optocoupler bias resistor		R22	[kΩ]	1.00
TL431 bias resistor		R23	[kΩ]	1.0
Compensation network resistor		R24	[kΩ]	22.0
Compensation network capacitor		C26	[nF]	1.00
Compensation network capacitor		C25	[nF]	220.0

12 References

[1] Infineon Technologies AG: ICE5xRxxxxxZ Datasheet (V 1.0); 2022-02-22; **ICE5xRxxxxxZ Datasheet**

[2] Infineon Technologies AG: Fifth-generation fixed-frequency design guide (V 1.1); 2019-07-24; **Fifth-generation fixed-frequency design guide**

[3] Infineon Technologies AG: Calculation tool for fixed-frequency flyback converter using fifth-generation CoolSET™ (V 1.1); 2018-02-26; **Calculation tool fixed-frequency CoolSET™ 5th generation**

Revision history

Document version	Date of release	Description of changes
V 1.0	2022-06-15	First release
V 1.1	2023-06-11	Changed “m” to “M” in BOM list

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