ON Semiconductor®

System Hardware Monitor with Remote Diode Thermal Sensing

ADM1024

FEATURES

- Up to Nine Measurement Channels
- Inputs Programmable-to-Measure Analog Voltage, Fan Speed or External Temperature
- External Temperature Measurement with Remote Diode (Two Channels)
- On-Chip Temperature Sensor
- Five Digital Inputs for VID Bits
- LDCM Support
- System Management Bus (SMBus)
- Chassis Intrusion Detect
- Interrupt and Over Temperature Outputs
- Programmable $\overline{\text{RESET}}$ Input Pin
- Shutdown Mode to Minimize Power Consumption
- Limit Comparison of all Monitored Values

APPLICATIONS

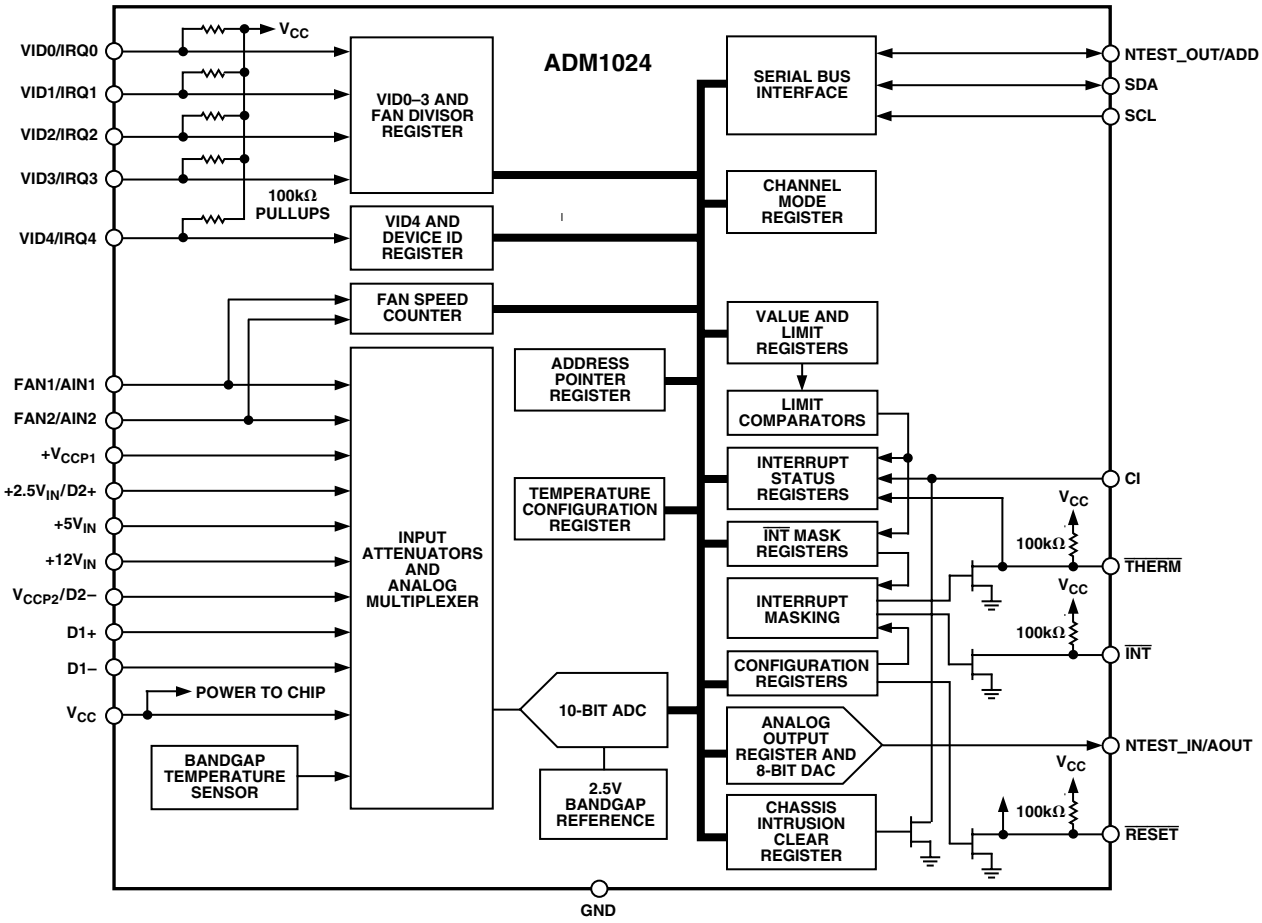
- Network Servers and Personal Computers
- Microprocessor-Based Office Equipment
- Test Equipment and Measuring Instruments

PRODUCT DESCRIPTION

The ADM1024 is a complete system hardware monitor for microprocessor-based systems, providing measurement and limit comparison of various system parameters. Eight measurement inputs are provided, of which three are dedicated to monitoring 5 V and 12 V power supplies and the processor core voltage. The ADM1024 can monitor a fourth power-supply voltage by measuring its own V_{CC}. One input (two pins) is dedicated to a remote temperature-sensing diode. Two further pins can be

(*continued on page 7*)

FUNCTIONAL BLOCK DIAGRAM



REVISION HISTORY

02/08—Rev 1: Conversion to ON Semiconductor

February 2008 - Rev. 1

Publication Order Number:
ADM1024/D

ADM1024–SPECIFICATIONS[1, 2] ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
Supply Voltage, V_{CC}	2.8	3.30	5.5	V	
Supply Current, I_{CC}		1.4	3.5	mA	Interface Inactive, ADC Active
		1.0		mA	ADC Inactive, DAC Active
		45	145	µA	Shutdown Mode
TEMPERATURE-TO-DIGITAL CONVERTER					
Internal Sensor Accuracy			±3	°C	$0°C \le T_A \le 100°C$
			±2	°C	$T_A = 25°C$
Resolution		±1		°C	
External Diode Sensor Accuracy			±5	°C	$0°C \le T_A \le 100°C$
		±3		°C	25°C
Resolution		±1		°C	
Remote Sensor Source Current	80	110	150	µA	High Level
	4	6.5	9	µA	Low Level
ANALOG-TO-DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Total Unadjusted Error, TUE (12 V_{IN})			±4	%	(See Note 3)
TUE (AIN, V_{CCP}, 2.5 V_{IN}, 5 V_{IN})			±3	%	
Differential Nonlinearity, DNL			±1	LSB	
Power Supply Sensitivity		±1		%/V	
Conversion Time (Analog Input or Int. Temp)		754.8	856.8	µs	$0°C \le T_A \le 100°C$[4]
Conversion Time (External Temperature)		9.6		ms	(See Note 4)
Input Resistance (2.5 V, 5 V, 12 V, V_{CCP1}, V_{CCP2})	80	140	200	kΩ	
Input Resistance (AIN1, AIN2)		5		MΩ	
ANALOG OUTPUT					
Output Voltage Range	0		2.5	V	
Total Unadjusted Error, TUE			±3	%	I_L = 2 mA
Full-Scale Error		±1	±5	%	
Zero-Scale Error		2		LSB	No Load
Differential Nonlinearity, DNL			±1	LSB	Monotonic by Design
Integral Nonlinearity		±1		LSB	
Output Source Current		2		mA	
Output Sink Current		1		mA	
FAN RPM-TO-DIGITAL CONVERTER					
Accuracy			±12	%	$0°C \le T_A \le 100°C$
Full-Scale Count			255		
FAN1 and FAN2 Nominal Input RPM[5]		8800		rpm	Divisor = 1, Fan Count = 153
		4400		rpm	Divisor = 2, Fan Count = 153
		2200		rpm	Divisor = 3, Fan Count = 153
		1100		rpm	Divisor = 4, Fan Count = 153
Internal Clock Frequency	19.8	22.5	25.2	kHz	$0°C \le T_A \le 100°C$
DIGITAL OUTPUTS NTEST_OUT					
Output High Voltage, V_{OH}	2.4			V	I_{OUT} = +3.0 mA, V_{CC} = 2.85 V – 3.60 V
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = –3.0 mA, V_{CC} = 2.85 V – 3.60 V
OPEN-DRAIN DIGITAL OUTPUTS (INT, $\overline{\text{THERM}}$, $\overline{\text{RESET}}$)					(See Note 6)
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = –3.0 mA, V_{CC} = 3.60 V
High Level Output Current, I_{OH}		0.1	100	µA	$V_{OUT} = V_{CC}$
$\overline{\text{RESET}}$ and CI Pulsewidth	20	45		ms	
OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = –3.0 mA, V_{CC} = 2.85 V – 3.60 V
High Level Output Current, I_{OH}		0.1	100	µA	$V_{OUT} = V_{CC}$

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL BUS DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}	2.2			V	
Input Low Voltage, V_{IL}			0.8	V	
Hysteresis		500		mV	
Glitch Immunity		100		ns	
DIGITAL INPUT LOGIC LEVELS (ADD, CI, $\overline{\text{RESET}}$, VID0–VID4, FAN1, FAN2)					(See Note 7)
Input High Voltage, V_{IH}	2.2			V	V_{CC} = 2.85 V – 5.5 V
Input Low Voltage, V_{IL}			0.8	V	V_{CC} = 2.85 V – 5.5 V
NTEST_IN					
Input High Voltage, V_{IH}	2.2			V	V_{CC} = 2.85 V – 5.5 V
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}	–1			µA	$V_{IN} = V_{CC}$
Input Low Current, I_{IL}			1	µA	V_{IN} = 0
Input Capacitance, C_{IN}		20		pF	
SERIAL BUS TIMING[8]					
Clock Frequency, f_{SCLK}			400	kHz	See Figure 1
Glitch Immunity, t_{SW}			50	ns	See Figure 1
Bus Free Time, t_{BUF}	1.3			µs	See Figure 1
Start Setup Time, $t_{SU;STA}$	600			ns	See Figure 1
Start Hold Time, $t_{HD;STA}$	600			ns	See Figure 1
SCL Low Time, t_{LOW}	1.3			µs	See Figure 1
SCL High Time, t_{HIGH}	0.6			µs	See Figure 1
SCL, SDA Rise Time, t_r			300	ns	See Figure 1
SCL, SDA Fall Time, t_f			300	µs	See Figure 1
Data Setup Time, $t_{SU;DAT}$	100			ns	See Figure 1
Data Hold Time, $t_{HD;DAT}$			900	ns	See Figure 1

NOTES

[1]All voltages are measured with respect to GND, unless otherwise specified.

[2]Typicals are at T_A = 25°C and represent most likely parametric norm. Shutdown current typ is measured with V_{CC} = 3.3 V.

[3]TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC, multiplexer and on-chip input attenuators, including an external series input protection resistor value between zero and 1 kΩ.

[4]Total monitoring cycle time is nominally $m \times 755$ µs + $n \times 33244$ µs, where m is the number of channels configured as analog inputs, plus two for the internal V_{CC} measurement and internal temperature sensor, and n is the number of channels configured as external temperature channels (D1 and D2).

[5]The total fan count is based on two pulses per revolution of the fan tachometer output.

[6]Open-drain digital outputs may have an external pull-up resistor connected to a voltage lower or higher than V_{CC} (up to 6.5 V absolute maximum).

[7]All logic inputs except ADD are tolerant of 5 V logic levels, even if V_{CC} is less than 5 V. ADD is a three-state input that may connected to V_{CC}, GND, or left open-circuit.

[8]Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge and V_{IH} = 2.2 V for a rising edge.

Specifications subject to change without notice.

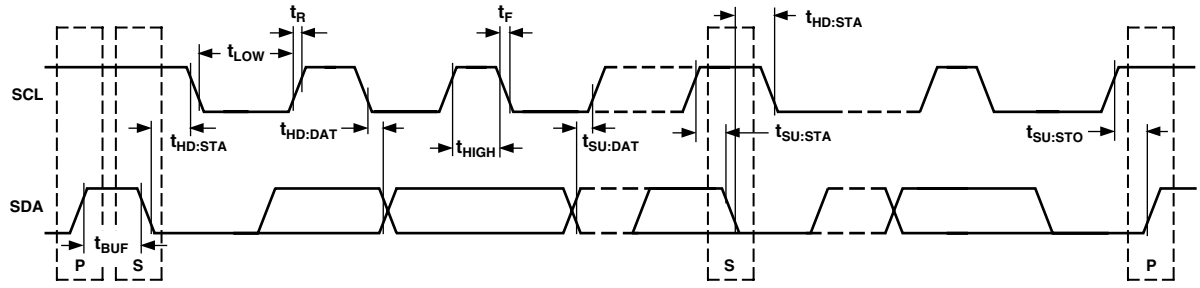


Figure 1. Diagram for Serial Bus Timing

ABSOLUTE MAXIMUM RATINGS*

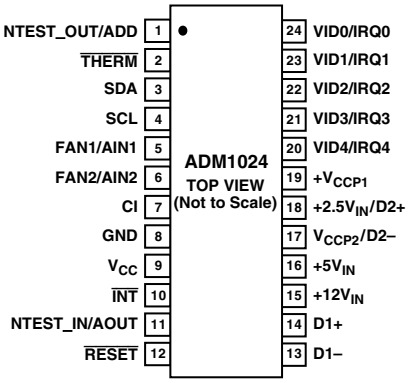
Positive Supply Voltage (V_{CC}) . . . . . 6.5 V
Voltage on 12 V V_{IN} Pin . . . . . 20 V
Voltage on AOUT, N TEST_OUT ADD, 2.5 V_{IN}/D2+ . . . . . –0.3 V to (V_{CC} + 0.3 V)
Voltage on Any Other Input or Output Pin . . –0.3 V to +6.5 V
Input Current at Any Pin . . . . . ±5 mA
Package Input Current . . . . . ±20 mA
Maximum Junction Temperature (T_J max) . . . . . 150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature, Soldering
Vapor Phase 60 sec . . . . . 215°C
Infrared 15 sec . . . . . 200°C
ESD Rating All Pins . . . . . 2000 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

24-Lead Small Outline Package: θ_{JA} = 50°C/W, θ_{JC} = 10°C/W.

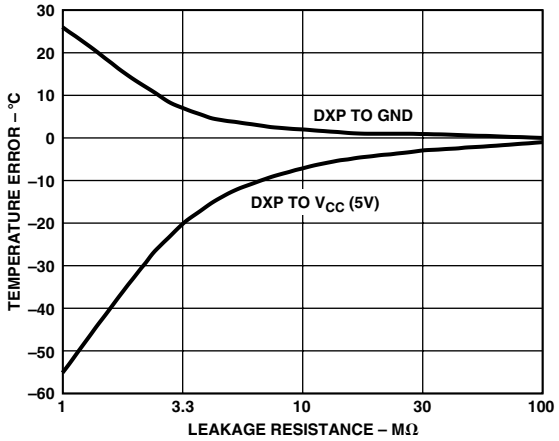
PIN CONFIGURATION



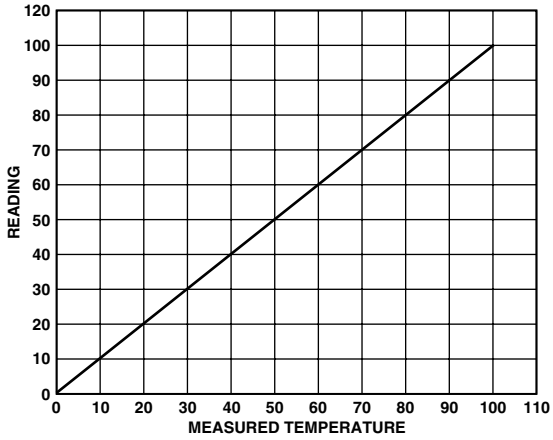
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	NTEST_OUT/ADD	Digital I/O. Dual Function pin. This is a three-state input that controls the 2 LSBs of the Serial Bus Address. This pin functions as an output when doing a NAND test.
2	$\overline{\text{THERM}}$	Digital I/O. Dual Function pin. This pin functions as an interrupt output for temperature interrupts only, or as an interrupt input for fan control. It has an on-chip 100 kΩ pull-up resistor.
3	SDA	Digital I/O. Serial Bus bidirectional Data. Open-drain output.
4	SCL	Digital Input. Serial Bus Clock.
5	FAN1/AIN1	Programmable Analog/Digital Input. 0 V to 2.5 V analog input or digital (0 to V_{CC}) amplitude fan tachometer input.
6	FAN2/AIN2	Programmable Analog/Digital Input. 0 V to 2.5 V analog input or digital (0 to V_{CC}) amplitude fan tachometer input.
7	CI	Digital I/O. An active high input from an external latch which captures a Chassis Intrusion event. This line can go high without any clamping action, regardless of the powered state of the ADM1024. The ADM1024 provides an internal open drain on this line, controlled by Bit 6 of Register 40h or Bit 7 of Register 46h, to provide a minimum 20 ms pulse on this line, to reset the external Chassis Intrusion Latch.
8	GND	System Ground.
9	V_{CC}	POWER (2.8 V to 5.5 V). Typically powered from 3.3 V power rail. Bypass with the parallel combination of 10 μF (electrolytic or tantalum) and 0.1 μF (ceramic) bypass capacitors.
10	$\overline{\text{INT}}$	Digital Output. Interrupt Request (open-drain). The output is enabled when Bit 1 of Register 40h is set to 1. The default state is disabled. It has an on-chip 100 kΩ pull-up resistor.
11	NTEST_IN/AOUT	Digital Input/Analog Output. An active-high input that enables NAND Test mode board-level connectivity testing. Refer to section on NAND testing. Also functions as a programmable analog output when NAND Test is not selected.
12	$\overline{\text{RESET}}$	Digital I/O. Master Reset, 5 mA driver (open drain), active low output with a 45 ms minimum pulsewidth. Set using Bit 4 in Register 40h. Also acts as reset input when pulled low (e.g., power-on reset). It has an on-chip 100 kΩ pull-up resistor.
13	D1–	Analog Input. Connected to cathode of first external temperature sensing diode.
14	D1+	Analog Input. Connected to anode of first external temperature sensing diode.
15	+12 V_{IN}	Programmable Analog Input. Monitors 12 V supply.
16	+5 V_{IN}	Analog Input. Monitors 5 V supply.
17	V_{CCP2}/D2–	Programmable Analog Input. Monitors second processor core voltage or cathode of second external temperature sensing diode.
18	+2.5 V_{IN}/D2+	Programmable Analog Input. Monitors 2.5 V supply or anode of second external temperature sensing diode.
19	$+V_{CCP1}$	Analog Input. Monitors 1st processor core voltage (0 V to 3.6 V).
20	VID4/IRQ4	Digital Input. Core Voltage ID readouts from the processor. This value is read into the VID4 Status Register. Can also be reconfigured as an interrupt input. It has an on-chip 100 kΩ pull-up resistor.
21	VID3/IRQ3	Digital Input. Core Voltage ID readouts from the processor. This value is read into the VID0–VID3 Status Register. Can also be reconfigured as an interrupt input. It has an on-chip 100 kΩ pull-up resistor.
22	VID2/IRQ2	Digital Input. Core Voltage ID readouts from the processor. This value is read into the VID0-VID3 Status Register. Can also be reconfigured as an interrupt input. It has an on-chip 100 kΩ pull-up resistor.
23	VID1/IRQ1	Digital Input. Core Voltage ID readouts from the processor. This value is read into the VID0–VID3 Status Register. Can also be reconfigured as an interrupt input. It has an on-chip 100 kΩ pull-up resistor.
24	VID0/IRQ0	Digital Input. Core Voltage ID readouts from the processor. This value is read into the VID0–VID3 Status Register. Can also be reconfigured as an interrupt input. It has an on-chip 100 kΩ pull-up resistor.

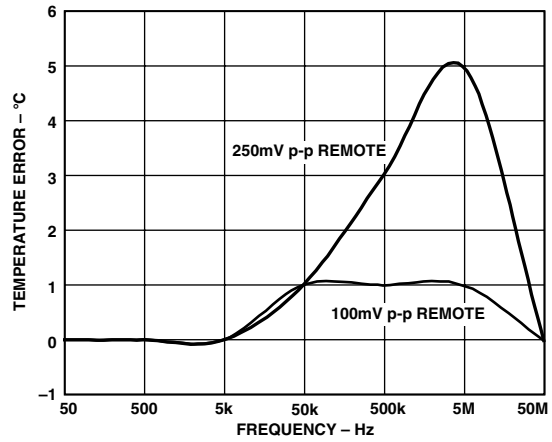
ADM1024–Typical Performance Characteristics



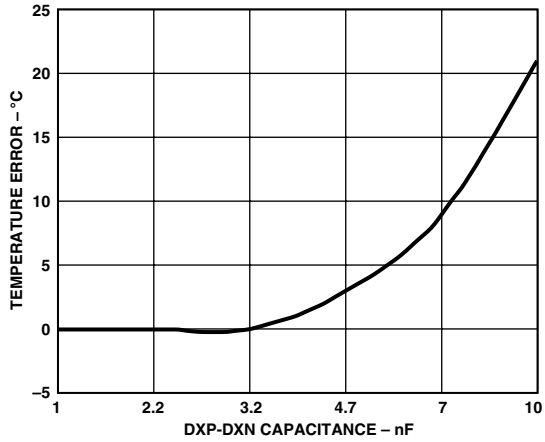
TPC 1. Temperature Error vs. PC Board Track Resistance



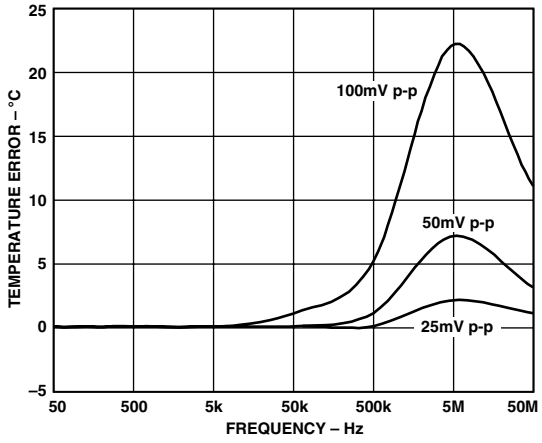
TPC 4. Pentium® III Temperature Measurement vs. ADM1024 Reading



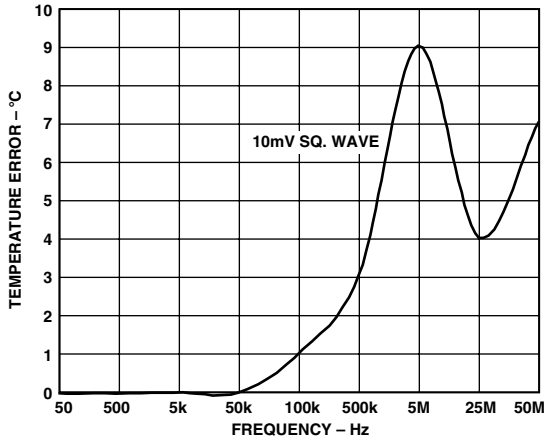
TPC 2. Temperature Error vs. Power Supply Noise Frequency



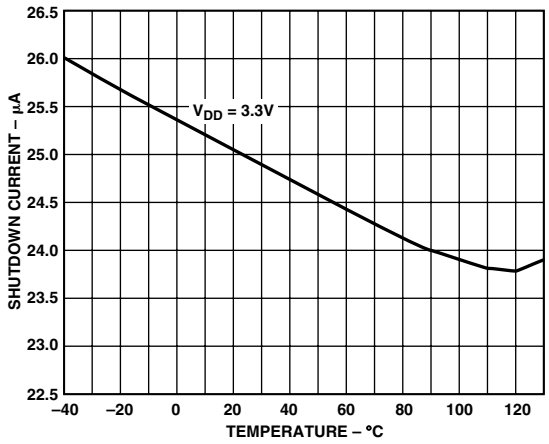
TPC 5. Temperature Error vs. Capacitance Between D+ and D–



TPC 3. Temperature Error vs. Common-Mode Noise Frequency



TPC 6. Temperature Error vs. Differential-Mode Noise Frequency



TPC 7. Standby Current vs. Temperature

(continued from page 1)

configured as inputs to monitor a 2.5 V supply and a second processor core voltage, or as a second temperature sensing input. The remaining two inputs can be programmed as general-purpose analog inputs or as digital fan-speed measuring inputs.

Measured values can be read out via an SMBus serial System Management Bus, and values for limit comparisons can be programmed in over the same serial bus. The high-speed successive-approximation ADC allows frequent sampling of all analog channels to ensure a fast interrupt response to any out-of-limit measurement.

The ADM1024's 2.8 V to 5.5 V supply voltage range, low supply current, and SMBus interface make it ideal for a wide range of applications. These include hardware monitoring and protection applications in personal computers, electronic test equipment, and office electronics.

GENERAL DESCRIPTION

The ADM1024 is a complete system hardware monitor for microprocessor-based systems. The device communicates with the system via a serial System Management Bus. The serial bus controller has a hardwired address line for device selection (Pin 1), a serial data line for reading and writing addresses and data (Pin 3), and an input line for the serial clock (Pin 4). All control and programming functions of the ADM1024 are performed over the serial bus.

MEASUREMENT INPUTS

Programmability of the measurement inputs makes the ADM1024 extremely flexible and versatile. The device has a 10-bit A-to-D converter, and nine measurement input pins that can be configured in different ways.

Pins 5 and 6 can be programmed as general-purpose analog inputs with a range of 0 V to 2.5 V, or as digital inputs to monitor the speed of fans with digital tachometer outputs. The fan inputs can be programmed to accommodate fans with different speeds and different numbers of pulses per revolution from their tach outputs.

Pins 13 and 14 are dedicated temperature inputs and may be connected to the cathode and anode of an external temperature-sensing diode.

Pins 15, 16, and 19 are dedicated analog inputs with on-chip attenuators, configured to monitor 12 V, 5 V and the processor core voltage, respectively.

Pins 17 and 18 may be configured as analog inputs with on-chip attenuators to monitor a second processor core voltage and a 2.5 V supply, or they may be configured as a temperature input and connected to a second temperature-sensing diode.

The ADC also accepts input from an on-chip bandgap temperature sensor that monitors system-ambient temperature.

Finally, the ADM1024 monitors the supply from which it is powered, so there is no need for a separate 3.3 V analog input, if the chip V_{CC} is 3.3 V. The range of this V_{CC} measurement can be configured for either a 3.3 V or 5 V V_{CC} by Bit 3 of the Channel Mode Register.

SEQUENTIAL MEASUREMENT

When the ADM1024 monitoring sequence is started, it cycles sequentially through the measurement of analog inputs and the temperature sensor, while at the same time the fan speed inputs are independently monitored. Measured values from these inputs are stored in Value Registers. These can be read out over the serial bus, or can be compared with programmed limits stored in the Limit Registers. The results of out-of-limit comparisons are stored in the Interrupt Status Registers, and will generate an interrupt on the $\overline{INT}$ line (Pin 10).

Any or all of the Interrupt Status Bits can be masked by appropriate programming of the Interrupt Mask Register.

PROCESSOR VOLTAGE ID

Five digital inputs (VID4 to VID0—Pins 20 to 24) read the processor voltage ID code. These inputs can also be reconfigured as interrupt inputs.

The VID pins have internal 100 kΩ pull-up resistors.

CHASSIS INTRUSION

A chassis intrusion input (Pin 7) is provided to detect unauthorized tampering with the equipment.

$\overline{RESET}$

A $\overline{RESET}$ input/output (Pin 12) is provided. Pulling this pin low will reset all ADM1024 internal registers to default values. The ADM1024 can also be programmed to give a low-going 45 ms reset pulse at this pin.

The $\overline{RESET}$ pin has an internal, 100 kΩ pull-up resistor.

ANALOG OUTPUT

The ADM1024 contains an on-chip, 8-bit digital-to-analog converter with an output range of zero to 2.5 V (Pin 11). This is typically used to implement a temperature-controlled fan by controlling the speed of a fan dependent upon the temperature measured by the on-chip temperature sensor.

Testing of board level connectivity is simplified by providing a NAND tree test function. The AOUT (Pin 11) also doubles as a NAND test input, while Pin 1 doubles as a NAND tree output.

INTERNAL REGISTERS OF THE ADM1024

A brief description of the ADM1024's principal internal registers is given below. More detailed information on the function of each register is given in Tables VI to XIX.

Configuration Registers: Provide control and configuration.

Channel Mode Register: Stores the data for the operating modes of the input channels.

Address Pointer Register: This register contains the address that selects one of the other internal registers. When writing to the ADM1024, the first byte of data is always a register address, which is written to the Address Pointer Register.

Interrupt ($\overline{\text{INT}}$) Status Registers: Two registers to provide status of each Interrupt event. These registers are also mirrored at addresses 4Ch and 4Dh.

Interrupt ($\overline{\text{INT}}$) Mask Registers: Allow masking of individual interrupt sources.

Temperature Configuration Register: The configuration of the temperature interrupt is controlled by the lower three bits of this register.

VID/Fan Divisor Register: The status of the VID0 to VID4 pins of the processor can be written to and read from these registers. Divisor values for fan-speed measurement are also stored in this register.

Value and Limit Registers: The results of analog voltage inputs, temperature and fan speed measurements are stored in these registers, along with their limit values.

Analog Output Register: The code controlling the analog output DAC is stored in this register.

Chassis Intrusion Clear Register: A signal latched on the chassis intrusion pin can be cleared by writing to this register.

SERIAL BUS INTERFACE

Control of the ADM1024 is carried out via the serial bus. The ADM1024 is connected to this bus as a slave device, under the control of a master device, e.g., ICH.

The ADM1024 has a 7-bit serial bus address. When the device is powered up, it will do so with a default serial bus address. The five MSBs of the address are set to 01011, the two LSBs are determined by the logical states of Pin 1 (NTESTOUT/ADD). This is a three-state input that can be grounded, connected to V_{CC} or left open-circuit to give three different addresses.

Table I. ADD Pin Truth Table

ADD Pin	A1	A0
GND	1	0
No Connect	0	0
V_{CC}	0	1

If ADD is left open-circuit the default address will be 0101100. ADD is sampled only at power-up, so any changes made while power is on will have no immediate effect.

The facility to make hardwired changes to A1 and A0 allows the user to avoid conflicts with other devices sharing the same serial bus, for example if more than one ADM1024 is used in a system.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high-to-low transition on the serial data line SDA while the serial clock line, SCL, remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/$\overline{\text{W}}$ bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device.

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{\text{W}}$ bit is a 0, the master will write to the slave device. If the R/$\overline{\text{W}}$ bit is a 1, the master will read from the slave device.
2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an Acknowledge Bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low-to-high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will override the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the tenth clock pulse, then high during the tenth clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the case of the ADM1024, write operations contain either one or two bytes, and read operations contain one byte and perform the following functions.

To write data to one of the device data registers or read data from it, the Address Pointer Register must be set so that the correct data register is addressed, then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the Address Pointer Register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register. This is illustrated in Figure 2a. The device address is sent over the bus followed by R/$\overline{\text{W}}$ set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the Address Pointer Register. The second data byte is the data to be written to the internal data register.

When reading data from a register there are two possibilities:

1. If the ADM1024's Address Pointer Register value is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the ADM1024 as before, but only the data byte containing the register address is sent, as data is not to be written to the register. This is shown in Figure 2b.

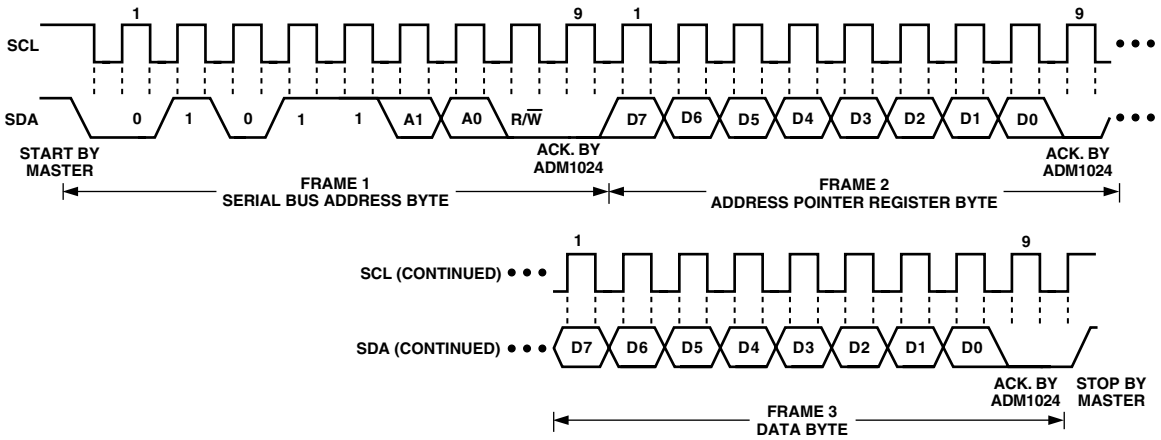


Figure 2a. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

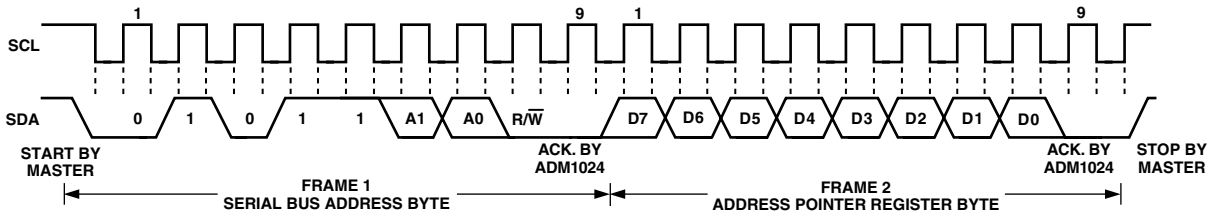


Figure 2b. Writing to the Address Pointer Register Only

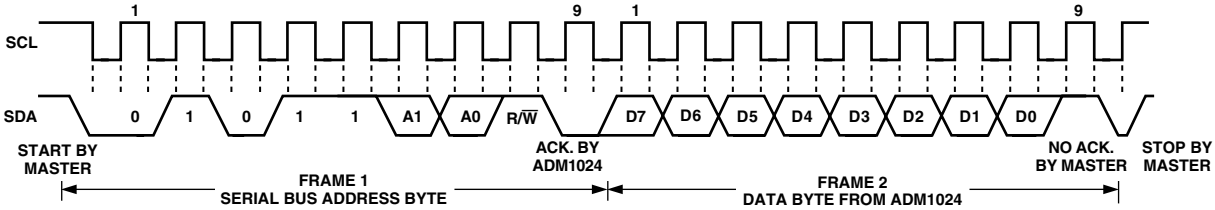


Figure 2c. Reading Data from a Previously Selected Register

A read operation is then performed consisting of the serial bus address, R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register. This is shown in Figure 2c.

2. If the Address Pointer Register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the Address Pointer Register, so Figure 2b can be omitted.

NOTES

1. Although it is possible to read a data byte from a data register without first writing to the Address Pointer Register, if the Address Pointer Register is already at the correct value, it is not possible to write data to a register without writing to the Address Pointer Register because the first data byte of a write is always written to the Address Pointer Register.
2. In Figures 2a to 2c, the serial bus address is shown as the default value 01011(A1)(A0), where A1 and A0 are set by the three-state ADD pin.

MEASUREMENT INPUTS

The ADM1024 has nine external measurement pins that can be configured to perform various functions by programming the Channel Mode Register.

Pins 13 and 14 are dedicated to temperature measurement, while Pins 15, 16, and 19 are dedicated analog input channels. Their function is unaffected by the Channel Mode Register.

Pins 5 and 6 can be individually programmed as analog inputs, or as digital fan speed measurement inputs, by programming Bits 0 and 1 of the Channel Mode Register.

Pins 17 and 18 can be configured as analog inputs or as inputs for external temperature-sensing diodes by programming Bit 2 of the Channel Mode Register.

Bit 3 of the Channel Mode Register configures the internal V_{CC} measurement range for either 3.3 V or 5 V.

Bits 4 to 6 of the Channel Mode Register enable or disable Pins 22 to 24, when they are configured as interrupt inputs by setting Bit 7 of the Channel Mode Register. This function is controlled for Pins 20 and 21 by Bits 6 and 7 of Configuration Register 2.

Bit 7 of the Channel Mode Register allows the processor core voltage ID bits (VID0 to VID4, Pins 24 to 20) to be reconfigured as interrupt inputs.

A truth table for the Channel Mode Register is given in Table II.

Table II. Channel Mode Register

Channel Mode Register Bit	Controls Pin(s)	Function
0	5	0 = FAN1, 1 = AIN1
1	6	0 = FAN2, 1 = AIN2
2	17, 18	0 = 2.5 V, V_{CCP2}, 1 = D2–, D2+
3	Int. V_{CC} Meas.	0 = 3.3 V, 1 = 5 V
4	24	0 = VID0, 1 = IRQ0
5	23	0 = VID1, 1 = IRQ1
6	22	0 = VID2, 1 = IRQ2
7	20–24	0 = VID0 to VID4, 1 = Interrupt Inputs

Power-on Default = 0000 0000

Table III. A/D Output Code vs. V_{IN}

Input Voltage							A/D Output	
+12 V_{IN}	+5 V_{IN}	V_{CC} (3.3 V)	V_{CC} (5 V)	+2.5 V_{IN}	+$V_{CCP1/2}$	AIN(1/2)	Decimal	Binary
<0.062	<0.026	<0.0172	<0.026	<0.013	<0.014	<0.010	0	00000000
0.062–0.125	0.026–0.052	0.017–0.034	0.026–0.052	0.013–0.026	0.014–0.028	0.010–0.019	1	00000001
0.125–0.188	0.052–0.078	0.034–0.052	0.052–0.078	0.026–0.039	0.028–0.042	0.019–0.029	2	00000010
0.188–0.250	0.078–0.104	0.052–0.069	0.078–0.104	0.039–0.052	0.042–0.056	0.029–0.039	3	00000011
0.250–0.313	0.104–0.130	0.069–0.086	0.104–0.130	0.052–0.065	0.056–0.070	0.039–0.049	4	00000100
0.313–0.375	0.130–0.156	0.086–0.103	0.130–0.156	0.065–0.078	0.070–0.084	0.049–0.058	5	00000101
0.375–0.438	0.156–0.182	0.103–0.120	0.156–0.182	0.078–0.091	0.084–0.098	0.058–0.068	6	00000110
0.438–0.500	0.182–0.208	0.120–0.138	0.182–0.208	0.091–0.104	0.098–0.112	0.068–0.078	7	00000111
0.500–0.563	0.208–0.234	0.138–0.155	0.208–0.234	0.104–0.117	0.112–0.126	0.078–0.087	8	00001000
4.000–4.063	1.666–1.692	1.100–1.117	1.666–1.692	• • • 0.833–0.846	0.900–0.914	0.625–0.635	64 (1/4-Scale)	01000000
8.000–8.063	3.330–3.560	2.200–2.217	3.330–3.560	• • • 1.667–1.680	1.800–1.814	1.250–1.260	128 (1/2-Scale)	10000000
12.000–12.063	5.000–5.026	3.300–3.317	5.000–5.026	• • • 2.500–2.513	2.700–2.714	1.875–1.885	192 (3/4-Scale)	11000000
15.312–15.375	6.380–6.406	4.210–4.230	6.380–6.406	• • • 3.190–3.203	3.445–3.459	2.392–2.402	245	11110101
15.375–15.437	6.406–6.432	4.230–4.245	6.406–6.432	3.203–3.216	3.459–3.473	2.402–2.412	246	11110110
15.437–15.500	6.432–6.458	4.245–4.263	6.432–6.458	3.216–3.229	3.473–3.487	2.412–2.422	247	11110111
15.500–15.563	6.458–6.484	4.263–4.280	6.458–6.484	3.229–3.242	3.487–3.501	2.422–2.431	248	11111000
15.563–15.625	6.484–6.510	4.280–4.300	6.484–6.510	3.242–3.255	3.501–3.515	2.431–2.441	249	11111001
15.625–15.688	6.510–6.536	4.300–4.314	6.510–6.536	3.255–3.268	3.515–3.529	2.441–2.451	250	11111010
15.688–15.750	6.536–6.562	4.314–4.331	6.536–6.562	3.268–3.281	3.529–3.543	2.451–2.460	251	11111011
15.750–15.812	6.562–6.588	4.331–4.348	6.562–6.588	3.281–3.294	3.543–3.558	2.460–2.470	252	11111100
15.812–15.875	6.588–6.615	4.348–4.366	6.588–6.615	3.294–3.307	3.558–3.572	2.470–2.480	253	11111101
15.875–15.938	6.615–6.640	4.366–4.383	6.615–6.640	3.307–3.320	3.572–3.586	2.480–2.490	254	11111110
>15.938	>6.640	>4.383	>6.640	>3.320	>3.586	>2.490	255	11111111

A-TO-D CONVERTER

These inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. This has a resolution of eight bits. The basic input range is zero to 2.5 V, which is the input range of AIN1 and AIN2, but five of the inputs have built-in attenuators to allow measurement of 2.5 V, 5 V, 12 V and the processor core voltages V_{CCP1} and V_{CCP2}, without any external components. To allow for the tolerance of these supply voltages, the A-to-D converter produces an output of 3/4 full-scale (decimal 192) for the nominal input voltage, and so has adequate headroom to cope with overvoltages. Table III shows the input ranges of the analog inputs and output codes of the A-to-D converter.

When the ADC is running, it samples and converts an input every 748 μs, except for the external temperature (D1 and D2) inputs. These have special input signal conditioning and are averaged over 16 conversions to reduce noise, and a measurement on one of these inputs takes nominally 9.6 ms.

INPUT CIRCUITS

The internal structure for the analog inputs are shown in Figure 3. Each input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first-order low-pass filter which gives the input immunity to high frequency noise.

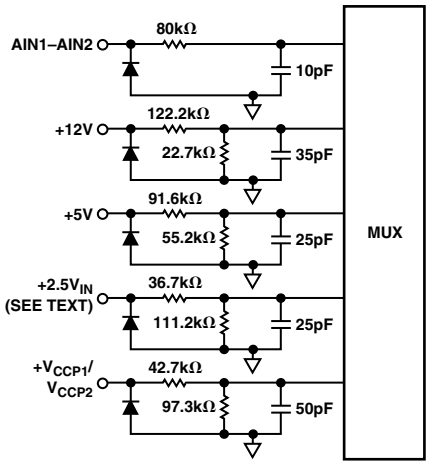


Figure 3. Structure of Analog Inputs

2.5 V INPUT PRECAUTIONS

When using the 2.5 V input, the following precautions should be noted. There is a parasitic diode between Pin 18 and V_{CC} due to the presence of a PMOS current source (which is used when Pin 18 is configured as a temperature input). This will become forward-biased if Pin 18 is more than 0.3 V above V_{CC}. Therefore, V_{CC} should never be powered off with a 2.5 V input connected.

SETTING OTHER INPUT RANGES

AIN1 and AIN2 can easily be scaled to voltages other than 2.5 V. If the input voltage range is zero to some positive voltage, all that is required is an input attenuator, as shown in Figure 4.

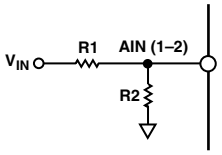


Figure 4. Scaling AIN(1–2)

$$\frac{R1}{R2} = \frac{(V_{FS} - 2.5)}{2.5}$$

Negative and bipolar input ranges can be accommodated by using a positive reference voltage to offset the input voltage range so it is always positive.

To measure a negative input voltage, an attenuator can be used as shown in Figure 5.

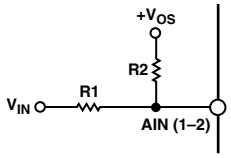


Figure 5. Scaling and Offsetting AIN(1–2) for Negative Inputs

$$\frac{R1}{R2} = \frac{|V_{FS-}|}{V_{OS}}$$

This is a simple and cheap solution, but the following point should be noted. Since the input signal is offset but not inverted, the input range is transposed. An increase in the magnitude of the –12 V supply (going more negative), will cause the input voltage to fall and give a lower output code from the ADC. Conversely, a decrease in the magnitude of the –12 V supply will cause the ADC code to increase. The maximum negative voltage corresponds to zero output from the ADC. This means that the upper and lower limits will be transposed.

Bipolar input ranges can easily be accommodated. By making R1 equal to R2 and V_{OS} = 2.5 V, the input range is ±2.5 V. Other input ranges can be accommodated by adding a third resistor to set the positive full-scale input voltage.

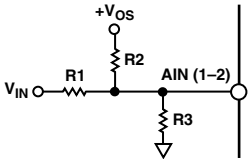


Figure 6. Scaling and Offsetting AIN(1–2) for Bipolar Inputs

$$\frac{R1}{R2} = \frac{|V_{FS-}|}{R2}$$

(R3 has no effect as the input voltage at the device Pin is zero when V_{IN} = minus full-scale.)

$$\frac{R1}{R3} = \frac{(V_{FS+} - 2.5)}{2.5}$$

(R2 has no effect as the input voltage at the device pin is 2.5 V when V_{IN} = plus full-scale).

Offset voltages other than 2.5 V can be used, but the calculation becomes more complicated.

TEMPERATURE MEASUREMENT SYSTEM

Internal Temperature Measurement

The ADM1024 contains an on-chip bandgap temperature sensor, whose output is digitized by the on-chip ADC. The temperature data is stored in the Temperature Value Register (address 27h) and the LSB from Bits 6 and 7 of the Temperature Configuration

Register (address 4Bh). As both positive and negative temperatures can be measured, the temperature data is stored in two's complement format, as shown in Table IV. Theoretically, the temperature sensor and ADC can measure temperatures from –128°C to +127°C with a resolution of 1°C, although temperatures below –40°C and above +125°C are outside the operating temperature range of the device.

External Temperature Measurement

The ADM1024 can measure the temperature of two external diode sensors or diode-connected transistors, connected to Pins 13 and 14 or 17 and 18.

Pins 13 and 14 are a dedicated temperature input channel. Pins 17 and 18 can be configured to measure a diode sensor by setting Bit 2 of the Channel Mode Register to 1.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about –2 mV/°C. Unfortunately, the absolute value of V_{BE}, varies from device to device, and individual calibration is required to null this out, so the technique is unsuitable for mass-production.

The technique used in the ADM1024 is to measure the change in V_{BE} when the device is operated at two different currents.

This is given by:

$$\Delta V_{BE} = KT/q \times ln(N)$$

where:

K is Boltzmann's constant
q is charge on the carrier
T is absolute temperature in Kelvins
N is ratio of the two currents.

Figure 7 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors, but it could equally well be a discrete transistor.

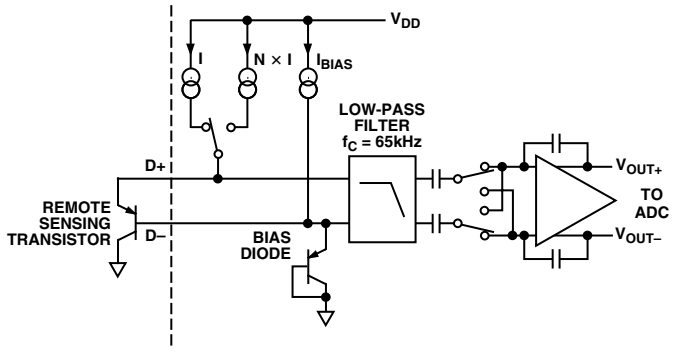


Figure 7. Signal Conditioning for External Diode Temperature Sensors

If a discrete transistor is used, the collector will not be grounded, and should be linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base to the D+ input.

To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D– input. As the sensor is operating in a noisy environment, C1 is provided as a noise filter. See the section on layout considerations for more information on C1.

To measure ΔV_{BE}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a 65 kHz low-pass filter to remove noise, thence to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 8-bit two's complement format. To further reduce the effects of noise. Digital filtering is performed by averaging the results of 16 measurement cycles. An external temperature measurement takes nominally 9.6 ms.

The results of external temperature measurements are stored in 8-bit, two's-complement format, as illustrated in Table IV.

Table IV. Temperature Data Format

Temperature	Digital Output
–128°C	1000 0000
–125°C	1000 0011
–100°C	1001 1100
–75°C	1011 0101
–50°C	1100 1110
–25°C	1110 0111
0°C	0000 0000
+0.5°C	0000 0000
+10°C	0000 1010
+25°C	0001 1001
+50°C	0011 0010
+75°C	0100 1011
+100°C	0110 0100
+125°C	0111 1101
+127°C	0111 1111

LAYOUT CONSIDERATIONS

Digital boards can be electrically noisy environments, and care must be taken to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. The following precautions should be taken:

1. Place the ADM1024 as close as possible to the remote sensing diode. Provided that the worst noise sources such as clock generators, data/address buses and CRTs are avoided, this distance can be 4 to 8 inches.
2. Route the D+ and D– tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
3. Use wide tracks to minimize inductance and reduce noise pickup. Ten mil track minimum width and spacing is recommended.

Figure 8. Arrangement of Signal Tracks

4. Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D– path and at the same temperature.

   Thermocouple effects should not be a major problem as 1°C corresponds to about 240 μV, and thermocouple voltages are about 3 μV/°C of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200 mV.

5. Place 0.1 μF bypass and 2200 pF input filter capacitors close to the ADM1024.

6. If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. This will work up to about 6 feet to 12 feet.

7. For really long distances (up to 100 feet) use shielded twisted pair such as Belden #8451 microphone cable. Connect the twisted pair to D+ and D– and the shield to GND close to the ADM1024. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor may be reduced or removed.

Cable resistance can also introduce errors. One Ω series resistance introduces about 0.5°C error.

LIMIT VALUES

Limit values for analog measurements are stored in the appropriate limit registers. In the case of voltage measurements, high and low limits can be stored so that an interrupt request will be generated if the measured value goes above or below acceptable values. In the case of temperature, a Hot Temperature or High Limit can be programmed, and a Hot Temperature Hysteresis or Low Limit, which will usually be some degrees lower. This can be useful as it allows the system to be shut down when the hot limit is exceeded, and restarted automatically when it has cooled down to a safe temperature.

MONITORING CYCLE TIME

The monitoring cycle begins when a one is written to the Start Bit (Bit 0), and a zero to the $\overline{\text{INT}}$_Clear Bit (Bit 3) of the Configuration Register. $\overline{\text{INT}}$_Enable (Bit 1) should be set to one to enable the $\overline{\text{INT}}$ output. The ADC measures each analog input in turn, as each measurement is completed the result is automatically stored in the appropriate value register. This "round-robin" monitoring cycle continues until it is disabled by writing a 0 to Bit 0 of the Configuration Register.

As the ADC will normally be left to free-run in this manner, the time taken to monitor all the analog inputs will normally not be of interest, as the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it can be calculated as follows:

$$m \times t_1 \times n \times t_2$$

where:

m is the number of inputs configured as analog inputs, plus the internal V_{CC} measurement and internal temperature sensor.

t_1 is the time taken for an analog input conversion, nominally 755 μs.

n is the number of inputs configured as external temperature inputs.

t_2 is the time taken for a temperature conversion, nominally 33.24 ms.

This rapid sampling of the analog inputs ensures a quick response in the event of any input going out of limits, unlike other monitoring chips that employ slower ADCs.

FAN MONITORING CYCLE TIME

When a monitoring cycle is started, monitoring of the fan speed inputs begins at the same time as monitoring of the analog inputs. However, the two monitoring cycles are not synchronized in any way. The monitoring cycle time for the fan inputs is dependent on fan speed and is much slower than for the analog inputs. For more details see Fan Speed Measurement section.

INPUT SAFETY

Scaling of the analog inputs is performed on chip, so external attenuators are normally not required. However, since the power supply voltages will appear directly at the pins, its is advisable to add small external resistors in series with the supply traces to the chip to prevent damaging the traces or power supplies should a accidental short such as a probe connect two power supplies together.

As the resistors will form part of the input attenuators, they will affect the accuracy of the analog measurement if their value is too high. The analog input channels are calibrated assuming an external series resistor of 500 Ω, and the accuracy will remain within specification for any value from zero to 1 kΩ, so a standard 510 Ω resistor is suitable.

The worst such accident would be connecting –12 V to +12 V—a total of 24 V difference, with the series resistors this would draw a maximum current of approximately 24 mA.

ANALOG OUTPUT

The ADM1024 has a single analog output from a unsigned 8-bit DAC which produces 0 V–2.5 V. The analog output register defaults to FF during power-on reset, which produces maximum fan speed. The analog output may be amplified and buffered with external circuitry such as an op amp and transistor to provide fan speed control.

Suitable fan drive circuits are given in Figures 9a to 9f. When using any of these circuits, the following points should be noted:

1. All of these circuits will provide an output range from zero to almost 12 V, apart from Figure 10a which loses the base-emitter voltage drop of Q1 due to the emitter-follower configuration.
2. To amplify the 2.5 V range of the analog output up to 12 V, the gain of these circuits needs to be around 4.8.
3. Care must be taken when choosing the op amp to ensure that its input common-mode range and output voltage swing are suitable.
4. The op amp may be powered from the 12 V rail alone or from ±12 V. If it is powered from 12 V then the input common-mode range should include ground to accommodate the minimum output voltage of the DAC, and the output voltage should swing below 0.6 V to ensure that the transistor can be turned fully off.
5. If the op amp is powered from –12 V, precautions such as a clamp diode to ground may be needed to prevent the base-emitter junction of the output transistor being reverse-biased in the unlikely event that the output of the op amp should swing negative for any reason.

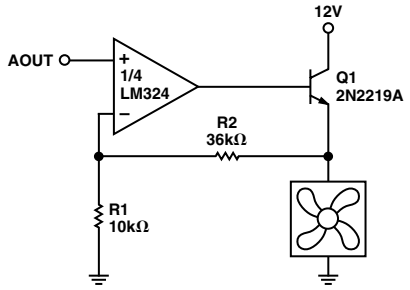


Figure 9a. Fan Drive Circuit with Op Amp and Emitter—Follower

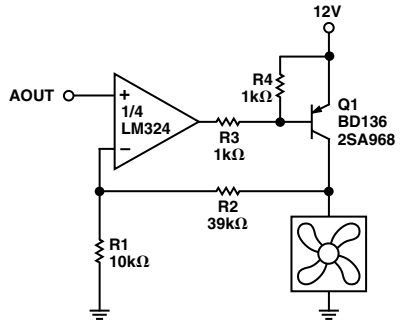


Figure 9b. Fan Drive Circuit with Op Amp and PNP Transistor

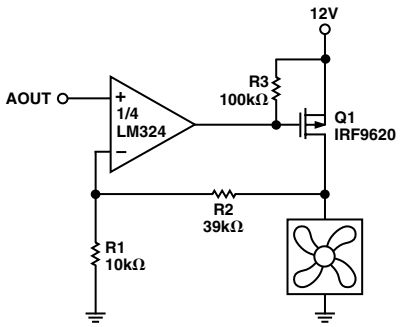


Figure 9c. Fan Driver Circuit with Op Amp and P-Channel MOSFET

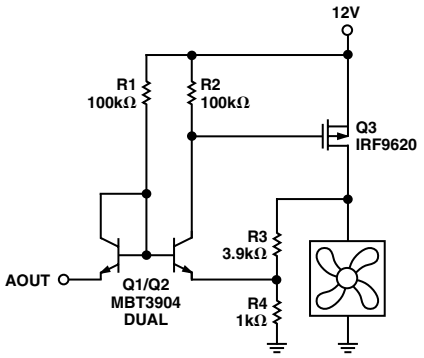


Figure 9d. Discrete Fan Drive Circuit with P-Channel MOSFET, Single Supply

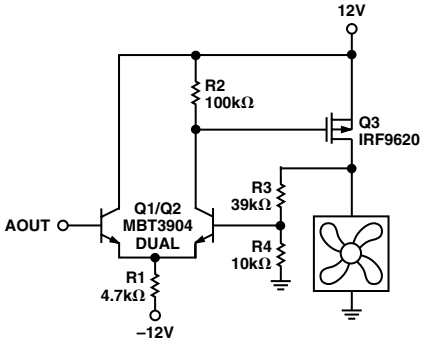


Figure 9e. Discrete Fan Drive Circuit with P-Channel MOSFET, Dual Supply

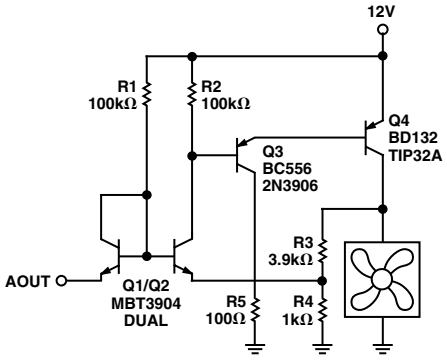


Figure 9f. Discrete Fan Drive Circuit with Bipolar Output Dual Supply

6. In all these circuits, the output transistor must have an I_{CMAX} greater than the maximum fan current, and be capable of dissipating power due to the voltage dropped across it when the fan is not operating at full speed.
7. If the fan motor produces a large back e.m.f when switched off, it may be necessary to add clamp diodes to protect the output transistors in the event that the output goes very quickly from full scale to zero.

FAULT-TOLERANT FAN CONTROL

The ADM1024 incorporates a fault-tolerant fan control capability that can override the setting of the analog output and force it to maximum to give full fan speed in the event of a critical over-temperature problem even if, for some reason, this has not been handled by the system software.

There are four temperature set points that will force the analog output to FFh if any one of them is exceeded for three or more consecutive measurements. Two of these limits are programmable by the user and two are hardware limits intended as *must not exceed* limits that cannot be changed.

The analog output will be forced to FFh if:

The temperature measured by the on-chip sensor exceeds the limit programmed into register address 13h.

or

The temperature measured by either of the remote sensors exceeds the limit programmed into address 14h.

or

The temperature measured by the on-chip sensor exceeds 70°C, which is hardware programmed into a read-only register at address 17h.

or

The temperature measured by either of the remote sensors exceeds 85°C, which is hardware programmed into a read-only register at address 18h.

Once the hardware override of the analog output is triggered, it will only return to normal operation after three consecutive measurements that are 5 degrees lower than each of the above limits.

The analog output can also be forced to FFh by pulling the $\overline{\text{THERM}}$ pin (Pin 2) low.

The limits in registers 13h and 14h can be programmed by the user. Obviously these limits should not exceed the hardware values in registers 17h and 18h, as they would have no effect. The power-on default values of these registers are the same as the two hardware registers, 70°C and 85°C respectively, so there is no need to program them if these limits are acceptable.

Once these registers have been programmed, or if the defaults are acceptable, the values in these registers can be locked by writing a 1 to Bits 1 and 2 of Configuration Register 2 (address 4Ah). This prevents any unauthorized tampering with the limits. These lock bits can only be written to 1 and can only be cleared by power-on reset or by taking the $\overline{\text{RESET}}$ pin low, so registers 13h and 14h cannot be written to again unless the device is powered off, then on.

LAYOUT AND GROUNDING

Analog inputs will provide best accuracy when referred to a clean ground. A separate, low-impedance ground plane for analog ground, which provides a ground point for the voltage dividers and analog components, will provide best performance but is not mandatory.

The power supply bypass, the parallel combination of 10 μF (electrolytic or tantalum) and 0.1 μF (ceramic) bypass capacitors connected between Pin 9 and ground, should also be located as close as possible to the ADM1024.

FAN INPUTS

Pins 5 and 6 may be configured as analog inputs or fan speed inputs by programming Bits 0 and 1 of the Channel Mode Register. The power-on default for these bits is all zeroes, which makes Pins 5 and 6 fan inputs.

Signal conditioning in the ADM1024 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 to V_{CC}. In the event that these inputs are supplied from fan outputs that exceed 0 V to 6.5 V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figures 10a to 10d show circuits for most common fan tach outputs.

If the fan tach output has a resistive pull-up to V_{CC} it can be directly connected to the fan input, as shown in Figure 10a.

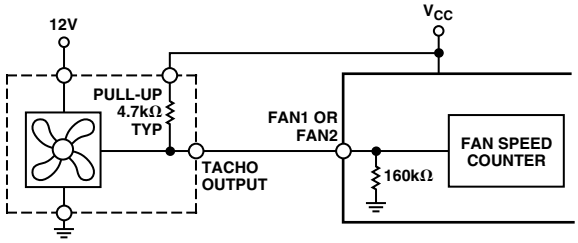


Figure 10a. Fan with Tach. Pull-Up to +V_{CC}

If the fan output has a resistive pull-up to 12 V (or other voltage greater than 6.5 V), the fan output can be clamped with a Zener diode, as shown in Figure 10b. The Zener voltage should be chosen so it is greater than V_{IH} but less than 6.5 V, allowing for the voltage tolerance of the Zener. A value of between 3 V and 5 V is suitable.

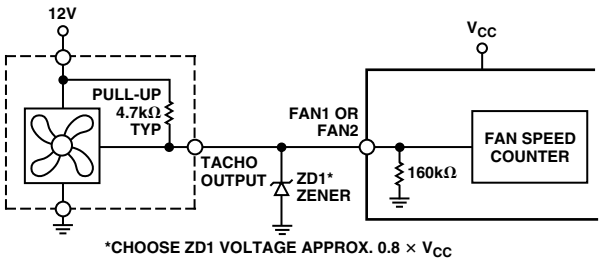


Figure 10b. Fan with Tach. Pull-Up to Voltage >6.5 V (e.g., 12 V) Clamped with Zener Diode

If the fan has a strong pull-up (less than 1 kΩ) to 12 V, or a totem-pole output, then a series resistor can be added to limit the Zener current, as shown in Figure 10c. Alternatively, a resistive attenuator may be used, as shown in Figure 10d.

R1 and R2 should be chosen such that:

$$2\ V < V_{PULL\text{-}UP} \times R2/(R_{PULL\text{-}UP} + R1 + R2) < 5\ V$$

The fan inputs have an input resistance of nominally 160 kΩ to ground, so this should be taken into account when calculating resistor values.

With a pull-up voltage of 12 V and pull-up resistor less than 1 kΩ, suitable values for R1 and R2 would be 100 kΩ and 47 kΩ. This will give a high-input voltage of 3.83 V.

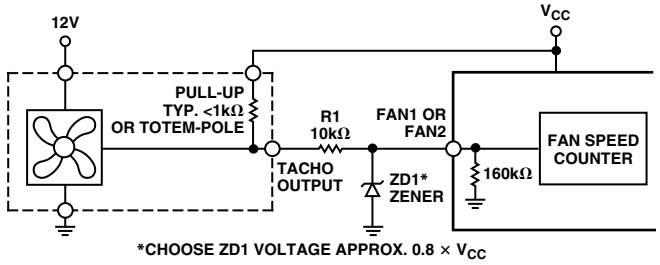


Figure 10c. Fan with Strong Tach. Pull-Up to >V_{CC} or Totem-Pole Output, Clamped with Zener and Resistor

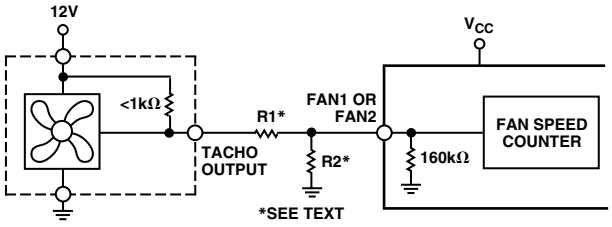


Figure 10d. Fan with Strong Tach. Pull-Up to >V_{CC} or Totem-Pole Output, Attenuated with R1/R2

FAN SPEED MEASUREMENT

The fan counter does not count the fan tach output pulses directly, because the fan speed may be less than 1000 rpm and it would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on-chip 22.5 kHz oscillator into the input of an 8-bit counter for two periods of the fan tach output, as shown in Figure 11; the accumulated count is actually proportional to the fan tach period and inversely proportional to the fan speed.

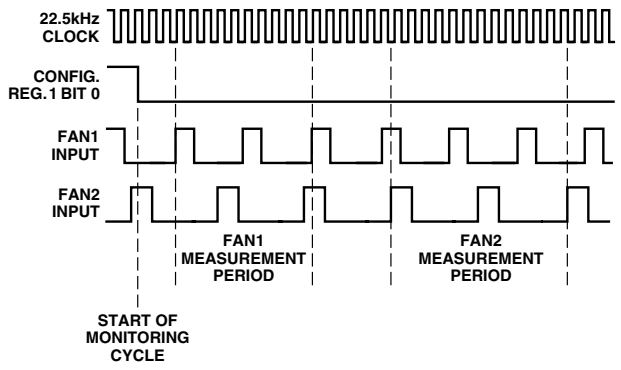


Figure 11. Fan Speed Measurement

The monitoring cycle begins when a one is written to the Start Bit (Bit 0), and a zero to the $\overline{\text{INT}}$_Clear Bit (Bit 3) of the Configuration Register. $\overline{\text{INT}}$_Enable (Bit 1) should be set to one to enable the $\overline{\text{INT}}$ output. The measurement begins on the rising edge of a fan tach pulse, and ends on the next-but-one rising edge. The fans are monitored sequentially, so if only one fan is monitored the monitoring time is the time taken after the Start Bit for it to produce two complete tach cycles or for the counter to reach full scale, whichever occurs sooner. If more than one fan is monitored, the monitoring time depends on the speed of the fans and the timing relationship of their tach pulses. This is illustrated in Figure 12. Once the fan speeds have been measured, they will be stored in the Fan Speed Value Registers and the most recent value can be read at any time. The measurements will be updated as long as the monitoring cycle continues.

To accommodate fans of different speed and/or different numbers of output pulses per revolution, a prescaler (divisor) of 1, 2, 4, or 8 may be added before the counter. The default value is 2, which gives a count of 153 for a fan running at 4400 rpm producing two output pulses per revolution.

The count is calculated by the equation:

$$Count = (22.5 \times 10^3 \times 60)\ /(rpm \times Divisor)$$

For constant speed fans, fan failure is normally considered to have occurred when the speed drops below 70% of nominal, which would correspond to a count of 219. Full scale (255) would be reached if the fan speed fell to 60% of its nominal value. For temperature-controlled variable speed fans the situation will be different.

Table V shows the relationship between fan speed and time per revolution at 60%, 70%, and 100% of nominal rpm for fan speeds of 1100, 2200, 4400, and 8800 rpm, and the divisor that would be used for each of these fans, based on two tach pulses per revolution.

Table V. Fan Speeds and Divisors

Divisor	Nominal rpm	Time per Rev (ms)	70% rpm	Time per Rev (70%) (ms)	60% rpm	Time per Rev (60%) (ms)
÷1	8800	6.82	6160	9.74	5280	11.36
÷2	4400	13.64	3080	19.48	2640	22.73
÷4	2200	27.27	1540	38.96	1320	45.44
÷8	1100	54.54	770	77.92	660	90.90

FAN1 and FAN2 Divisors are programmed into Bits 4 to 7 of the VID 0–3/Fan Divisor Register.

LIMIT VALUES

Fans in general will not overspeed if run from the correct voltage, so the failure condition of interest is underspeed due to electrical or mechanical failure. For this reason only, low-speed limits are programmed into the limit registers for the fans. It should be noted that, since fan period rather than speed is being measured, a fan failure interrupt will occur when the measurement *exceeds* the limit value.

MONITORING CYCLE TIME

The monitoring cycle time depends on the fan speed and number of tach output pulses per revolution. Two complete periods of the fan tach output (three rising edges) are required for each fan

measurement. Therefore, if the start of a fan measurement just misses a rising edge, the measurement can take almost three tach periods. In order to read a valid result from the fan value registers, the total monitoring time allowed after starting the monitoring cycle should, therefore, be three tach periods of FAN1 plus three tach periods of FAN2 at the lowest normal fan speed.

Although the fan monitoring cycle and the analog input monitoring cycle are started together, they are not synchronized in any other way.

FAN MANUFACTURERS

Manufacturers of cooling fans with tachometer outputs are listed below:

NMB Tech
9730 Independence Ave.
Chatsworth, California 91311
Phone: 818-341-3355; Fax: 818-341-8207

Model	Frame Size	Airflow CFM
2408NL	2.36 in sq. × 0.79 in (60 mm sq. × 20 mm)	9–16
2410ML	2.36 in sq. × 0.98 in (60 mm sq. × 25 mm)	14–25
3108NL	3.15 in sq. × 0.79 in (80 mm sq. × 20 mm)	25–42
3110KL	3.15 in sq. × 0.98 in (80 mm sq. × 25 mm)	25–40

Mechatronics Inc.
P.O. Box 613
Preston, WA 98050
800-453-4569
Models—Various sizes available with tach output option.

Sanyo Denki, America, Inc.
468 Amapola Avenue
Torrance, CA 90501
310-783-5400
Models—109P Series

CHASSIS INTRUSION INPUT

The Chassis Intrusion input is an active high input/open-drain output intended for detection and signalling of unauthorized tampering with the system. An external circuit powered from the system's CMOS backup battery is used to detect and latch a chassis intrusion event, whether or not the system is powered up. Once a chassis intrusion has been detected and latched, the CI input will generate an interrupt when the system is powered up.

The actual detection of chassis intrusion is performed by an external circuit that will, for example, detect when the cover has been removed. A wide variety of techniques may be used for the detection, for example:

- Microswitch that opens or closes when the cover is removed.
- Reed switch operated by magnet fixed to the cover.
- Hall-effect switch operated by magnet fixed to the cover.
- Phototransistor that detects light when cover is removed.

The chassis intrusion interrupt will remain asserted until the external detection circuit is reset. This can be achieved by setting Bit 7 of the Chassis Intrusion Clear Register to one, which will cause the CI pin to be pulled low for at least 20 ms. This register bit is self-clearing.

The chassis intrusion circuit should be designed so that it can be reset by pulling its output low. A suitable chassis intrusion circuit using a phototransistor is shown in Figure 12. Light falling on the phototransistor when the PC cover is removed will cause it to turn on and pull up the input of N1, thus setting the latch N3/N4. After the cover is replaced, a low reset on the CI output will pull down the input of N4, resetting the latch.

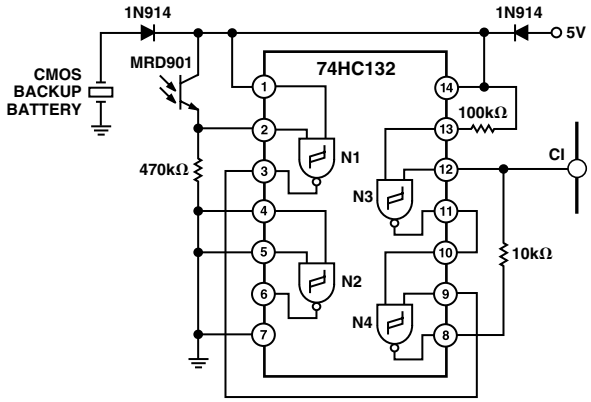


Figure 12. Chassis Intrusion Detector and Latch

The Chassis Intrusion input can also be used for other types of alarm input. Figure 13 shows a temperature alarm circuit using an AD22105 temperature switch sensor. This produces a low-going output when the preset temperature is exceeded, so the output is inverted by Q1 to make it compatible with the CI input. Q1 can by almost any small-signal NPN transistor, or a TTL or CMOS inverter gate may be used if one is available. See the AD22105 data sheet for information on selecting R_{SET}.

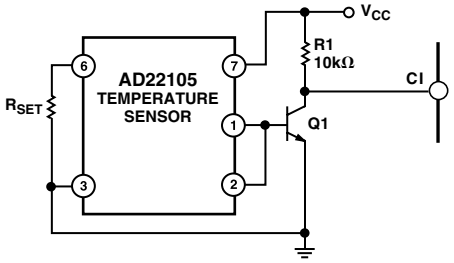


Figure 13. Using the CI Input with a Temperature Sensor

Note: The chassis intrusion input does not have a protective clamp diode to V_{CC}, as this could pull down the chassis intrusion latch and reset it when the ADM1024 was powered down.

THE ADM1024 INTERRUPT STRUCTURE

The Interrupt Structure of the ADM1024 is shown in Figure 14. As each measurement value is obtained and stored in the appropriate value register, the value and the limits from the corresponding limit registers are fed to the high and low limit comparators. The result of each comparison (1 = out of limit, 0 = in limit) is routed to the corresponding bit input of the Interrupt Status Registers via a data demultiplexer, and used to set that bit high or low as appropriate.

The Interrupt Mask Registers have bits corresponding to each of the Interrupt Status Register Bits. Setting an Interrupt Mask Bit high forces the corresponding Status Bit output low, while setting an Interrupt Mask Bit low allows the corresponding Status Bit

to be asserted. After masking, the status bits are all OR'd together to produce the $\overline{INT}$ output, which will pull low if any unmasked status bit goes high, i.e., when any measured value goes out of limit. The ADM1024 also has a dedicated output for temperature interrupts only, the $\overline{THERM}$ input/output Pin 2. The function of this is described later.

The $\overline{INT}$ output is enabled when Bit 1 of Configuration Register 1 ($\overline{INT}$_Enable) is high, and Bit 3 ($\overline{INT}$_Clear) is low.

The $\overline{INT}$ pin has an internal, 100 kΩ pull-up resistor.

VID/IRQ INPUTS

The processor voltage ID inputs VID0 to VID4 can be reconfigured as interrupt inputs by setting Bit 7 of the Channel Mode Register (address 16h). In this mode they operate as level-triggered interrupt inputs, with VID0/IRQ0 to VID2/IRQ2 being active low and VID2/IRQ2 and VID4/IRQ4 being active high. The individual interrupt inputs can be enabled or masked by setting or clearing Bits 4 to 6 of the Channel Mode Register and Bits 6 and 7 of Configuration Register 2 (address 4Ah). These interrupt inputs are not latched in the ADM1024, so they do not require clearing as do bits in the Status Registers. However, the external interrupt source should be cleared once the interrupt has been serviced, or the interrupt request will be reasserted.

INTERRUPT CLEARING

Reading an Interrupt Status Register will output the contents of the Register, then clear it. It will remain cleared until the monitoring cycle updates it, so the next read operation should not be performed on the register until this has happened, or the result will be invalid. The time taken for a complete monitoring cycle is mainly dependent on the time taken to measure the fan speeds, as described earlier.

The $\overline{INT}$ output is cleared with the $\overline{INT}$_Clear bit, which is Bit 3 of the Configuration Register, without affecting the contents of the Interrupt ($\overline{INT}$) Status Registers.

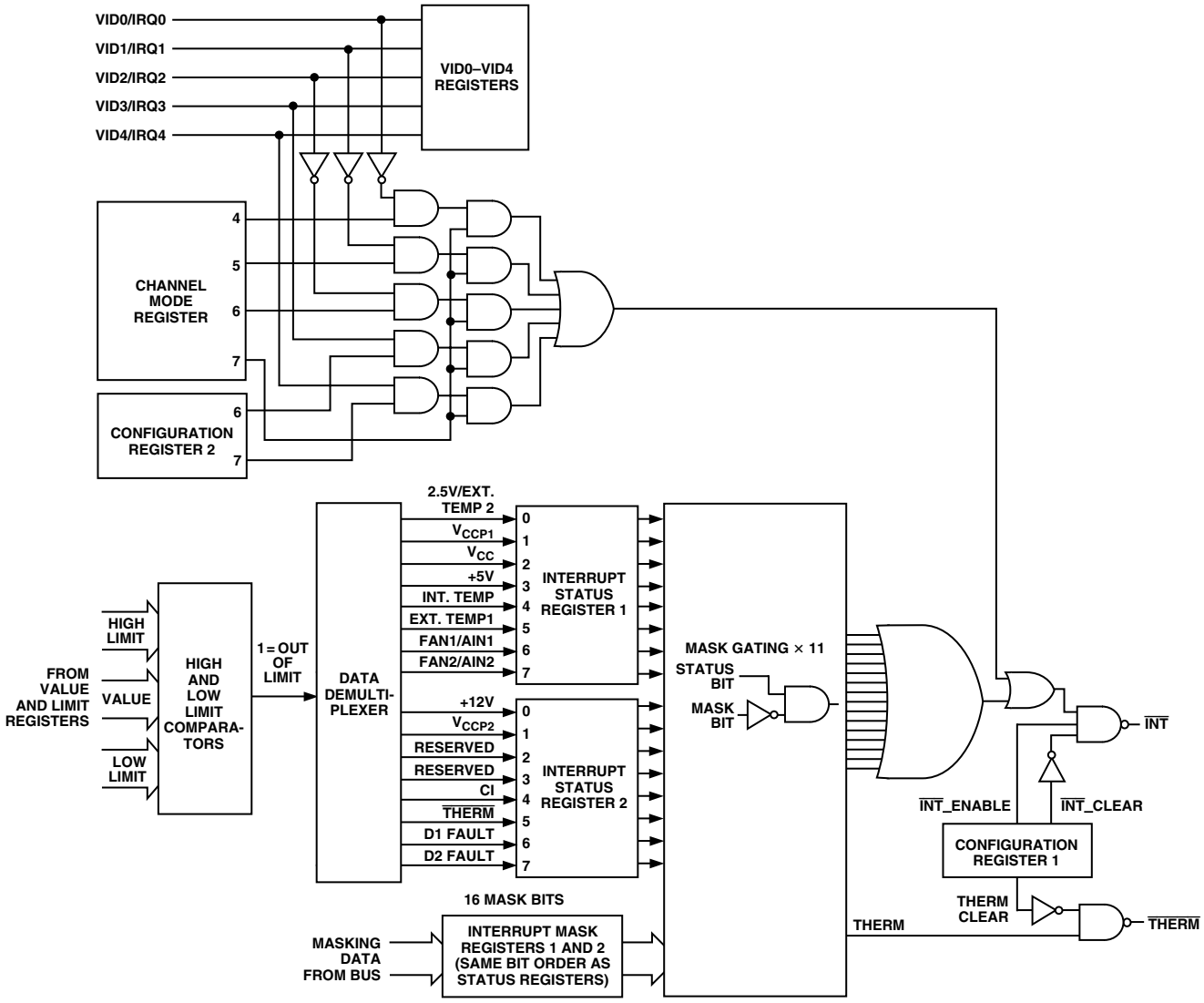


Figure 14. Interrupt Register Structure

INTERRUPT STATUS MIRROR REGISTERS

Whenever a bit in one of the Interrupt Status Registers is updated, the same bit is written to duplicate registers at addresses 4Ch and 42h. These registers allow a second management system to access the status data without worrying about clearing the data. The data in these registers is for reading only and has no effect on the interrupt output.

TEMPERATURE INTERRUPT MODES

The ADM1024 has two distinct methods of producing interrupts for out-of-limit temperature measurements from the internal or external sensors. Temperature errors can generate an interrupt on the $\overline{INT}$ pin along with other interrupts, but there is also a separate $\overline{THERM}$ pin that generates an interrupt only for temperature errors.

Operation of the $\overline{INT}$ output for temperature interrupts is illustrated in Figure 15. Assuming that the temperature starts off within the programmed limits and that temperature interrupt sources are not masked, $\overline{INT}$ will go low if the temperature measured by any of the internal or external sensors exceeds the programmed high temperature limit for that sensor, or the hardware limits in register 13h, 14h, 17h, or 18h.

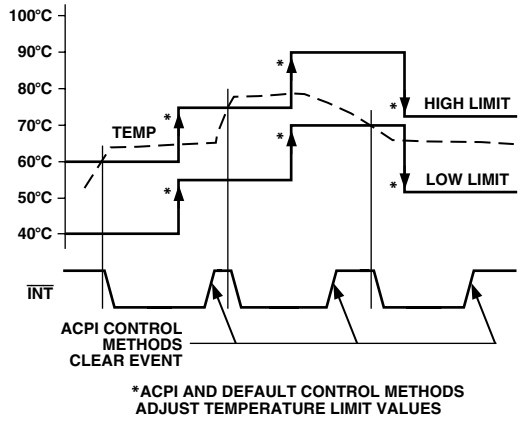


Figure 15. Operation of $\overline{INT}$ for Temperature Interrupts

Once the interrupt has been cleared, it will not be reasserted even if the temperature remains above the high limit(s). However, $\overline{INT}$ will be reasserted if:

a. the temperature falls below the low limit for the sensor

or

b. the high limit is/are reprogrammed to a new value, and the temperature then rises above the new high limit on the next monitoring cycle

or

c. the $\overline{THERM}$ pin is pulled low externally, which sets Bit 5 of Interrupt Status Register 2

or

d. An interrupt is generated by another source.

Similarly, should the temperature measured by a sensor start off within limits then fall below the low limit, $\overline{INT}$ will be asserted. Once cleared, it will not be reasserted unless:

a. the temperature rises above the high limit

or

b. the low limit is/are reprogrammed, and the temperature then falls below the new low limit

or

c. the $\overline{THERM}$ pin is pulled low externally, which sets Bit 5 of Interrupt Status Register 2

or

d. an interrupt is generated by another source.

$\overline{THERM}$ INPUT/OUTPUT

The Thermal Management Input/Output ($\overline{THERM}$) is a logic input/output with an internal, 100 kΩ pull-up resistor, that provides a separate output for temperature interrupts only. It is enabled by setting Bit 2 of Configuration Register 1. The $\overline{THERM}$ output has two operating modes that can be programmed by Bit 3 of Configuration Register 2 (address 4Ah). With this bit set to the default value of 0, the $\overline{THERM}$ output operates in "Default" interrupt mode. With this bit set to 1, the $\overline{THERM}$ output operates in "ACPI" mode.

Thermal interrupts can still be generated at the $\overline{INT}$ output while $\overline{THERM}$ is enabled, but if these are not required they can be masked by writing a 1 to bit 0 of Configuration Register 2 (address 4Ah). The $\overline{THERM}$ pin can also function as a logic input for an external sensor, for example a temperature sensor such as the ADM22105 used in Figure 16b. If $\overline{THERM}$ is taken low by an external source, the analog output will be forced to FFh to switch a controlled fan to maximum speed. This also generates an $\overline{INT}$ output as previously described.

DEFAULT MODE

In Default mode, the $\overline{THERM}$ output operates like a thermostat with hysteresis. $\overline{THERM}$ will go low and Bit 5 of Interrupt Status Register 2 will be set, if the temperature measured by any of the sensors exceeds the high limit programmed for that sensor. It will remain asserted until reset by reading Interrupt Status Register 2, by setting Bit 6 of Configuration Register 1, or when the temperature falls below the low limit programmed for that sensor.

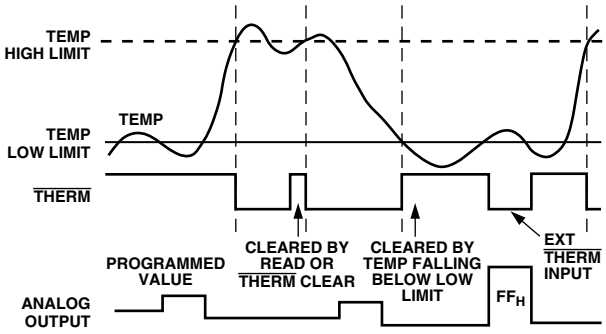


Figure 16a. $\overline{INT}$ or $\overline{THERM}$ Output in Default Mode

If $\overline{\text{THERM}}$ is cleared by reading the status register, it will be reasserted after the next temperature reading and comparison if it remains above the high limit.

If $\overline{\text{THERM}}$ is cleared by setting Bit 6 of Configuration Register 1, it cannot be reasserted until this bit is cleared.

$\overline{\text{THERM}}$ will also be asserted if one of the hardware temperature limits at addresses 13h, 14h, 17h, or 18h is exceeded for three consecutive measurements. When this happens, the analog output will be forced to FFh to boost a controlled cooling fan to full speed.

Reading Status Register 1 will not clear $\overline{\text{THERM}}$ in this case, because errors caused by exceeding the hardware temperature limits are stored in a separate register that is not cleared by reading the status register. In this case, $\overline{\text{THERM}}$ can only be cleared by setting Bit 0 of Configuration Register 2.

$\overline{\text{THERM}}$ will be cleared automatically if the temperature falls at least 5 degrees below the limit for three consecutive measurements.

ACPI MODE

In ACPI mode, $\overline{\text{THERM}}$ responds only to the hardware temperature limits at addresses 13h, 14h, 17h and 18h, not to the software programmed limits.

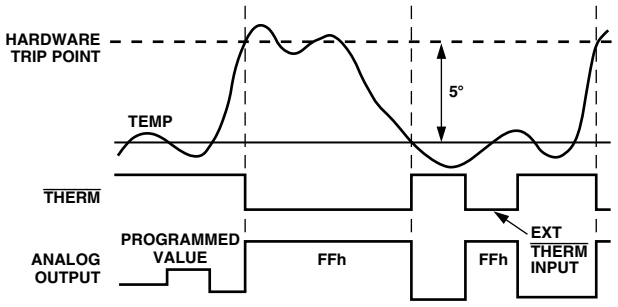


Figure 16b. $\overline{\text{THERM}}$ Output in ACPI Mode

$\overline{\text{THERM}}$ will go low if either the internal or external hardware temperature limit is exceeded for three consecutive measurements. It will remain low until the temperature falls at least 5 degrees below the limit for three consecutive measurements. While $\overline{\text{THERM}}$ is low, the analog output will go to FFh to boost a controlled fan to full speed.

$\overline{\text{RESET}}$ INPUT/OUTPUT

$\overline{\text{RESET}}$ (Pin 12) is an I/O pin that can function as an open-drain output, providing a low-going 20 ms output pulse when Bit 4 of the Configuration Register is set to 1, provided the reset function has first been enabled by setting Bit 7 of Interrupt Mask Registers #2 to 1. The bit is automatically cleared when the reset pulse is output. Pin 11 can also function as a $\overline{\text{RESET}}$ input by pulling this pin low to reset the internal registers of the ADM1024 to default values. Only those registers that have power on default values as listed in Table VI are affected by this function. The DAC register, Value and Limit Registers are not affected.

NAND TESTS

A NAND gate is provided in the ADM1024 for Automated Test Equipment (ATE) board level connectivity testing. The device is placed into NAND Test Mode by powering up with Pin 11 held high. This pin is automatically sampled after power-up and if it is connected high, then the NAND test mode is invoked.

In NAND test mode, all digital inputs may be tested as illustrated below. NTEST_OUT/ADD will become the NAND test output pin. To perform a NAND tree test all pins included in the NAND tree should first be driven high. Each pin can then be toggled and a resulting toggle can be observed on NTEST_OUT/ADD.

Allow for a typical propagation delay of 500 ns. The structure of the NAND tree is shown in Figure 17.

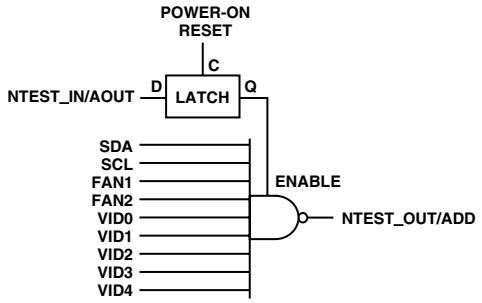


Figure 17. NAND Tree

Note that NTEST_OUT/ADD is a dual function line and if both functions are required, then this line should not be hard-wired directly to V_{CC}/GND. Instead it should be connected via a 5 kΩ resistor.

Note: If any of the inputs shown in Figure 17 are unused, they should not be connected directly to ground, but via a resistor such as 10 kΩ. This will allow the ATE (Automatic Test Equipment) to drive every input high so that the NAND tree test can be carried out properly.

USING THE ADM1024

POWER-ON RESET

When power is first applied, the ADM1024 performs a "power-on reset" on several of its registers. Registers whose power-on values are not shown have power-on conditions that are indeterminate (this includes the Value and Limit Registers). The ADC is inactive. In most applications, usually the first action after power-on would be to write limits into the Limit Registers.

Power-on reset clears or initializes the following registers (the initialized values are shown in Table VIII):

- Configuration Registers #1 and #2
- Channel Mode Register
- Interrupt ($\overline{\text{INT}}$) Status Registers #1 and #2
- Interrupt ($\overline{\text{INT}}$) Status Mirror Registers #1 and #2
- Interrupt ($\overline{\text{INT}}$) Mask Registers #1 and #2
- VID/Fan Divisor Register
- VID4 Register
- Chassis Intrusion Clear Register
- Test Register
- Analog Output Register
- Hardware Trip Registers

INITIALIZATION

Configuration Register INITIALIZATION performs a similar, but not identical, function to power-on reset. The Test Register and Analog Output Register are not initialized.

Configuration Register INITIALIZATION is accomplished by setting Bit 7 of the Configuration Register high. This bit automatically clears after being set.

USING THE CONFIGURATION REGISTERS

Control of the ADM1024 is provided through two configuration registers. The ADC is stopped upon power-up, and the $\overline{\text{INT}}$_Clear signal is asserted, clearing the $\overline{\text{INT}}$ output. The Configuration Registers are used to start and stop the ADM1024; enable or disable interrupt outputs and modes, and provide the initialization function described above.

Bit 0 of Configuration Register 1 controls the monitoring loop of the ADM1024. Setting Bit 0 low stops the monitoring loop and puts the ADM1024 into a low power mode thereby reducing power consumption. Serial bus communication is still possible with any register in the ADM1024 while in low-power mode. Setting Bit 0 high starts the monitoring loop.

Bit 1 of Configuration Register 1 enables or disables the $\overline{\text{INT}}$ Interrupt output. Setting Bit 1 high enables the $\overline{\text{INT}}$ output, setting Bit 1 low disables the output.

Bit 2 of Configuration Register 1 enables or disables the $\overline{\text{THERM}}$ output. Setting Bit 1 high enables the $\overline{\text{INT}}$ output, setting Bit 1 low disables the output.

Bit 3 of Configuration Register 1 is used to clear the $\overline{\text{INT}}$ interrupt output when set high. The ADM1024 monitoring function will stop until Bit 3 is set low. Interrupt Status register contents will not be affected.

Bit 4 of Configuration Register 1 causes a low-going 45 ms (typ) pulse at the $\overline{\text{RESET}}$ pin (Pin 12).

Bit 6 of Configuration Register 1 is used to clear an interrupt at the $\overline{\text{THERM}}$ output when it is set to 1.

Bit 7 of Configuration Register 1 is used to start a Configuration Register Initialization when it is set to 1.

Bit 0 of Configuration Register 2 is used to mask temperature interrupts at the $\overline{\text{INT}}$ output when it is set to 1. The $\overline{\text{THERM}}$ output is unaffected by this bit.

Bits 1 and 2 of Configuration Register 2 lock the values stored in the Local and Remote Fan Control Registers at addresses 13h and 14h. The values in these registers cannot be changed until a power-on reset is performed.

Bit 3 of Configuration Register 2 selects the $\overline{\text{THERM}}$ interrupt mode. The default value of 0 selects one-time mode. Setting this bit to 1 selects ACPI mode.

STARTING CONVERSION

The monitoring function (analog inputs, temperature, and fan speeds) in the ADM1024 is started by writing to Configuration Register 1 and setting Start (Bit 0), high. The $\overline{\text{INT}}$_Enable (Bit 1) should be set to 1, and $\overline{\text{INT}}$ Clear (Bit 3) set to 0 to enable interrupts. The $\overline{\text{THERM}}$ enable bit (Bit 2) should be set to 1 and the $\overline{\text{THERM}}$ Clear bit (Bit 6) should be set to 0 to enable temperature interrupts at the $\overline{\text{THERM}}$ pin. Apart from initially starting together, the analog measurements and fan speed measurements proceed independently, and are not synchronized in any way.

The time taken to complete the analog measurements depends on how they are configured, as described elsewhere. The time taken to complete the fan speed measurements depends on the fan speed and the number of tach output pulses per revolution.

Once the measurements have been completed, the results can be read from the Value Registers at any time.

REDUCED POWER AND SHUTDOWN MODE

The ADM1024 can be placed in a low-power mode by setting Bit 0 of the Configuration Register to 0. This disables the internal ADC. Full shutdown mode may then be achieved by setting Bit 0 of the Test Register to 1. This turns off the analog output and stops the monitoring cycle, if running, but it does not affect the condition of any of the registers. The device will return to its previous state when this bit is reset to zero.

APPLICATION CIRCUIT

Figure 18 shows a generic application circuit using the ADM1024. The analog monitoring inputs are connected to the power supplies including two processor core voltage inputs. The VID inputs are connected to the processor voltage ID pins. There are two tach inputs from fans, and the analog output is used to control the speed of a third fan. An opto-sensor for chassis intrusion detection is connected to the CI input. Of course, in an actual application, every input and output may not be used, in which case unused analog and digital inputs should be tied to analog or digital ground as appropriate.

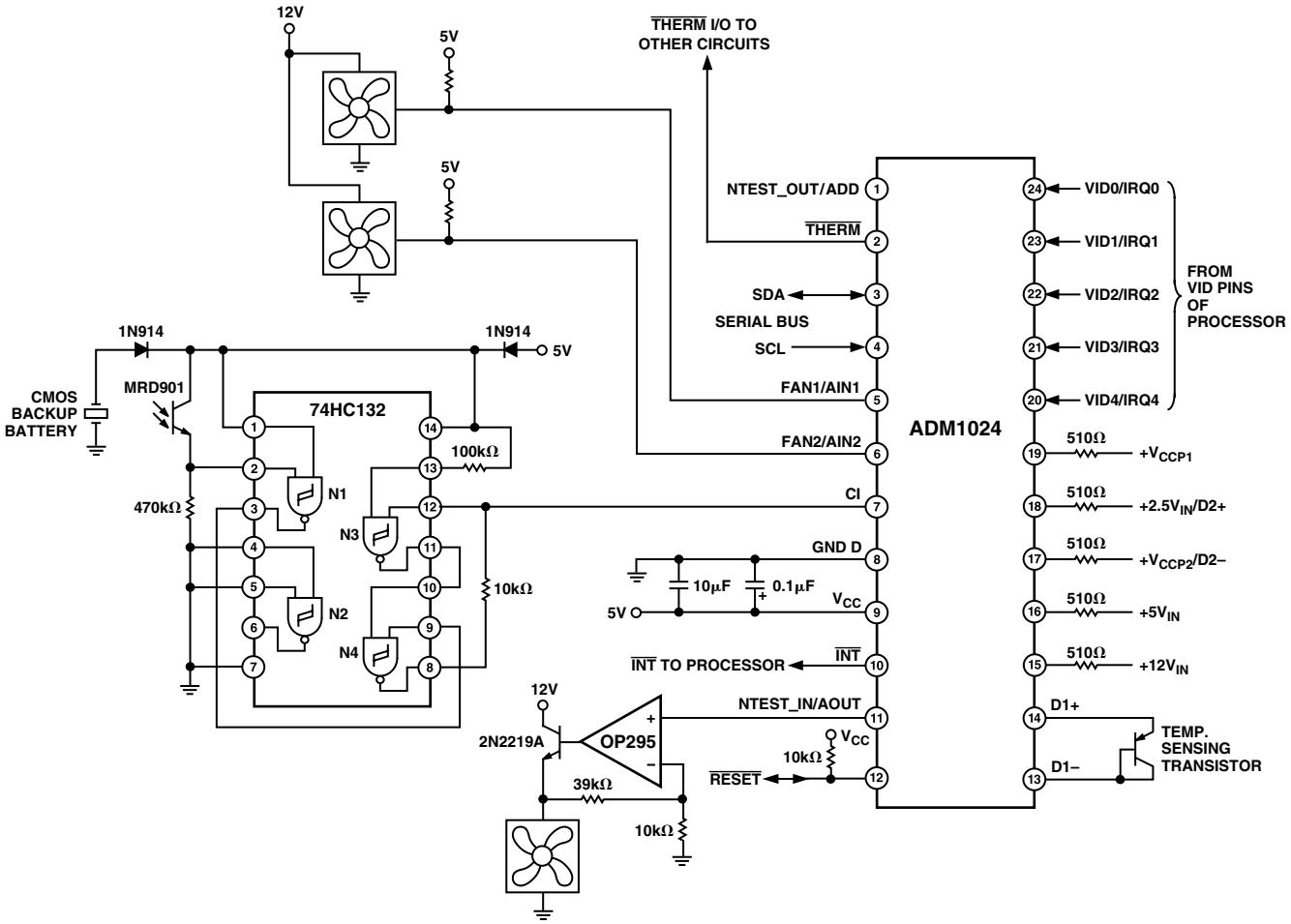


Figure 18. Application Circuit

ADM REGISTERS

Table VI. Address Pointer Register

Bit	Name	R/$\overline{W}$	Description
7–0	Address Pointer	Write	Address of ADM1024 Registers. See the tables below for detail.

Table VII. List of Registers

Hex Address	Description	Power-On Value (Binary Bit 7–0)	Notes
13h	Internal Temperature Hardware Trip Point	= 70°C	Can be written only if the write once bit in Configuration Register 2 has not been set. Values higher than 70°C will have no affect as the fixed trip point in register 16h will be reached first.
14h	External Temp Hardware Trip Point	= 85°C	Can be written only if the write once bit in Configuration Register 2 has not been set. Values higher than 85°C will have no affect as the fixed trip point in register 17h will be reached first.
15h	Test Register	0000 00X0	Setting Bit 0 of this register to 1 selects shutdown mode. Caution: Do not write to any other bits in this register.
16h	Channel Mode Register	0000 0000	This register configures the input channels and configures VID0 to VID as processor voltage ID or interrupt inputs.
17h	Internal Temperature Fixed Hardware Trip Point	= 70°C	Read Only. Cannot be changed.
18h	External Temperature Fixed Hardware Trip Point	= 85°C	Read Only. Cannot be changed.
19h	Programmed Value of Analog Output	1111 1111	
1Ah	AIN1 Low Limit	Indeterminate	
1Bh	AIN2 Low Limit	Indeterminate	
20h	2.5 V Measured Value/EXT Temp2	Indeterminate	Read Only.
21h	V_{CCP1} Measured Value	Indeterminate	Read Only.
22h	V_{CC} Measured Value	Indeterminate	Read Only.
23h	5 V Value	Indeterminate	Read Only.
24h	12 V Measured Value	Indeterminate	Read Only.
25h	V_{CCP2} Measured Value	Indeterminate	Read Only
26h	Ext. Temp1 Value	Indeterminate	Read Only. Stores the measurement from a diode sensor connected to Pins 13 and 14.
27h	Internal Temperature Value	Indeterminate	Read Only. This register is used to store eight bits of the internal temperature reading.
28h	FAN1/AIN1 Value	Indeterminate	Read Only. Stores FAN1 or AIN1 reading depending on the configuration of Pin 5.
29h	FAN2/AIN1 Value	Indeterminate	Read Only. Stores FAN2 or AIN2 reading depending on the configuration of Pin 6.
2Ah	Reserved	Indeterminate	
2Bh	2.5 V/Ext. Temp2 High Limit	Indeterminate	Stores high limit for 2.5 V input or, in temperature mode, this register stores the high limit for a diode sensor connected to Pins 17 and 18.
2Ch	2.5 V/Ext. Temp2 Low Limit	Indeterminate	Stores low limit for 2.5 V input or, in temperature mode, this register stores the low limit for a diode sensor connected to Pins 17 and 18.
2Dh	V_{CCP1} High Limit	Indeterminate	
2Eh	V_{CCP1} Low Limit	Indeterminate	
2Fh	V_{CC} High Limit	Indeterminate	
30h	V_{CC} Low Limit	Indeterminate	
31h	5 V High Limit	Indeterminate	
32h	5 V Low Limit	Indeterminate	
33h	12 V High Limit	Indeterminate	
34h	12 V Low Limit	Indeterminate	

Table VII (continued)

Hex Address	Description	Power-On Value (Binary Bit 7–0)	Notes
35h	V_{CCP2} High Limit	Indeterminate	
36h	V_{CCP2} Low Limit	Indeterminate	
37h	Ext Temp1. High Limit	Indeterminate	Stores high limit for a diode sensor connected to Pins 13 and 14.
38h	Ext Temp1. Low Limit	Indeterminate	Stores low limit for a diode sensor connected to Pins 13 and 14.
39h	Internal Temp. High Limit	Indeterminate	Stores the high limit for the internal temperature reading.
3Ah	Internal Temp. Low Limit	Indeterminate	Stores the low limit for the internal temperature reading.
3Bh	AIN1/FAN1 High Limit	Indeterminate	Stores high limit for AIN1 or FAN1, depending on the configuration of Pin 5.
3Ch	AIN2/FAN2 High Limit	Indeterminate	Stores high limit for AIN2 or FAN2, depending on the configuration of Pin 6.
3Dh	Reserved	Indeterminate	
3Eh	Company ID Number	0100 0001	This location will contain the company identification number (Read Only).
3Fh	Revision Number	0001 nnnn	Last four bits of this location will contain the revision number of the part. (Read Only)
40h	Configuration Register 1	0000 1000	See Table IX.
41h	Interrupt INT Status Register 1	0000 0000	See Table X.
42h	Interrupt INT Status Register 2	0000 0000	See Table XI.
43h	INT Mask Register 1	0000 0000	See Table XII.
44h	INT Mask Register 2	0000 0000	See Table XIII.
46h	Chassis Intrusion Clear Register	0000 0000	See Table XIV.
47h	VID 0–3/Fan Divisor Register	0101 (VID3–VID0)	See Table XV.
49h	VID4 Register	1000 000 (VID4)	See Table XVI.
4Ah	Configuration Register 2	0000 0000	See Table XVII.
4Ch	Interrupt Status Register Mirror No. 1	0000 0000	See Table XVIII.
4Dh	Interrupt Status Register Mirror No. 2	0000 0000	See Table XIX.

Table VIII. Register 16h, Channel Mode Register (Power-On Default = 00h)

Bit	Name	R/$\overline{W}$	Description
0	FAN1/AIN1	R/$\overline{W}$	Clearing this bit to 0 configures Pin 5 as FAN1 input. Setting this bit to 1 configures Pin 5 as AIN1. Power-on default = 0.
1	FAN2/AIN2	R/$\overline{W}$	Clearing this bit to 0 configures Pin 6 as FAN2 input. Setting this bit to 1 configures Pin 6 as AIN2. Power-on default = 0.
2	2.5 V, V_{CCP}/D2	R/$\overline{W}$	Clearing this bit to 0 configures Pins 17 and 18 to measure 2.5 V and V_{CCP2}. Setting this bit to 1 configures Pins 18 and 19 as an input for a second remote temperature-sensing diode. Power-on default = 0.
3	Int V_{CC}	R/$\overline{W}$	Clearing this bit to 0 sets the measurement range for the internal V_{CC} measurement to 3.3 V. Setting this bit to 1 sets the internal V_{CC} measurement range to 5 V. Power-on default = 0.
4	IRQ0 EN	R/$\overline{W}$	Setting this bit to 1 enables Pin 24 as an active high interrupt input, provided Pins 20 to 24 have been configured as interrupts by setting Bit 7 of the Channel Mode Register. Power-on default = 0.
5	IRQ1 EN	R/$\overline{W}$	Setting this bit to 1 enables Pin 23 as an active high interrupt input, provided have been configured as interrupts by setting Bit 7 of the Channel Mode Register. Power-on default = 0.
6	IRQ2 EN	R/$\overline{W}$	Setting this bit to 1 enables Pin 22 as an active high interrupt input, provided Pins 20 to 24 have been configured as interrupts by setting Bit 7 of the Channel Mode Register. Power-on default = 0.
7	VID/IRQ	R/$\overline{W}$	Clearing this bit to 0 configures Pins 20 to 24 as processor voltage ID inputs. Setting this bit to 1 configures Pins 20 to 24 as interrupt inputs. Power-on default = 0.

Table IX. Register 40h, Configuration Register 1 (Power-On Default = 08h)

Bit	Name	R/$\overline{W}$	Description
0	START	R/$\overline{W}$	Logic 1 enables start-up of ADM1024, logic 0 places it in standby mode. Caution: The outputs of the interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred (see "$\overline{INT}$ Clear" bit). At start-up, limit checking functions and scanning begins. Note, all high and low limits should be set into the ADM1024 prior to turning on this bit. (Power-Up Default = 0)
1	$\overline{INT}$_Enable	R/$\overline{W}$	Logic 1 enables the $\overline{INT}$_output. 1 = Enabled 0 = Disabled (Power-Up Default = 0).
2	$\overline{THERM}$ Enable	R/$\overline{W}$	0 = $\overline{THERM}$ disabled. 1 = $\overline{THERM}$ enabled.
3	$\overline{INT}$_Clear	R/$\overline{W}$	During Interrupt Service Routine (ISR) this bit is asserted Logic 1 to clear INT output without affecting the contents of the Interrupt Status Register. The device will stop monitoring. It will resume upon clearing of this bit. (Power-Up Default = 0)
4	$\overline{RESET}$	R/$\overline{W}$	Setting this bit generates a low-going 45 ms reset pulse at Pin 12. This bit is self-clearing and power-up default is 0.
5	Reserved	R/$\overline{W}$	Default = 0.
6	$\overline{THERM}$ CLR	R/$\overline{W}$	A one clears the $\overline{THERM}$ output without changing the Status Register contents.
7	Initialization	R/$\overline{W}$	Logic 1 restores Power-Up default values to the Configuration register, Interrupt status registers, Interrupt Mask Registers, Fan Divisor Register, and the Temperature Configuration Register. This bit automatically clears itself since the power-on default is zero.

Table X. Register 41h, Interrupt Status Register 1 (Power-On Default = 00h)

Bit	Name	R/$\overline{W}$	Description
0	2.5 V/External Temp2 Error	Read Only	A one indicates that a High or Low limit has been exceeded.
1	V_{CCP1} Error	Read Only	A one indicates that a High or Low limit has been exceeded.
2	V_{CC} Error	Read Only	A one indicates that a High or Low limit has been exceeded.
3	5 V Error	Read Only	A one indicates that a High or Low limit has been exceeded.
4	Internal Temp Error	Read Only	A one indicates that a temperature interrupt has been set, or that a High or Low limit has been exceeded.
5	External Temp1 Error	Read Only	A one indicates that a temperature interrupt has been set, or that a High or Low limit has been exceeded.
6	FAN1/AIN1 Error	Read Only	A one indicates that a High or Low limit has been exceeded.
7	FAN2/AIN2 Error	Read Only	A one indicates that a High or Low limit has been exceeded.

Table XI. Register 42h, Interrupt Status Register 2 (Power-On Default = 00h)

Bit	Name	R/$\overline{W}$	Description
0	12 V Error	Read Only	A one indicates a High or Low limit has been exceeded.
1	V_{CCP2} Error	Read Only	A one indicates a High or Low limit has been exceeded.
2	Reserved	Read Only	Undefined.
3	Reserved	Read Only	Undefined.
4	Chassis Error	Read Only	A one indicates Chassis Intrusion has gone high.
5	$\overline{THERM}$ Interrupt	Read Only	Indicates that $\overline{THERM}$ pin has been pulled low by an external source.
6	D1 Fault	Read Only	Short or open-circuit sensor diode D1.
7	D2 Fault	Read Only	Short or open-circuit sensor diode D2.

NOTES
1. Any time the STATUS Register is read out, the conditions (i.e., Register) that are read are automatically reset. In the case of the channel priority indication, if two or more channels were out of limits, then another indication would automatically be generated if it was not handled during the ISR.
2. In the Mask Register, the errant voltage interrupt may be disabled, until the operator has time to clear the errant condition or set the limit higher/lower.

Table XII. Register 43h, $\overline{INT}$ Interrupt Mask Register 1 (Power-On Default = 00h)

Bit	Name	R/$\overline{W}$	Description
0	2.5 V/Ext. Temp2	Read/$\overline{Write}$	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
1	V_{CCP1}	Read/$\overline{Write}$	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
2	V_{CC}	Read/$\overline{Write}$	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
3	5 V	Read/$\overline{Write}$	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
4	Int. Temp	Read/$\overline{Write}$	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
5	Ext. Temp1	Read/$\overline{Write}$	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
6	FAN1/AIN1	Read/$\overline{Write}$	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
7	FAN2/AIN2	Read/$\overline{Write}$	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.

Table XIII. Register 44h, $\overline{INT}$ Mask Register 2 (Power-On Default = 00h)

Bit	Name	R/$\overline{W}$	Description
0	12 V	Read/$\overline{Write}$	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
1	V_{CCP2}	Read/$\overline{Write}$	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
2	Reserved	Read/$\overline{Write}$	Power-up default set to Low.
3	Reserved	Read/$\overline{Write}$	Power-up default set to Low.
4	CI	Read/$\overline{Write}$	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
5	$\overline{THERM}$ (Input)	Read/$\overline{Write}$	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
6	D1 Fault	Read/$\overline{Write}$	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
7	D2 Fault	Read/$\overline{Write}$	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.

Table XIV. Register 46h, Chassis Intrusion Clear (Power-On Default = 00h)

Bit	Name	R/$\overline{W}$	Description
0–6	Reserved	Read Only	Undefined, always reads as 00h.
7	Chassis Int. Clear	Read/$\overline{Write}$	A one outputs a minimum 20 ms active low pulse on the Chassis Intrusion pin. The register bit clears itself after the pulse has been output.

Table XV. Register 47h, VID0–3/FAN Divisor Register (Power-On Default 0101(VID3–0))

Bit	Name	R/$\overline{W}$	Description
0–3	VID	Read	The VID[3:0] inputs from processor core power supplies to indicate the operating voltage (e.g., 1.3 V to 3.5 V)
4–5	FAN1 Divisor	Read/$\overline{Write}$	Sets counter prescaler for FAN1 speed measurement <5:4> = 00 – divide by 1 <5:4> = 01 – divide by 2 <5:4> = 10 – divide by 4 <5:4> = 11 – divide by 8.
6–7	FAN2 Divisor	Read/$\overline{Write}$	Sets counter prescaler for FAN2 speed measurement <7:6> = 00 – divide by 1 <7:6> = 01 – divide by 2 <7:6> = 10 – divide by 4 <7:6> = 11 – divide by 8.

Table XVI. Register 49h, VID4/Device ID Register (Power-On Default 1000000(VID4))

Bit	Name	R/$\overline{W}$	Description
0	VID4	Read Only	VID4 Input from Pentium.
1–7	Reserved	Read Only	Undefined, always reads as 1000 000(VID4).

Table XVII. Register 4AH, Configuration Register 2 (Power-On Default [7:0] = 0x00h)

Bit	Name	R/$\overline{W}$	Description
0	Thermal $\overline{INT}$ Mask	Read/$\overline{Write}$	Setting this bit masks the thermal interrupts for the $\overline{INT}$ output ONLY. The $\overline{THERM}$ output will still be generated, regardless of the setting of this bit.
1	Ambient Temp Fan Control Register Write Once Bit	Read/$\overline{Write}$ Once	Writing a one to this bit will lock in the values set into the ambient temperature automatic fan control register 13h. This register will not be able to be written again until a reset is performed (either POR, Hard or Soft Reset).
2	Remote Temp Fan Control Register Write Once Bit	Read/$\overline{Write}$ Once	Writing a one to this bit will lock in the values set into the remote temperature automatic fan control register 14h. This register will not be able to be written again until a reset is performed (either POR, Hard or Soft Reset).
3	$\overline{THERM}$ Interrupt Mode	Read/$\overline{Write}$	If this bit is 0 the $\overline{THERM}$ output operates in default mode. If this bit is 1, the $\overline{THERM}$ output operates in ACPI mode.
4, 5	Reserved	Read Only	Reserved.
6	IRQ3 EN	Read/$\overline{Write}$	Setting this bit to 1 enables Pin 21 as an active high interrupt input, provided Pins 20 to 24 have been configured as interrupts by setting Bit 7 of the Channel Mode Register. Power-on default = 0.
7	IRQ4 EN	Read/$\overline{Write}$	Setting this bit to 1 enables Pin 20 as an active high interrupt input, provided Pins 20 to 24 have been configured as interrupts by setting Bit 7 of the Channel Mode Register. Power-on default = 0.

Table XVIII. Register 4Ch, Interrupt Status Register 1 Mirror (Power-On Default <7:0> = 00h)

Bit	Name	R/$\overline{W}$	Description
0	2.5 V/Ext. Temp2 Error	Read Only	A one indicates that a High or Low limit has been exceeded.
1	V_{CCP1} Error	Read Only	A one indicates that a High or Low limit has been exceeded.
2	V_{CC} Error	Read Only	A one indicates that a High or Low limit has been exceeded.
3	5 V Error	Read Only	A one indicates that a High or Low limit has been exceeded.
4	Internal Temp Error	Read Only	A one indicates that a temperature interrupt has been set, or that a High or Low limit has been exceeded.
5	External Temp1 Error	Read Only	A one indicates that a temperature interrupt has been set, or that a High or Low limit has been exceeded.
6	FAN1/AIN1 Error	Read Only	A one indicates that a High or Low limit has been exceeded.
7	FAN2/AIN2 Error	Read Only	A one indicates that a High or Low limit has been exceeded.

Table XIX. Register 4DH, Interrupt Status Register 2 Mirror (Power-On Default <7:0> = 00h)

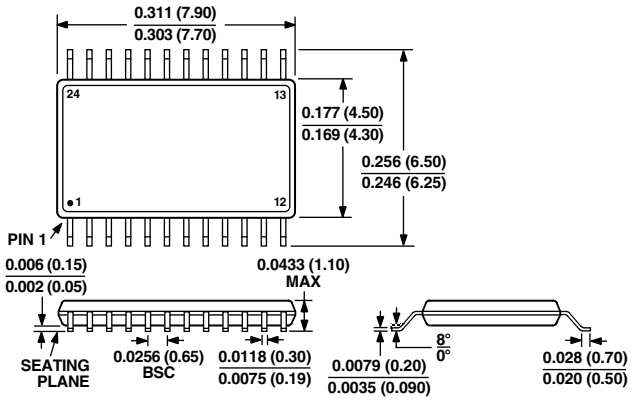
Bit	Name	R/$\overline{W}$	Description
0	12 V Error	Read Only	A one indicates a High or Low limit has been exceeded.
1	V_{CCP2} Error	Read Only	A one indicates a High or Low limit has been exceeded.
2	Reserved	Read Only	Undefined.
3	Reserved	Read Only	Undefined.
4	Chassis Error	Read Only	A one indicates Chassis Intrusion has gone high.
5	$\overline{THERM}$ Interrupt	Read Only	Indicates that $\overline{THERM}$ pin has been pulled low by an external source.
6	D1 Fault	Read Only	Short or open-circuit sensor diode D1.
7	D2 Fault	Read Only	Short or open-circuit sensor diode D2.

NOTE
An error that causes continuous interrupts to be generated may be masked in its respective mask register, until the error can be alleviated.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Lead TSSOP Package
(RU-24)



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ADM1024ARU-REEL7	0°C to 100°C	24-Lead TSSOP	RU-24
ADM1024ARUZ[1]	0°C to 100°C	24-Lead TSSOP	RU-24
ADM1024ARUZ-REEL[1]	0°C to 100°C	24-Lead TSSOP	RU-24
ADM1024ARUZ-R7[1]	0°C to 100°C	24-Lead TSSOP	RU-24
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[1]Z = Pb-Free part

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