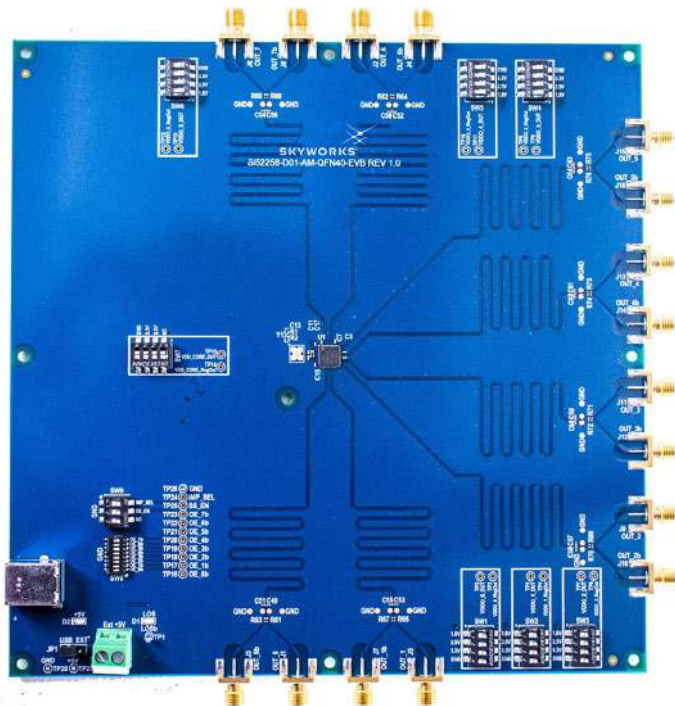


# UG399: Si52258-EVB User's Guide (Using Si52258-D01-AM-QFN40-EVB)

The Si52258-EVB is used for evaluating the eight output Si52258A-D01AM Automotive grade PCIe Reference Clock Generator. The Si52258A-D01AM device uses the on-board 25 MHz crystal as reference clock source and generates 8 copies of a 100 MHz HCSL format output clock compliant to PCIe Gen 1/2/3/4/5 common clock and separate reference clock specifications.



## EVB FEATURES

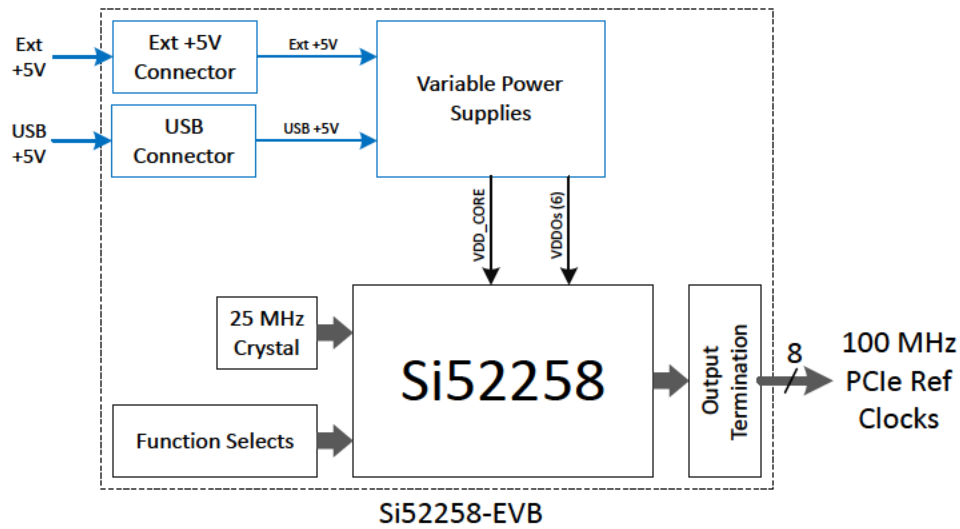
- Powered from either USB port or external +5V power supply.
- On-board 25 MHz crystal reference.
- Programmable device core VDD supply for operation at 3.3 V, 2.5 V, or 1.8 V.
- Programmable VDDO (output driver) supplies allow each of the clock output banks to have its own power supply voltage selectable from 3.3 V, 2.5 V, or 1.8 V.
- SMA connectors for all output clocks.
- PCIe compliant spread spectrum enabled/ disabled via on-board switch.
- Internal output termination switch selectable for 100  $\Omega$  or 85  $\Omega$  operation.
- Output enable (OE) control switch per output.
- All output trace lengths matched to 10 inches.
- Loss of Signal (LOS) indication LED.

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## 1. Functional Block Diagram

Below is a functional block diagram of the Si52258-EVB. The +5V required by the EVB can come from a powered USB connection (only +5V is required) or from an external +5V power supply.



**Figure 1.1. Si52258-EVB Functional Block Diagram**

## 2. Si52258-EVB Operation

### 2.1 EVB Configuration: Switches & Jumpers

#### Power Supplies:

DIP switches SW1 – SW7 control the on-board power supplies. The table below is a guide to show how to select output voltages for each supply and the EVB default settings. Jumper JP1 selects the source of the +5V used by all the power supply regulators. JP1 jumper pin 1 to 2 selects USB as power source (default) and pin 2 to 3 selects external +5V source via J17 terminal block (refer to schematic).

Switch Position:		1	2	3	4	
DIP Switch #	Control Function	1.8V*	2.5V*	3.3V*	Enable	EVB Default
SW1	VDDO0	0	1	1	0	Enabled, +1.8V
SW2	VDDO1	0	1	1	0	Enabled, +1.8V
SW3	VDDO2	0	1	1	0	Enabled, +1.8V
SW4	VDDO3	0	1	1	0	Enabled, +1.8V
SW5	VDDO4	0	1	1	0	Enabled, +1.8V
SW6	VDDO5	0	1	1	0	Enabled, +1.8V
SW7	VDD_CORE	NC	1	1	0	Enabled, +1.8V

#### Note:

- 0 = Switch Position Closed (On)
- 1 = Switch Position Open (Off)

**\*Caution:** Only 1 voltage select switch position can be 0 (On) at a time. Do not set more than 1 position to On and only change switches with power OFF.

#### Output Enables:

DIP switch SW8 is used to control the clock output enables. There are 8 output enables (OE), one per output clock. The EVB default setting is all outputs enabled.

Switch Position:		1	2	3	4	5	6	7	8	
DIP Switch #	Control Function	OE_0b	OE_1b	OE_2b	OE_3b	OE_4b	OE_5b	OE_6b	OE_7b	EVB Default
SW8	Output Enables	0	0	0	0	0	0	0	0	All Enabled

#### Note:

- 0 = Switch Position Closed (On)
- 1 = Switch Position Open (Off)

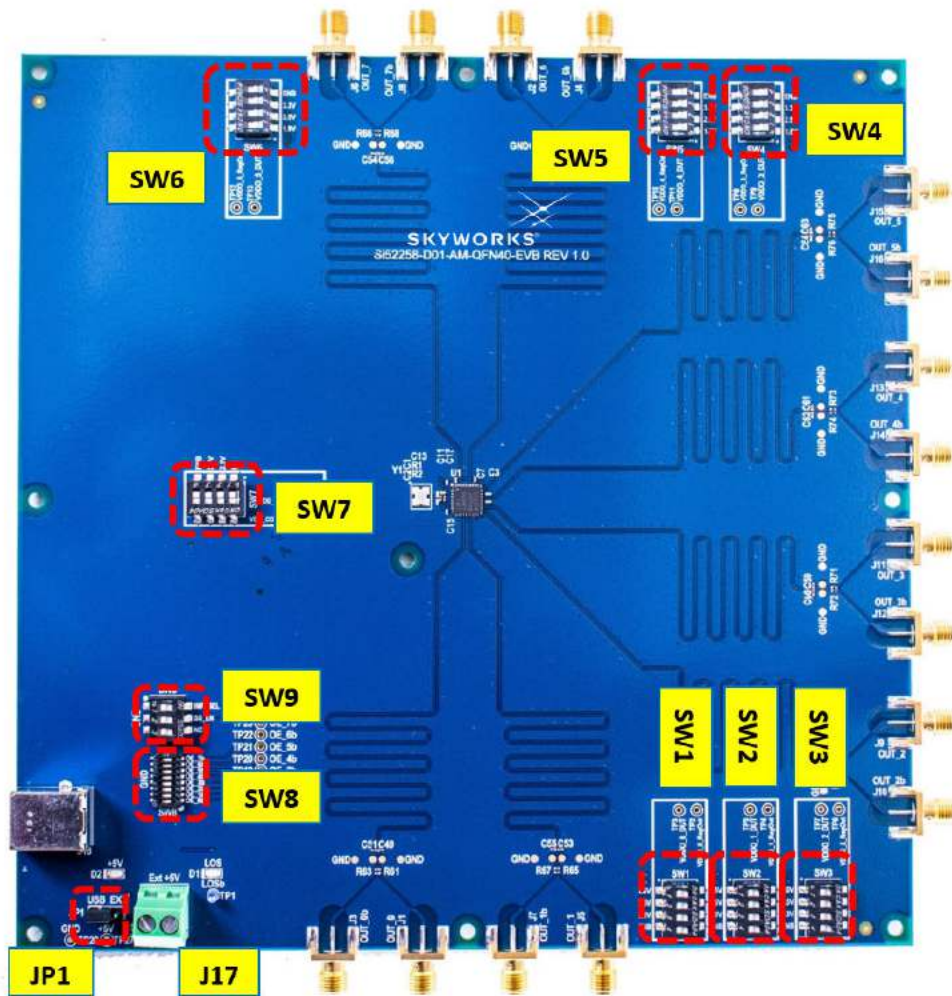
**Function Enables:**

DIP switch SW9 is used to select Spread Spectrum (On or Off) and Output Termination Impedance (85 Ω or 100 Ω).

Switch Position:		1	2	3	
DIP Switch #	Control Function	IMP_SEL	SS_EN	NC	EVB Default
SW9	Impedance	1	–	NC	Imp = 85 Ω
	Spread Spectrum	–	0	NC	SS_EN (active high) = Off

- Note:**
- 0 = Switch Position Closed (On)
  - 1 = Switch Position Open (Off)

**Location of DIP Switches:**



**Figure 2.1. DIP Switches Location**

### 3. LEDs

The Si52258-EVB has 2 LEDs defined below.

D2: **Blue LED** indicating +5V presence.

D3: **Red LED** indicating Loss of Signal (LOS). When lit, this LED indicates a problem was detected with the crystal or crystal oscillator circuit which is preventing proper oscillation, resulting in a loss or degradation of the input reference for the Clock Generator.

## 4. Output Clocks

The Si52258-EVB supports all 8 differential pair output clocks, each terminated as shown in the figure below. The EVB has locations to install 2 pF parallel termination capacitors if desired, which are tagged with “NI” in schematic to indicate they are not installed by default. The outputs are otherwise direct DC coupled to the SMA connectors. Convenient connection pads are also provided for measuring the output with a differential probe, in which case removal of the 0 Ω resistors to isolate the SMA “stub” from the transmission line is suggested.

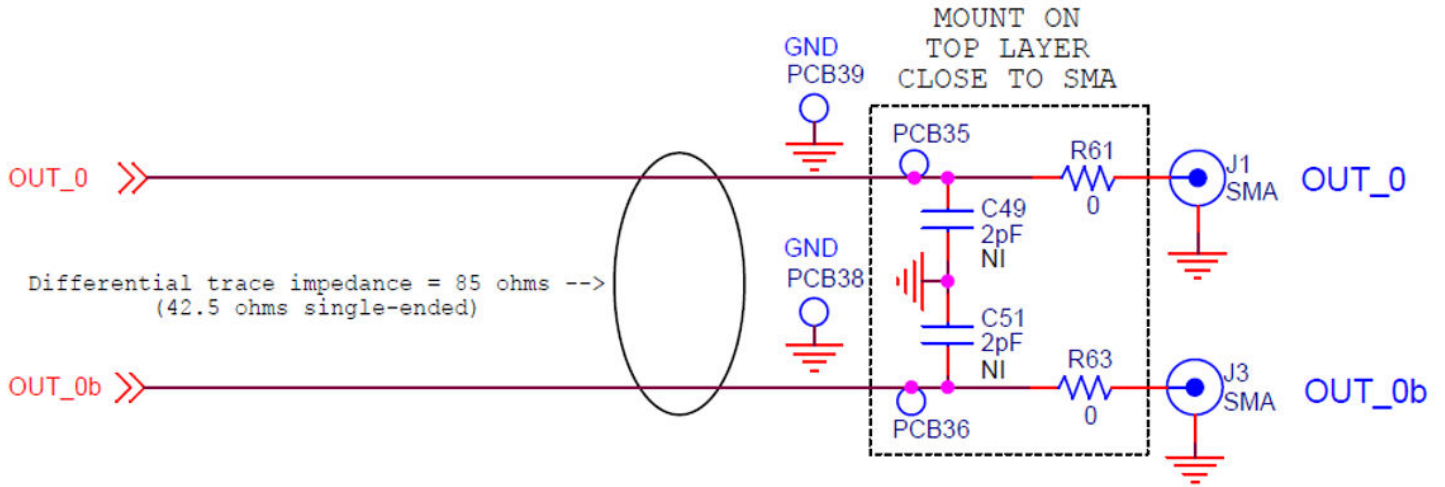
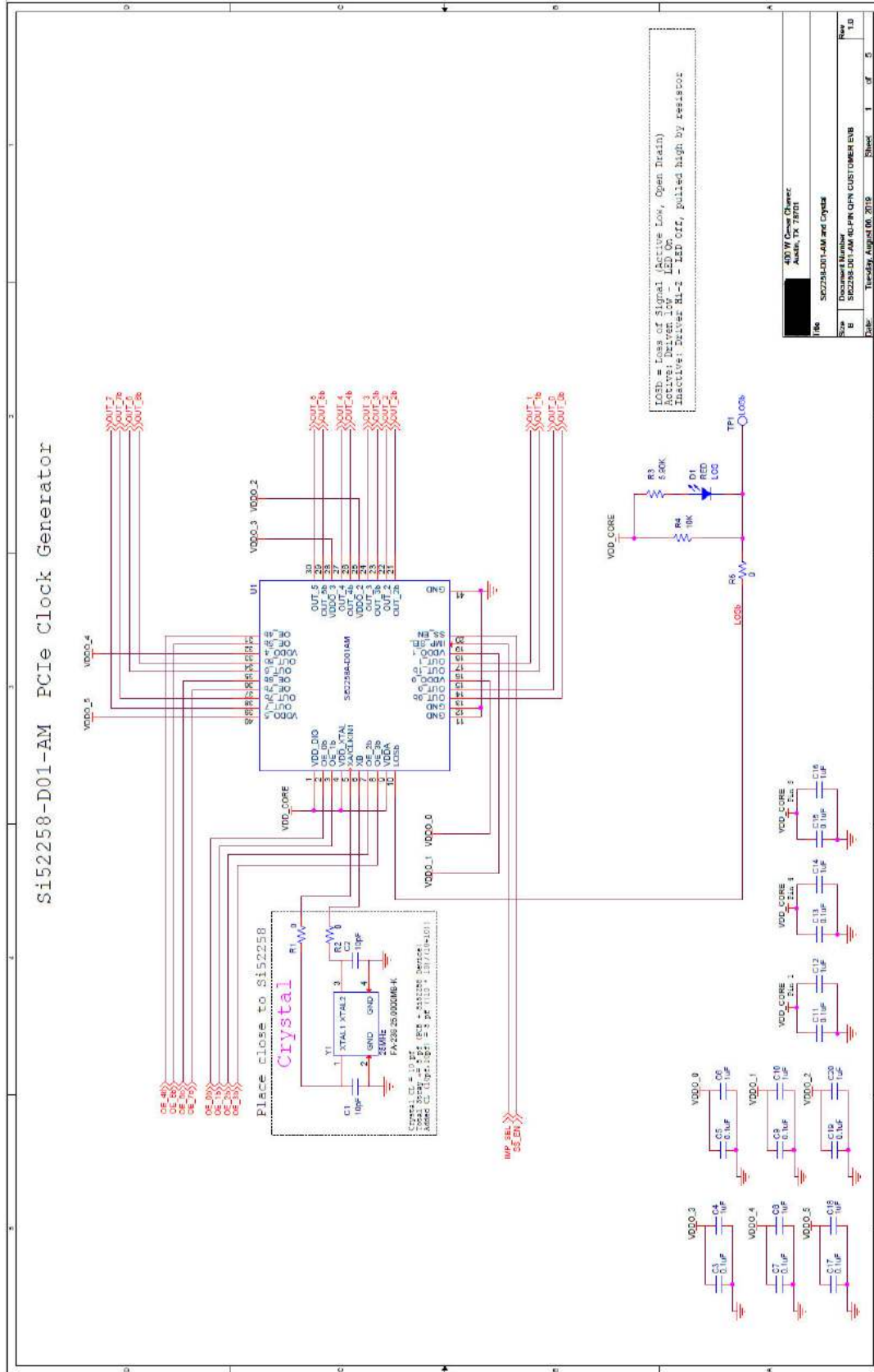
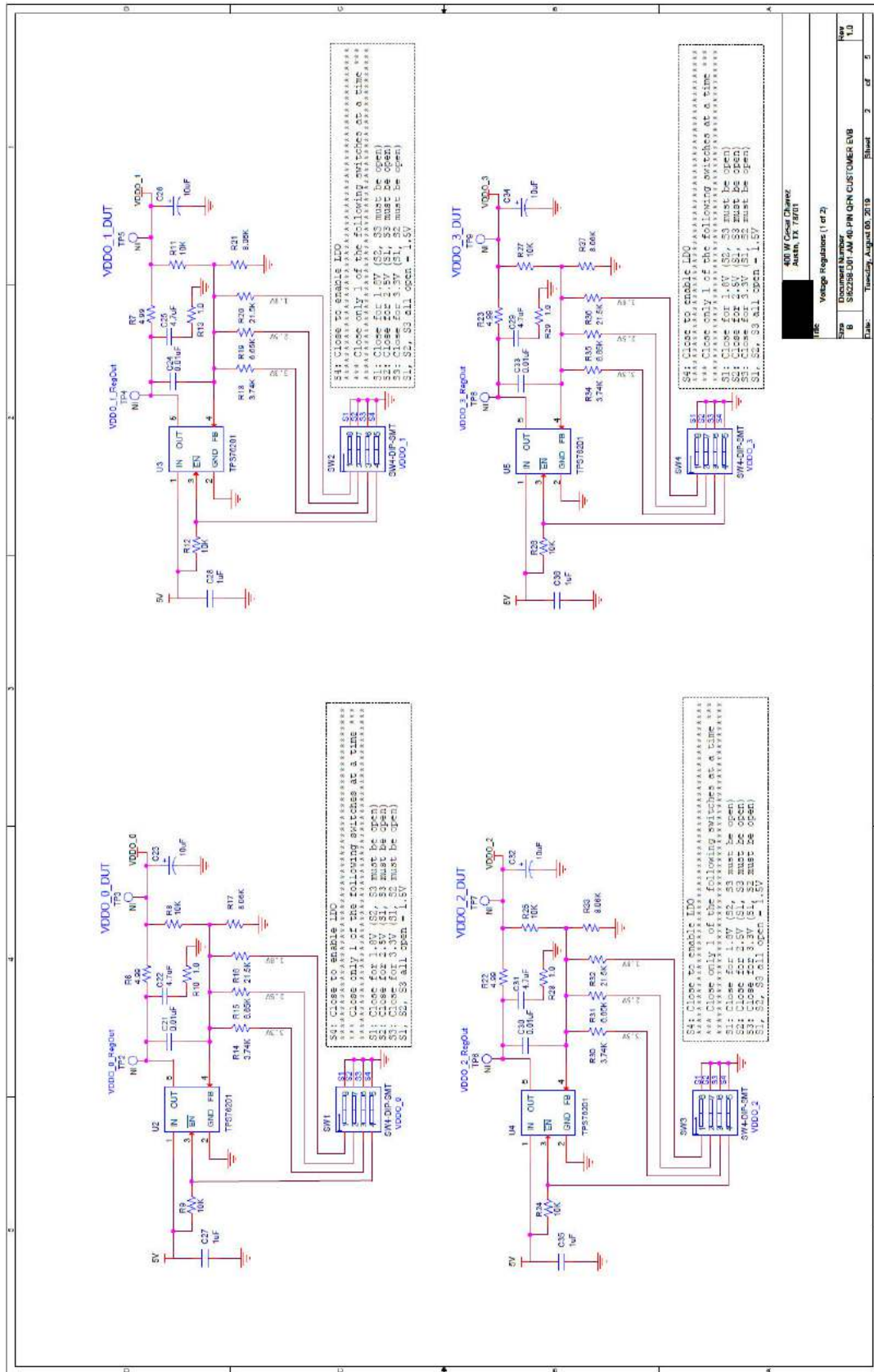


Figure 4.1. Si52258-EVB Output Clock Differential Pair Termination Circuit

### 5. Si52258-EVB Rev 1.0 Schematics







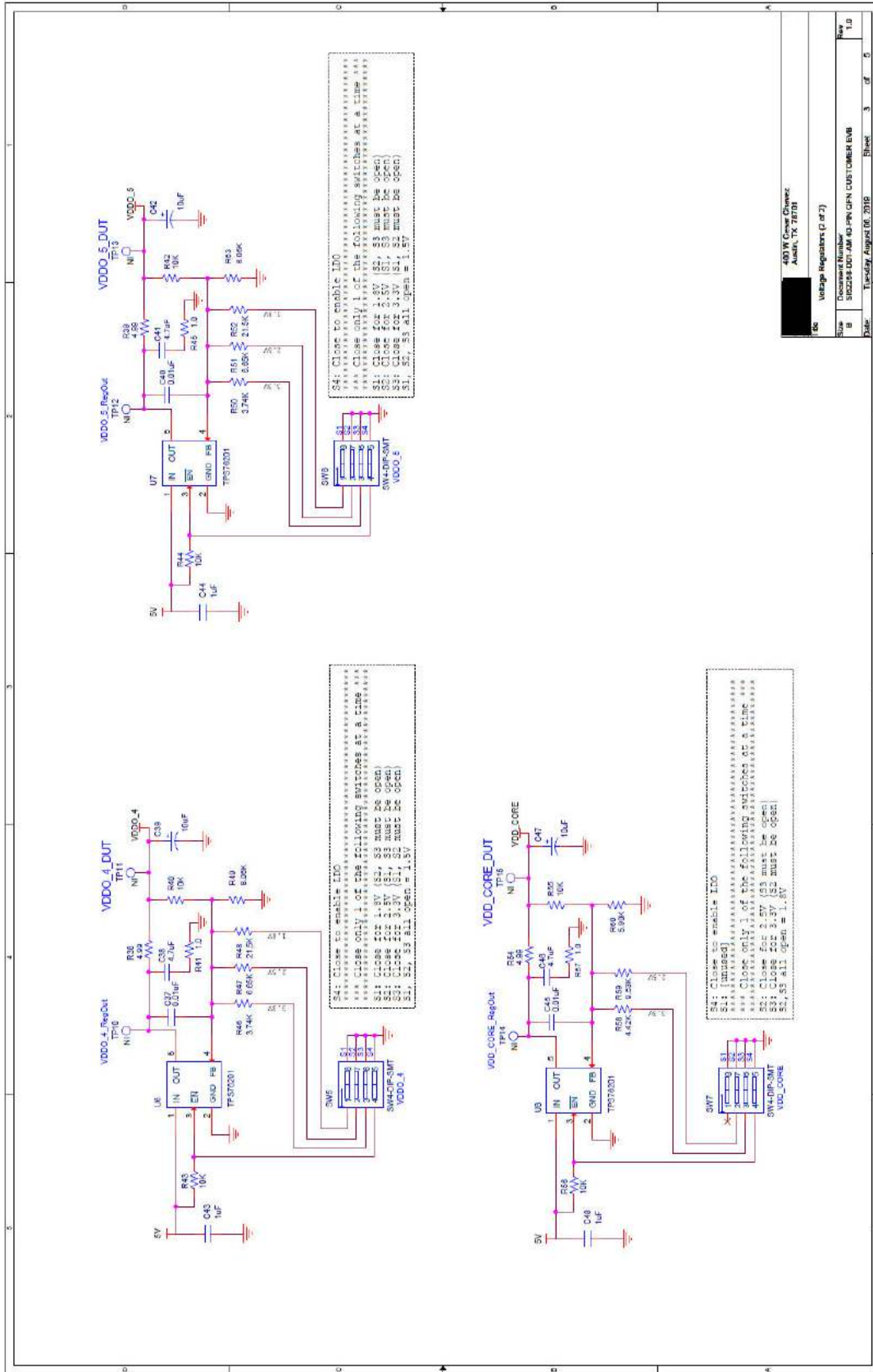
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Title: Voltage Regulators (1 of 2)

Rev: SK52258-D01-AM-QFN-QFN CUSTOMER EVB

Rev: 1.0

Date: Tuesday, August 06, 2019 Sheet: 2 of 3

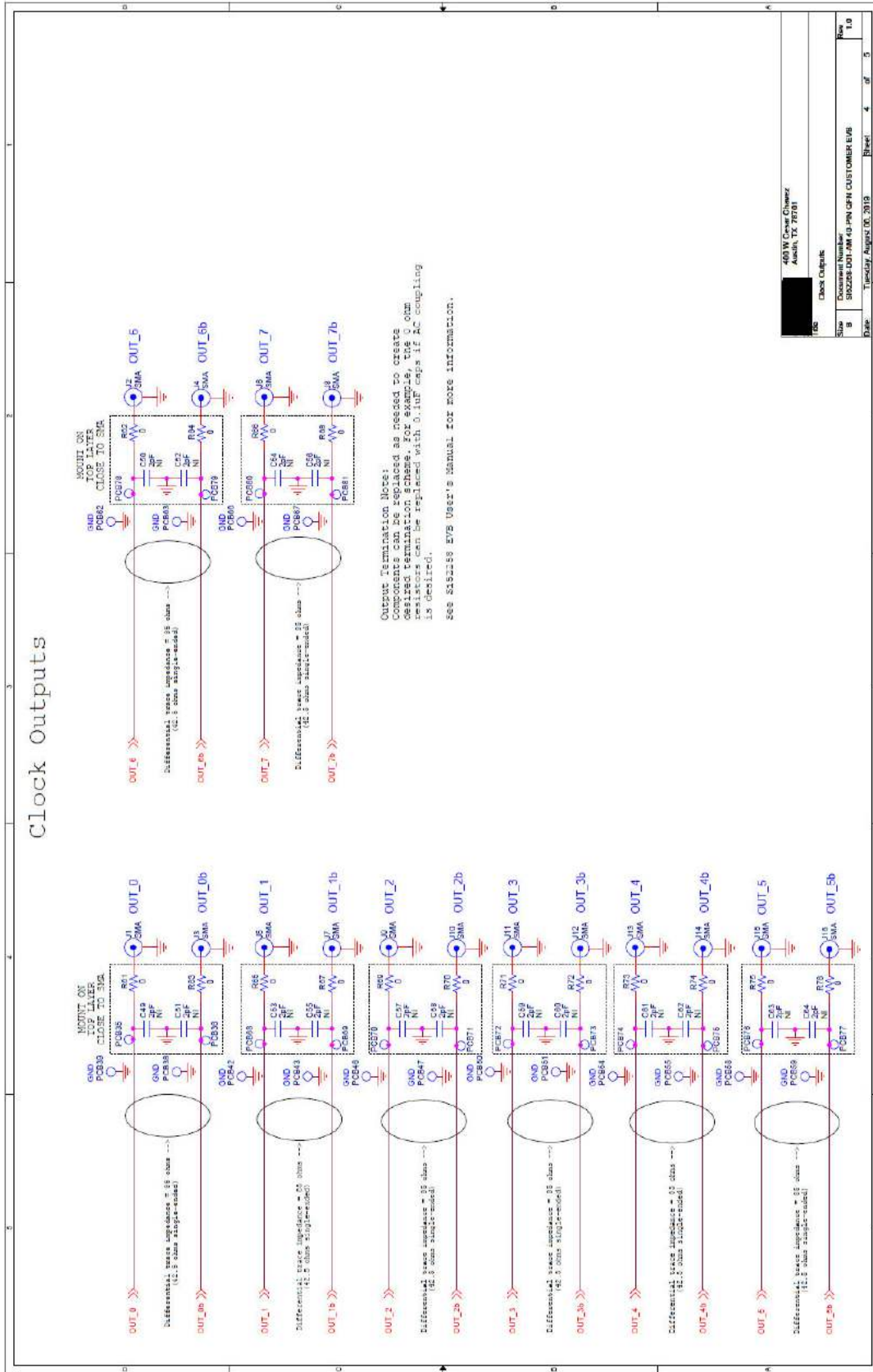


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SW4 Voltage Regulators (2 of 2)

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