General Description

The epc200 is a high-sensitive, high-speed, low-cost photodiode for light-barriers, light-curtains and similar applications. These photodiodes are designed to be used in a reverse-bias mode, whereas the reverse bias voltage can be between 1.5 and 20 Volts. This device allows the design of short to long range light-barriers from a few millimeters up to tens of meters. The diodes feature a very high quantum efficiency of 90% in the near IR range, a reverse breakdown voltage of up to 30 Volts and a response time down to less than 100ns.

The advanced Chips Scale Package (CSP) makes this device ideal for miniaturized systems where a minimal space requirement is the key.

Features

- Low dark current
- High sensitivity
- High dynamic range
- CSP package with very small footprint
- Customer specific wavelength filter upon request
- Fully standard SMD assembly process compatible

Applications

- Light-barriers and light-curtains ranging from millimeters to tens of meters
- Smoke detectors, liquid detectors, level detectors
- Heartbeat monitors, oximeters
- Position detection (linear, rotary, angle, etc.)
- IR remote control of Hi-Fi, TV sets and other equipment

Product image

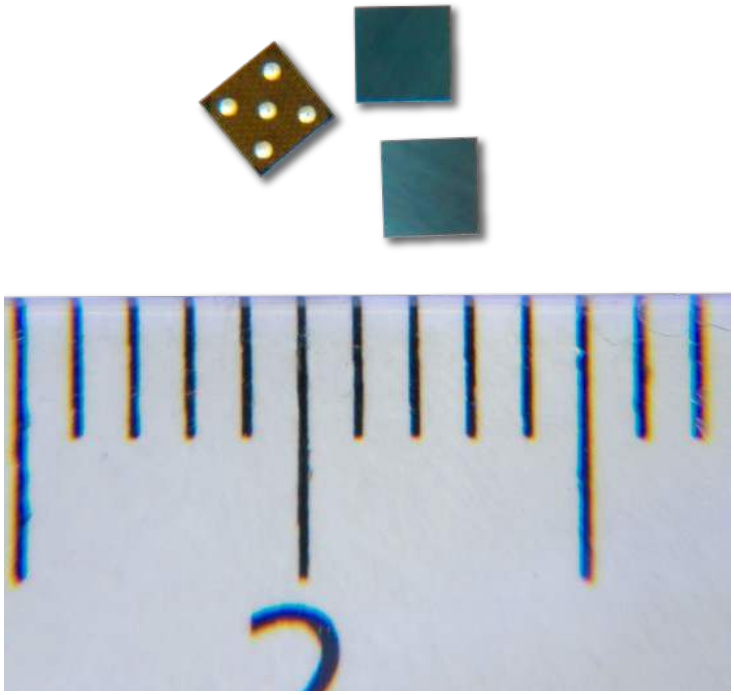


Figure 1: epc200 photodiodes

1. Electrical, optical and timing characteristics

All characteristics are at typical operational ratings, V_R = 5.0 V, R_L = 50 Ω, -40°C < T_A < +85°C, unless otherwise stated

Parameter	Description	Conditions/Comments		Min.	Typ.	Max.	Units
V_R	Reverse voltage			1.5	5	20	V
λ_S max.	Wavelength	At max. sensitivity			850		nm
λ	Wavelength range	S = 20 % of S_{max}		400		1'030	nm
S_λ	Spectral sensitivity	λ = 850 nm, V_R = 5V, I_e = 1 mW/cm² λ = 940 nm, V_R = 5V, I_e = 1 mW/cm²			0.61 0.43		A/W
η	Quantum efficiency	λ = 850 nm, V_R = 5V, I_e = 1 mW/cm² λ = 940 nm, V_R = 5V, I_e = 1 mW/cm²			90 62		%
φ	Half angle				±75		°
V_O	Open circuit voltage	I_e = 0.5 mW/cm²			250		mV
TC_V	Temperature coefficient of I_{SC}				0.25		%/K
TC_O	Temperature coefficient of V_O				-3.0		mV/K
I_P	Photocurrent	λ = 850 nm, V_R = 5V, I_e = 1 mW/cm² λ = 940 nm, V_R = 5V, I_e = 1 mW/cm² Refer to Figure 4.			18.7 13.2		µA
I_R	Dark Current	V_R = 5 V, T_A= 20°C V_R = 20 V, T_A= 20°C Selected types available upon request.			2 5	20	nA
I_{SC}	Short-circuit current	λ = 850 nm, I_e = 1 mW/cm²			20		µA
t_r / t_f	Rise / fall time	Photocurrent I_P = 200 µA at R_L = 50 Ω , λ = 850 nm. Refer to Figure 5.	V_R = +1.5 V		300		ns
			V_R = +5.0 V		140		
			V_R = +10.0 V		70		
C_O	Capacitance	V_R = +5V, f = 100kHz, E = 0			22		pF
NEP	Noise equivalent power	V_R = +5V			1.2 x 10^{-14}		W/√Hz

Table 1: General characteristics and operating conditions

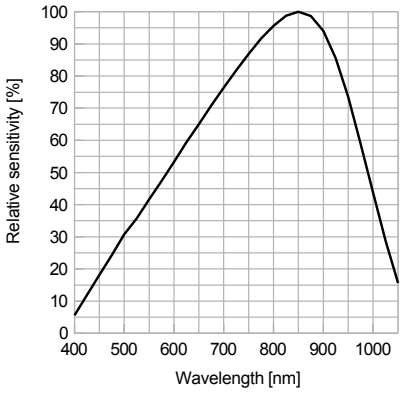


Figure 2: Relative spectral sensitivity (Sλ) vs. wavelength

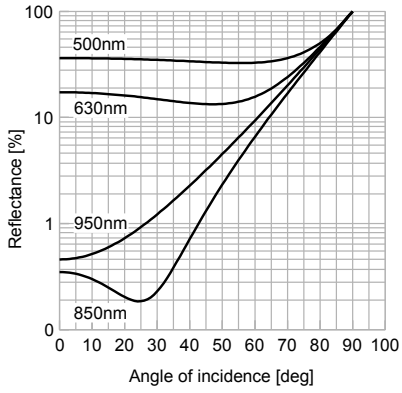


Figure 3: Reflectance vs. illumination angle (AOI)

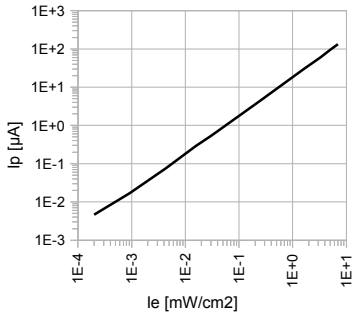


Figure 4: Photocurrent $I_P = f(I_e)$, V_R = 5 V, λ = 850nm

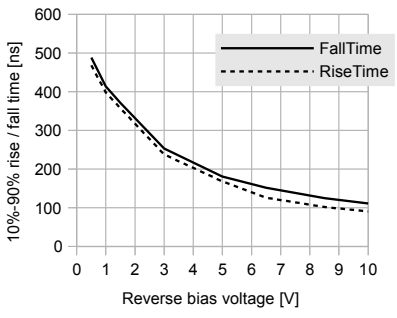


Figure 5: Rise / fall time vs. reverse bias voltage

1.1. Absolute maximum ratings

Parameter	Conditions
Reverse voltage V_R	30 V
ESD rating	JEDEC HBM class 2 (2kV to < 4kV)
Expected lifetime (MTBF)	500 * 106 h @ 25°C, < 2 FIT
Operating temperature range (T_a)	-40°C to +85°C
Storage temperature range (T_S)	-40°C to +85°C
Relative humidity	0 ... 95%, non-condensing

2. Pin-out

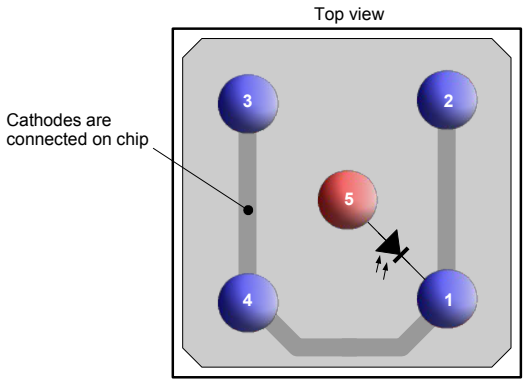
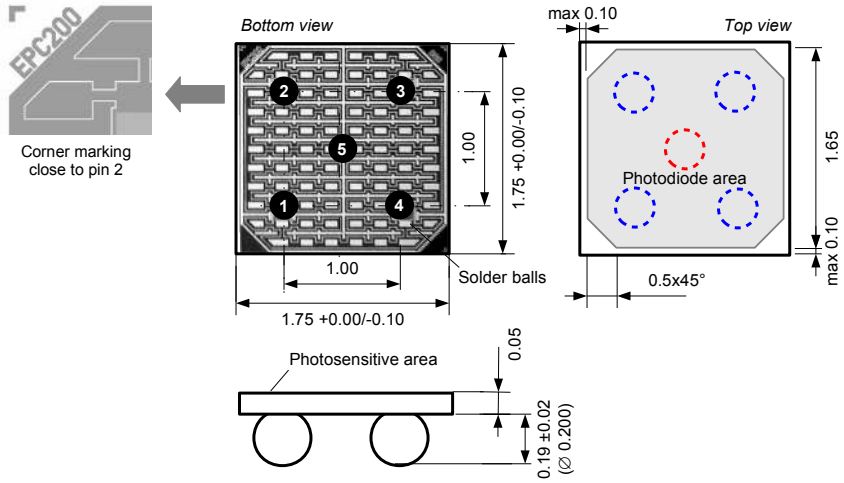


Figure 6: Pin-out

3. Packaging and layout information

3.1. Mechanical dimensions



Notes:

- 
- Dimensions in mm
- Not specified tolerances: ±0.001mm
- Top side is illumination side

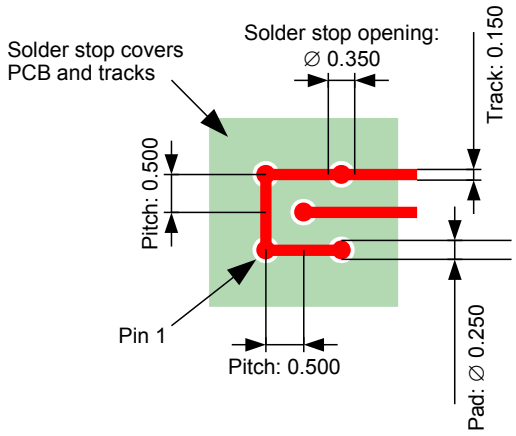
Figure 7: Dimensions epc200-CSP5

3.2. Location of the photosensitive area

The photosensitive area is not marked (neither on the front nor on the backside of the IC). As a visible reference, the metal ring of the IC can be used. It is visible from the solder ball side. It can be seen also from the front side (photosensitive area) with a camera which is sensitive in the near infrared wavelength domain (950 ... 1'150nm).

3.3. PCB design and SMD manufacturing process considerations

As the epc200 chip comes in chip scale packages with only 50µm thickness, the PCB layout should be made with special care. In addition, careful handling during the assembly process shall be assured in order to avoid mechanical damage during the assembly process.



Important Note
Due to the thin chip substrate, unevenness of the substrate surface will be visible on the top surface of the chip. This may cause optical issues and has to be considered carefully.

Vias underneath the chip:
They must be filled solid or covered by a solder pad or solder mask to prevent drain of solder or underfill into or through the vias

Figure 8: Recommended PCB layout (all measures in mm)

Because the silicon chip is small and light weight compared to the solder balls, it is highly recommended that all tracks to the chip should come straight from the side (Figure 8). A symmetrical design regarding the landing pads and their openings is highly recommended to achieve high production yield. The pads and the tracks should also have exactly the same width at least for 1mm from the pad. They shall be covered by a solder resist mask in order to avoid drain of the solder tin alloy to the track.

Note: Connect all cathode pins to the same voltage level.

Underfill of the components reduces stress to the solder pads caused by e.g. temperature cycling or mechanical bending. Furthermore the thermal and mechanical fatigue will be reduced and the longterm reliability will be increased. Underfill material and underfill selection is application specific. It shall follow JEDEC-STD JEP150: Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components. Refer also to the application note AN08 Process-Rules CSP Assembly which can be downloaded from the ESPROS website at www.espros.com/downloads. Obeying these recommendations a high manufacturing yield can be achieved.

3.4. Tape & reel information

The devices are mounted on embossed tape for automatic placement systems. The tape is wound on 178 mm (7 inch) or 330 mm (13 inch) reels and individually packaged for shipment. General tape-and-reel specification data are available in a separate datasheet and indicate the tape sizes for various package types. Further tape-and-reel specifications can be found in the Electronic Industries Association (EIA) standard 481-1, 481-2, 481-3.

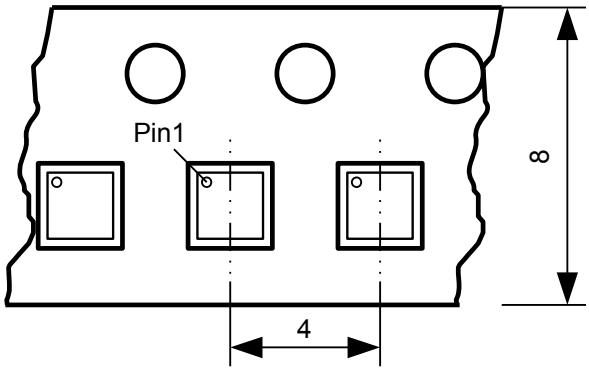


Figure 9: Tape dimensions (all measures in mm)
Note: Solder balls are bottom side

ESPROS does not guarantee that there are no empty cavities. Thus, the pick-and-place machine should check the presence of a chip during picking.

4. Ordering information

Part Number	Part Name	Package	RoHS compliance
P100 179	epc200-CSP5	CSP5	Yes
P100 205	epc200 Chip Carrier	PCB LCC2	Yes

Table 2: Ordering Information

Figure 10: epc200 photodiodes on chip carrier

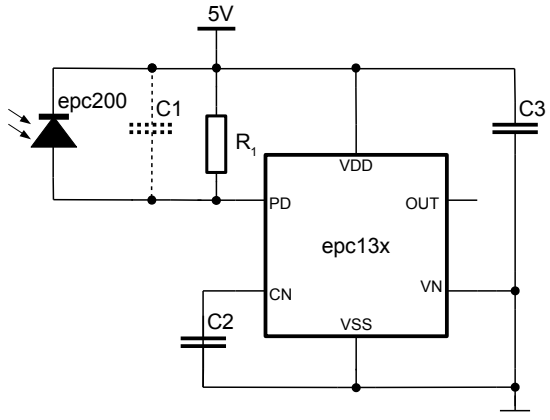
5. Application information

5.1. Spectral sensitivity

These photodiodes contain an anti-reflection coating on the photosensitive surface. Standard versions have no optical filter in order to allow applications from the near UV to the near IR range. However, optical filters deposited on the photosensitive surface are available upon request. The filter parameters can be adjusted in a wide range according to specific customer requirements.

5.2. Light-barrier application

A typical application of this chip is shown in Figure 11. In this application, a reverse bias voltage of approx. 1.5 V is used. Since the applications are typically light-barriers, dark current is not important at all, even in the range of up to 100nA. The circuit uses an epc200 photodiode in combination with an epc13x PD amplifier chip. It offers a very high AC photocurrent sensitivity and a tremendous DC backlight suppression.



Recommended components values
example only – depends on particular application case

R1: 27k (bias resistor). Reduction of this resistor reduces sensitivity.
C1: Not needed. May be up to 100 pF. Refer to datasheet epc13x.
C2: 33nF (DC input current filter capacitor)
C3: 100nF or more (power supply filter capacitor)

Figure 11: Typical schematic using an epc13x PD amplifier

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