MAX20340

Bidirectional DC Powerline Communication Management IC

General Description

The MAX20340 is a universal bidirectional DC powerline communication (PLC) management IC with a 166.7kbps maximum bit rate. The device is capable of a maximum of 1.2A charge current.

The MAX20340 features a slave detection circuit that flags an interrupt to the system when the PLC master detects the presence of a PLC slave on the power line. This function allows the system to remain in a low-power state until a slave device is connected.

Many of the features of the MAX20340, such as master/slave mode, I²C address, dual/single PLC slave mode, and PLC slave address, are pin configurable.

The device is available in a 9-bump, 0.4mm pitch, 1.358mm x 1.358mm wafer-level package (WLP).

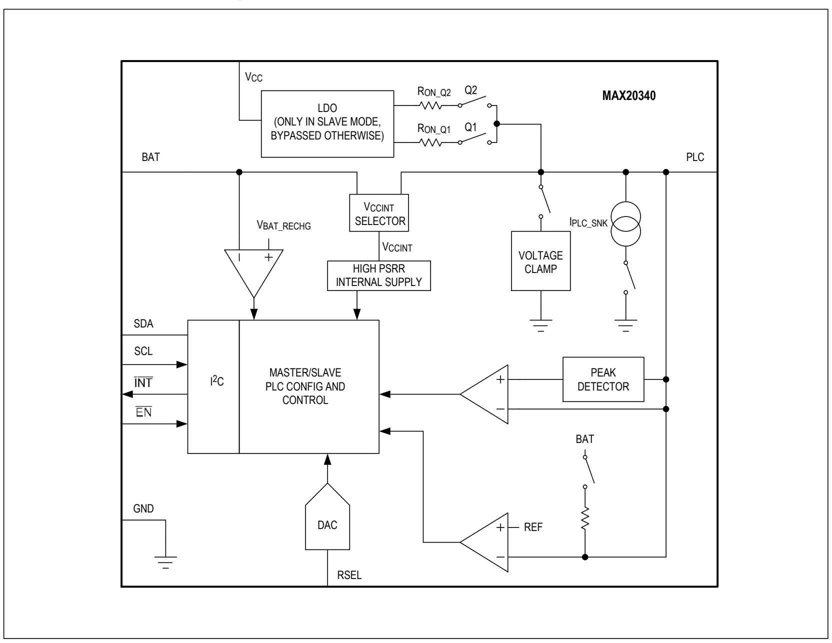
Applications

- Truly Wireless Earbuds
- Tethered Wireless Headphones
- Hearing Aids
- Wearables
- Game Controllers
- Handheld Radios
- Point of Sales Devices

Benefits and Features

- Compact, Simple Solution for PLC
  - Up to 166.7kbps Bit Rate
    - 5.7kbps Data Throughput in Automatic Mode
  - 1.2A Charge Current
  - Automatic Detection of PLC Slave Presence
- Flexible Configuration
  - Single Resistor to Program
  - PLC Master or Slave
  - Dual or Single Slave Mode (Master Only)
  - PLC Slave Address (Slave Only)
  - I²C Address
- Small Solution Size
  - Space-Saving 0.4mm Pitch, 9-Bump, 1.358mm x 1.358mm WLP

Functional Diagram



Absolute Maximum Ratings

V_{CC}, PLC, SCL, SDA, $\overline{INT}$, BAT, $\overline{EN}$, RSEL to GND.... .. -0.3V to +6V

Continuous Current V_{CC}, Q1, Q2 closed, PLC ..-1.2A to +1.2A

Continuous Current into Any Other Terminal .-20mA to +20mA

Continuous Power Dissipation (Multilayer Board) (T_A = 70°C, derate 11.91mW/°C above +70°C) 952.8mW

Operating Temperature Range .... -40°C to +85°C

Junction Temperature .... +150°C

Storage Temperature Range .... -40°C to +150°C

Soldering Temperature (reflow).................................. +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

9 WLP

Package Code	W91R1+1
Outline Number	21-100389
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	83.98°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layerboard. For detailed information on package thermal considerations see www.maxim-ic.com/thermal-tutorial.

Electrical Characteristics

(T_A = -40°C to +85°C, V_{CC} = +3.4V to +5.5V, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CCINT} (V_{CCINT_MASTER} = BAT, V_{CCINT_SLAVE} = PLC if V_{PLC} > V_{PLC_DET}, otherwise V_{CCINT} = BAT)						
V_{CCINT} POR Threshold	V_{CCINT_POR}	Rising and falling	1.7	2.15	2.4	V
V_{CCINT} POR Threshold Hysteresis	V_{CCINT_PORH}			166		mV
V_{CC}						
Input Supply Voltage Range	V_{CC}	Supply range to operate PLC	3.4		5.5	V
V_{CC} Shutdown Current	I_{CC_SHDN}	V_{CC} = +5.0V, $\overline{EN}$ = 1			1	μA
V_{CC} Supply Current	I_{CC}	V_{CC} = +5.0V, $\overline{EN}$ = 0, V_{BAT} = +3.6V, master in slave found charging state, PLC unconnected		28.5	50	μA
BAT						
Input Supply Voltage Range	V_{BAT}	Master/slave mode	2.8		5.5	V
BAT Shutdown Current	I_{BAT_SHDN}	V_{CC}/V_{PLC} = 0, V_{BAT} = +3.6V, $\overline{EN}$ = 1, Device in Low Power Shutdown		0.8	2.1	μA
BAT Supply Current	I_{BAT}	V_{BAT} = +3.6V, $\overline{EN}$ = 0, PLC unconnected, master in slave detection state		4	9	μA

(T_A = -40°C to +85°C, V_{CC} = +3.4V to +5.5V, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		PLC = 0, V_{BAT} = +3.6V, $\overline{EN}$ = 0, slave in master detection state		0.7	2	
		V_{CC} = +5.0V, V_{BAT} = +3.6V, $\overline{EN}$ = 0, master only, slave found charging state, PLC unconnected		75	115	
		V_{PLC} = +5.0V, $\overline{EN}$ = 0, slave in master found PLC communication enabled state, LDO enabled		1	2	
		Slave in idle state, V_{PLC} = +3.6V, V_{BAT} = +4.2V, V_{CC} unconnected		0.6	1.4	
Recharge Voltage Threshold Range	V_{BAT_RECHG}	Programmable in 200mV steps through bits BAT_RECHG[2:0] of register 0x03; if V_{BAT} < V_{BAT_RECHG}, a device in slave idle state automatically transitions to master detection state		3 to 4.4		V
Recharge Threshold Voltage Accuracy	V_{RECHG_ACC}		-8		+8	%
PLC						
Input Supply Voltage Range	V_{PLC}	Supply range to operate PLC	3.4		5.5	V
PLC Shutdown Current	I_{PLC_SHDN}	Slave only, $\overline{EN}$ = 1, V_{PLC} = +3.6V, V_{BAT} = +3.4V, V_{CC} unconnected		3	6.5	µA
PLC Supply Current	I_{PLC}	V_{PLC} = +5.0V, $\overline{EN}$ = 0, slave only, LDO enabled, master found communication enabled state, PLC communication not ongoing		160	270	µA
PLC Supply Current	I_{PLC}	Slave in slave idle state, $\overline{EN}$ = 0, V_{PLC} = +3.6V, V_{BAT} = +4.2V, V_{CC} unconnected		3.4	7	µA
PLC Detection Threshold	V_{PLC_DET}	Slave only, V_{PLC} rising		2.5		V
Short-Circuit Detection Threshold	V_{PLC_SHT}	Master only, V_{PLC} falling		2.4		V
Short Detection Blanking Time	t_{SHT_BLK}			2.5		ms
V_{CC} – PLC						
PLC Logic Threshold ($\|V_{PLC\_PEAK} - V_{PLC}\|$)	V_{COM_DET}	COM_THRS [1:0] = 00	38	50	62	mV
		COM_THRS [1:0] = 01	53	65	77	
		COM_THRS [1:0] = 10	68	80	92	
		COM_THRS [1:0] = 11	88	100	112	
Q1, Q2 SWITCH						
Q1, Q2 R_{ON}	R_{ON_Q1Q2}	V_{CC} = 5V		72	110	mΩ
Q2 R_{ON}	R_{ON_Q2}	450mA	0.46	0.53	0.65	Ω
Q1 LDO						
LDO Output Voltage	V_{LDO}	Slave only, LDO_RNG = 0, V_{PLC} = 5V, V_{BAT} = 3.4V, I_{LOAD} = 200mA, MAX[V_{BAT} + DV, V_{MIN}], where VMIN is set by V_LDO_MIN[2:0] and DV is set by	-2%		+2%	V

(T_A = -40°C to +85°C, V_{CC} = +3.4V to +5.5V, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

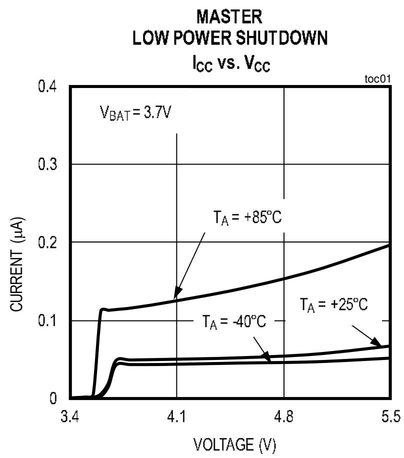
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		D_LDO_BAT[2:0] with D_LDO_BAT[2:0] != 000.				
		Slave only, LDO_RNG = 1, V_{PLC} = 5.5V, V_{BAT} = 3.4V, I_{LOAD} = 200mA, LDO output = V_{MIN}, where V_{MIN} ranges from 4.4V to 5.1V set by V_LDO_MIN[2:0] with D_LDO_BAT[2:0] != 000.	-2%		+2%	
LDO PSRR	$PSRR_{LDO}$	Ripple induced by a PLC square wave current, minimum LDO drop = 200mV, LDO load current = 200mA, ripple frequency 1/TU min, rising and falling edge at 200ns		-20		dB
LDO Load Regulation	$LOADR_{LDO}$	Load from 0mA to 200mA		100		µV
LDO Input Line Regulation	$LINER_{LDO}$	V_{PLC} from 3.4V to 5.5V, load = 200mA		620		µV
DEVICE CONFIGURATION (R_{SEL})						
RSEL Config 1 Threshold	R_{SEL1}				4.581	kΩ
RSEL Config 2 Threshold	R_{SEL2}		5.864	6.65	7.677	kΩ
RSEL Config 3 Threshold	R_{SEL3}		9.289	10.2	11.347	kΩ
RSEL Config 4 Threshold	R_{SEL4}		13.301	14.3	15.613	kΩ
RSEL Config 5 Threshold	R_{SEL5}		17.966	19.1	20.667	kΩ
RSEL Config 6 Threshold	R_{SEL6}		23.491	24.9	26.662	kΩ
RSEL Config 7 Threshold	R_{SEL7}		30.046	31.6	33.599	kΩ
RSEL Config 8 Threshold	R_{SEL8}		37.631			kΩ
POWERLINE COMMUNICATION						
Time Unit	t_{UNIT}	I²C programmable		24		µs
PLC Current Sink	I_{PLC_SNK}	PLC_SINK = 00		200		mA
		PLC_SINK = 01		244		
		PLC_SINK = 10		288		
		PLC_SINK = 11		355		
DYNAMIC						
Device Identification Ready Time	t_{ID}	From BAT (master) or PLC (slave) above POR threshold to RSEL_DONEi (0x07[4]) bit set		3	3.48	ms
General Timing Accuracy	t_{ACC}		-16		+16	%
DIGITAL SIGNALS (SDA, SCL, $\overline{INT}$, $\overline{EN}$)						
Input Logic-High	V_{IH}		1.4			V
Input Logic-Low	V_{IL}				0.4	V

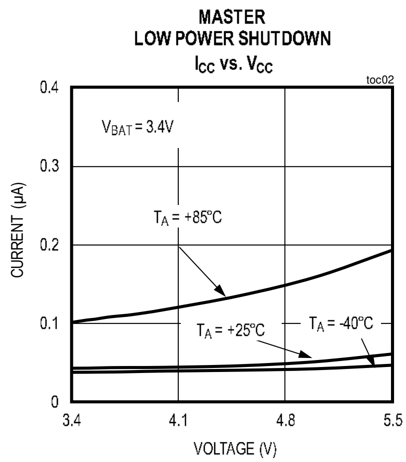
(T_A = -40°C to +85°C, V_{CC} = +3.4V to +5.5V, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

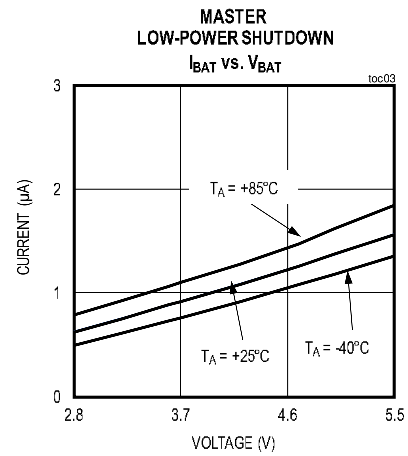
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IN_LKG}	$\overline{EN}$, SCL	-1		+1	µA
Output Logic-High Leakage Current (Open Drain)	I_{OH_LKG}	V_{IO} = 5.5V, SDA and $\overline{INT}$			1	µA
Output Logic-Low	V_{OL}	I_{SINK} = 20mA			0.4	V
I²C TIMING (Figure 4)						
I²C Serial Clock Frequency	f_{SCL}			400		kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
START Condition (Repeated) Hold Time	$t_{HD:STA}$		0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}		50			ns
ESD PROTECTION						
PLC		Human Body Model		±30		kV
		IEC 61000-4-2 Air-Gap		±3		
		IEC 61000-4-2 Contact Discharge		±10		
All Other Pins		Human Body Model		±2		kV
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}	Low to high		130		°C
Thermal Hysteresis	T_{HYS}	High to low		20		°C

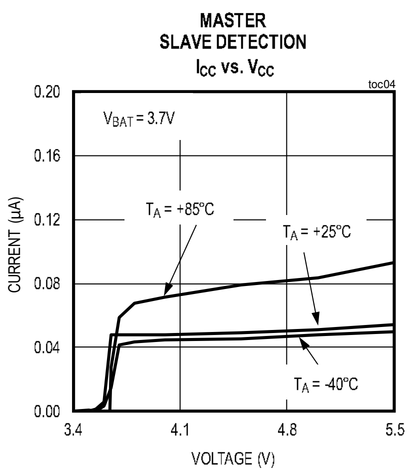
Note 1: All devices are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

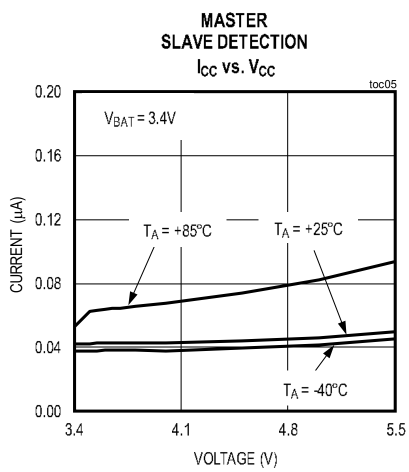
Typical Operating Characteristics

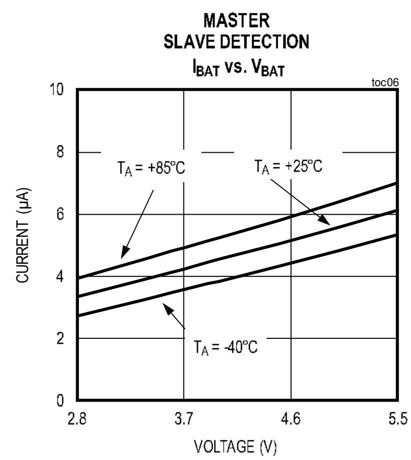


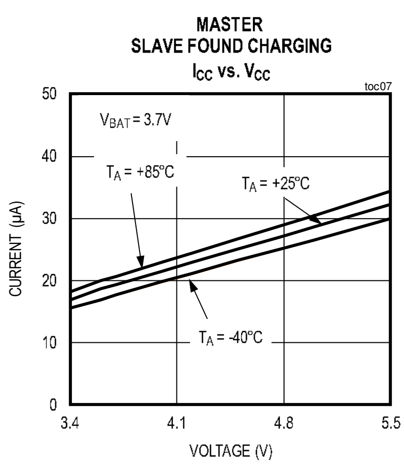


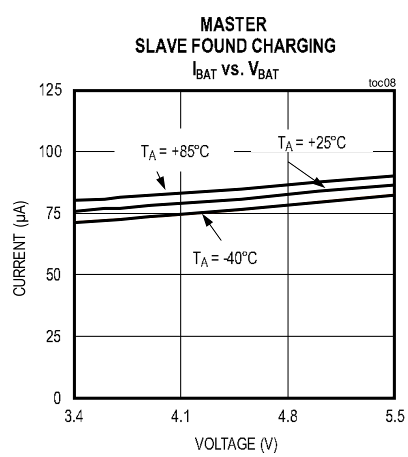


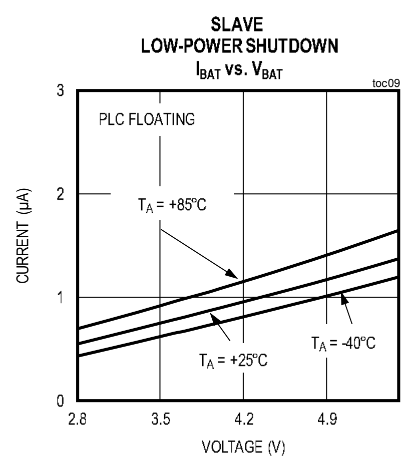




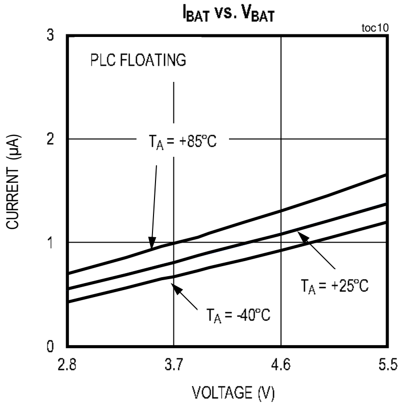




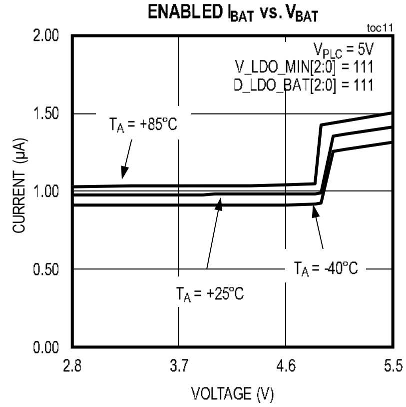




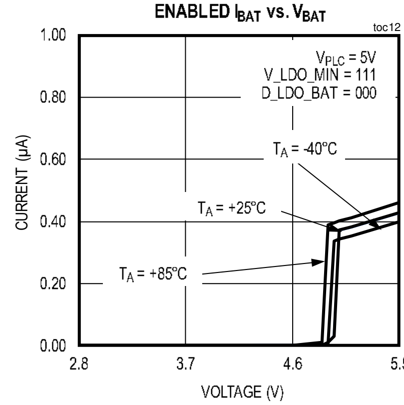
SLAVE MASTER DETECTION I_{BAT} vs. V_{BAT}



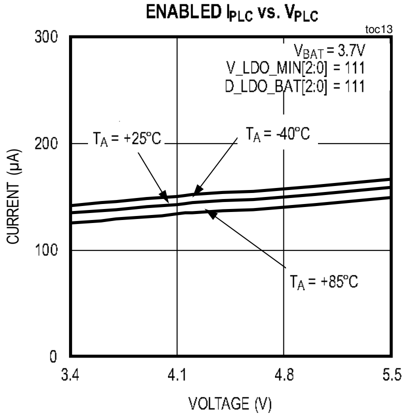
SLAVE MASTER FOUND COMMUNICATION ENABLED I_{BAT} vs. V_{BAT}



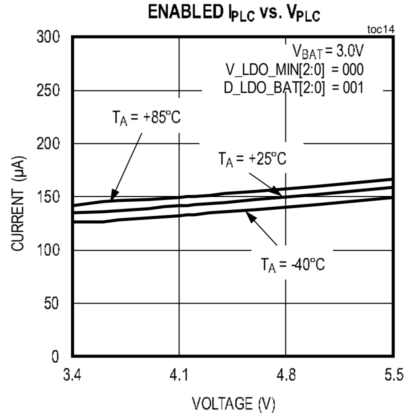
SLAVE MASTER FOUND COMMUNICATION ENABLED I_{BAT} vs. V_{BAT}



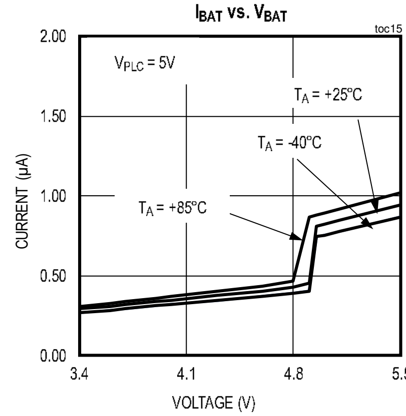
SLAVE MASTER FOUND COMMUNICATION ENABLED I_{PLC} vs. V_{PLC}



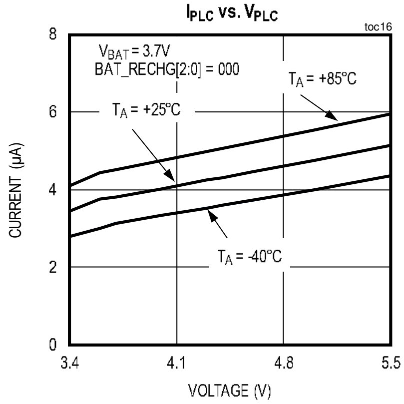
SLAVE MASTER FOUND COMMUNICATION ENABLED I_{PLC} vs. V_{PLC}



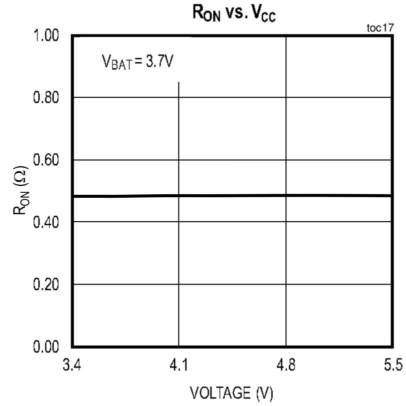
SLAVE IDLE I_{BAT} vs. V_{BAT}



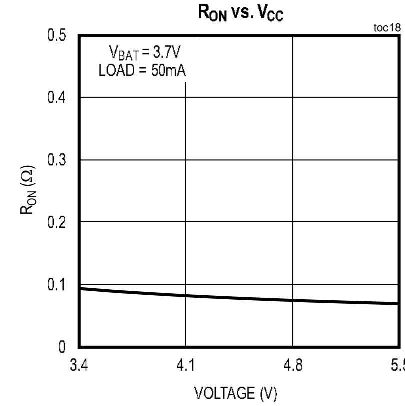
SLAVE IDLE I_{PLC} vs. V_{PLC}



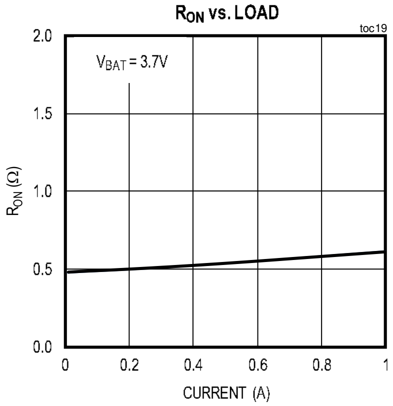
MASTER PLC MODE R_{ON} vs. V_{CC}



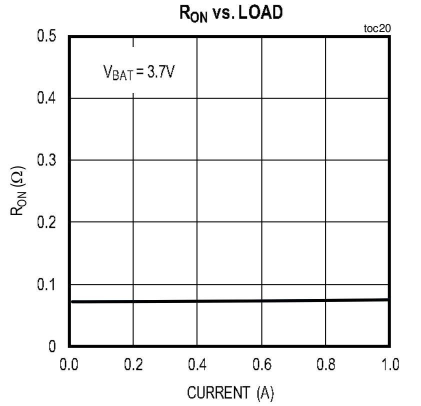
MASTER SLAVE FOUND CHARGING R_{ON} vs. V_{CC}



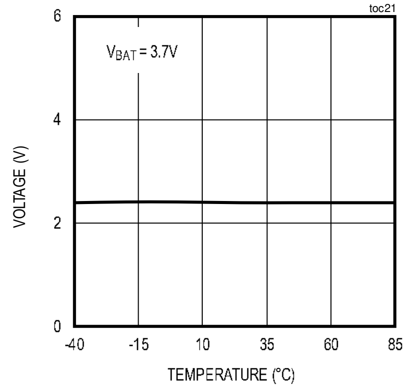
MASTER PLC MODE R_{ON} vs. LOAD



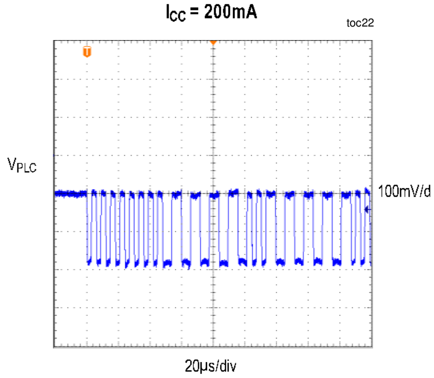
MASTER SLAVE FOUND CHARGING R_{ON} vs. LOAD



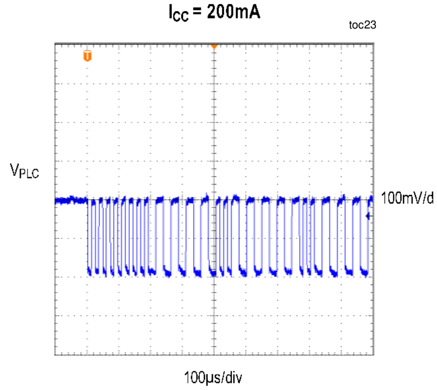
SHORT CIRCUIT DETECTION THRESHOLD



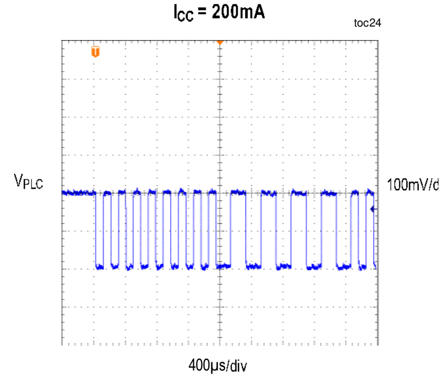
DATA TRANSMISSION FREQ[1:0] = 00, PLC_SINK[1:0] = 10, I_{CC} = 200mA



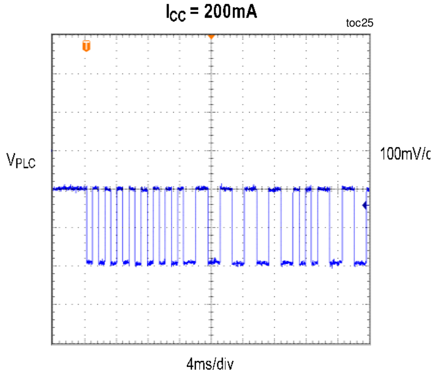
DATA TRANSMISSION FREQ[1:0] = 01, PLC_SINK[1:0] = 10, I_{CC} = 200mA



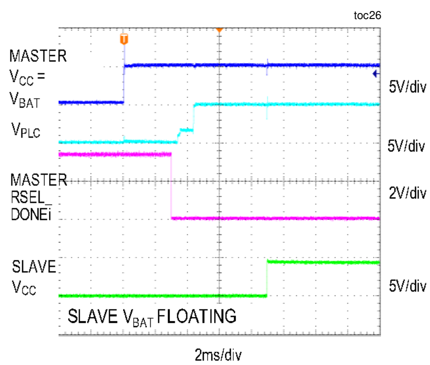
DATA TRANSMISSION FREQ[1:0] = 10, PLC_SINK[1:0] = 10, I_{CC} = 200mA



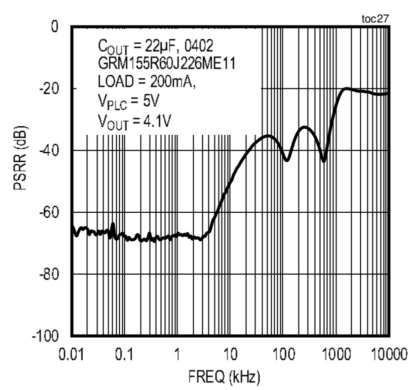
DATA TRANSMISSION FREQ[1:0] = 11, PLC_SINK[1:0] = 10, I_{CC} = 200mA

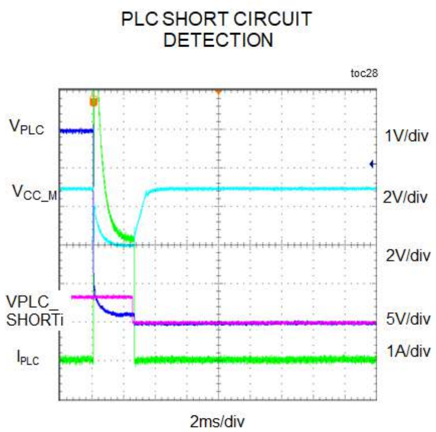


POWER-ON

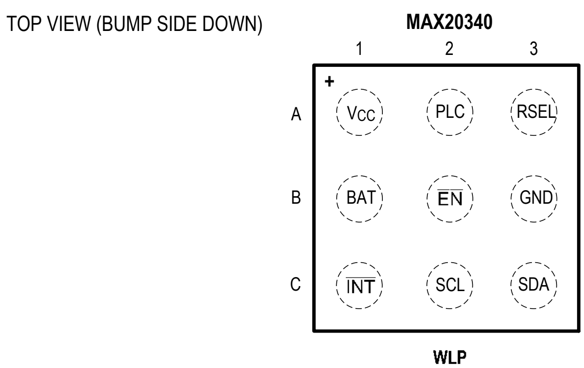


LDO PSRR





Pin Configuration



Pin Descriptions

PIN	NAME	FUNCTION
A1	V_{CC}	Supply Voltage Input (Master). LDO output, bypass V_{CC} to ground with a 10µF capacitor (Slave).
A2	PLC	PLC Master Output or PLC Slave Input
A3	RSEL	Resistor Programming Input. Connect a resistor of desired value based on Table 1 to configure I^2C address, master/slave mode, PLC mode (master only) and PLC slave address (slave only).
B1	BAT	Battery Connection. Connect to system battery and bypass with a 1µF capacitor to GND.
B2	$\overline{EN}$	Active-Low Enable Input. Drive $\overline{EN}$ pin high to place the MAX20340 in a low-power shutdown mode. Note that the EN bit of register 0x01[0] can still be used to exit the low-power shutdown mode even if the $\overline{EN}$ pin is high.
B3	GND	Ground
C1	$\overline{INT}$	Active-Low Open-Drain Interrupt Output. Connect $\overline{INT}$ to IO supply through a pullup resistor.
C2	SCL	I^2C Clock Input
C3	SDA	I^2C Data Input/Output

Detailed Description

The MAX20340 is a universal bidirectional DC powerline (PLC) communication management IC with a 166.7kbps maximum bit rate. The device is capable of a maximum of 1.2A charge current.

The MAX20340 features a slave detection circuit that flags an interrupt to the system when the PLC master detects the presence of a PLC slave on the power line. This function allows the system to remain in a low power state until a slave device is connected. Many of the features of the MAX20340, such as master/slave mode, I^2C address, dual/single PLC slave mode, and PLC slave address, are pin configurable.

Device Configuration

After power-on reset (POR), the master/slave mode, PLC slave address (slave only), PLC slave address mode (master only) and I^2C address are configured based on the value of the RSEL resistor. The configuration status can be queried by reading I2C_ADD and PS_ADD bits of the register 0x05.

Table 1. RSEL Configuration

RESISTOR VALUE (kΩ)	DEVICE MODE	PLC SLAVE ADDRESSING MODE	PLC SLAVE ADDRESS (PS_ADD)	I^2C ADDRESS
< 4.581	Master	Single	X	0010101
6.65	Master	Single	X	1101010
10.2	Master	Dual	X	0010101
14.3	Master	Dual	X	1101010
19.1	Slave	X	0	0010101
24.9	Slave	X	0	1101010
31.6	Slave	X	1	0010101
> 37.631	Slave	X	1	1101010

Device Initialization

After POR, the device starts by checking the resistor present on the RSEL pin. It is recommended to have the OTP bit RSEL_DONEm (0x08[4]) default high so that an interrupt occurs at the end of this RSEL identification phase. As an alternative to detecting the interrupt, the user can also choose to wait 3ms or more after POR to give enough time for RSEL to be properly identified. The I^2C interface cannot be used until RSEL identification is complete because RSEL defines also the I^2C slave address. With RSEL identified, the PLC master/slave mode, the I^2C slave address, the number of PLC slaves (master mode), and the PLC slave address (slave mode) are automatically configured. The configuration result can be determined through bit PS_ADD (0x05[0]). The user can also read bits FSM_STAT[2:0] (0x05[4:2]) to determine whether the MAX20340 is configured as a master or a slave. If the MAX20340 is configured as a PLC master, see the *Master Mode Operation* section for more details. Otherwise, see the *Slave Mode Operation* section for PLC slave operation details. Figure 1 shows the flow chart for transmitting 3 bytes from the PLC master and receiving the response from the PLC slave. It assumes that all relevant interrupts have been unmasked.

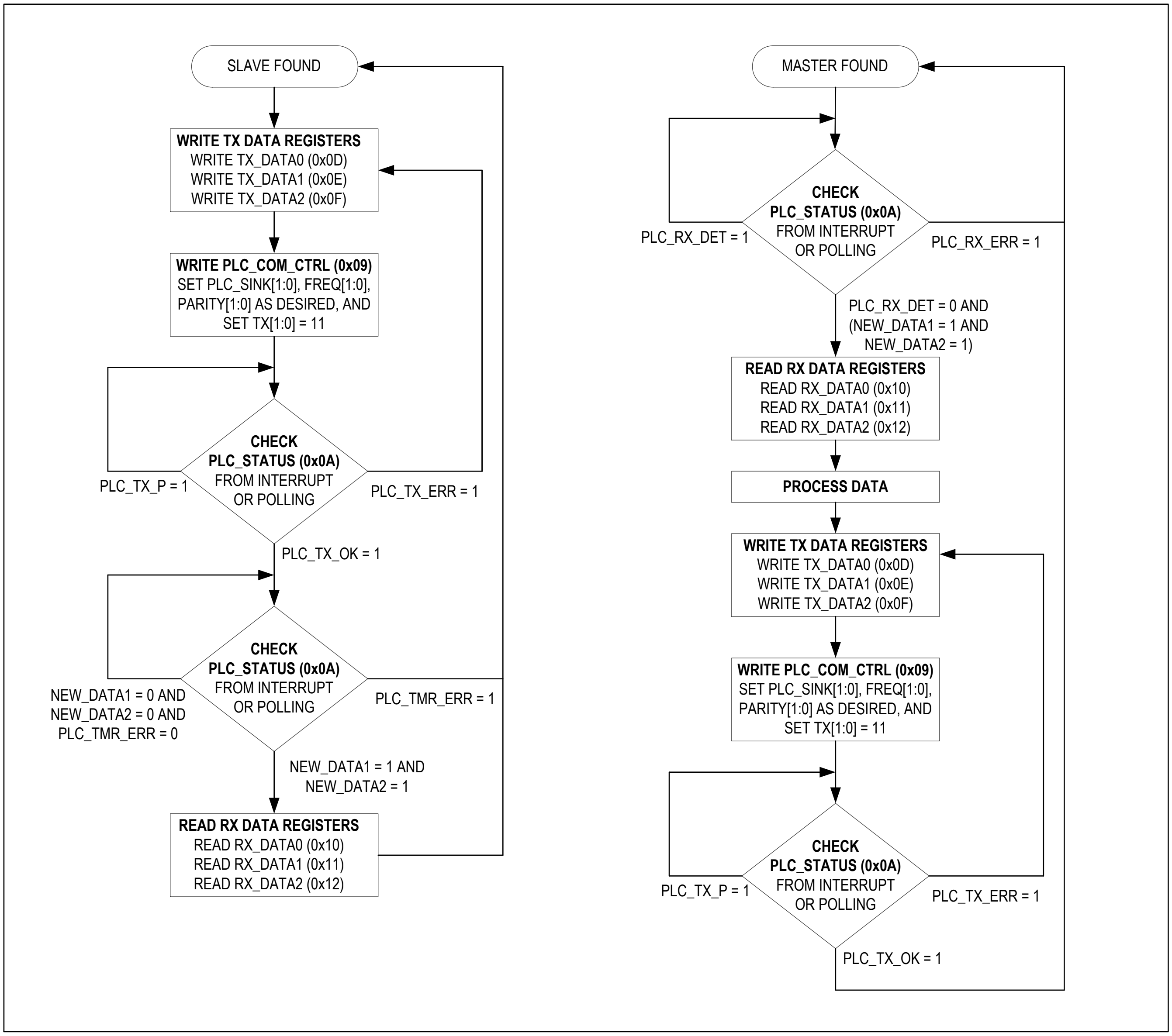


Figure 1. Flow Chart for Transmitting 3 Bytes

Master Mode Operation

After the RSEL and master mode identifications, the MAX20340 stays in the master low-power shutdown mode as long as $\overline{EN}$ input is high and EN bit of register 0x01[0] is 0. When $\overline{EN}$ is driven low or EN bit is set to 1, the device transitions to the slave detection state. The user can unmask the FSM_STATi interrupt (0x08[0]) to be notified of any change of master FSM (finite state machine) state through the $\overline{INT}$ pin. When a slave is detected as described in the *PLC Master and Slave Detection* section, the state machine transitions to the slave found state. In this state, both the Q1 and Q2 switches are on to provide a low-resistance charging path between V_{CC} and PLC pins with a 1.2A maximum charge current on the PLC line. In the slave found state, PLC communication can be initiated by the PLC master using the following procedure:

Set PLC_STATm bit of the DEV_STATUS_MASK (0x08) register to 1 to unmask the PLC_STAT interrupts. Then unmask the PLC interrupts in the PLC_IRQ register (0x0B) and the PLC_MASK (0x0C) register.

Load the bytes to be transmitted into TX_DATAx registers (0x0D, 0x0E, and 0x0F).

Select the desired slave response time through the TWAIT_TMR (0x02[1:0]) bit or leave it at the default setting.

Choose the desired PLC speed through the FREQ[1:0] (0x09[5:4]) bit, the parity through the PARITY[1:0] (0x09[3:2]) bit, and the PLC sink current through the PLC_SINK[1:0] (0x09[7:6]) bit. Write 01 into TX[1:0] (0x09[1:0]) to send one byte, 10 to send two bytes, or 11 to send three bytes. The checksum is automatically calculated by the MAX20340 and appended after the actual data bytes.

The master state machine transitions automatically to PLC mode and starts sending data.

If the transmission is completed without errors, PLC_TX_OKi (0x0B[5]) goes high. Otherwise, PLC_TX_ERRi (0x0B[6]) goes high instead.

If the PLC slave responds within the time specified by the Rx wait timer bits 0x02[1:0], the received data are available in the RX_DATAx registers (0x10, 0x11, and 0x12). The response includes one, two, or three bytes plus the checksum. If the response is received without errors, NEW_DATA2i (0x0B[1]) or NEW_DATA1i (0x0B[2]) bits (or both at the same time) are high. In case of parity, checksum or any other error, PLC_RX_ERRi (0x0B[3]) goes high and the new data is not be updated in RX_DATAx.

The master state machine switches automatically between PLC mode and slave found states based on the PLC communication requirements.

Slave Mode Operation

After RSEL and slave mode identification, the MAX20340 stays in the slave low-power shutdown mode as long as $\overline{EN}$ input is high and the EN bit of register 0x01[0] is 0. When $\overline{EN}$ is driven low or EN bit is set to 1, the device transitions to master detection state. The user can unmask the FSM_STATi interrupt using FSM_STATm (0x08[0]) to notify through the $\overline{INT}$ pin when any change of state occurs. When a master is detected as described in the *PLC Master and Slave Detection* section, the state machine switches to master found state. In this state, PLC communication is enabled. The detected PLC master is always the one that initiates the communication by sending one, two or three data bytes. When the PLC slave detects the beginning of a valid PLC communication, PLC_RX_DETi (0x0B[0]) becomes high. If the packet is received without errors, NEW_DATA2i (0x0B[1]) or NEW_DATA1i (0x0B[2]) bits (or both at the same time) becomes high and the received data are available in the RX_DATAx registers (0x10, 0x11, and 0x12). The PLC slave can be switched from master found state to slave idle state by setting SLAVE_TO_IDLE (0x04[3]) to 1.

In the master found state, use the following procedure to control the PLC slave for PLC communication:

Set PLC_STATm bit of the DEV_STATUS_MASK (0x08) register to 1 to unmask PLC_STAT interrupts. Then unmask the PLC interrupts in the PLC_IRQ register (0x0B) through the PLC_MASK (0x0C) register.

Configure the slave to match the PLC speed (FREQ[1:0]) and parity (PARITY[1:0]) of the master through the PLC_COM_CTRL register (0x09).

When ongoing PLC communication is detected, the PLC slave indicates that by setting PLC_RX_DETi (0x0B[0]) to high. After that, wait for the assertion of interrupts NEW_DATA2i (0x0B[1]) or NEW_DATA1i (0x0B[2]) indicating that the received data is available in the RX_DATAx registers. In case of parity, checksum or any other error, PLC_RX_ERRi (0x0B[3]) is high and the new data is not updated in the RX_DATAx registers.

To respond to the PLC master after processing the received data, load the bytes to be transmitted into the slave's TX_DATAx registers (0x0D, 0x0E, and 0x0F).

Write 01 into TX[1:0] bits (0x09[1:0]) to send just one byte, 10 to send two bytes, or 11 to send three bytes. The checksum is automatically calculated by the MAX20340 and appended after the actual data bytes.

PLC Master and Slave Detection

When the PLC master is in slave detection state, its PLC line is pulled up to BAT through an internal 8.4kΩ (typical) resistor. If a PLC slave is attached, the PLC line is pulled below the V_{PLC_SHT} threshold by the clamp circuit of the slave. Once the master detects that V_{PLC} is less than V_{PLC_SHT}, it enters the slave found charging state, disconnects the 8.4kΩ internal pullup resistor, and closes the power switch between V_{CC_M} (V_{CC} of the master) and PLC line.

After the master enters the slave found charging state, the power source (e.g., a buck-boost regulator) providing V_{CC_M} needs to be enabled (if not already) to pull V_{PLC} above V_{PLC_DET} within the short-circuit detection blanking time t_{SHT_BLK}. Failing to do so causes the master to leave the slave found charging state and enter the safe state. The application processor (AP) can unmask FSM_STATi interrupt to be notified of the slave found charging state change event through the $\overline{INT}$ pin so that it can enable the power source before t_{SHT_BLK} elapses. With the master now in the slave found charging, the slave detects that V_{PLC} is above V_{PLC_DET} and enters the master found communication enabled state. This completes the PLC master and slave detection.

After a slave is detected, there is no build-in mechanism for the master to detect when the slave is detached. This means that the master stays in the slave found charging state even if the slave is removed. Therefore, the master AP should poll the slave intermittently through PLC and set DET_RST to 1 to return to the slave detection state based on the polled result.

Dual Slave Configuration

When an MAX20340 PLC master interfaces with two MAX20340 PLC slaves in the dual slave configuration, both PLC slaves should be configured to have a different PLC slave address using different RSEL values according to Table 1. The configured PLC slave address can be determined by reading bit PS_ADD (0x05[0]). When the PLC master intends to send a packet to one of the PLC slaves, the PLC slave address of the intended recipient should be embedded in the data bytes. The user has the flexibility to assign the PLC slave address to any bit of the data bytes. Since both PLC slaves receive the same data, each slave's application processor is expected to extract the PLC slave address from the user-defined bit location in the PLC frame and compare it with the PLC slave address indicated by PS_ADD bit to determine which slave is the intended recipient. The intended slave then processes the data accordingly while the other slave simply discards the data.

LDO Operation

When the device is in PLC slave mode, the V_{CC} pin becomes the LDO output. The LDO has two output ranges selected by LDO_RNG. When LDO_RNG is 0, the output voltage on V_{CC} follows the battery voltage plus a voltage difference programmable by the D_LDO_BAT[2:0] (register 0x02[4:2]) until V_{CC} drops to a threshold programmable by V_LDO_MIN[2:0] (register 0x02[7:5]), in which case the MAX20340 keeps V_{CC} regulated at the voltage set by V_LDO_MIN[2:0].

When LDO_RNG is 1, the output voltage is always regulated at the voltage set by the V_LDO_MIN[2:0] regardless of V_{BAT}, provided that the LDO input (V_{PLC}) is above the output regulation voltage (V_{CC}).

The PLC slave can also operate in the LDO-bypassed mode. Regardless of the value of LDO_RNG, the V_{CC} output of the slave follows the V_{PLC} input voltage when D_LDO_BAT[2:0] is set to 000, effectively bypassing the LDO.

Charge Timer

When the MAX20340 is configured as a PLC master. The charge timer starts when the master state machine switches from the slave detection state to the slave found state. It continues counting without being interrupted or reset when the state machine switches back and forth between the slave found state and the PLC mode state. The charge timer is reset and stopped in the slave detection state and the master low-power shutdown state. The charge timer setting can be changed by CHG_TMR_SET[1:0] bits (0x03[5:4]). The charge timer status is reflected by CHG_TMRS[1:0] bits (0x05[7:6]).

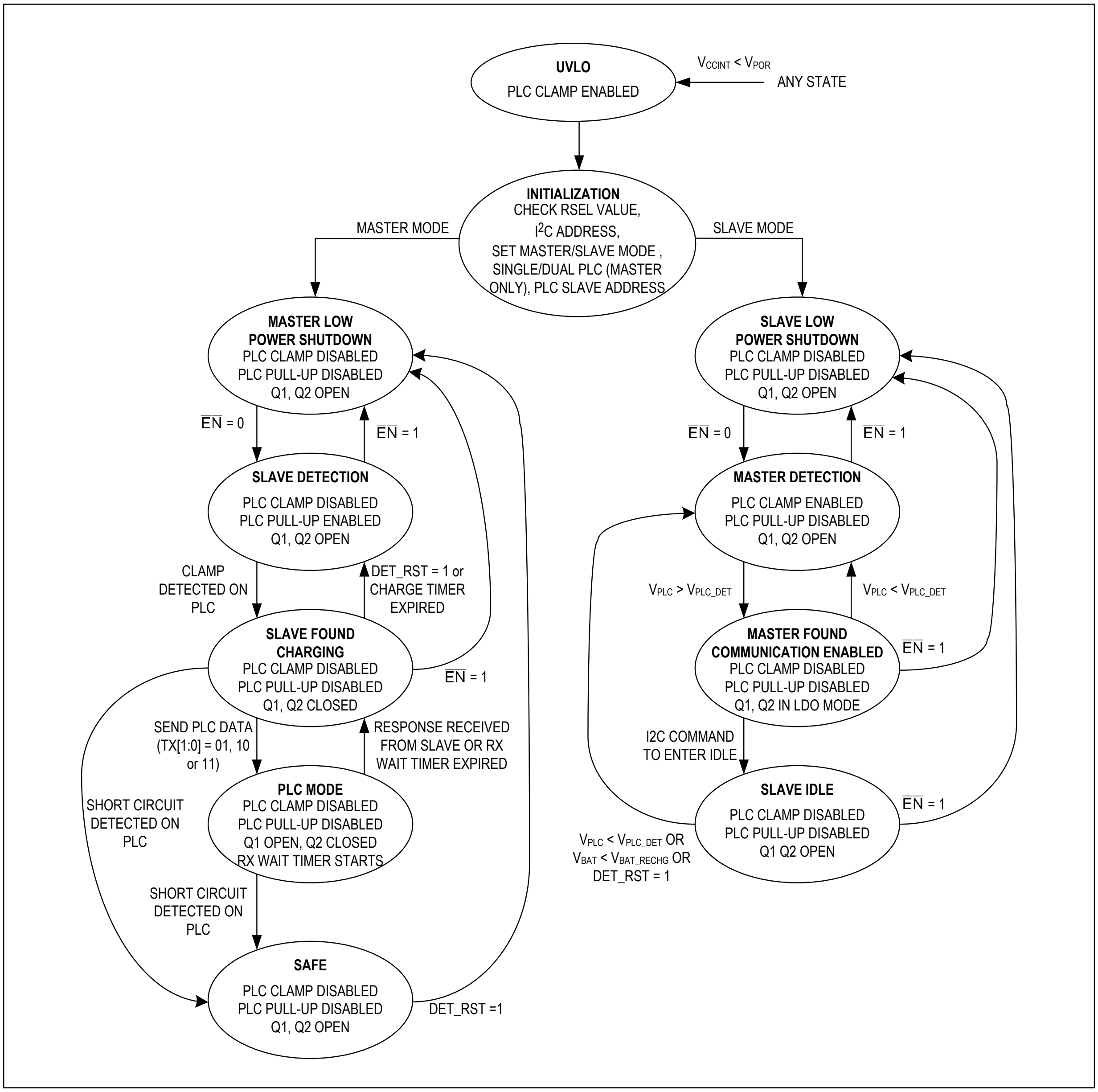


Figure 2. Master and Slave Mode Operation State Diagram

Thermal Shutdown

When the MAX20340 enters thermal shutdown, the Q1/Q2 switches are open and the THM_SHDNi interrupt bit (0x07[5]) becomes high while the master/slave state machines are not affected.

INT Interrupt Output

The MAX20340 interrupts can be unmasked to indicate to the application processor (AP) that the status of the MAX20340 has changed. The $\overline{\text{INT}}$ pin asserts low whenever one or more unmasked interrupts are toggled. The device has two read-only interrupt registers: DEV_STATUS_IRQ and PLC_IRQ. The DEV_STATUS_IRQ register indicates that the top-level block has an interrupt generated. PLC_IRQ is an additional interrupt register dedicated to the PLC block for indicating any change of the PLC communication status. The PLC_STATi bit in the DEV_STATUS_IRQ register goes high if any bit of the register PLC_IRQ is asserted.

$\overline{\text{INT}}$ goes high (cleared) after the last interrupt register that contains an active interrupt is read. All interrupts can be masked to prevent $\overline{\text{INT}}$ from being asserted through the DEV_STATUS_MASK and PLC_MASK registers. The DEV_STATUS1, DEV_STATUS2, and PLC_STATUS registers can still provide the actual interrupt status of the masked interrupts, but $\overline{\text{INT}}$ is not asserted. The interrupt structure is depicted in *Figure 3*.

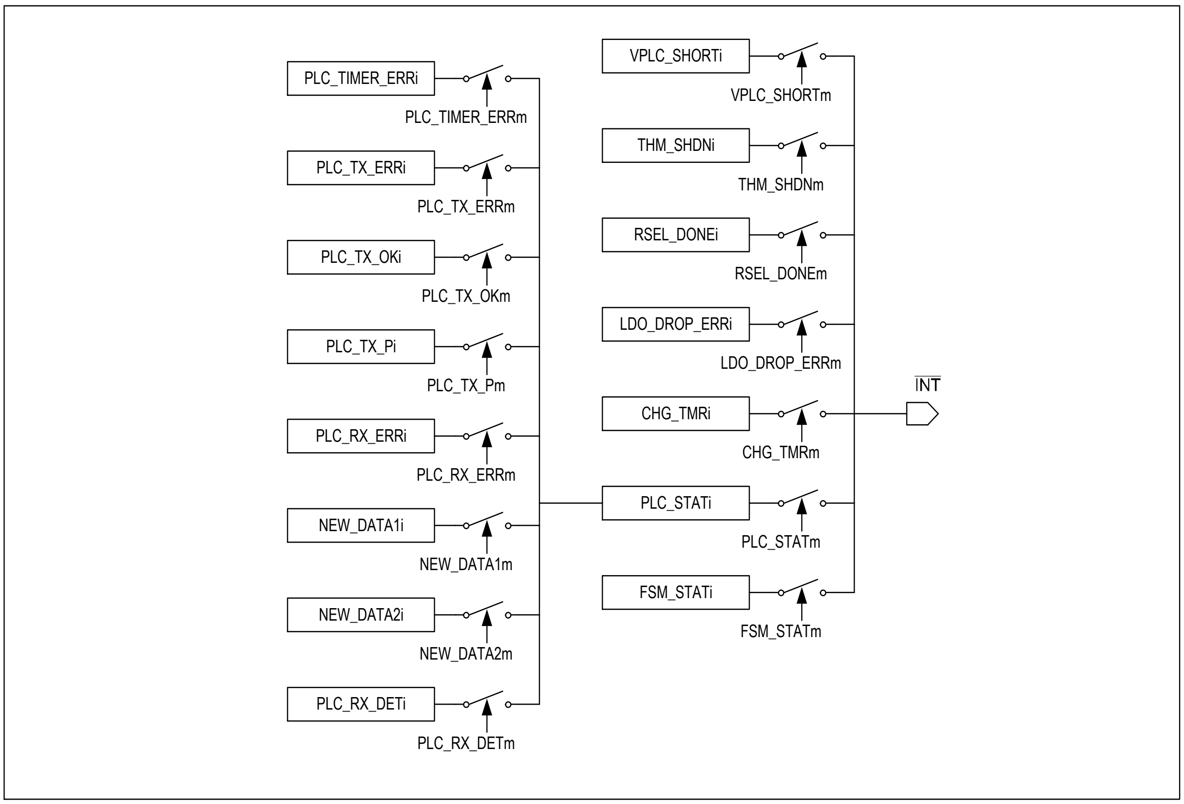


Figure 3. Interrupt Structure

I²C Interface

The device contains an I²C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

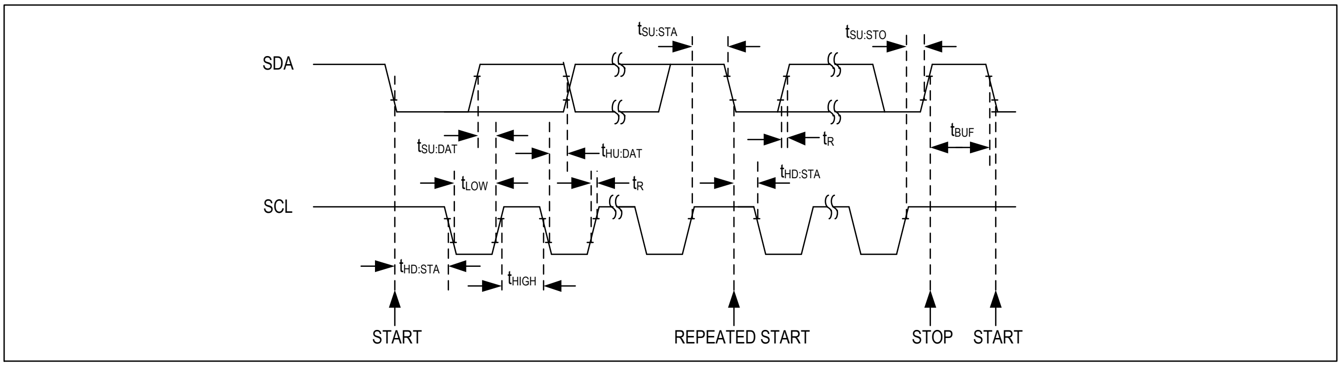


Figure 4. I²C Interface Timing

START, STOP, and REPEATED START Conditions

When writing to the device using I²C, the master sends a START condition (S) followed by the device I²C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I²C slave. See *Figure 5*.

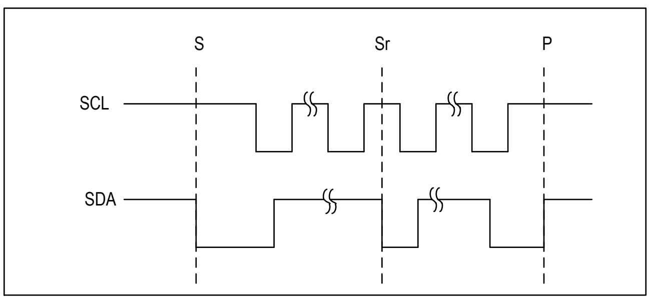


Figure 5. I²C START, STOP, and REPEATED START Conditions

Slave Address

Set the R/$\overline{W}$ bit high to configure the device to read mode. Set the R/$\overline{W}$ bit low to configure the device to write mode. The address is the first byte of information sent to the device after the START condition.

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals. See the START, STOP, and REPEATED START Conditions. Both SDA and SCL remain high when the bus is not active.

Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device (Figure 6). The following procedure describes the single byte write operation:

1) The master sends a START condition.
2) The master sends the 7-bit slave address plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends the 8-bit register address.
5) The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6) The master sends 8 data bits.

7) The slave asserts an ACK on the data line.
8) The master generates a STOP condition.

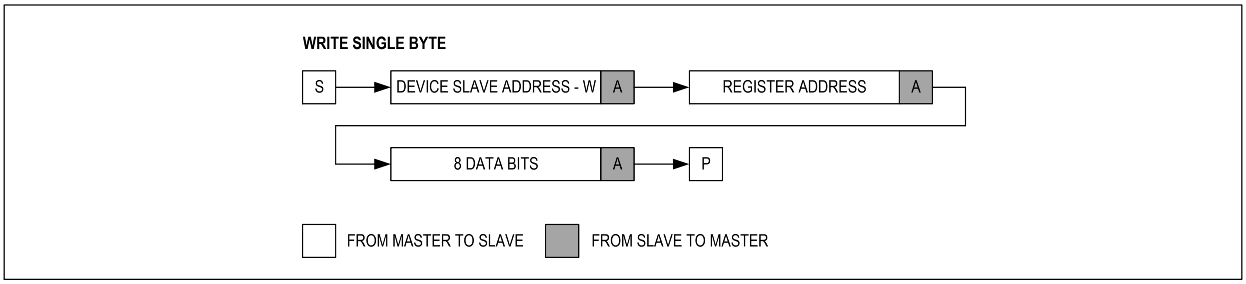


Figure 6. Write Byte Sequence

Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device (*Figure 7*). The slave device automatically increments the register address after each data byte is sent. The following procedure describes the burst write operation:

1) The master sends a START condition.
2) The master sends the 7-bit slave address plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends the 8-bit register address.
5) The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6) The master sends eight data bits.
7) The slave asserts an ACK on the data line.
8) Repeat steps 6 and 7 N - 1 times.
9) The master generates a STOP condition.

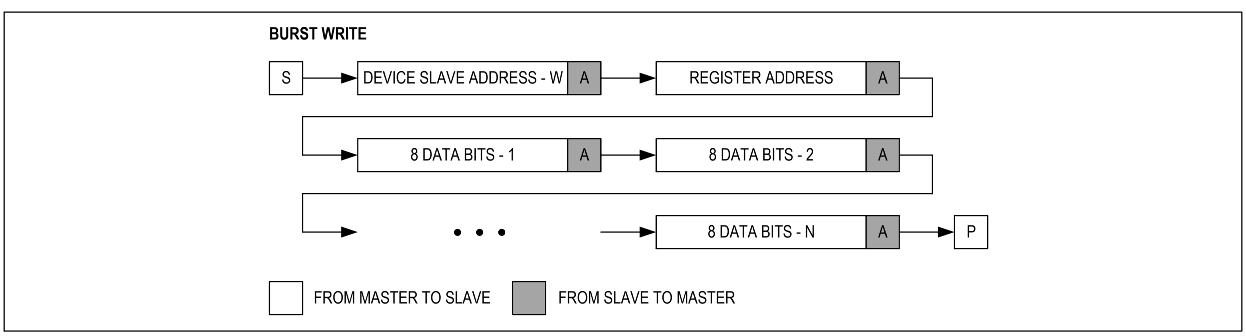


Figure 7. Burst Write Sequence

Single-Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (*Figure 8*). The following procedure describes the single-byte read operation:

The master sends a START condition.

1) The master sends the 7-bit slave address plus a write bit (low).
2) The addressed slave asserts an ACK on the data line.
3) The master sends the 8-bit register address.
4) The slave asserts an ACK on the data line only if the address is valid (NAK if not).
5) The master sends a REPEATED START condition.
6) The master sends the 7-bit slave address plus a read bit (high).
7) The addressed slave asserts an ACK on the data line.
8) The slave sends eight data bits.
9) The master asserts a NACK on the data line.
10) The master generates a STOP condition.

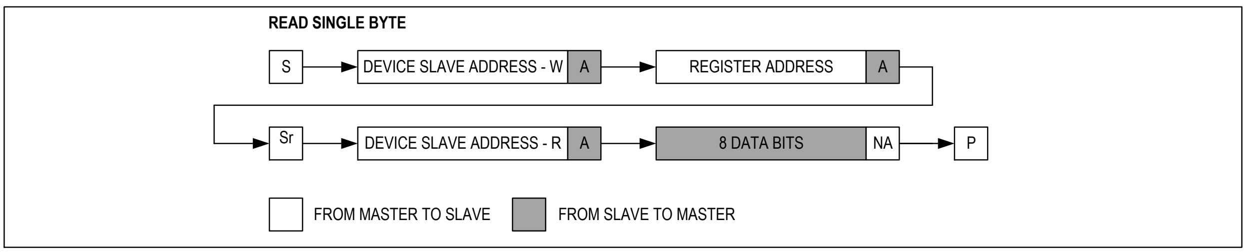


Figure 8. Read Byte Sequence

Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (*Figure 9*). The following procedure describes the burst-byte read operation:

1) The master sends a START condition.
2) The master sends the 7-bit slave address plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends the 8-bit register address.
5) The slave asserts an ACK on the data line only if the address is valid (NAK if not).
6) The master sends a REPEATED START condition.
7) The master sends the 7-bit slave address plus a read bit (high).
8) The slave asserts an ACK on the data line.
9) The slave sends eight data bits.
10) The master asserts an ACK on the data line.
11) Repeat steps 9 and 10 N - 2 times.
12) The slave sends the last eight data bits.
13) The master asserts a NACK on the data line.
14) The master generates a STOP condition.

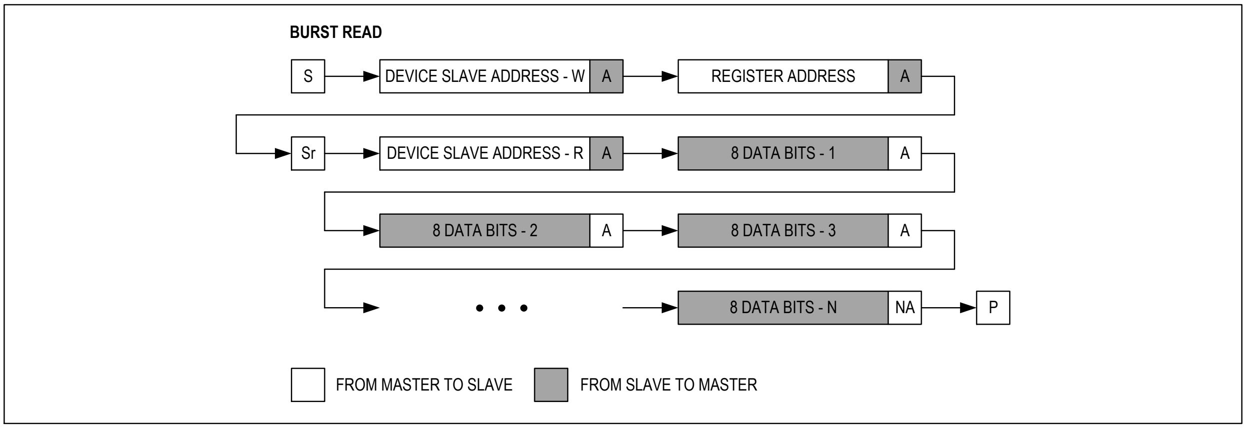


Figure 9. Burst Read Sequence

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the device generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (Figure 10). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

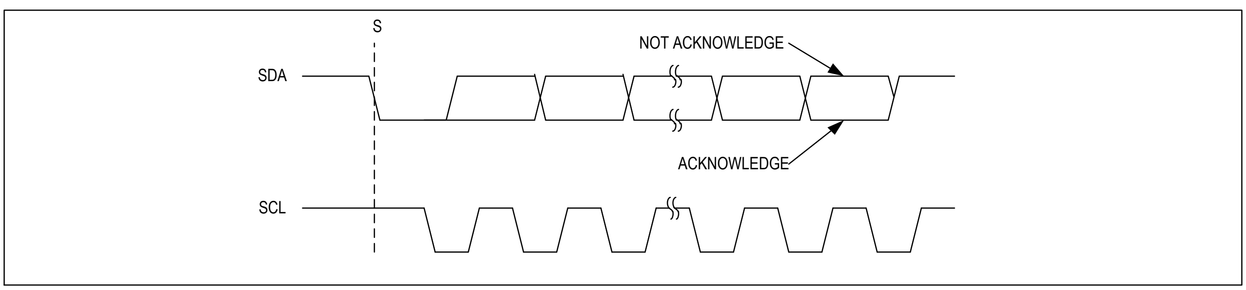


Figure 10. Acknowledge

Applications Information

Powerline Communication (PLC)

To communicate reliably over the PLC line, it is critical to keep V_{CC} of the master stable by minimizing the trace between V_{CC} and its voltage source. A voltage source with a good load transient, load regulation, and output ripple performance is recommended.

In addition, the capacitance present on the PLC can distort the PLC transmission waveform and therefore should be minimized. This is an important consideration when the LDO of the slave is in the dropout state (LDO_DROP = 1) or when the LDO is bypassed. In both cases, the output capacitance on the LDO output (V_{CC} of the PLC slave) is effectively affecting the PLC line and should therefore be minimized as well. Figure 11 illustrates the voltage waveform on the PLC line during a PLC transmission.

The time unit (t_{UNIT}) determines the PLC transmission speed. A time unit longer than 24µs can be selected in case the slave device, such as a battery charger in a wireless earbud, has poor PSRR performance.

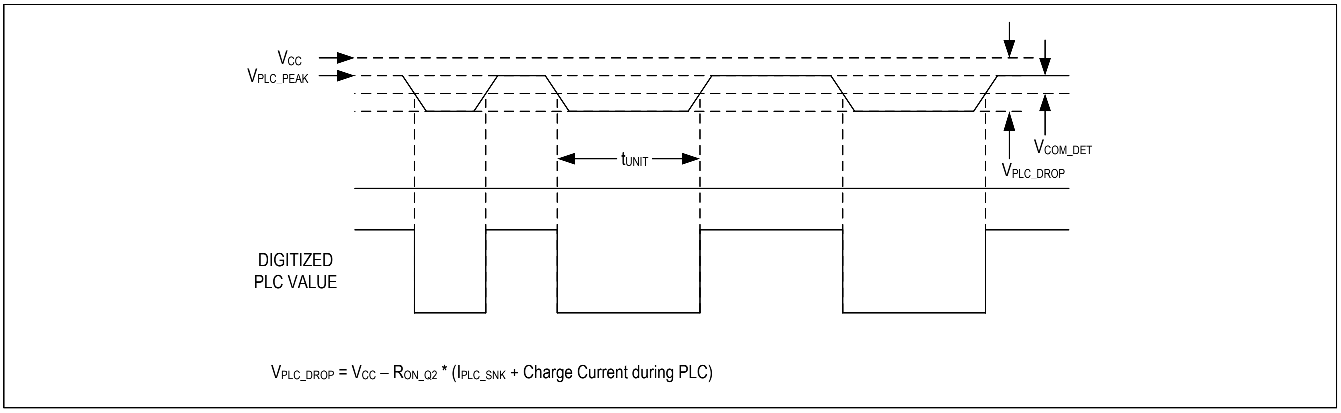


Figure 11. Powerline Communication Signal Waveform

High-ESD Protection

Electrostatic discharge (ESD)-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV Human Body Model (HBM) encountered during handling and assembly. PLC pin is further protected against ESD up to ±30kV (HBM), ±3kV (Air-Gap Discharge), and ±10kV (Contact Discharge) without damage. The ESD structures withstand high ESD in both normal operation and when the device is powered down. After an ESD event, the MAX20340 continues to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 12 shows the Human Body Model. *Figure 13* shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

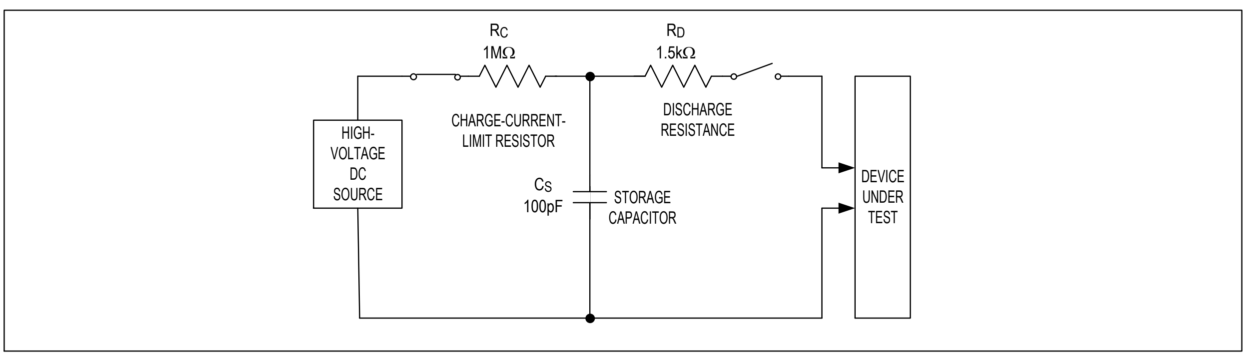


Figure 12. Human Body ESD Test Model

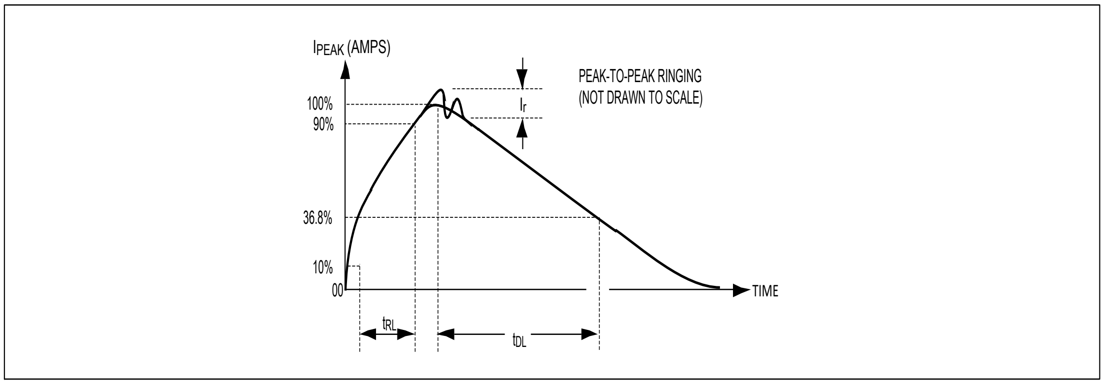


Figure 13. Human Body Current Waveform

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The MAX20340 is specified for ±3kV Air-Gap and ±10kV Contact Discharge IEC 61000-4-2 on the PLC pin.

The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (*Figure 14*), the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. *Figure 15* shows the current waveform for the ±6kV IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Contact Discharge method connects the probe to the device before the probe is energized.

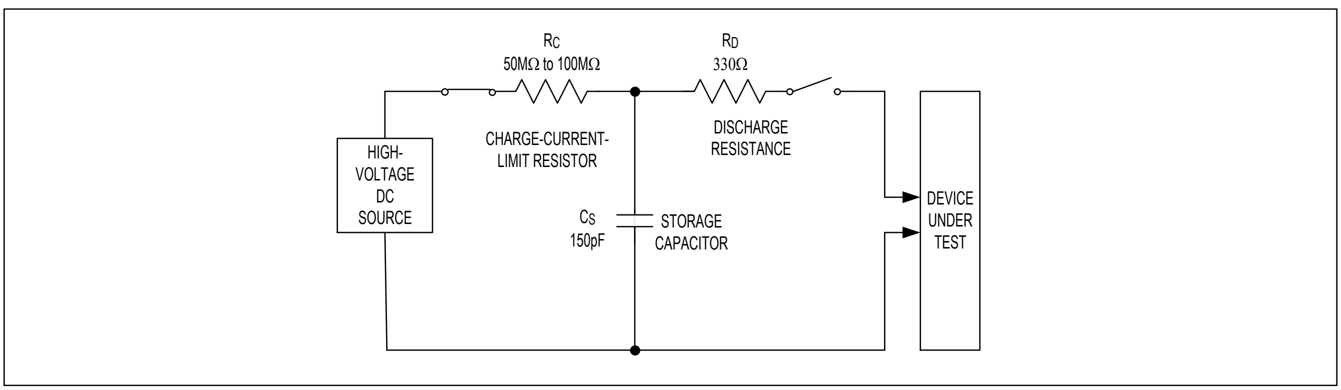


Figure 14. IEC61000-4-2 ESD Test Model

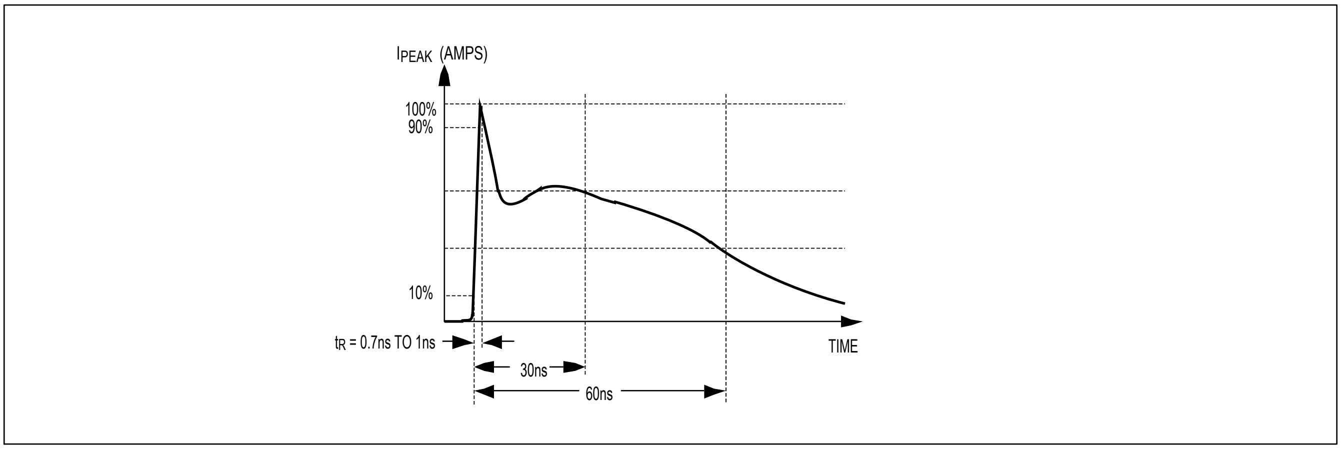


Figure 15. IEC61000-4-2 ESD Generator Current Waveform

Register Map

MAX20340

ADDRESS	NAME	MSB							LSB
I2C MAP									
0x00	DEVICE_ID[7:0]	CHIP_ID[3:0]				CHIP_REV[3:0]			
0x01	CONTROL1[7:0]	—	—	—	—	—	—	DET_RST	EN
0x02	CONTROL2[7:0]	V_LDO_MIN[2:0]			D_LDO_BAT[2:0]			TWAIT_TMR[1:0]	
0x03	CONTROL3[7:0]	COM_THRS[1:0]		CHG_TMR_SET[1:0]		LDO_RNG	BAT_RECHG[2:0]		
0x04	CONTROL4[7:0]	—	—	—	TXRX_RESET	SLAVE_TO_IDLE	—	—	TXFILT_ENB
0x05	DEV_STATUS1[7:0]	CHG_TMR_STAT[1:0]		PLC_STAT	FSM_STAT[2:0]			I2C_ADD	PS_ADD
0x06	DEV_STATUS2[7:0]	LDO_DROP	ENb	—	—	—	—	THM_SHDN	PLC_CMP_OUT
0x07	DEV_STATUS_IRQ[7:0]	—	VPLC_SHORTi	THM_SHDNi	RSEL_DONEi	LDO_DROP_ERRi	CHG_TMR_STATi	PLC_STATi	FSM_STATi
0x08	DEV_STATUS_MASK[7:0]	—	VPLC_SHORTm	THM_SHDNm	RSEL_DONEm	LDO_DROP_ERRm	CHG_TMRm	PLC_STATm	FSM_STATm

ADDRESS	NAME	MSB							LSB
0x09	PLC_COM_CTRL[7:0]	PLC_SINK[1:0]		FREQ[1:0]		PARITY[1:0]		TX[1:0]	
0x0A	PLC_STATUS[7:0]	PLC_TMR_ERR	PLC_TX_ERR	PLC_TX_OK	PLC_TX_P	PLC_RX_ERR	NEW_DATA1	NEW_DATA2	PLC_RX_DET
0x0B	PLC_IRQ[7:0]	PLC_TMRi	PLC_TX_ERRi	PLC_TX_OKI	PLC_TX_Pi	PLC_RX_ERRi	NEW_DATA1i	NEW_DATA2i	PLC_RX_DETi
0x0C	PLC_MASK[7:0]	PLC_TMRm	PLC_TX_ERRm	PLC_TX_OKm	PLC_TX_Pm	PLC_RX_ERRm	NEW_DATA1m	NEW_DATA2m	PLC_RX_DETm
0x0D	TX_DATA0[7:0]	TXDATA0[7:0]							
0x0E	TX_DATA1[7:0]	TXDATA1[7:0]							
0x0F	TX_DATA2[7:0]	TXDATA2[7:0]							
0x10	RX_DATA0[7:0]	RXDATA0[7:0]							
0x11	RX_DATA1[7:0]	RXDATA1[7:0]							
0x12	RX_DATA2[7:0]	RXDATA2[7:0]							

Register Details

DEVICE_ID (0x0)

BIT	7	6	5	4	3	2	1	0
Field	CHIP_ID[3:0]				CHIP_REV[3:0]			
Reset	0x1				0x1			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
CHIP_ID	7:4	CHIP_ID[3:0] shows information about the version of the MAX20340.
CHIP_REV	3:0	CHIP_REV[3:0} shows information about the revision of the MAX20340 silicon.

CONTROL1 (0x1)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	—	—	DET_RST	EN
Reset	0x1	0x1	0x1	0x0	0x0	0x0	0x0	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
—	7	Reserved. Used internally.	
—	6	Reserved. Used internally.	
—	5	Reserved. Used internally.	
—	4	Reserved. Used internally.	
—	3	Reserved. Used internally.	
—	2	Reserved. Used internally.	
DET_RST	1	Master/Slave Detection Reset	Writing a 1 to this bit will reset the FSM to the master/slave detection state.
EN	0	Device Enable. If the external pin /EN\ is low, this bit is ignored. If the external pin /EN\ is high, this bit can be used to enter or exit low-power shutdown mode by software rather than by driving EN.	0x0: Device enters low-power shutdown mode (both master and slave). 0x1: Device exits low-power shutdown mode.

CONTROL2 (0x2)

BIT	7	6	5	4	3	2	1	0
Field	V_LDO_MIN[2:0]			D_LDO_BAT[2:0]			TWAIT_TMR[1:0]	
Reset	0x7			0x0			0x1	
Access Type	Write, Read			Write, Read			Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
V_LDO_MIN	7:5	LDO Voltage Select. In slave mode, except when D_LDO_BAT[2:0] = 000, this sets the minimum allowed LDO output voltage, overriding D_LDO_BAT[2:0].	**LDO_RNG = 0** **LDO_RNG = 1** 0x0: 2.8V 4.4V 0x1: 2.9V 4.5V 0x2: 3.0V 4.6V 0x3: 3.1V 4.7V 0x4: 3.2V 4.8V 0x5: 3.3V 4.9V

BITFIELD	BITS	DESCRIPTION	DECODE
			0x6: 3.4V 5.0V 0x7: 3.5V 5.1V
D_LDO_BAT	4:2	Regulated LDO-BAT Difference. In slave mode and LDO_RNG = 0, this sets the regulated voltage difference between the LDO output and BAT. This setting is overridden if LDO output is reduced to the voltage level set by V_LDO_MIN. When LDO_RNG = 1, D_LDO_BAT has no effect on the LDO output except the 000 setting.	**LDO_RNG = 0** **LDO_RNG = 1** 0x0: LDO Bypassed LDO Bypassed 0x1: 100mV N/A 0x2: 150mV N/A 0x3: 200mV N/A 0x4: 250mV N/A 0x5: 300mV N/A 0x6: 350mV N/A 0x7: 400mV N/A
TWAIT_TMR	1:0	PLC Master's Rx Wait Time After Transmission	0x0: 2ms 0x1: 10ms (default) 0x2: 100ms 0x3: 800ms

CONTROL3 (0x3)

BIT	7	6	5	4	3	2	1	0
Field	COM_THRS[1:0]		CHG_TMR_SET[1:0]		LDO_RNG	BAT_RECHG[2:0]		
Reset	0x2		0x2		0x0	0x4		
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
COM_THRS	7:6	Communication Detection Threshold	0x0: 50mV 0x1: 65mV 0x2: 80mV 0x3: 100mV
CHG_TMR_SET	5:4	Charge TImer Setting (Master Only and Master/Slave State Machine Active).	When the charge timer expires, the device automatically transitions from slave found state to the slave detection state. 0x0: Charge timer disabled. 0x1: 60min 0x2: 120min 0x3: 240min
LDO_RNG	3	LDO range select. This selects the range of the minimum LDO output voltage set by V_LDO_MIN[2:0].	0x0: 2.8V to 3.5V output range 0x1: 4.4V to 5.1V output range
BAT_RECHG	2:0	Battery Recharge Threshold. Programmable in 200mV steps (slave mode only and master/slave state machine active). When the voltage on BAT drops below this level, the device automatically transitions from slave idle state to master detection state and applies the clamp on PLC.	0x0: 3V 0x1: 3.2V ... 0x7: 4.4V

CONTROL4 (0x4)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	TXRX_RESET	SLAVE_TO_IDLE	—	—	TXFILT_ENB
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
—	7	Reserved. Do not change the default value.	
—	6	Reserved. Do not change the default value.	
—	5	Reserved. Do not change the default value.	
TXRX_RESET	4	When high, this bit clears asynchronously the PLC transmitter, receiver, and tracking state machines. The I^2C map and master/slave state machines are not affected.	
SLAVE_TO_IDLE	3	When high, this bit causes the transition from the master found communication enabled state to slave idle state. It is ignored in the other states or if the MAX20340 is configured as a master. This bit autoclears.	
—	2	Reserved. Do not change the default value.	
—	1	Reserved. Do not change the default value.	
TXFILT_ENB	0	Tx Filter Active-Low Enable.	0x0: Filter that compares transmitted PLC data to real-time received data is enabled. In case of a mismatch, a counter is incremented. When this counter reaches 15, the PLC_TX_ERR flag is generated and the transmission is interrupted. 0x1: Filter disabled.

DEV_STATUS1 (0x5)

BIT	7	6	5	4	3	2	1	0
Field	CHG_TMR_STAT[1:0]		PLC_STAT	FSM_STAT[2:0]			I2C_ADD	PS_ADD
Reset	0x0		0x0	0x0			0x0	0x0
Access Type	Read Only		Read Only	Read Only			Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_TMR_STAT	7:6	Charge Timer Status	0x0: Timer inactive 0x1: Timer running 0x2: Timer expired 0x3: Reserved
PLC_STAT	5	This bit is set high if one or more bits of the read-only register PLC_STATUS are high.	0x0: PLC_STATUS register has zero value. 0x1: PLC_STATUS register has nonzero value.
FSM_STAT	4:2	FSM State Status	0x0: Initialization (master/slave)/safe state (master) 0x1: Slave low power shutdown 0x2: Master low power shutdown 0x3: Master detection 0x4: Slave detection 0x5: Master found communication enabled 0x6: Slave found charging 0x7: PLC mode (master)/slave idle (slave)
I2C_ADD	1	Configured I²C Slave Address	0x0: 7-bit I²C slave address = 0010101b 0x1: 7-bit I²C slave address = 1101010b
PS_ADD	0	Configured PLC Slave Address	0x0: Slave mode: PLC slave address is 0b0. Master mode: PLC master in single slave mode. 0x1: Slave mode: PLC slave address is 0b1. Master mode: PLC master in dual slave mode.

DEV_STATUS2 (0x6)

BIT	7	6	5	4	3	2	1	0
Field	LDO_DROP	ENb	—	—	—	—	THM_SHDN	PLC_CMP_OUT
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LDO_DROP	7	Output Status of LDO_DROP Comparator	0x0: LDO_DROP comparator output is low. 0x1: LDO_DROP comparator output is high.
ENb	6	Status of /EN\ input pin	0x0: /EN\ input pin is low. 0x1: /EN\ input pin is high.
—	5	Reserved. Used internally.	
—	4	Reserved. Used internally.	
—	3	Reserved. Used internally.	
—	2	Reserved. Used internally.	
THM_SHDN	1	Temperature Status Indicator	0x0: Device not in thermal shutdown. 0x1: Device in thermal shutdown.
PLC_CMP_OUT	0	In slave mode, this bit indicates if V_{PLC} is greater than the PLC detection threshold (V_{PLC_DET}). In master mode, this bit indicates whether V_{PLC} is less than the short-circuit detection threshold (V_{PLC_SHT}).	0x0: $V_{PLC} \leq V_{PLC\_DET}$. 0x1: $V_{PLC} > V_{PLC\_DET}$.

DEV_STATUS_IRQ (0x7)

BIT	7	6	5	4	3	2	1	0
Field	—	VPLC_SHORTi	THM_SHDNi	RSEL_DONEi	LDO_DROP_ERRi	CHG_TMR_STATi	PLC_STATi	FSM_STATi
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
—	7	Reserved	
VPLC_SHORTi	6	PLC Short Circuit Indicator	0x0: No short circuit detected on the PLC line. 0x1: Short circuit detected on the PLC line.
THM_SHDNi	5	Thermal Shutdown Status Indicator	0x0: Temperature below the thermal shutdown threshold. 0x1: Temperature above the thermal shutdown threshold.
RSEL_DONEi	4	RSEL Measurement Status Indicator	0x0: RSEL measurement not yet completed. 0x1: RSEL measurement completed.
LDO_DROP_ERRi	3	LDO Drop Error Status Change Indicator	0x0: LDO is not in dropout condition. 0x1: LDO is in dropout condition.
CHG_TMR_STATi	2	CHG_TMR_STAT Status Change Interrupt	0x0: No change in CHG_TMR_STAT since last read. 0x1: Change in CHG_TMR_STAT (from running to expired).
PLC_STATi	1	PLC_STAT Status Change Interrupt	0x0: No change in PLC_STAT since last read. 0x1: Change in PLC_STAT since last read.
FSM_STATi	0	FSM_STAT Status Change Interrupt	0x0: No change in FSM_STAT since last read. 0x1: Change in FSM_STAT since last read.

DEV_STATUS_MASK (0x8)

BIT	7	6	5	4	3	2	1	0
Field	—	VPLC_SHORTm	THM_SHDNm	RSEL_DONEm	LDO_DROP_ERRm	CHG_TMRm	PLC_STATm	FSM_STATm
Reset	0x0	0x0	0x0	0x1	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
—	7	Reserved. Do not change the default value.	
VPLC_SHORTm	6	VPLC_SHORTi Interrupt Mask	0x0: Interrupt masked 0x1: Interrupt not masked

BITFIELD	BITS	DESCRIPTION	DECODE
THM_SHDNm	5	THM_SHDNi Interrupt Mask	0x0: Interrupt masked 0x1: Interrupt not masked
RSEL_DONEm	4	RSEL_DONEi Interrupt Mask	0x0: Interrupt masked 0x1: Interrupt not masked
LDO_DROP_ERRm	3	LDO_DROP_ERRi Interrupt Mask	0x0: Interrupt masked 0x1: Interrupt not masked
CHG_TMRm	2	CHG_TMR_STATi Interrupt Mask	0x0: Interrupt masked 0x1: Interrupt not masked
PLC_STATm	1	PLC_STATi Interrupt Mask	0x0: Interrupt masked 0x1: Interrupt not masked
FSM_STATm	0	FSM_STATi Interrupt Mask	0x0: Interrupt masked 0x1: Interrupt not masked

PLC_COM_CTRL (0x9)

BIT	7	6	5	4	3	2	1	0
Field	PLC_SINK[1:0]		FREQ[1:0]		PARITY[1:0]		TX[1:0]	
Reset	0x2		0x1		0x1		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
PLC_SINK	7:6	PLC Sink Current	0x0: 200mA 0x1: 244mA 0x2: 288mA (default) 0x3: 355mA
FREQ	5:4	Communication Frequency, Unit Time	0x0: 6µs 0x1: 24µs (default) 0x2: 192µs 0x3: 1536µs
PARITY	3:2	Parity bit	0x0: No parity (parity bit is ignored) 0x1: Odd 0x2: Even 0x3: No parity (parity bit is ignored)
TX	1:0	PLC Transmit. Autoclears to 0b00 at the end of transmission.	0x0: No action. 0x1: Send one byte stored in register 0x0D. 0x2: Send two bytes stored in registers 0x0E and 0x0F. 0x3: Send three bytes stored in registers 0x0D, 0x0E and 0x0F.

PLC_STATUS (0xA)

BIT	7	6	5	4	3	2	1	0
Field	PLC_TMR_ERR	PLC_TX_ERR	PLC_TX_OK	PLC_TX_P	PLC_RX_ERR	NEW_DATA1	NEW_DATA2	PLC_RX_DET

Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PLC_TMR_ERR	7	PLC Rx Timer Status. Master mode only.	0x0: Rx wait timer running or in idle. 0x1: Rx wait timer expired.
PLC_TX_ERR	6	PLC Transmission Error Indicator. This bit is cleared when a new PLC send command is issued.	0x0: No Tx error 0x1: Tx error
PLC_TX_OK	5	PLC Transmission Success Indicator. This bit is cleared when a new PLC send command is issued.	0x0: Not successful 0x1: Successful
PLC_TX_P	4	PLC Transmission Status Indicator	0x0: Not transmitting 0x1: PLC transmission in progress
PLC_RX_ERR	3	PLC Rx Error Status	0x0: No error 0x1: Error (start bit, parity, checksum, or stalled line)
NEW_DATA1	2	When a new data byte is available in register RX_DATA0 (reg 0x10), this bit is set. Once the RX_DATA0 register is read, this bit is cleared.	0x0: No new data byte 0x1: One new data byte arrived
NEW_DATA2	1	When two new data bytes are available in the RX_DATA1 and RX_DATA2 registers (0x11 and 0x12), this bit is set.	0x0: No new data bytes 0x1: Two new data bytes arrived
PLC_RX_DET	0	PLC Receiving Detection. Only during preamble and data.	0x0: No PLC (within 4-bit length of no or invalid signal) 0x1: PLC is ongoing (within 4 bits of preamble signal)

PLC_IRQ (0xB)

BIT	7	6	5	4	3	2	1	0
Field	PLC_TMRi	PLC_TX_ERRi	PLC_TX_OKI	PLC_TX_Pi	PLC_RX_ERRi	NEW_DATA1i	NEW_DATA2i	PLC_RX_DETi
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
PLC_TMRi	7	PLC Rx Wait Timer Expiration Interrupt	0x0: Interrupt has not occurred 0x1: Interrupt occurred
PLC_TX_ERRi	6	PLC Transmission ERROR Interrupt	0x0: Interrupt Not occurred 0x1: Interrupt occurred
PLC_TX_OKI	5	PLC Transmission Success Interrupt	0x0: Interrupt not occurred 0x1: Interrupt occurred

BITFIELD	BITS	DESCRIPTION	DECODE
PLC_TX_Pi	4	PLC Transmission in Progress Interrupt	0x0: Interrupt not occurred 0x1: Interrupt occurred
PLC_RX_ERRi	3	PLC Rx Error Interrupt	0x0: Interrupt not occurred 0x1: Interrupt occurred
NEW_DATA1i	2	NEW_DATA1 Interrupt	0x0: Interrupt not occurred 0x1: Interrupt occurred
NEW_DATA2i	1	NEW_DATA2 Interrupt	0x0: Interrupt not occurred 0x1: Interrupt occurred
PLC_RX_DETi	0	PLC Receiving Detection Interrupt	0x0: Interrupt not occurred 0x1: Interrupt occurred

PLC_MASK (0xC)

BIT	7	6	5	4	3	2	1	0
Field	PLC_TMRm	PLC_TX_ERRm	PLC_TX_OKm	PLC_TX_Pm	PLC_RX_ERRm	NEW_DATA1m	NEW_DATA2m	PLC_RX_DETm
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PLC_TMRm	7	PLC_TMRi Interrupt Mask	0x0: Masked 0x1: Not masked
PLC_TX_ERRm	6	PLC_TX_ERRi Interrupt Mask	0x0: Masked 0x1: Not masked
PLC_TX_OKm	5	PLC_TX_OKi Interrupt Mask	0x0: Masked 0x1: Not masked
PLC_TX_Pm	4	PLC_TX_Pi Interrupt Mask	0x0: Masked 0x1: Not masked
PLC_RX_ERRm	3	PLC_RX_ERRi Interrupt Mask	0x0: Masked 0x1: Not masked
NEW_DATA1m	2	NEW_DATA1i Interrupt Mask	0x0: Masked 0x1: Not masked
NEW_DATA2m	1	NEW_DATA2i Interrupt Mask	0x0: Masked 0x1: Not masked
PLC_RX_DETm	0	PLC_RX_DETi Interrupt Mask	0x0: Masked 0x1: Not masked

TX_DATA0 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	TXDATA0[7:0]							

Reset	0x0
Access Type	Write, Read

BITFIELD	BITS	DESCRIPTION
TXDATA0	7:0	Transmit Data Byte 0

TX_DATA1 (0xE)

BIT	7	6	5	4	3	2	1	0
Field	TXDATA1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TXDATA1	7:0	Transmit Data Byte 1

TX_DATA2 (0xF)

BIT	7	6	5	4	3	2	1	0
Field	TXDATA2[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TXDATA2	7:0	Transmit Data Byte 2

RX_DATA0 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	RXDATA0[7:0]							
Reset	0x0							

Access Type	Read Only

BITFIELD	BITS	DESCRIPTION
RXDATA0	7:0	Receive Data Byte 0

RX_DATA1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	RXDATA1[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RXDATA1	7:0	Receive Data Byte 1

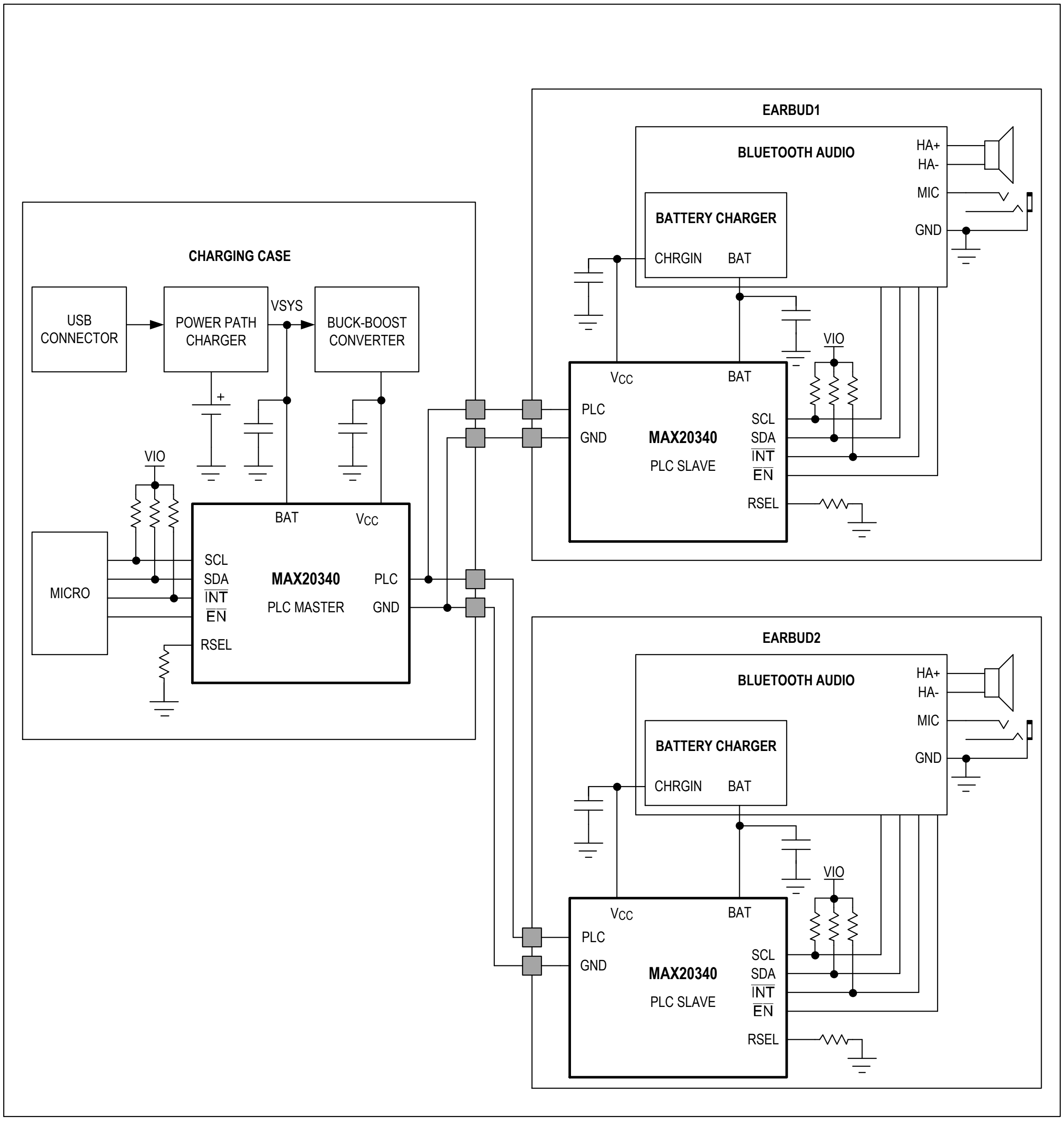
RX_DATA2 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	RXDATA2[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RXDATA2	7:0	Receive Data Byte 2

Typical Application Circuits

Wireless Earbud Charging with Cradle


EARBUD1
BLUETOOTH AUDIO
HA+
HA-
MIC
GND
BATTERY CHARGER
CHRGIN
BAT
VIO
VCC
BAT
PLC
GND
MAX20340
PLC SLAVE
SCL
SDA
INT
EN
RSEL
CHARGING CASE
USB CONNECTOR
POWER PATH CHARGER
VSYS
BUCK-BOOST CONVERTER
VIO
BAT
VCC
MICRO
SCL
SDA
INT
EN
RSEL
MAX20340
PLC MASTER
PLC
GND
EARBUD2
BLUETOOTH AUDIO
HA+
HA-
MIC
GND
BATTERY CHARGER
CHRGIN
BAT
VIO
VCC
BAT
PLC
GND
MAX20340
PLC SLAVE
SCL
SDA
INT
EN
RSEL

Ordering Information

PART NUMBER	PIN-PACKAGE	TOP MARKING	PACKAGE CODE	PACKAGE OUTLINE
MAX20340EWL+	9 WLP	ALT	W91R1+1	21-100389
MAX20340EWL+T	9 WLP	ALT	W91R1+1	21-100389

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/19	Initial release	—
1	2/20	Added new LDO output range to condition of "LDO Output Voltage" spec. Added TOC 28. Added more description in Master Mode Operation and Slave Mode Operation sections. Added PLC Master and Slave Detection section. Expanded LDO Operation section. Added LDO_RNG bit (reg 0x03 bit 0x03) and its description. Updated description for CONTROL2 register. Changed default values of the following registers: DEVICE_ID, CONTROL1, CONTROL2, CONTROL3. Changed Decode block of PLC_SINK[1:0] bit description	4, 9, 12, 13, 22, 23, 24, 25, 28

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.