M100PFS Hardware Manual

Version: **1.3**

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CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.2 Disclaimer

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1.3 Copyright

1.4 Registered Trademarks

1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices. Test

1.6 Change Log

Revision	Date	Revised	Comment
1.0	01.04.2021	dk	Initial creation
1.1	14.10.2022	dk	Connector Location added
1.2	01.12.2022	dk	J2 Connector layout changed
1.3	22.05.2023	aw	Corrected and updated 1. assignment TX5_N to FPGA-signal N8 in section 3.7.8 2. updated GPIO table in section 3.7.5 3. assignment GPIO_E14 to J1-75 and GPIO_E16 to J1-34 in section 3.7.7 Connector J1

CHAPTER

TWO

OVERVIEW

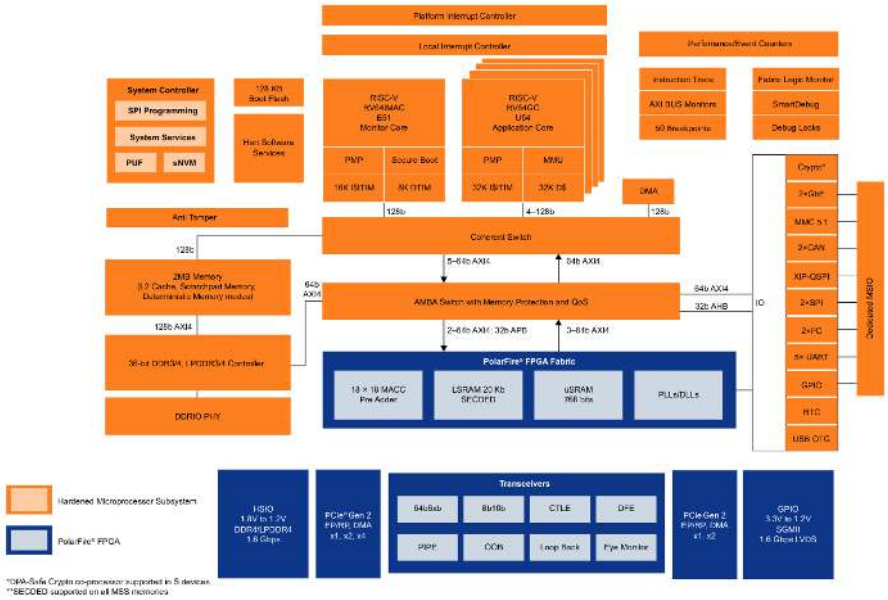
2.1 M100PFS System on Module

The M100PFS is based on the PolarFire SoC FPGA family by Microchip. The SoM is based on the PolarFire SoC FPGA architecture by Microchip and combines high-performance 64-bit RISC-V cores with outstanding FPGA technology. The platform integrates a hardened real-time, Linux capable, RISC-V-based MPU subsystem on the mid-range PolarFire FPGA family, bringing low power consumption, thermal efficiency and defence grade security to embedded systems.

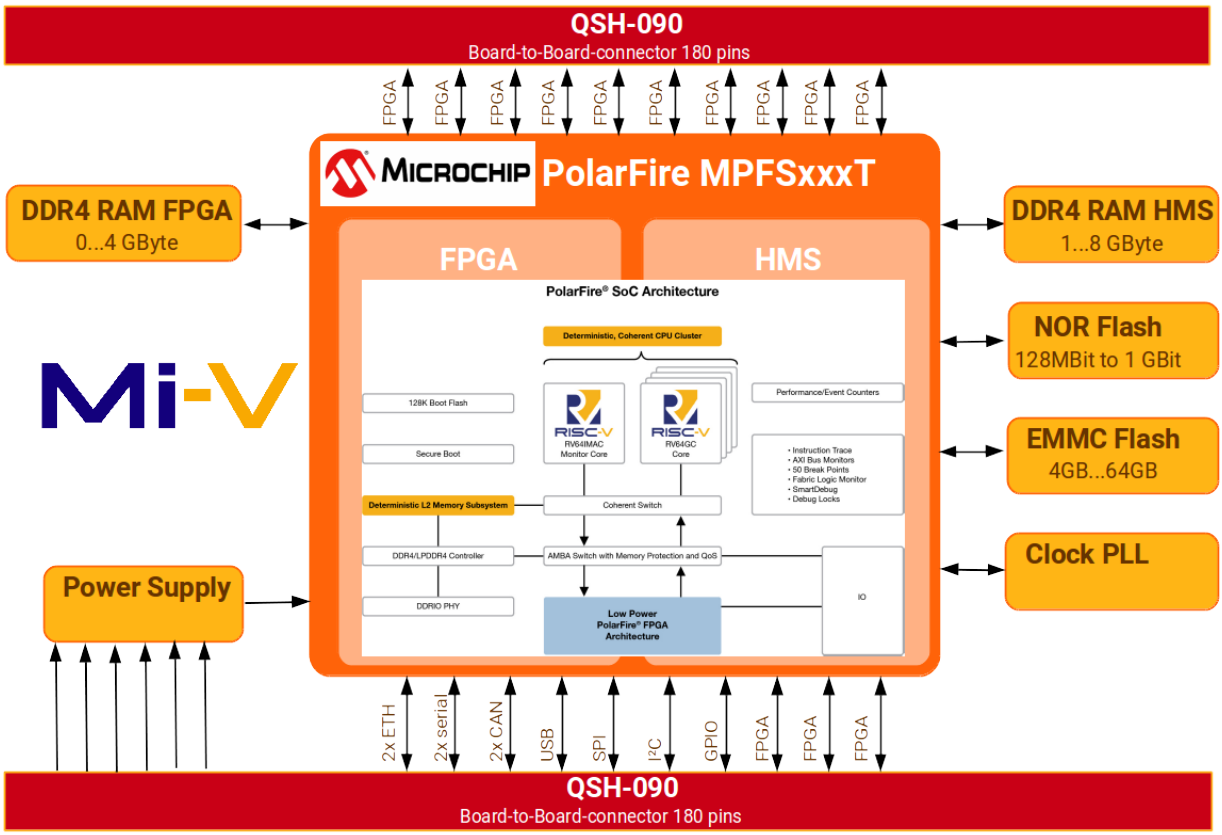
The SoM targets demanding industrial and medical applications and offers the full flexibility of the populated SoC-FPGAs. It is addressing key markets such as

- Communications
- Industrial Automation
- Smart Embedded Vision
- Automotive
- Internet-of-Things
- Defense

PolarFire SoC FPGAs deliver up to 50% lower power than equivalent SRAM SoC FPGAs. PolarFire SoC is built upon the award winning, non-volatile PolarFire FPGA platform and features a five-core Linux® capable processor subsystem based on the RISC-V ISA. The RISC-V CPU micro-architecture implementation is a simple 5 stage, single issue, in-order pipeline that doesn't suffer from the Meltdown and Spectre exploits found in common out-of-order machines. All five CPU cores are coherent with the memory subsys-tem allowing a versatile mix of deterministic real time systems and Linux in a single multi-core CPU cluster.



2.2 Block Diagram



2.3 Feature Set

- Microsemi PolarFire SoC FPGAThe following figure provides an overview of the I2C busses:
  - MPFS025T

    23KLE, 68 math blocks, 4x SERDES 12.5Gbit/s, 2x PCIe root port/end point
  - MPFS095T, available on request

    93KLE, 292 math blocks, 4x SERDES 12.5Gbit/s, 2x PCIe root port/end point
  - MPFS160T, available on request

    161KLE, 498 math blocks, 8x SERDES 12.5Gbit/s, 2x PCIe root port/end point
  - MPFS250T

    254KLE, 784 math blocks, 16x SERDES 12.5Gbit/s, 2x PCIe root port/end point
  - Quad 64-bit RV64GC cores, 667 MHz
  - 64-bit RV64IMAC monitor core, 667 MHz
  - Processor I/O
    - 2x Gigabit Ethernet
    - 1x USB 2.0 OTG
    - 1x MMC 5.1 SD/SDIO
    - 2x CAN 2.0 A and B
    - Execute in place Quad SPI flash controller
    - 5x multi-mode UARTs
    - 2x SPI
    - 2x I2C
    - RTC
    - GPIO
    - 5x watchdog timers
    - timers
  - Processor to FPGA Interconnect
    - 2x 64-bit AXI4 processor-to-fabric interfaces
    - 3x 64-bit AXI4 fabric-to-processor interfaces
    - 1x 32-bit APB processor-to-fabric interface
- Memory
  - 1 to 8 GByte DDR4 RAM dedicated to the HMS
  - 512MByte to 4 GByte DDR4 RAM dedicated to the FPGA
  - 128 Mbit to 1GBit NOR Flash
  - 8 - 64 GByte eMMC memory
- Clock distribution

- default configuration:
  - Gigabit Ethernet
  - UART
  - CAN
  - SPI
  - I^2C
  - USB
- single 3,3V supply
- size 74mmx42mm
- 2 x Samtec QSH-090-01-F-D-A board-to-board interconnect
- commercial (0°C...+70°C) / industrial (-40°C...+85°C) temperature range

2.4 Order Codes

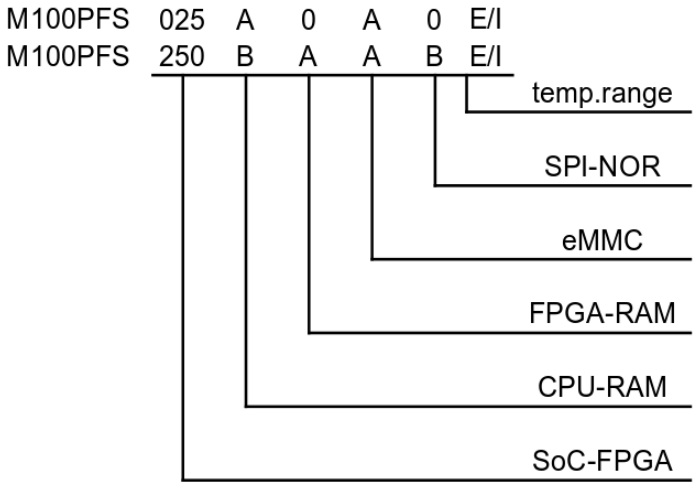
The M100PFS SoM is available in the following standard configurations:

- **M100PFS-025A0A0**
  - MPFS025T PolarFire SoC FPGA
    - 23 KLEs
    - 68 Math Blocks (18x18 MACC)
    - 4x 12.5 Gbps SERDES lanes
    - 2x PCIe Gen2 end points/root points
    - Total User I/O: MSS-IO / HSIO / GPIO / XCVRs: 136 / 60 / 48 / 4
  - 1GB DDR4 SDRAM dedicated to the HMS
  - 4GByte eMMC
  - size 74mm x 42mm
  - 2 x Samtec QSH-090-01-F-D-A board-to-board interconnect
  - 0°C...+70°C
- **M100PFS-250BAAB**
  - MPFS250T PolarFire SoC FPGA
    - 254 KLEs
    - 784 Math Blocks (18x18 MACC)
    - 16x 12.5 Gbps SERDES lanes
    - 2x PCIe Gen2 end points/root points
    - Total User I/O: MSS-IO / HSIO / GPIO / XCVRs: 136 / 60 / 48 / 4
  - 2GB DDR4 SDRAM dedicated to the HMS
  - 512MB DDR4 SDRAM dedicated to the FPGA
  - 32 MBit SPI NOR Flash
  - 4GByte eMMC
  - size 74mm x 42mm
  - 2 x Samtec QSH-090-01-F-D-A board-to-board interconnect
  - 0°C...+70°C

Please contact ARIES Embedded for more information about the availability of other standard products of M100PFS or custom configurations.

2.5 Variant Key

The following options are available for M100PFS:



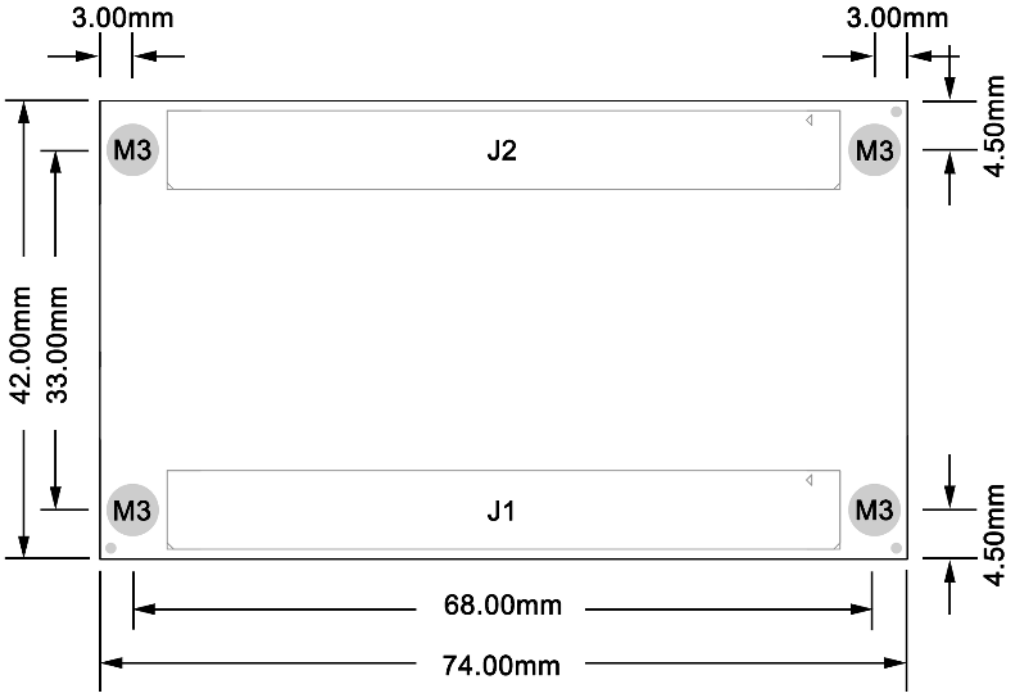
Coding					Component / Feature
PolarFire SoC-FPGA					
025	L	S	1		MPFS025TLS-1FCVG484EI
095	L	S	1		MPFS095TLS-1FCVG484EI
160	L	S	1		MPFS160TLS-1FCVG484EI
250	L	S	1		MPFS250TLS-1FCVG484EI
FPGA DDR4					
A	4 Gbit, 512Mx16				
B	8 Gbit, 1Mx16				
C	16 Gbit, 2Gx16				
D	32 Gbit, 4Gx16				
MMS DDR4					
A	2x4 Gbit, 512Mx16				
B	2x8 Gbit, 1Gx16				
C	2x16 Gbit, 2Gx16				
D	2x32 Gbit, 4Gx16				
eMMC					
A	4 GByte				
B	8 GByte				
C	16 GByte				
D	32 GByte				
E	64 GByte				
SPI NOR					
A	128 MBit				
B	256 MBit				
C	512 MBit				

continues on next page

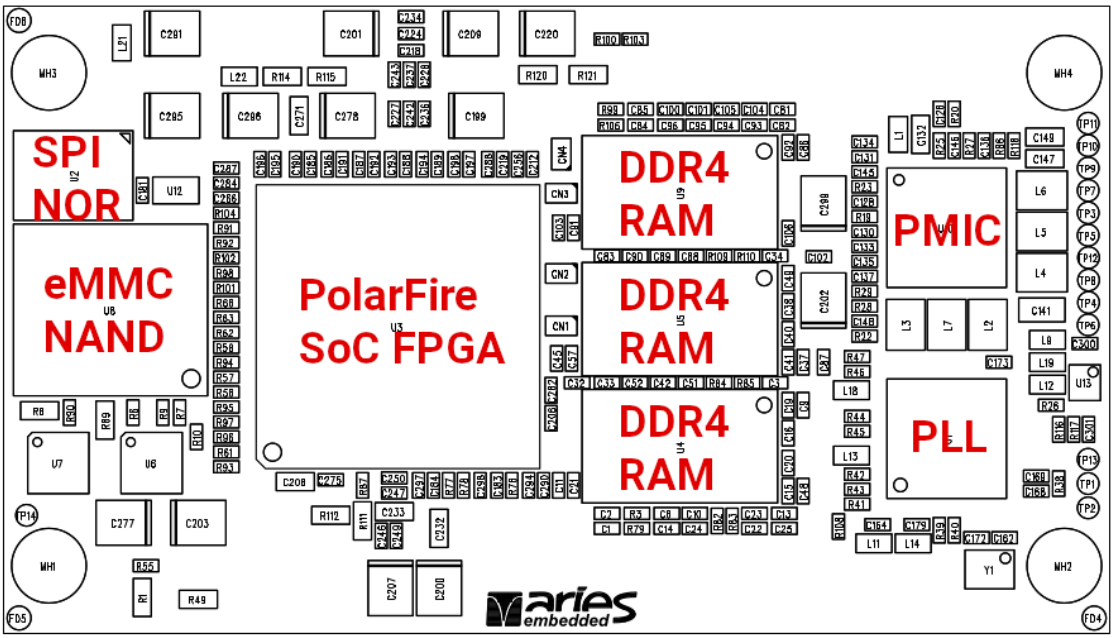
Table 1 – continued from previous page

Coding		Component / Feature
D	1 GBit	
Temperature Range		
_	0°C....+70°C	
E	-25°C....+85°C	
I	-40°C...+85°C	

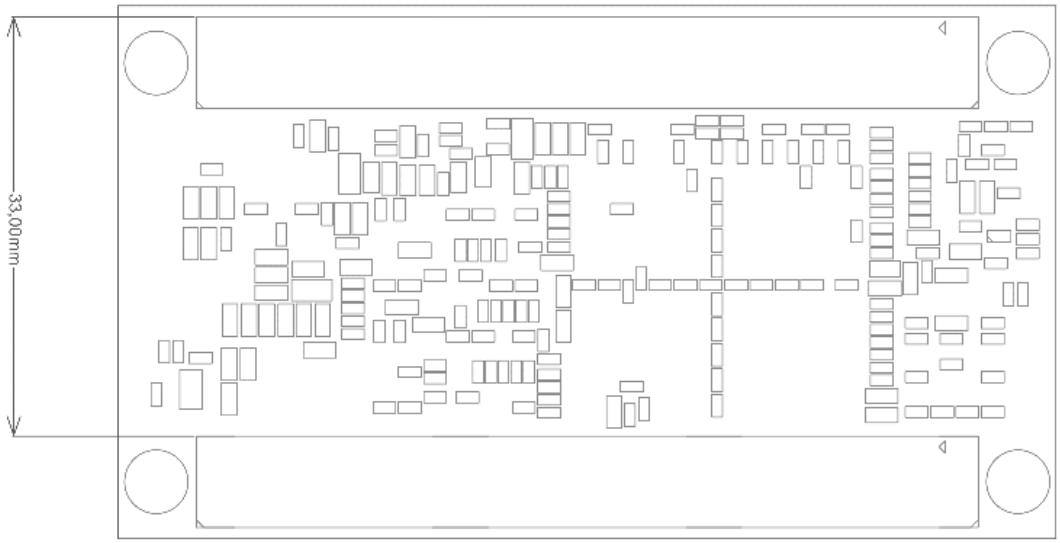
2.6 Dimensions



2.7 Part Overview

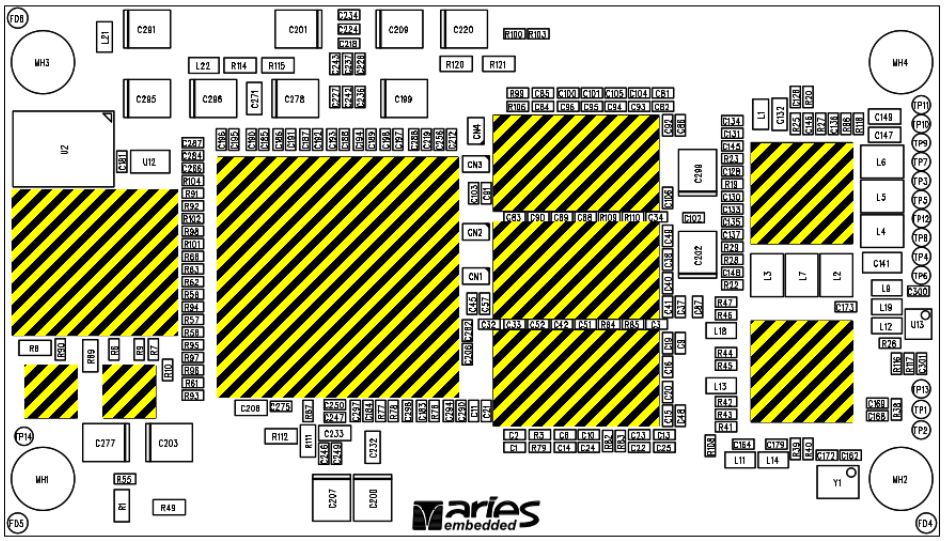


Connector Location:



2.8 Handling Recommendations

The populated Samtec connectors require certain mechanical force to insert the SoM into its mating baseboard connectors. To avoid mechanical damage to the components populated on M100PFS SoM it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:



CHAPTER

THREE

RESOURCES

3.1 Components

3.1.1 PolarFire SoC-FPGA

The M100PFS SoM is based on the PolarFire SoC-FPGA in the FCVG484 package. The following devices will be available on the SoM:

Device	MPFS025T	MPFS095T	MPFS160T	MPFS250T
Logic Elements 4LUT + DFF	23k	93k	161k	254k
Math Blocks 18x18 MACC	68	292	498	784
SERDES	4x/12.5GB/s	4x/12.5GB/s	8x/12.5GB/s	16x/12.5GB/s
PCIe	2x root port / end point			
MSS IO	136			
HSIO	60			
GPIO	48			
XCVRs	4			

For more information on the PolarFire SoC-FPGA please refer to the documentation which is available from Microsemi

3.1.2 DDR4 RAM Types

The M100PFS SoM supports

- two 16 bit wide DDR4 RAMs resulting in a max. capacity of 8 GByte DDR4 RAM for the Microprocessor Subsystem (MSS).
- optional one 16 wide DDR4 RAM resulting in a max. capacity of 4 GByte DDR4 RAM for the FPGA

The memory interface is clocked at max. 800 MHz using the 1.2V DDR4 standard.

The following devices are used on the M100PFS SoM:

Device	Density	Capacity	Organization	temp.range
K4A4G165WF-BCTD	4Gb	512MB	256M x 16	0 ~ 85 °C
K4A4G165WE-BITD	4Gb	512MB	256M x 16	-40 ~ 95 °C
K4A8G165WB-BCTD	8Gb	1GB	512M x 16	0 ~ 85 °C
K4A8G165WB-BITD	8Gb	1GB	512M x 16	-40 ~ 95 °C
K4AAG165WA-BCTD	16Gb	2GB	1G x 16	0 ~ 85 °C
K4ABG165WA-MCTD	32Gb	4GB	2G x 16	0 ~ 85 °C

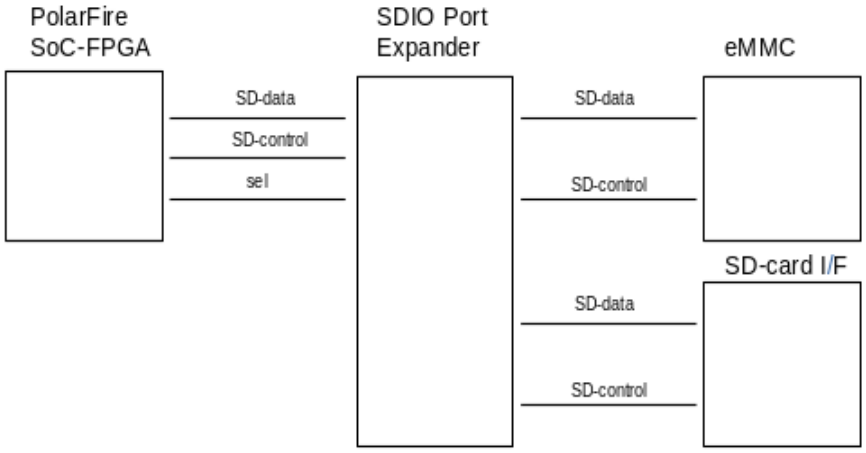
3.1.3 FPGA HSIO Sygnals for DDR4

Function	MSS Pin		Function	FPGA Pin
PF_DDR4_A0	V22		PF_DDR4_CS_N	AA17
PF_DDR4_A1	W22		PF_DDR4_CKE	AB17
PF_DDR4_A2	Y21		PF_DDR4_ODT	Y16
PF_DDR4_A3	Y20		PF_DDR4_RST_N	AA16
PF_DDR4_CK_N	V21		PF_DDR4_PAR	W17
PF_DDR4_CK_P	W21		PF_DDR4_DQ4	AB15
PF_DDR4_A4	AB20		PF_DDR4_DQ2	AA15
PF_DDR4_A5	AB19		PF_DDR4_DQ6	Y15
PF_DDR4_A6	AA20		PF_DDR4_DQ0	AB13
PF_DDR4_A7	AB21		PF_DDR4_DQ7	AA13
PF_DDR4_ALERT_N	V19		PF_DDR4_GQS0_N	W14
PF_DDR4_TEN	V20		PF_DDR4_DQS0_P	Y14
PF_DDR4_A8	U17		PF_DDR4_DQ3	AB12
PF_DDR4_A9	T17		PF_DDR4_DQ5	AA12
PF_DDR4_A10	R16		PF_DDR4_DQ1	Y13
PF_DDR4_A11	T16		PF_DDR4_DM0	W13
PF_DDR4_A12	V16		PF_DDR4_DQ13	V15
PF_DDR4_A13	V17		PF_DDR4_DQ14	T15
PF_DDR4_A14	R14		PF_DDR4_DQ15	U15
PF_DDR4_A15	R15		PF_DDR4_DQ11	V12
PF_DDR4_A16	AA18		PF_DDR4_DQ9	W12
PF_DDR4_BA0	AB18		PF_DDR4_DQS1_N	U13
PF_DDR4_BA1	W18		PF_DDR4_DQS1_P	U14
PF_DDR4_ACT_N	W19		PF_DDR4_DQ10	T12
PF_DDR4_BG0	Y18		PF_DDR4_DQ8	U12
PF_DDR4_BG1	Y19		PF_DDR4_DQ12	T13
PF_DDR4_DM1	R12		MSS_DDR4_TEN	AA22

3.1.4 SDIO Port Expander

The M100PFS includes TXS02612 SDIO Port Expanders which connects the PF SoC SD-card interface to the on-board eMMC NAND Flash as well as the SD-card interface. This enables developers to flexibly switch i.e. between SD-card interface and SD-card for development purpose or an update procedure and the eMMC NAND Flash.

The eMMC is connected 8bit wide to the MSS while the SD-card interface is available on the board-to-board-connector 4 bit wide. The SEL-Signal selects between the two interfaces.



SoC FPGA Pin	SoC FPGA Ball	Port Expander	eMMC Signal	SD-card Signal
MSS_IO0	J1	CLK	EMMC_CLK	SD_CLK
MSS_IO1	K5	CMD	EMMC_CMD	SD_CMD
MSS_IO2	H1	DAT0	EMMC_DAT0	SD_DAT0
MSS_IO3	J4	DAT1	EMMC_DAT1	SD_DAT1
MSS_IO4	K4	DAT2	EMMC_DAT2	SD_DAT2
MSS_IO5	J7	DAT3	EMMC_DAT3	SD_DAT3
MSS_IO6	K3	PRES_N	EMMC_GND	SD_PRES_N
MSS_IO7	H4	RTS_N	EMMC_RST_N	SD_RTS_N
MSS_IO8	J6	DAT4	EMMC_DAT4	n.c.
MSS_IO9	H6	DAT5	EMMC_DAT5	n.c.
MSS_IO10	J3	DAT6	EMMC_DAT6	n.c.
MSS_IO11	H2	DAT7	EMMC_DAT7	n.c.
MSS_IO12	H5	SEL	n.c.	n.c.

3.1.5 eMMC NAND Flash

The M100PFS SoM supports 4GB-64GB eMMC NAND Flash.

The following devices are used on the M100PFS SoM:

Device	Capacity	temp.range
THGBMNG5D1LBAIT	4GB	-25°C...+85 °C
THGBMJG6C1LBAIL	8GB	-25°C...+85 °C
THGBMJG6C1LBAU7	8GB	-40°C...+105°C
THGBMJG7C1LBAIL	16GB	-25°C...+85 °C
THGBMJG7C2LBAU8	16GB	-40°C...+105°C
THGAMRG8T13BAIL	32GB	-25°C...+85 °C
THGBMJG8C4LBAU8	32GB	-40°C...+105°C
THGAMRG9T23BAIL	64GB	-25°C...+85 °C

3.1.6 SPI NOR Flash

The SPI flash memory interfaces with the system controller's SPI interface and can store the programming images.

On M100PFS the following devices are available optionally:

Device	Density	Capacity	temp.range
MT25QU128ABA8E12-0SIT	128MBit	16MB	-40°C...+85°C
S25FS128SDSBHB203	128MBit	16MB	-40°C...+85°C
MT25QU256ABA8E12-1SIT	256MBit	32MB	-40°C...+85°C
S25FS256SAGBHI200	256MBit	32MB	-40°C...+85°C
MT25QU512ABB8E12-0SIT	512MBit	64MB	-40°C...+85°C
S25FS512SAGBHI210	512MBit	64MB	-40°C...+85°C
MT25QU01GBBB8E12-0AAT	1GBit	128MB	-40°C...+105°C
S70FS01GSAGBHB213	1GBit	128MB	-40°C...+105°C

3.1.7 PMIC

Power on the M100PFS is controlled by a factory programmed Dialog DA9063L-00 PMIC.

3.1.8 SERDES Transceiver

M100PFS provides up to 16 SERDES lanes each with up 12.5 Gbps datarate.

Function	FPGA Pin	Connector		Function	FPGA Pin	Connector
XCVR_0_TX0_N	F21	J2-17		XCVR_0_TX0_P	F22	J2-15
XCVR_0_TX1_N	H21	J2-29		XCVR_0_TX1_P	H22	J2-27
XCVR_0_TX2_N	P21	J2-41		XCVR_0_TX2_P	P22	J2-39
XCVR_0_TX3_N	T21	J2-18		XCVR_0_TX3_P	T22	J2-16
XCVR_0_RX0_N	G19	J2-11		XCVR_0_RX0_P	G20	J2-9
XCVR_0_RX1_N	K21	J2-23		XCVR_0_RX1_P	K22	J2-21
XCVR_0_RX2_N	M21	J2-35		XCVR_0_RX2_P	M22	J2-33
XCVR_0_RX3_N	R19	J2-12		XCVR_0_RX3_P	R20	J2-10
XCVR_0A_REFCLK_N	L20	J2-3		XCVR_0A_REFCLK_P	L19	J2-5
XCVR_0C_REFCLK_N	J20	J2-4		XCVR_0C_REFCLK_P	J19	J2-6
XCVR1_RX1_P	C20	--		XCVR1_RX1_N	C19	--

3.1.9 SGMII Transceiver

Function	MSS Pin	Connector
MSS_SGMII_TXN1	N8	J2-42
MSS_SGMII_TXP1	M7	J2-40
MSS_SGMII_RXN1	K7	J2-36
MSS_SGMII_RXP1	K6	J2-34
MSS_SGMII_TXN0	N7	J2-30
MSS_SGMII_TXP0	N6	J2-28
MSS_SGMII_RXN0	L6	J2-24
MSS_SGMII_RXP0	L5	J2-22
MSS_REFCLK_IN_P	L7	--
MSS_REFCLK_IN_N	L8	--

3.2 SPI Configuration and Programming

FPGA and SPI Flash are connected on a shared SPI interface. This allows the FPGA to load configuration images stored on the Flash.

For more information about programming the Polarfire FPGA see the PolarFire FPGA Programming User Guide (UG0714).

3.3 Clocking

The clocking scheme on the M100PF is generated by an ID ZL30265LD Clock Generator (PLL). Its base is sourced from a 25 MHz oscillator to generate the required clocks for the board's components. The ID ZL30265LD provides any output frequency from 1Hz to 1045MHz and any input frequency from 9.72MHz to 1.25GHz. The ID ZL30265LD is accessible from FPGA on the I2C 1 bus at address 0x74 for reconfiguration. The Polarfire FPGA itself provides an internal 2 MHz and an internal 160 MHz oscillator. The ZL30265LD with internal EEPROM is a slave on the I2C bus.

Function	Pin	Oscillator
MSS_CLK_P	L7	125MHz
MSS_CLK_N	L8	125MHz
X_REF_CLK_P	N19	125MHz
X_REF_CLK_N	N20	125MHz
CLK25_0	J-2C 174	25MHz

3.4 I2C

The Polarfire FPGA is connected to I2C bus as master.

I2C 1		
Address	**Device**	**Description**
0x74	ZL30265LD Clock Generator	Allows reconfiguration of the clocks present on M100PFS
Master	Polarfire FPGA	Connected to MSS Pins C1 (SCL) and B1 (SDA)

Function	FPGA Pin	Connector	Component MSS
PMIC_SDA	--	J2-165	--
PMIC_SCL	--	J2-167	--
PLL_SDA	B1	J2-126	MSS_IO27
PLL_SCL	C1	J2-139	MSS_IO26

3.5 JTAG

The M100PFS Baseboard provides a JTAG header for the FlashPro programmer to programm the FPGA using Microchip's standard tools.

Function	FPGA Pin	Connector
TCK	E9	J1-6
TMS	F8	J1-10
TDI	G9	J1-8
TDO	E8	J1-4
TRSTB	G8	J1-2
VIO	1.8V	J1-12

3.6 UART

The FPGA and PIC microcontroller are connected via UART providing access to the FPGA from the host PC. The PIC uses the CDC-ACM interface to communicate with the host. On the Linux Operating System it is visible as */dev/ttyACMx* device.

Function	FPGA Pin	Connector	Component MSS/FPGA
UART0_TX	E3	J2-C 132	MSS_IO36
UART0_RX	A3	J2-C 138	MSS_IO35
TXD2	E14	J1-B 75	GPIO9NB1
RXD2	B14	J1-B 77	GPIO3NB1

These signals refer to the functionality available on the M100PFSEVP baseboard. When using a custom baseboard the connections can be used as GPIO, however for some signals there may be resistors present.

3.7 Pin Out

3.7.1 CAN

Function	FPGA	Connector	Component MSS
CAN0_TX	B4	J2-129	MSS_IO31
CAN0_RX	B2	J2-137	MSS_IO32
CAN1_TX	D3	J2-135	MSS_IO28
CAN1_RX	B5	J2-130	MSS_IO29

These signals refer to the functionality available on the MPFS250T baseboard. When using a custom baseboard the connections can be used as GPIO, however for some signals there may be resistors present.

3.7.2 ULPI Interface

Function	FPGA	Connector	Component MSS
USB_DIR	F1	J2-81	MSS_IO15
USB_CLK	G2	J2-83	MSS_IO14
USB_D4	D1	J2-85	MSS_IO22
USB_D1	E1	J2-87	MSS_IO19
USB_STP	G4	J2-95	MSS_IO17
USB_D3	F5	J2-99	MSS_IO21
USB_D6	F6	J2-82	MSS_IO24
USB_D7	F3	J2-84	MSS_IO25
USB_D5	D2	J2-86	MSS_IO23
USB_NXT	G5	J2-88	MSS_IO16
USB_D2	G3	J2-98	MSS_IO20
USB_D0	F2	J2-100	MSS_IO18

These signals refer to the functionality available on the MPFS250T baseboard. When using a custom baseboard the connections can be used as GPIO, however for some signals there may be resistors present.

3.7.3 Ethernet

Function	FPGA Pin	Connector		Function	FPGA Pin	Connector
ETH0_MDIO	H17	J2-115		ETH1_MDIO	E18	J1-164
ETH0_MDC	B15	J2-112		ETH1_MDC	B5	J1-161
ETH0_GTXCLK	G17	J2-113		ETH1_GTXCLK	D18	J1-159
ETH0_TX_EN	A15	J2-114		ETH1_TX_EN	C5	J1-172
ETH0_TXD0	G14	J2-106		ETH1_TXD0	D8	J1-174
ETH0_TXD1	F15	J2-107		ETH1_TXD1	D9	J1-163
ETH0_TXD2	H15	J2-108		ETH1_TXD2	B8	J1-171
ETH0_TXD3	G15	J2-105		ETH1_TXD3	A8	J1-166
ETH0_RXC	E15	J2-118		ETH1_RXC	C6	J1-110
ETH0_RXD0	D22	J2-110		ETH1_RXD0	A5	J1-169
ETH0_RXD1	C22	J2-116		ETH1_RXD1	A6	J1-170
ETH0_RXD2	D14	J2-111		ETH1_RXD2	B7	J1-168
ETH0_RXD3	D13	J2-109		ETH1_RXD3	A7	J1-173
ETH0_RX_DV	B13	J2-117		ETH1_RX_DV	C4	J1-165

These signals refer to the functionality available on the MPFS250T baseboard. When using a custom baseboard the connections can be used as GPIO, however for some signals there may be resistors present.

3.7.4 SD Card

Interface selection is implemented through MSS_IO12.

Function	FPGA Pin	Connector
SD_CLK	J1	J1-33
SD_DAT0	H1	J1-35
SD_DAT1	J4	J1-37
SD_DAT2	K4	J1-27
SD_DAT3	J7	J1-29
SD_CMD	K5	J1-31
SD_PRS_N	K3	J1-39

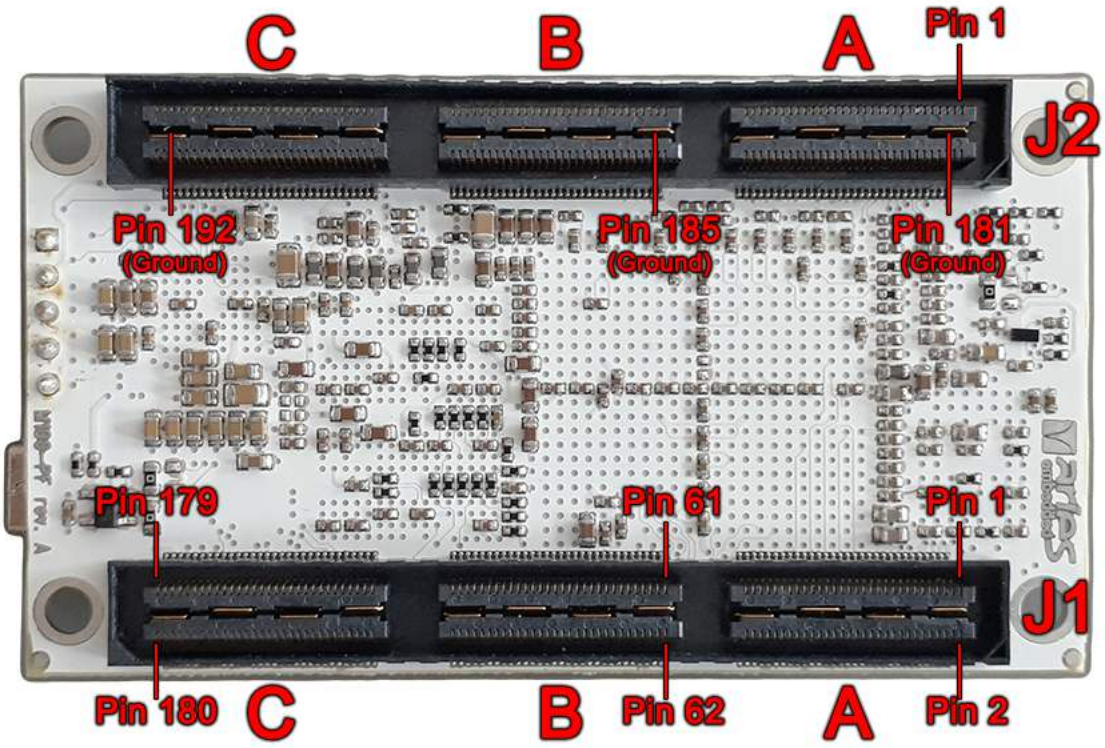
3.7.5 GPIO

The following pins are available for GPIO:

FPGA	Connector		FPGA	Connector		FPGA	Connector
A10	J1-51		B21	J2-124		D21	J2-131
A11	J1-49		B22	J2-128		D20	J2-134
C5	J1-172		C16	J1-42		E16	J1-34
A13	J2-172		C9	J1-45		E19	J1-52
A16	J1-48		C10	J1-47		E10	J1-74
A17	J1-46					E14	J1-75
B17	J1-56		C11	J1-55		E11	J1-118
A20	J2-123		C19	J2-127		E13	J1-133
A21	J2-121		C20	J2-136		F16	J1-36
			C12	J1-28		F17	J1-38
B9	J1-64		C7	J1-41		F10	J1-72
B10	J1-66		D19	J1-50		F11	J1-76
B12	J1-30		D11	J1-53		F12	J1-78
B14	J1-77		D6	J1-58		F13	J1-131
			D7	J1-60		G12	J1-113
			D12	J1-120		G13	J1-162
B19	J2-70		D16	J1-32		H12	J1-115
B20	J2-71		D17	J1-40		H13	J1-160

3.7.6 Samtec Connector

M100PFs uses two Samtec QSH-090-01-F-D-A connectors to supply its signals to a baseboard.



Below are tables with the pins of the connectors and their corresponding function.

3.7.7 Connector J1

Pin	Function	FPGA		Pin	Function	FPGA
Connector J1 A						
1	3.3V	–		2	JTAG_TRSTN	G8
3	3.3V	–		4	JTAG_TDO	E8
5	3.3V	–		6	JTAG_TCK	E9
7	3.3V	–		8	JTAG_TDI	G9
9	3.3V	–		10	JTAG_TMS	F8
11	3.3V	–		12	JTAG_VIO	–
13	–	–		14	ICLK_N	–
15	LPRB_B	C15		16	ICLK_P	–
17	LPRB_A	C14		18	–	–
19	–	–		20	–	–
21	–	–		22	–	–
23	–	–		24	–	–
25	3.3V	–		26	–	–
27	SD_DATA2	K4		28	GPIO_C12	C12
29	SD_DATA3	J7		30	GPIO_B12	B12

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Table 1 – continued from previous page

Pin	Function	FPGA		Pin	Function	FPGA
31	SD_CMD	K5		32	GPIO_D16	D16
33	SD_CLK	J1		34	GPIO_E16	E16
35	SD_DTA0	H1		36	GPIO_F16	F16
37	SD_DTA1	J4		38	GPIO_F17	F17
39	SD_PRS_N	K3		40	GPIO_D17	D17
41	GPIO_C7	A12		42	GPIO_C16	C16
43	–	–		44	–	–
45	GPIO_C9	C9		46	GPIO_A17	A17
47	GPIO_C10	C10		48	GPIO_A16	A16
49	GPIO_A11	A11		50	GPIO_D19	D19
51	GPIO_A10	A10		52	GPIO_E19	E19
53	GPIO_D11	D11		54	GPIO_C17	C17
55	GPIO_C11	C11		56	GPIO_B17	B17
57	--	–		58	GPIO_D6	D6
59	--	–		60	GPIO_D7	D7
Connector J1 B						
61	–	–		62	–	–
63	–	–		64	GPIO_B9	B9
65	–	–		66	GPIO_B10	B10
67	–	–		68	GPIO_B18	B18
69	–	–		70	GPIO_A18	A18
71	–	–		72	GPIO_F10	F10
73	–	–		74	GPIO_E10	E10
75	GPIO_E14	E14		76	GPIO_F11	F11
77	GPIO_B14	B14		78	GPIO_F12	F12
79	–	–		80	–	–
81	–	–		82	–	–
83	–	–		84	–	–
85	–	–		86	–	–
87	–	–		88	–	–
89	–	–		90	–	–
91	–	–		92	–	–
93	–	–		94	–	–
95	–	–		96	–	–
97	–	–		98	–	–
99	–	–		100	–	–
101	–	–		102	–	–
103	–	–		104	–	–
105	–	–		106	–	–
107	–	–		108	–	–
109	–	–		110	ETH1_RXC	C6
111	–	–		112	GPIO_A12	A12
113	GPIO_G12	G12		114	–	–
115	GPIO_H12	H12		116	–	–
117	–	–		118	GPIO_E11	E11
119	–	–		120	GPIO_D12	D12
Connector J1 C						
121	–	–		122	–	–
123	–	–		124	–	–

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Table 1 – continued from previous page

Pin	Function	FPGA		Pin	Function	FPGA
125	–	–		126	–	–
127	–	–		128	–	–
129	–	–		130	–	–
131	GPIO_F13	F13		132	–	–
133	GPIO_E13	E13		134	–	–
135	–	–		136	–	–
137	–	–		138	–	–
139	–	–		140	–	–
141	–	–		142	–	–
143	–	–		144	–	–
145	–	–		146	–	–
147	–	–		148	–	–
149	–	–		150	–	–
151	–	–		152	–	–
153	–	–		154	–	–
155	–	–		156	–	–
157	–	–		158	–	–
159	ETH1_GTXCLK	D18		160	GPIO_H13	F2
161	ETH1_MDC	B5		162	GPIO_G13	T6
163	ETH1_TXD1	D9		164	ETH1_MDIO	E18
165	ETH1_RX_DV	C4		166	ETH1_TXD3	G15
167	GPIO_B4	B4		168	ETH1_RXD2	B7
169	ETH1_RXD0	A5		170	ETH1_RXD1	A6
171	ETH1_TXD2	B8		172	ETH1_TX_EN	C5
173	ETH1_RXD3	A7		174	ETH1_TXD0	D8
175	–	–		176	–	–
177	3.3V	–		178	3.3V	–
179	3.3V	–		180	3.3V	–
181	Ground Plate	–		182	Ground Plate	–
183	Ground Plate	–		184	Ground Plate	–
185	Ground Plate	–		186	Ground Plate	–
187	Ground Plate	–		188	Ground Plate	–
189	Ground Plate	–		190	Ground Plate	–
191	Ground Plate	–		192	Ground Plate	–

3.7.8 Connector J2

Pin	Function	FPGA		Pin	Function	FPGA
Connector J2 A						
1	GND	–		2	GND	–
3	XCVR0_REF_CLK_PL20			4	XCVR1_REF_CLK_PJ20	
5	XCVR0_REF_CLK_NL19			6	XCVR1_REF_CLK_NJ19	
7	GND	–		8	GND	–
9	RX0_P	G20		10	RX3_P	R20
11	RX0_N	G19		12	RX3_N	R19
13	GND	–		14	GND	–

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Table 2 – continued from previous page

Pin	Function	FPGA		Pin	Function	FPGA
15	TX0_P	F22		16	TX3_P	T22
17	TX0_N	F21		18	TX3_N	T21
19	GND	–		20	GND	–
21	RX1_P	K22		22	RX4_P	L5
23	RX1_N	K21		24	RX4_N	L6
25	GND	–		26	GND	–
27	TX1_P	H22		28	TX4_P	N6
29	TX1_N	H21		30	TX4_N	N7
31	GND	–		32	GND	–
33	RX2_P	M22		34	RX5_P	K6
35	RX2_N	M21		36	RX5_N	K7
37	GND	–		38	GND	–
39	TX2_P	P22		40	TX5_P	M7
41	TX2_N	P21		42	TX5_N	N8
43	GND	–		44	GND	–
45	–	AA20		46	–	L20
47	–	AA19		48	–	L19
49	GND	–		50	GND	–
51	–	AB22		52	–	K22
53	–	AB21		54	–	K21
55	GND	–		56	GND	–
57	–	–		58	–	–
59	–	–		60	–	–
Connector J2 B						
61	3.3V	–		62	3.3V	–
63	–	–		64	–	–
65	–	–		66	–	–
67	–	–		68	–	–
69	–	–		70	GPIO_B19	B19
71	GPIO_B20	B20		72	–	–
73	–	–		74	–	–
75	3.3V	–		76	3.3V	–
77	–	–		78	–	–
79	–	–		80	–	–
81	MSS_IO15	F1		82	MSS_IO24	F6
83	MSS_IO14	G2		84	MSS_IO25	F3
85	MSS_IO22	D1		86	MSS_IO23	D2
87	MSS_IO19	E1		88	MSS_IO16	G5
89	–	–		90	–	–
91	–	–		92	–	–
93	–	–		94	–	–
95	MSS_IO17	G4		96	–	–
97	–	–		98	MSS_IO20	G3
99	MSS_IO21	F5		100	MSS_IO18	F2
101	–	–		102	–	–
103	3.3V	–		104	3.3V	–
105	ETH0_TXD3	G15		106	ETH0_TXD0	G14
107	ETH0_TXD1	F15		108	ETH0_TXD2	H15
109	ETH0_RXD3	D13		110	ETH0_RXD0	D22

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Table 2 – continued from previous page

Pin	Function	FPGA		Pin	Function	FPGA
111	ETH0_RXD2	D14		112	ETH0_MDC	B15
113	ETH0_GTXCLK	G17		114	ETH0_TX_EN	A15
115	ETH0_MDIO	H17		116	ETH0_RXD1	C22
117	ETH0_RX_DV	B13		118	ETH0_RXC	E15
119	3.3V	–		120	3.3V	–
Connector J2 C						
121	GPIO_A21	A21		122	–	–
123	GPIO_A20	A20		124	GPIO_B21	B21
125	–	–		126	MSS_IO27	B1
127	GPIO_C19	C19		128	GPIO_B22	B22
129	MSS_IO31	E4		130	MSS_IO29	E5
131	GPIO_D21	D21		132	MSS_IO36	E3
133	–	–		134	GPIO_D20	D20
135	MSS_IO28	D3		136	GPIO_C20	C20
137	MSS_IO32	B2		138	MSS_IO35	A3
139	MSS_IO26	C1		140	3.3V	–
141	3.3V	–		142	3.3V	–
143	–	–		144	–	–
145	–	–		146	–	–
147	–	–		148	–	–
149	–	–		150	–	–
151	–	–		152	–	–
153	MSS_IO37	D4		154	MSS_IO34	B3
155	MSS_IO30	E5		156	MSS_IO33	A2
157	3.3V	–		158	3.3V	–
159	POR_N	J7		160	OCLK_P	–
161	–	–		162	OCLK_N	–
163	3.3V	–		164	VDDOE_PLL	–
165	PMIC_SDA	–		166	–	–
167	PMIC_SCL	–		168	–	–
169	PMIC_TP	–		170	–	–
171	TP6	–		172	GPIO_A13	A13
173	TP7	–		174	CLK25_0	–
175	3.3V	–		176	3.3V	–
177	3.3V	–		178	3.3V	–
179	3.3V	–		180	3.3V	–
189	Ground Plate	–		190	Ground Plate	–
191	Ground Plate	–		192	Ground Plate	–
181	Ground Plate	–		182	Ground Plate	–
183	Ground Plate	–		184	Ground Plate	–
185	Ground Plate	–		188	Ground Plate	–
187	Ground Plate	–		186	Ground Plate	–

3.8 Schematics

Schematics for the M100PFS SoM may be obtained on request.