



($\div 1$, $\div 2/3$) OR ($\div 2$, $\div 4/6$)
CLOCK GENERATION CHIP

Precision Edge®
SY100S838
SY100S838L

FEATURES

- 3.3V and 5V power supply options
- 50ps output-to-output skew
- Synchronous enable/disable
- Master Reset for synchronization
- Internal 75K Ω input pull-down resistors
- Available in 20-pin SOIC package



Precision Edge®

DESCRIPTION

The SY100S838/L is a low skew ($\div 1$, $\div 2/3$) or ($\div 2$, $\div 4/6$) clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The devices can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the VBB output, a sinusoidal source can be AC-coupled into the device. If a single-ended input is to be used, the VBB output should be connected to the CLK input and bypassed to ground via a 0.01 μ F capacitor. The VBB output is designed to act as the switching reference for the input of the SY100S838/L under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

The Function Select (FSEL) input is used to determine what clock generation chip function is. When FSEL input is LOW, SY100S838/L functions as a divide by 2 and by 4/6 clock generation chip. However, if FSEL input is HIGH, it functions as a divide by 1 and by 2/3 clock chip.

The common enable (EN) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as for multiple SY100S838/Ls in a system.

TRUTH TABLE

CLK	\overline{EN}	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q ₀₋₃
X	X	H	Reset Q ₀₋₃

NOTES:

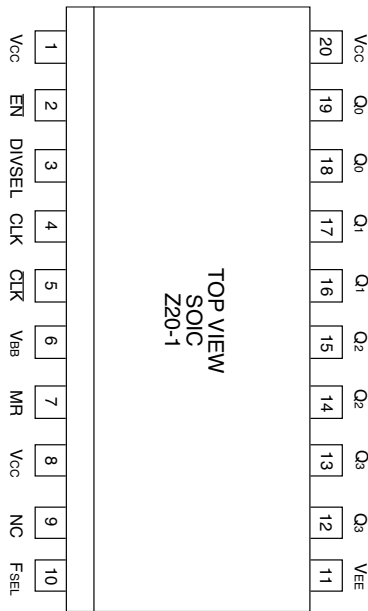
Z = LOW-to-HIGH transition
 ZZ = HIGH-to-LOW transition

FSEL	DIVSEL	Q ₀ , Q ₁ OUTPUTS	Q ₂ , Q ₃ OUTPUTS
L	L	Divide by 2	Divide by 4
L	H	Divide by 2	Divide by 6
H	L	Divide by 1	Divide by 2
H	H	Divide by 1	Divide by 3

PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
FSEL	Function Select Input
\overline{EN}	Synchronous Enable
MR	Master Reset
VBB	Reference Output
Q ₀ , Q ₁	Differential $\div 1$ or $\div 2$ Outputs
Q ₂ , Q ₃	Differential $\div 2/3$ or $\div 4/6$ Outputs
DIVSEL	Frequency Select Input

PACKAGE/ORDERING INFORMATION



20-Pin SOIC (Z20-1)

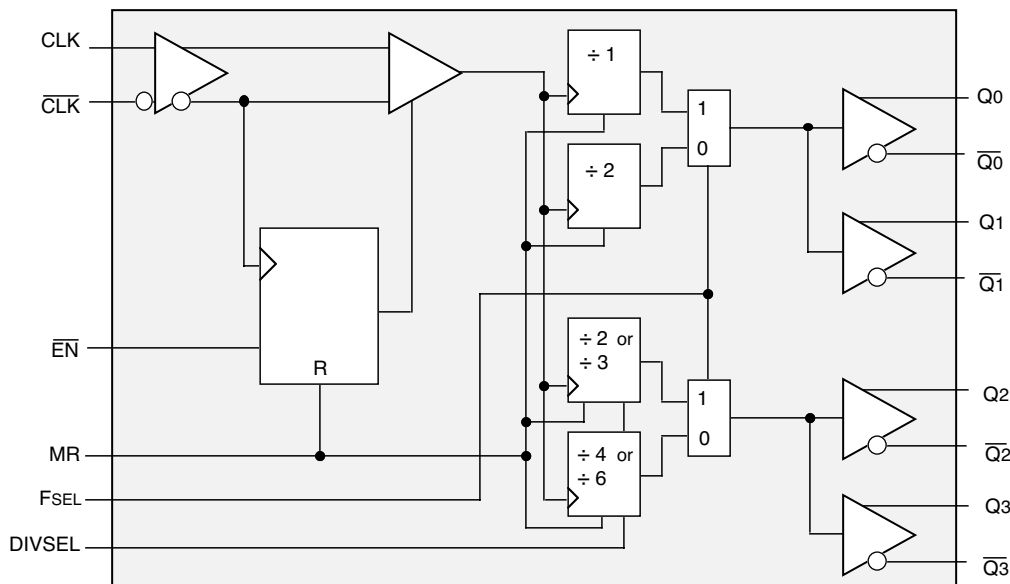
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S838ZC	Z20-1	Commercial	SY100S838ZC	Sn-Pb
SY100S838ZCTR ⁽¹⁾	Z20-1	Commercial	SY100S838ZC	Sn-Pb
SY100S838LZC	Z20-1	Commercial	SY100S838LZC	Sn-Pb
SY100S838LZCTR ⁽¹⁾	Z20-1	Commercial	SY100S838LZC	Sn-Pb
SY100S838ZI	Z20-1	Industrial	SY100S838ZI	Sn-Pb
SY100S838ZITR ⁽¹⁾	Z20-1	Industrial	SY100S838ZI	Sn-Pb
SY100S838LZI	Z20-1	Industrial	SY100S838LZI	Sn-Pb
SY100S838LZITR ⁽¹⁾	Z20-1	Industrial	SY100S838LZI	Sn-Pb
SY100S838ZG ⁽²⁾	Z20-1	Industrial	SY100S838ZG with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100S838ZGTR ^(1, 2)	Z20-1	Industrial	SY100S838ZG with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100S838LZG ⁽²⁾	Z20-1	Industrial	SY100S838LZG with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100S838LZGTR ^(1, 2)	Z20-1	Industrial	SY100S838LZG with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS⁽¹⁾

VEE = VEE (Min.) to VEE (Max.); VCC = GND

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
IEE	Power Supply Current	35	50	65	35	50	65	35	50	65	35	54	75	mA
VBB	Output Reference Voltage	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	V
I _{IH}	Input High Current	—	—	150	—	—	150	—	—	150	—	—	150	μA

Note:

- Parametric values specified at:

5 volt Power Supply Range	100S838 Series:	-4.2V to -5.5V.
3 volt Power Supply Range	100S838L Series	-3.0V to -3.8V.

AC ELECTRICAL CHARACTERISTICS⁽¹⁾

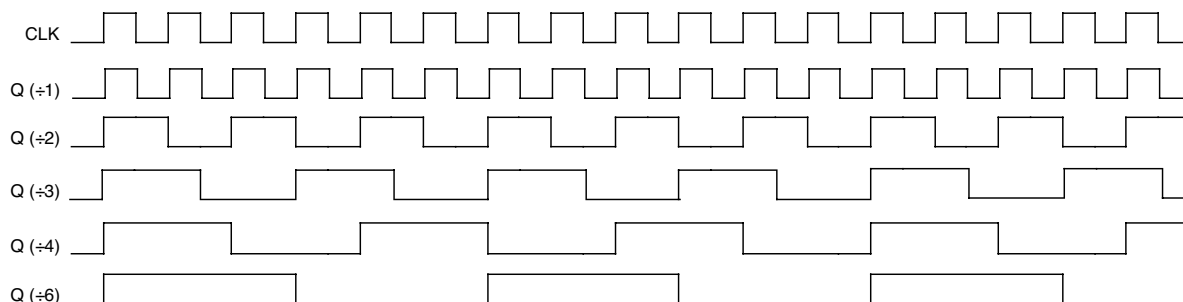
VEE = VEE (Min.) to VEE (Max.); VCC = GND

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
fMAX	Maximum Toggle Frequency	1000	—	—	1000	—	—	1000	—	—	1000	—	—	MHz
tPLH tPHL	Propagation Delay to Output CLK → Output (Diff.) CLK → Output (S.E.) MR → Q	950 900 600	— — —	1150 1200 900	950 900 600	— — —	1150 1200 900	970 920 600	— — —	1170 1220 900	1050 1000 600	— — —	1250 1300 900	ps
tskew	Within-Device Skew ⁽²⁾ Q0 — Q3	—	—	50	—	—	50	—	—	50	—	—	50	ps
	Part-to-Part Q0 — Q3 (Diff.)	—	—	200	—	—	200	—	—	200	—	—	200	ps
ts	Set-up Time EN → CLK	300	150	—	300	150	—	300	150	—	300	150	—	ps
	DIVSEL → CLK	300	—	—	300	—	—	300	—	—	300	—	—	ps
tH	Hold Time CLK → EN	400	150	—	400	150	—	400	150	—	400	150	—	ps
	CLK → DIVSEL	400	200	—	400	200	—	400	200	—	400	200	—	ps
VPP	Minimum Input Swing ⁽³⁾ CLK	250	—	—	250	—	—	250	—	—	250	—	—	mV
VCMR	Common Mode Range ⁽⁴⁾ CLK	(4)	—	-0.55	(4)	—	-0.55	(4)	—	-0.55	(4)	—	-0.55	V
tRR	Reset Recovery Time	—	—	100	—	—	100	—	—	100	—	—	100	ps
tpw	Minimum Pulse Width CLK	800	—	—	800	—	—	800	—	—	800	—	—	ps
	MR	700	—	—	700	—	—	700	—	—	700	—	—	ps
tr tf	Output Rise/Fall Times (20% —80%)	280	—	550	280	—	550	280	—	550	280	—	550	ps

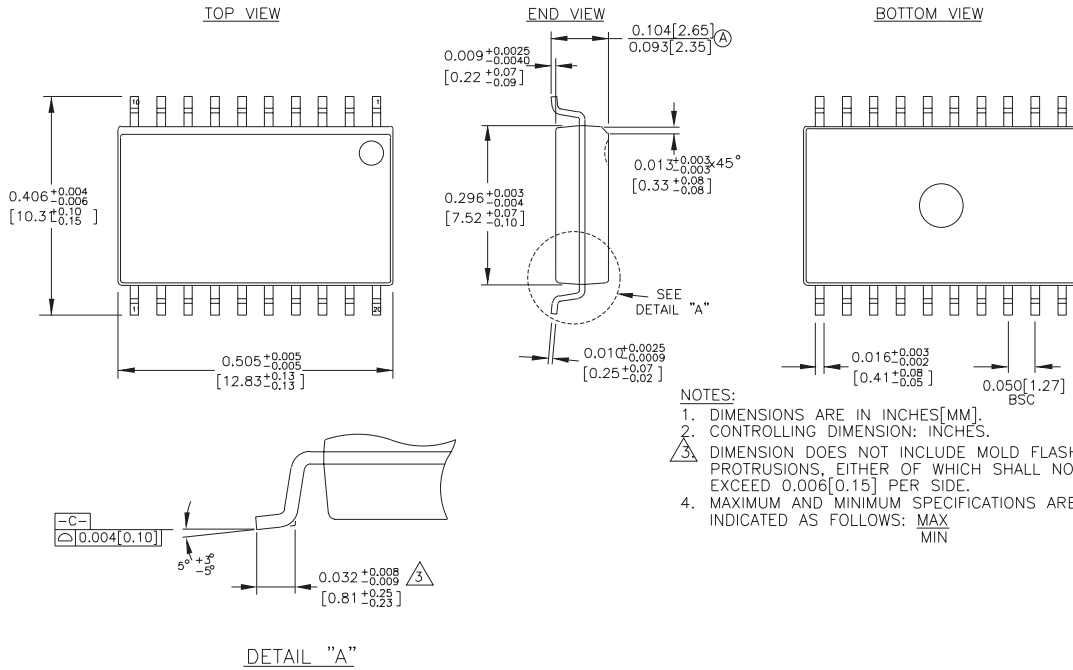
Notes:

1. Parametric values specified at: 5 volt Power Supply Range 100S838 Series: -4.2V to -5.5V.
3 volt Power Supply Range 100S838L Series -3.0V to -3.8V.
2. Skew is measured between outputs under identical transitions.
3. Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.
4. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between VPP (min) and 1.0V. The lower end of the CMR range is dependent on VEE and is equal to VEE +1.65V.

TIMING DIAGRAM



20-PIN SOIC .300" WIDE (Z20-1)



Rev. 03

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