60 Volt, 12 Amp Full-Function Load Disconnect Switch Solution

Product Description

The Cool-Switch® PI2161 is a complete full-function Load Disconnect Switch solution for medium voltage applications with a high-speed electronic circuit breaker and a very low on-state resistance MOSFET. It is designed to protect an input power bus from output load fault conditions. The PI2161 Cool-Switch solution is offered in an extremely small, thermally enhanced 7mm x 8mm LGA package. The PI2161 enables an extremely low power loss solution with fast dynamic response to an over current fault or high conditions. The PI2161 senses a small portion of the total MOSFET current and has a low voltage threshold allowing the use of low power sense resistors.

The switch is closed when the $\overline{EN}$ input is low and is open when $\overline{EN}$ is high. Once enabled, the PI2161 monitors the MOSFET current through a sense resistor. If an over current level is sensed, the switch is quickly latched off to prevent the power source from being overloaded. Bringing the $\overline{EN}$ pin high will reset the over current latch allowing retry. The PI2161 has an internal 10 kΩ bias resistor connected between the Drain (D) and VC to eliminate need for external resistor in a 44 V bus application (41 V to 48 V).

Features

- Integrated High Performance 12 A, 8.5 mΩ MOSFET
- Very small, high density fully-optimized solution with simple PCB layout
- Programmable latching over-current detection
- Fast 120ns disconnect response to load failures
- Low loss current sensing
- Fast disable via $\overline{EN}$ pin, typically 200 ns.
- Load Status output (VO scaled load voltage)

Applications

- N+1 Redundant Power Systems
- Servers & High End Computing
- Load Disconnect
- High Side Circuit Breaker

Package Information

- The PI2161 is offered in the following package:
  17-pin 7mm x 8mm thermally enhanced LGA package, achieving <10°C/W $R_{\theta J\text{-}PCB}$

Typical Application

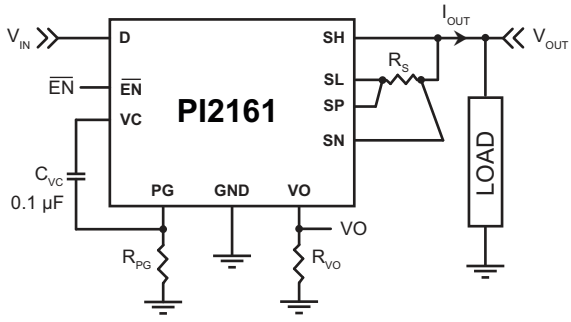


Figure 1 *— PI2161 High Side Disconnect switch*

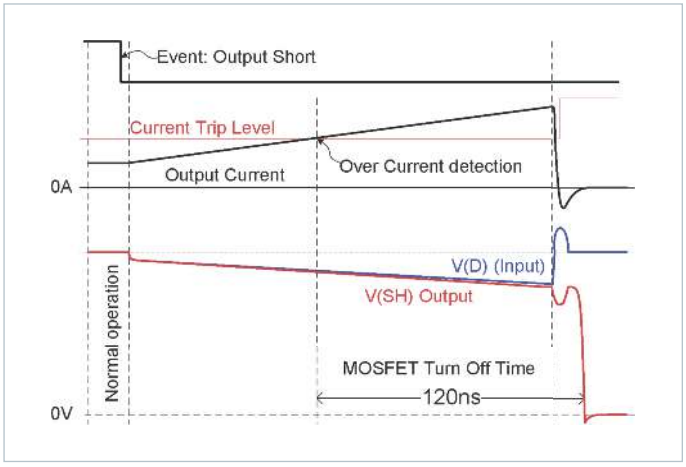


Figure 2 *— PI2161 response time to output short fault condition*

Order Information

Part Number	Package	Transport Media
PI2161-01-LGIZ	7mm x 8mm 17-pin LGA	T & R

Absolute Maximum Ratings

Note: Unless otherwise specified, all voltage nodes are referenced to "PG"

Name	Rating
Drain-to-Source Voltages (V_D to V_{SH} and V_{SL})	60 V @ 25°C
Source Current (I_{SH}+I_{SL}) Continuous	12 A @ 25°C
Source Current (I_{SH}+I_S) Pulsed (10 µs)	100 A
Source Current (I_{SH}+I_S) Pulsed (300 ns) [1]	150 A
Single Pulse Avalanche Current (TAV<11 µs) [1]	33 A
Junction-to-Ambient Thermal Resistance ($R_{\theta J\text{-}A}$)	45°C/W (0 LFM)
Junction-to-PCB Thermal Resistance ($R_{\theta J\text{-}PCB}$)	10°C/W
SH, SL, SP, SN to PG	-0.3 V to 13 V / 20 mA
SH to SL [4]	± 1.5 V
VC to PG	-0.3 V to 13 V / 10 mA
Drain (D) to PG, Drain (D) to GND	-0.3 V to 60 V / 10 mA
VO, $\overline{EN}$	-0.3 V to 60 V / 1 mA
Storage Temperature	-65°C to 150°C
Operating Junction Temperature	-40°C to 140°C
Internal MOSFET Operating Junction Temperature	-40°C to 150°C
Lead Temperature (Soldering, 20 sec)	250°C
ESD Rating	CDM Class IV

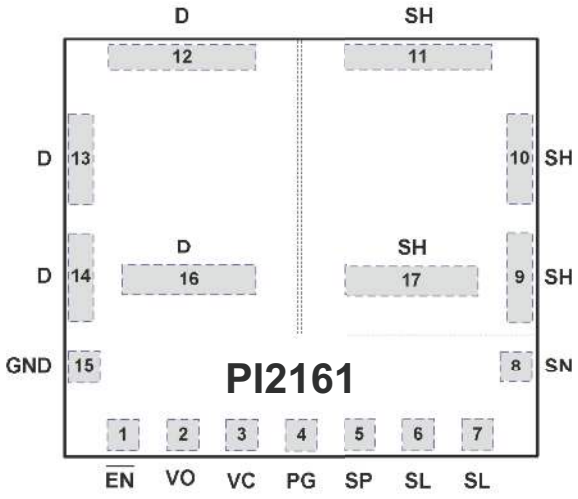
[1] These parameters are not production tested but are guaranteed by design, characterization, and correlation with statistical process control.

[4] A sense Resistor (Rs) has to be connected between SH and SL as shown in Figure 1, Rs ≤ 2 Ω.

Pin Description

Pin Number	Pin Name	Description
1	$\overline{EN}$	**Enable:** Logic level input, active low allows switch to reach 8.5 mΩ typical in the on state within 2 ms. A logic high input will turn the switch off in typically 200 ns. Leave this pin open to allow switch to turn on after application of input power.
2	VO	**Load Status Output:** This pin pulls to the load voltage once the switch is enabled through an internal 150 kΩ resistor. Connect a resistor from this pin to ground to scale the load voltage to the appropriate logic or analog level. Ground this pin if unused.
3	VC	**Voltage Bias:** This pin is the supply pin for the control circuitry and gate driver. Connect a 0.1 µF capacitor between the VC pin and the PG pin. Voltage on this pin is regulated to 11.7 V with respect to PG by an internal shunt regulator. A 10 kΩ internal resistor (R_{D-VC}) is connected between D pin and VC pin.
4	PG	**Control Circuitry Return:** PG is the floating return path for the controller circuitry. Connect this pin via a resistor to the GND (ground), as shown in Figure 1.
5	SP	**Sense-Positive Input:** Connect the SP pin to the SL pin side of the sense resistor as a Kelvin connection. The magnitude of the voltage difference between SP and SN provides an indication of the current through the sense resistor and the SL section of the MOSFET.
6,7	SL	**Source Low:** A low percentage of the internal N-channel MOSFET source current passes through this to the sense resistor. Refer to the Current Sense section in the Functional Description.
8	SN	**Sense-Negative Input:** Connect the SN pin to the SH pin side of the sense resistor as a Kelvin connection. The magnitude of the voltage difference between SP and SN provides an indication of the current through the sense resistor and the SL section of the MOSFET.
9, 10, 11, 17	SH	**Source High:** The Source of the internal N-channel MOSFET section providing the majority of the load current and alternate bias to the control circuitry.
12, 13, 14, 16	D	**Drain:** The Drain of the internal N-channel MOSFET, connect to the input power source bus voltage that provides the current to the load.
15	GND	**Ground:** This pin is the return (ground) for the enable circuitry. Connect this pin to the logic/system power ground.

Package Pin-Outs



Electrical Characteristics

Unless otherwise specified: -40°C < T_J < 125°C, V_{VC-PG} = 10.5 V, V_{PG} = V_{GND} = 0 V, C_{VC} = 0.1 µF

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Control Circuit Supply (VC to PG)						
Operating Supply Range	V_{VC-PG}	No VC limiting Resistor	8.5		10.5	V
Quiescent Current	I_{VC}	VC = 10.5 V, SP = SN = VC		1.7	2.1	mA
Quiescent Current at Start Up	I_{VCSU}	VC = 8.5 V, SP = SN = PG	2.0	2.5	3.0	mA
Clamp Voltage	V_{VC-CLM}	I_{VC} = 3 mA	11	11.7	12.5	V
Clamp Shunt Resistance	R_{SHUNT}	Delta I_{VC} = 10 mA			10	Ω
Under-Voltage Rising Threshold	V_{VCUVLO}	V_D = V_{VC} , measure when V_D = V_{SH}	6.2	7.32	8.5	V
Under-Voltage Falling Threshold	V_{VCUVF}		6	7.00	7.9	V
Under-Voltage Hysteresis	$V_{VCUV-HS}$		240	320	400	mV
Drain Supply						
Operating Supply Range	V_{VD-GND}	R_{PG} = 6 kΩ	41	44	48	V
D to VC resistance	R_{D-VC}		8	10	14	kΩ
D input UVLO Rising Threshold	$V_{VD-UVLO}$	R_{PG} = 6 kΩ, I_{SH} = -1 mA $\overline{EN}$ = 0 V	27	33	38	V
Differential Amplifier and Comparators						
Common Mode Input Voltage	V_{CM}		V_{PG}		V_{VC} +0.3	V
Differential Operating Input Voltage [1]	V_{SP-SN}	SP-SN			250	mV
SP Input Bias Current	I_{SP}	SP = SN = VC	15	25	35	µA
SN Input Bias Current	I_{SN}	SP = SN = VC	25	37	50	µA
D_{BST} Diode Forward Voltage (SN to VC)	V_{DBST}	I_{SN} = 3 mA		0.87	1.0	V
Low Range Overcurrent Threshold	V_{OC-THL}	VC-SN = 0 V	63	70	77	mV
Low Range Overcurrent Turn-off Time	T_{OC-OFF}	V_{SP-SN} = 0~200 mV step to 90% of V_{SH} max, SN = VC		120	200	ns
High Range Overcurrent Threshold	V_{OC-THH}	VC-SN = 6 V	133	166	200	mV
Overcurrent Hysteresis [1]	V_{OC-HY}		9	13	17	mV
Over Current Range switch over Threshold	V_{SOTH}	VC-SN	0.5	0.8	1	V
Over Current Range switch over delay [1]: Low to high Threshold	T_{SOL2H}	VC-SN = -0.7 V~1.7 V	100	170	300	ns
Over Current Range switch over delay: High to low threshold	T_{SOH2L}	SN-VC = -1.7 V~0.7 V	80	125	190	ns
Internal N-Channel MOSFET						
Drain-to-Source Breakdown Voltage	BV_{DSS}	I_D = 2 mA, Tj = 25°C	60			V
Source Current Continuous	I_{SH}+I_{SL}	In ON state, Tj=25°C			12	A
Drain to source Off State Current	I_{DS-OFF}	EN = 3.3 V, V_D = 44 V, V_{SH} = V_{SL} = 0 V		3.2	4.3	mA
Drain-to-Source On Resistance	R_{DSon}	In ON state, I_D = 10 A. Tj = 25°C		8.5	11	mΩ
Current Sense Ratio [3]	K_S	ISL/ (I_{SH}+I_{SL}), I_D = 10 A [4]			8	%

Electrical Characteristics (Cont.)

Unless otherwise specified: -40°C < T_J < 125°C, V_{VC-PG} = 10.5 V, V_{PG} = V_{GND} = 0 V, C_{VC} = 0.1 µF

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Schottky Diode (between PG and SH)						
D_{Clamp} Forward voltage	V_F	V_F = 10 mA, Tj = 25°C			400	mV
Load Status Voltage (VO)						
Source (SH) to VO resistance	R_{SH-VO}		142	150	158	kΩ
Source to VO leakage	I_{VOLK}				5	µA
Enable ($\overline{EN}$)						
Threshold Voltage	$V_{\overline{EN}}$		0.4		1.6	V
Input bias @ 3.3 V	$I_{\overline{EN}}$			50		µA

[1] These parameters are not production tested but are guaranteed by design, characterization, and correlation with statistical process control.

[2] Current sourced by a pin is reported with a negative sign.

[3] Refer to the Current Sense section in the Functional Description.

[4] A sense Resistor (Rs) has to be connected between SH and SL as shown in Figure 1, Rs ≤ 2 Ω.

Functional Description

The PI2161 integrated Cool-Switch product takes advantage of two different technologies combining low $R_{DS(on)}$ N-channel MOSFETs with high density control circuitry to provide a high side fast Circuit Breaker solution. The PI2161's 8.5 mΩ on state resistance MOSFET minimizes the voltage drop, at the maximum rated current of 12 A, significantly reducing power dissipation and eliminating the need for heat sinking.

As shown in the typical application Figure 1 and the block diagram Figure 5, the unique aspect of the load current sensing scheme is that only a small portion of the total MOSFET source current is routed through the sense resistor (Rs). This allows using a much lower power component compared to the conventional method of sensing the total current to the load. Figure 5, Figure 6 and Figure 7 show the PI2161 block diagram, timing diagram and state diagram respectively.

Differential Amplifier

The PI2161 integrates a high-speed fixed offset voltage differential amplifier to sense the difference between the Sense Positive (SP) pin and Sense Negative (SN) pin voltage. The amplifier output is connected to the control logic that determines the state of the fault latch. To avoid tripping the breaker due to load capacitance during initial power up, a higher threshold ($V_{OC\text{-}THH}$) is used. The amplifier will detect if the drop across the sense resistor reaches 166 mV and discharge the gate of the MOSFET if detected. Once the load voltage approaches the input potential, the threshold ($V_{OC\text{-}THL}$) is lowered to 70 mV. This allows for capacitive load charging and continuous current sensing without the use of a sense blanking timer.

Current Sense

The PI2161 internal MOSFET source is split into two portions, Source High current (SH) and Source Low current (SL). SH conducts the majority of the current and SL conducts a small portion of the load current. SL current is routed through the sense Resistor (Rs) for current sensing.

The value of the sense Resistor in the path of the sense current, will create a voltage drop and have an effect on the current ratio KS. The current ratio is expressed in the following equation as a function of $R_{DS(on)}$ and Rs.

Note that the MOSFET RDS(on) value is temperature dependent and temperature will effect the current ratio. For one $R_{DS(on)}$ value the current ratio is constant with respect to the load current. Current ratio vs. sense resistor over temperature performance is shown in Figure 3.

$$K_S = \frac{I_{SL}}{I_{Load}} = \frac{12 \bullet R_{DS(on)}}{144 \bullet R_{DS(on)} + (Rs + 17.5) \bullet (11)}$$

Where:

R_S : Sense Resistor value in [mΩ]
$R_{DS(on)}$: MOSFET ON resistance value [mΩ]
K_S: Current sense ratio
I_{SL}: SL sense current [A]
I_{Load}: Load Current [A]

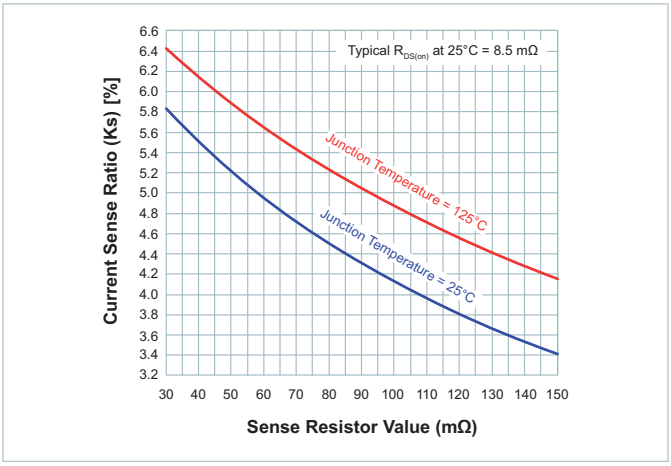


Figure 3 — *Current ratio vs. sense resistor over temperature*

Figure 4 characterizes the trip current range between 25°C and 125°C over a range of sense resistor values.

The equations and an example for calculating Rs value for a trip current level and the equation for the trip current at a given sense resistor value are provided in the Application Information section.

Enable Input ($\overline{EN}$)

This input provides control of the switch state enabling and disabling with logic level signals. The active low feature allows grounding or floating of the input resulting in switch closure upon application of input power. System control can disable the switch and reset the over current latch by pulling this pin to a logic high state.

Once enabled the load voltage will reach the input voltage in typically 1 ms and the device will sense the current continuously once the POR interval has cleared relative to the VC to PG potential. The disable control with this input is very fast, turning the switch off in typically 200 ns. The response to open during an over current event is typically 120 ns and the switch will latch off until reset by bringing this input high or recycling of the input power.

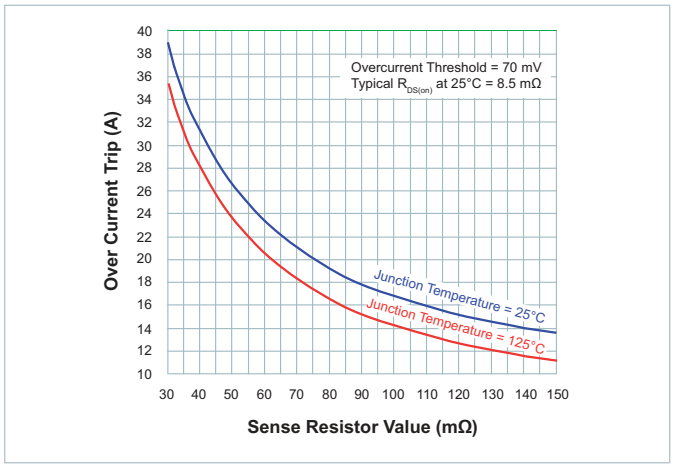


Figure 4 — *Over current trip vs. sense resistor over temperature*

VC Voltage Regulator and MOSFET Drive

The biasing scheme in the PI2161 uniquely enables the gate control relative to the PG pin via the resistor RPG shown in Figure 1. The VC input provides power to the control circuitry, the charge pump and the gate driver. An internal regulator clamps the VC voltage to 11.7 V with respect to PG.

The internal regulator circuit has a comparator to monitor VC voltage and pulls the gate low when VC to PG is lower than the VC Under-Voltage Threshold.

During start up or in a fault condition when the output (Load) is shorted, the VC pin is biased through a 10 KΩ ($R_{D\text{-}VC}$) internal resistor connected to the drain of the MOSFET. The VC pin will be biased through the load potential once the MOSFET is enabled.

In a high voltage application as shown in Figure 1 the lower bias resistor R_{PG} placed between the PG pin and system ground is required. R_{PG} creates an offset voltage at the PG pin to regulate VC with respect to PG when the MOSFET is enabled and the load voltage reaches the input voltage.

The PI2161 has an integrated charge pump that approximately doubles the regulated VC with respect to PG enhancing the N-Channel MOSFET gate to source voltage.

The internal gate driver controls the N-channel MOSFET such that in the on state, the gate driver applies current to the MOSFET gate driving it to bring the load up to the input voltage and into the $R_{DS(on)}$ condition.

When an over current condition is sensed the gate driver pulls the gate low to PG and discharges the MOSFET gate with 4 A peak capability.

Load Status (VO)

When the Gate is enabled, a 150 kΩ resistor is connected to the MOSFET source and VO. An external resistor between VO and ground creates a voltage divider that scales the load voltage down to the desired level to interface with the diagnostic circuit to represent a logic state or analog voltage level. The external resistor R_{VO} can be calculated using the following equation:

$$R_{VO} = 150K\Omega \bullet \frac{VO}{V_{SH} - VO}$$

Where:

VO : Desired voltage level at VO pin

V_{SH}: Enabled load or SH voltage

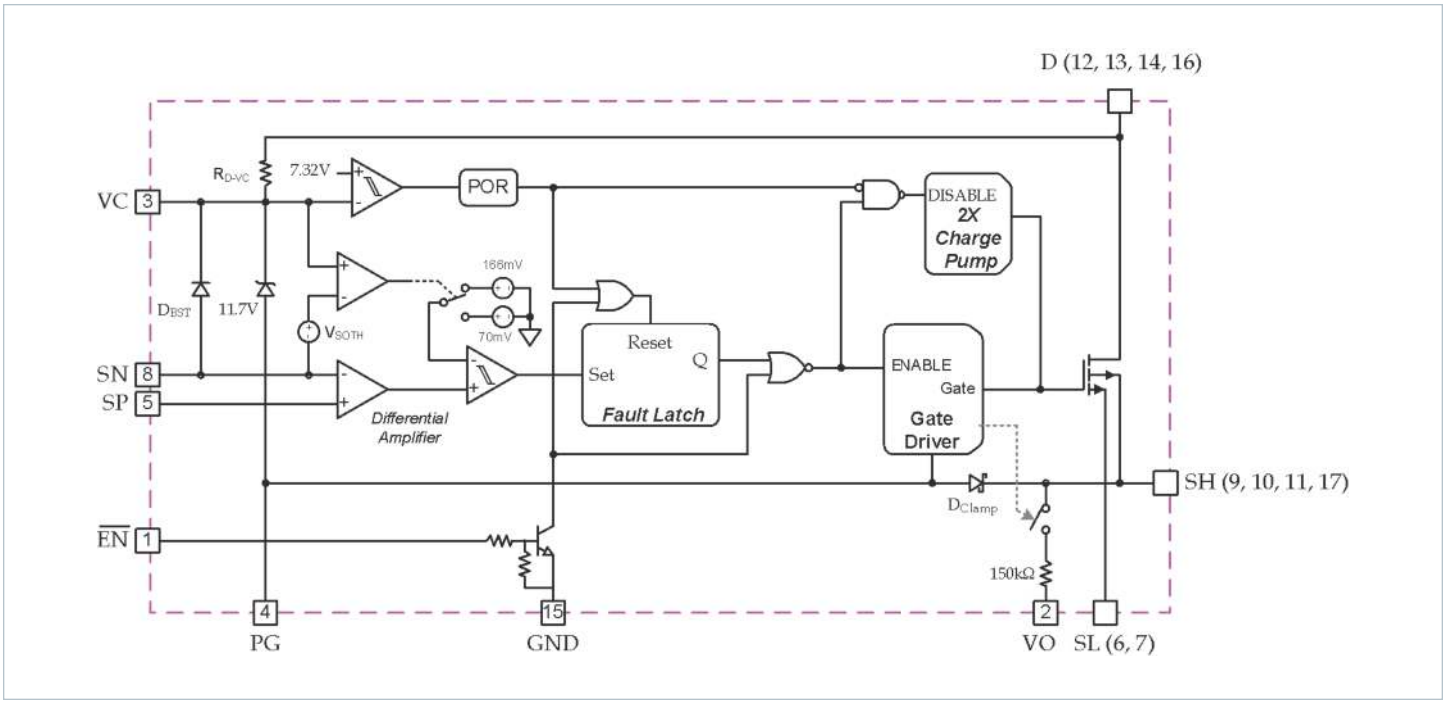


Figure 5 — *PI2161 block diagram*

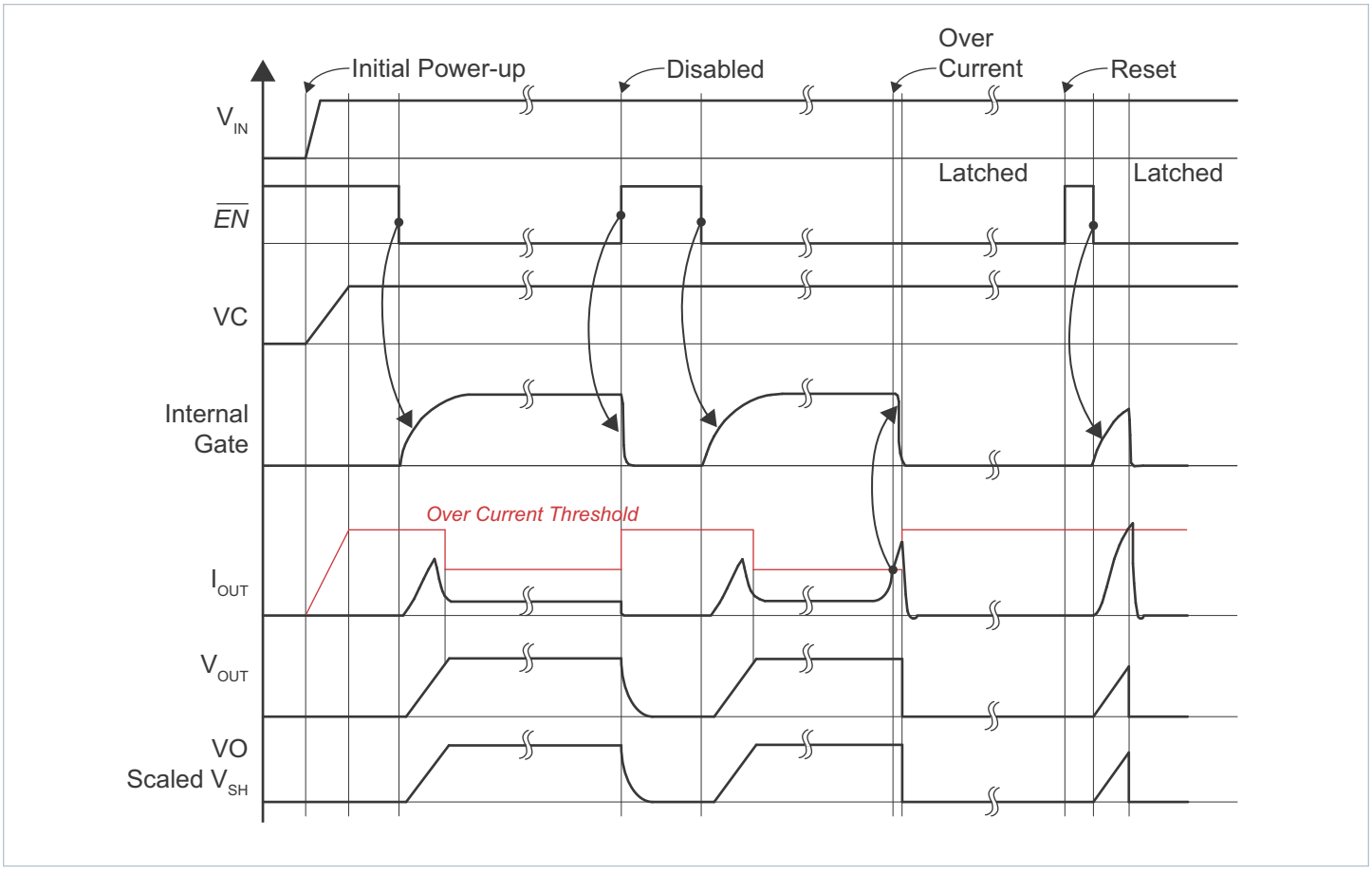


Figure 6 — *PI2161 timing diagram, referenced to Figure 1*

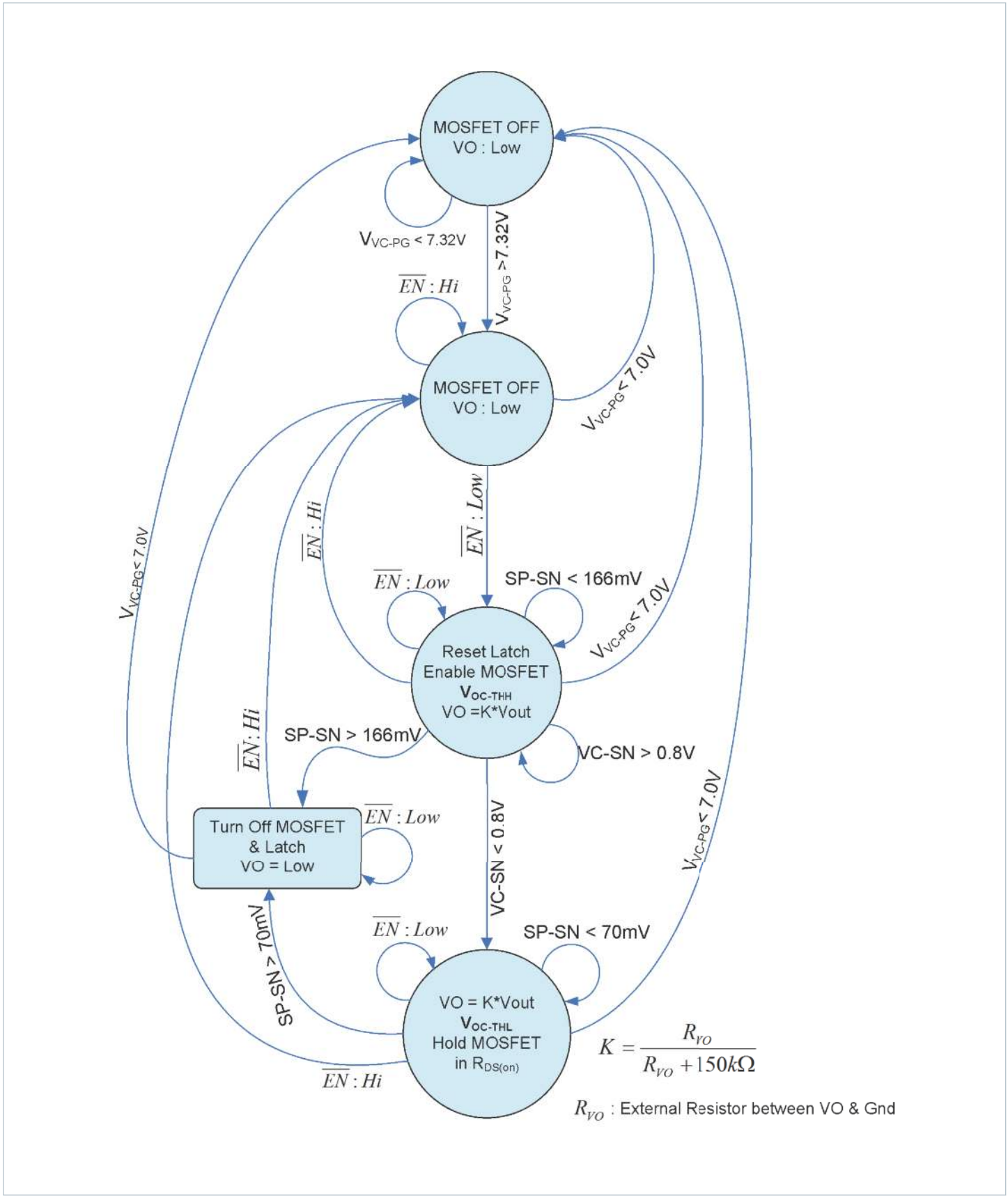


Figure 7 — *PI2161 State Diagram, referenced to Figure 1*

Typical Characteristics

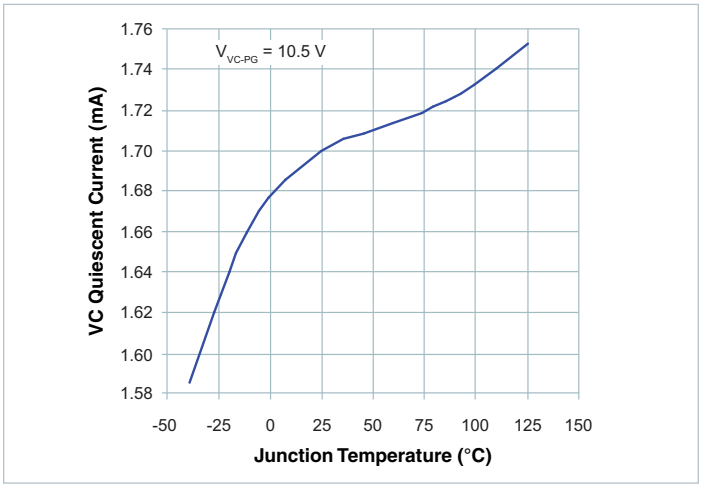


Figure 8 *— Controller bias current vs. temperature*

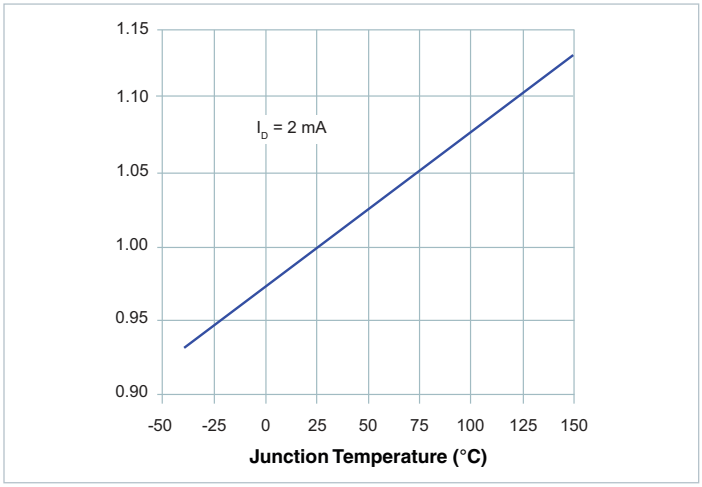


Figure 11 *— Internal MOSFET drain to source breakdown voltage vs.temperature*

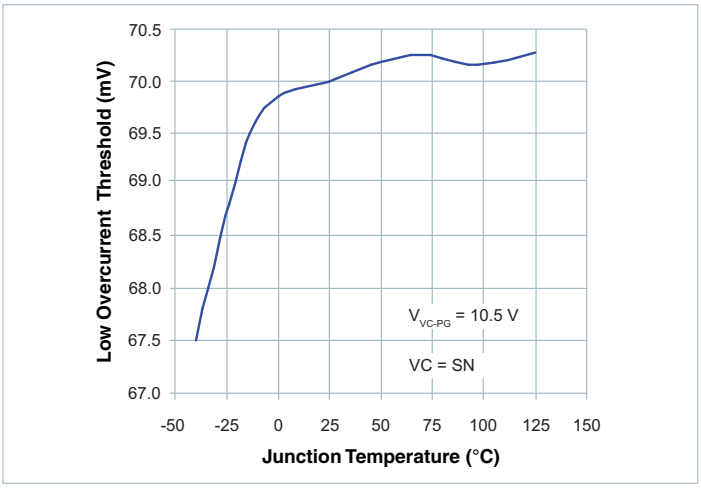


Figure 9 *— Low Range Overcurrent Threshold vs. temperature*

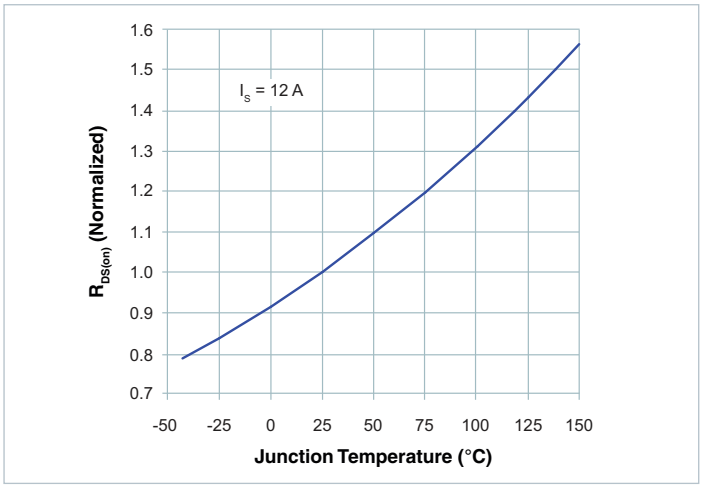


Figure 12 *— Internal MOSFET on-state resistance vs. temperature*

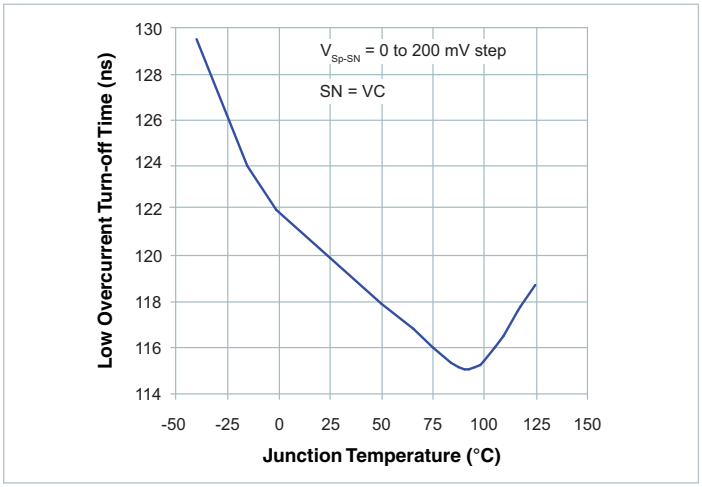


Figure 10 *— Low Range Overcurrent Turn-off time vs. temperature*

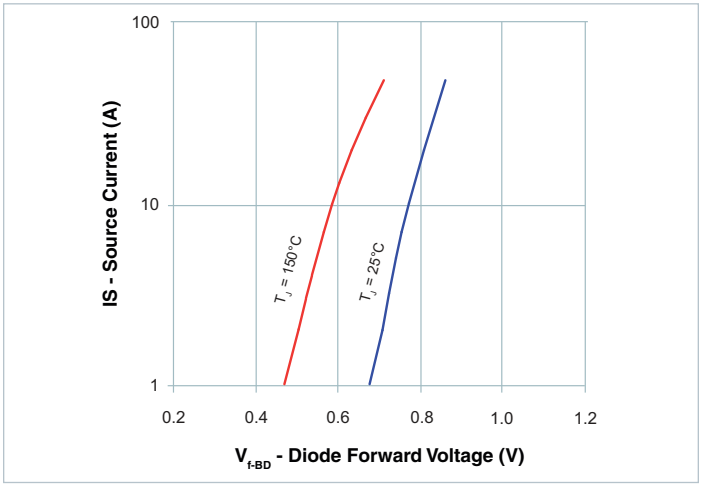


Figure 13 *— Internal MOSFET source to drain diode forward voltage (pulsed ≤300 µs).*

Thermal Characteristics

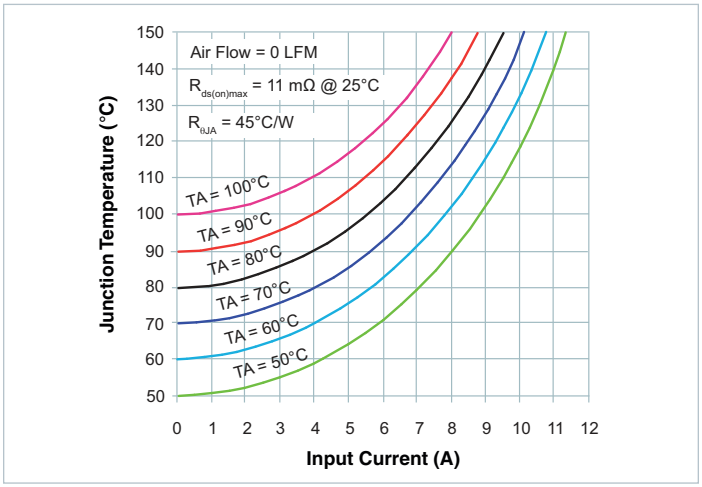


Figure 14 — *MOSFET Junction Temperature vs. Input Current for a given ambient temperature (0 LFM)*

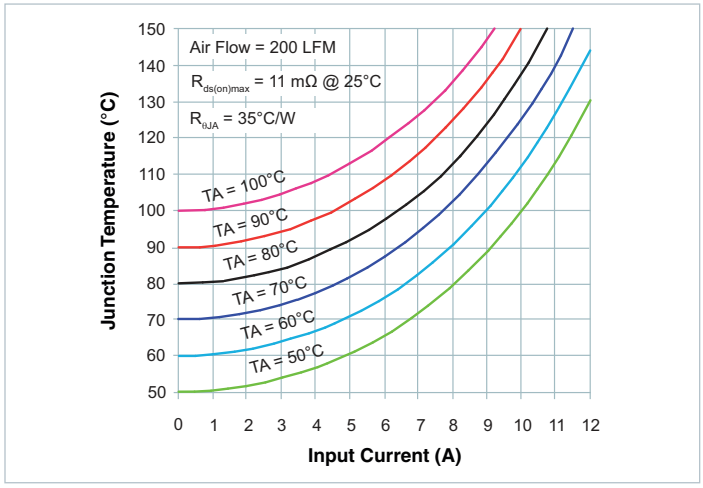


Figure 16 — *MOSFET Junction Temperature vs. Input Current for a given ambient temperature (200 LFM)*

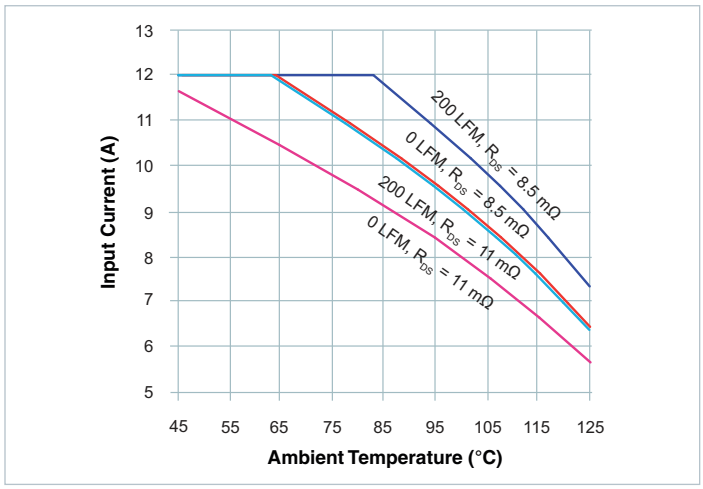


Figure 15 — *PI2161 input current de-rating based on the MOSFET maximum T_J = 150°C vs. ambient temperature*

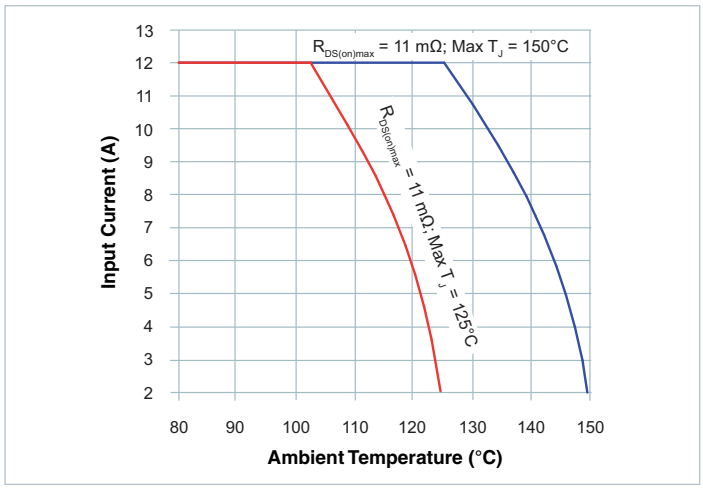


Figure 17 — *PI2161 input current de-rating vs. PCB temperature, for the MOSFET maximum T_J at 125°C and 150°C*

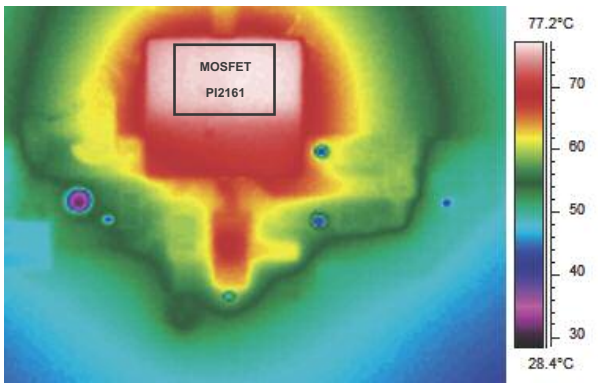


Figure 18 — *PI2161 mounted on a 1in² pad of 0.5 oz copper. Thermal Image picture, I_{OUT} = 10 A, T_A = 25°C, Air Flow = 0 LFM*

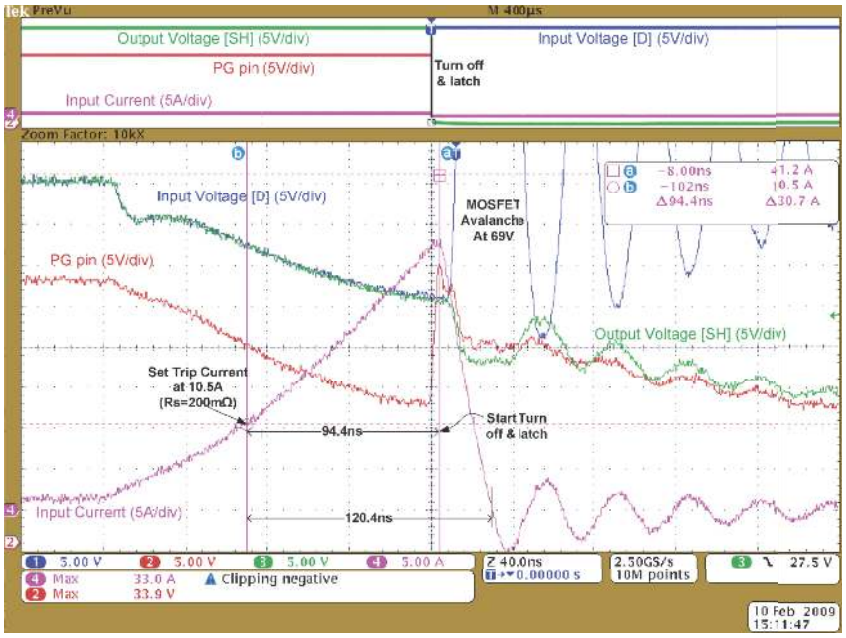


Figure 19 — *PI2161 response to an increase in load current*

Application Information

The PI2161 Cool-Switch is a medium voltage high side load disconnect switch.

This section describes in detail the procedure to follow when designing with the PI2161 load disconnect switch.

Lower Bias Resistor selection: R_{PG}

As described in Functional Description section, in a floating application as shown in Figure 1 the lower bias resistor R_{PG} placed between the PG pin and system ground is required. R_{PG} creates an offset voltage at the PG pin to regulate VC with respect to PG when the MOSFET is enabled.

The R_{PG} resistor can be calculated using the following expression:

$$R_{PG} = \frac{V_{VD-UVLO\,min} - VC_{clampMAX} - V_{DBST-MAX}}{I_{VCMAX} + 100\mu A}$$

The R_{PG} worst case condition for power dissipation is a function of the maximum BUS voltage and minimum VC clamp voltage.
Where:

$$Pd_{RPG} = \frac{(Vin_{max} - VC_{clampMIN})^2}{R_{PG}}$$

$V_{VD\text{-}UVLO\,min}$: Drain input UVLO minimum voltage, 27 V

V_{INMAX}: Vin maximum voltage, 48 V

$VC_{ClampMax}$: Controller maximum VC clamp voltage, 12.5 V

$V_{DBST\text{-}MAX}$: Maximum D_{BST} Forward Voltage, 1.0 V

$VC_{ClampMin}$: Controller minimum VC clamp voltage, 11 V

I_{VCMAX}: Controller maximum VC bias current. 2.1 mA

100 µA: 100 µA is added for a margin

Example: 41 V < V_{IN} < 48 V
Make sure that the PI2161 to turn on below the minimum required voltage, use 27 V for the minimum voltage to calculate R_{PG}.

$$R_{PG} = \frac{27V - 12.5V - 1V}{2.1mA + 100\mu A} = 6.136K\Omega \text{ or } 6.04K\Omega$$

$$Pd_{RPG} = \frac{(48V - 11V)^2}{6.04K\Omega} = 227mW$$

Enable Input: (~~EN~~)

This input provides control of the switch state enabling and disabling with logic level signals.

Current Sense Resistor Selection: Rs

The Rs value can be selected from Figure 4 to set the nominal trip current at junction temperature for internal MOSFET of 25°C or 125°C. To set the minimum trip current at specific junction temperature use the following procedure.

The current trip point is a function of the Low Range Overcurrent Threshold ($V_{OC\text{-}THL}$), the internal MOSFET on resistance ($R_{DS(on)}$) and current sense resistor (Rs). To insure that PI2161 will not trip within the expected nominal operating current range, include the variation of $V_{OC\text{-}THL}$ and $R_{DS(on)}$ in the calculation when selecting Rs. $V_{OC\text{-}THL}$ is 70 mV typical, 63 mV minimum and 77 mV maximum. The $R_{DS(on)}$ typical value at 25°C is 8.5 mΩ and 11 mΩ maximum. $R_{DS(on)}$ will increase with temperature as shown in Figure 12, and can be calculated by multiplying the $R_{DS(on)}$ value at 25°C by the normalized factor in Figure 12 at the expected operating junction temperature or use the following equation:

$$R_{DS(on)}(T_J) = R_{DS(on)}(25°C) \bullet \left(0.873 \bullet e^{3.75 \bullet T_J \bullet 10^{-3}} + 0.041\right)$$

Where:

T_J: Internal MOSFET Junction temperature
$R_{DS(on)}$: Internal MOSFET $R_{DS(on)}$ at T_J in °C
$R_{DS(on)}$: Internal MOSFET $R_{DS(on)}$ at T_J = 25°C

The sense resistor can be calculated from the following equation as a function of the trip current:

$$Rs = \frac{V_{OC\_THL} \bullet \left(144 \bullet R_{DS(on)} + 192.5\right)}{12 \bullet I_{TRIP} \bullet R_{DS(on)} - 11 \bullet V_{OC\_THL}}$$

And the trip current can be calculated from the following equation:

$$I_{TRIP} = \frac{V_{OC\_THL} \bullet \left(144 \bullet R_{DS(on)} + 11 \bullet (Rs + 17.5)\right)}{12 \bullet Rs \bullet R_{DS(on)}}$$

Sense resistor Maximum power dissipation is:

$$Pd_{RS} = \frac{V_{TH-MAX}^{\ 2}}{Rs}$$

Where:

Rs: Current sense resistor [mΩ]
I_{TRIP}: Current trip point [A]
V_{OC_THL}: Low Range Overcurrent Threshold [mV], 63 mV minimum
V_{TH-MAX}: Maximum Overcurrent Threshold [mV], 77 mV

Current trip calculation example:

Minimum current tripping point = 12 A

Maximum MOSEFET junction temperature = 100°C.

The lowest tripping current will occur at the internal MOSFET maximum $R_{DS(on)}$ and its maximum junction temperature, and minimum Low Range Overcurrent Threshold (V_{OC-THL}).

The MOSET maximum $R_{DS(on)}$ is 11mΩ at 25°C and at maximum junction temperature will be:

$$R_{DS(on)}(100) = 11m\Omega \bullet \left(0.873 \bullet e^{3.75 \bullet 100 \bullet 10^{-3}} + 0.041\right)$$

$$R_{DS(on)}(100) = 14.42m\Omega$$

Select Rs at minimum V_{OC-THL} =63 mV

$$Rs = \frac{63 \bullet \left(144 \bullet 14.42 + 192.5\right)}{12 \bullet 12 \bullet 14.42 - 11 \bullet 63} = 103.32m\Omega$$

Rs maximum power dissipation:

$$Pd_{RS} = \frac{V_{TH-MAX}^{\ 2}}{Rs} = \frac{0.077^2}{0.103} = 57.6mW$$

This is a low power dissipation resistor and any package size work as far by selecting the nearest standard value. The closest resistor available value in 1% accuracy in an 0603 or 0805 package is 0.10 Ω (100 mΩ).

If 0603 0.10 Ω 1% resistor selected, then the minimum trip current is:

$$I_{TRIP} = \frac{63 \bullet \left(144 \bullet 14.42 + 11 \bullet (100 + 17.5)\right)}{12 \bullet 100 \bullet 14.42} = 12.26A$$

Internal N-Channel MOSFET BV_{DSS}

The PI2161's internal N-Channel MOSFET breakdown voltage (BV_{DSS}) is rated for 60 V at 25°C and will degrade to 55.5 V at -40°C, refer to Figure 11. Drain to source voltage should not exceed BV_{DSS} in nominal operation. During a fast switching transient the MOSFET can tolerate voltages higher than its BV_{DSS} rating under avalanche conditions. Refer to the Absolute Maximum Ratings table.

In load disconnect switch applications when the load is shorted, a large current is sourced from the input supply through the MOSFET. Depending on the input impedance of the system and the parasitic inductance, the current in the MOSFET may exceed the source pulsed current rating (150 A) just before the PI2161 MOSFET is turned off.

The peak current during an output short condition is calculated as follows, assuming that the output has very low impedance and it is not a limiting factor:

$$I_{PEAK} = \frac{V_D \bullet t_{OC-OFF}}{L_{PARASITIC}}$$

Where:

I_{PEAK}: Peak current in PI2161 MOSFET before it is turned off
V_D: Input voltage or load voltage at D pin before input short condition did occur
t_{OC-OFF}: Low Range Overcurrent Turn-off Time.
$L_{PARASITIC}$: Circuit parasitic inductance

The high peak current during an output short and before the MOSFET turns off, stores energy in the circuit parasitic inductance, and as soon as the MOSFET turns off, the stored energy at the drain side of the internal MOSFET will be released to produce a voltage higher than the input voltage while the MOSFET source is at ground. This event will create a high voltage difference between the drain and source of the MOSFET. ***The MOSFET will avalanche, but this avalanche will not affect the MOSFET performance because the PI2161 has a fast response time to the input fault condition and the stored energy will be well below the MOSFET avalanche capability.***

MOSFET avalanche energy during an output short event is calculated as follows:

$$E_{AS} = \frac{1}{2} \bullet \frac{1.3 \bullet BV_{DSS}}{1.3 \bullet BV_{DSS} - V_S} \bullet L_{PARASITIC} \bullet I_{PEAK}^{\ 2}$$

Where:

E_{AS}: Avalanche energy
BV_{DSS}: MOSFET maximum rated voltage (60 V)

Power dissipation

In Load Disconnect Switch applications, the MOSFET is on in steady state operation and the power dissipation is derived from the total source current and the on-state resistance of the MOSFET.

The PI2161 internal MOSFET power dissipation can be calculated with the following equation:

$$Pd_{MOSFET} = Is^2 \bullet R_{DS(on)}$$

Where:

Is: Source Current

Pd_{MOSFET}: MOSFET power dissipation

$R_{DS(on)}$: MOSFET on-state resistance

Note: For the worst case condition, calculate with maximum rated $R_{DS(on)}$ at the MOSFET maximum operating junction temperature because $R_{DS(on)}$ is temperature dependent. Refer to Figure 12 for normalized $R_{DS(on)}$ values over temperature. The PI2161 maximum $R_{DS(on)}$ at 25°C is 11 mΩ and will increase by 43% at 125°C junction temperature.

The Junction Temperature rise is a function of power dissipation and thermal resistance.

$$Trise = R_{\theta JA} \bullet Pd_{MOSFET} = R_{\theta JA} \bullet Is^2 \bullet R_{DS(on)}$$

Where:

R_{qJA}: Junction-to-Ambient thermal resistance (45°C/Watt)

This calculation may require iteration to get to the final junction temperature. Figure 14 and Figure 16 show the PI2161 internal MOSFET final junction temperature curves versus conducted current at maximum $R_{DS(on)}$, given ambient temperatures and air flow.

Load Status Resistor Selection: (R_{VO})

R_{VO} can be calculated using the following equation:

$$R_{VO} = 150K\Omega \bullet \frac{VO}{V_{SH} - VO}$$

Typical Application Example

Load Disconnect Switch Requirement

Bus Voltage = 45 V ±5 V
Maximum Load Operating Current = 9 A
Minimum Trip Current = 10 A
Maximum Ambient Temperature = 60°C, no air flow (0 LFM)
The current flow parasitic inductance is 60 nH.
System logic voltage is 3.3 V and logic high = 2.0 V

Solution

In this application, PI2161 is used to protect the power source from load failure, configured as shown in the circuit schematic in Figure 21.

R_{PG} Selection

For a margin purpose, select R_{PG} to operate at input voltage below the required operating voltage, use 27 V minimum operating voltage:

$$R_{PG} = \frac{V_{VD-UVLO\,min} - VC_{clampMAX} - V_{DBST-MAX}}{I_{VCMAX} + 100\mu A}$$

$$R_{PG} = \frac{27V - 12.5V - 1V}{2.1mA + 0.1mA} = 6.136k\Omega$$

The closest 1% resistor available is 6.04 kΩ, R_{PG} power dissipation will be:

$$PdR_{PG} = \frac{(V_{S-max} - V_{S-PGMin})^2}{R_{PG}} = \frac{(50V - 11V)^2}{6.04k\Omega} = 252mW$$

The selected resistor should be capable of supporting the total power at maximum operating temperature, 60°C. An 0805 (2012) will support the power requirement.

VO pin

In this application use the minimum voltage output VSH = 40 V, and for VO use the logic high voltage (2.0 V) with margin, VO = 2.1 V

$$R_{VO} = 150K\Omega \bullet \frac{2.1V}{40V - 2.1V} = 8.3K\Omega$$

Closest 1% resistor is 8.45 kΩ to the high side Calculate VO at V_{SH} = 40 V and R_{VO}=8.45 kΩ

$$VO = V_{SH} \bullet \frac{R_{VO}}{150K\Omega + R_{VO}}$$

$$VO = 40V \bullet \frac{8.45K\Omega}{150K\Omega + 8.45K\Omega} = 2.133\ V$$

Power Dissipation and Junction Temperature

First use Figure 14 (MOSFET Junction Temperature vs. Input Current) to find the final junction temperature for 9 A load current at 60°C ambient temperature. In Figure 14 (illustrated in Figure 20) draw a vertical line from 9 A to intersect the 60°C ambient temperature line. At the intersection draw a horizontal line towards the Y-axis (Junction Temperature). The Junction Temperature at maximum load current (9 A) and 60°C ambient is 115°C.

$R_{DS(on)}$ is 11 mΩ maximum at 25°C and will increase as the Junction temperature increases. From Figure 12, at 115°C $R_{DS(on)}$ will increase by 38%, then maximum at 115°C.

Maximum power dissipation is:

$$Pd_{max} = Iin^2 \bullet R_{DS(on)} = (9A)^2 \bullet 15.18m\Omega = 1.23W$$

Recalculate T_J:

$$T_{J\,max} = 60°C + \left(\frac{45°C}{W} * (9A)^2 \bullet 15.18m\Omega\right) = 115.3°C$$

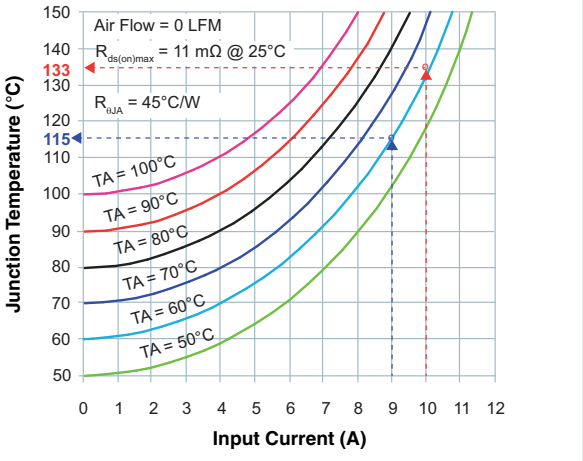


Figure 20 *— Example 1 final MOSFET junction temperature at 9 A/60°C T_A*

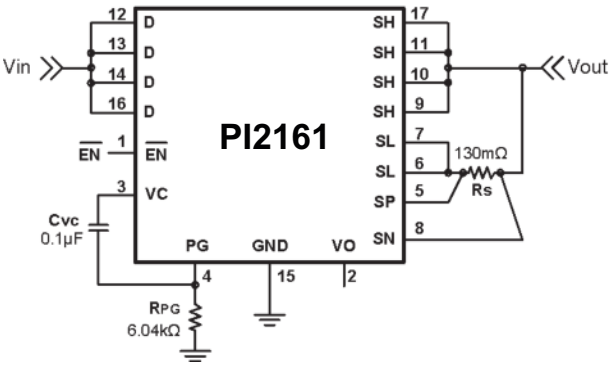


Figure 21 *— PI2161 configured for 10A minimum trip current*

Select Rs

The minimum trip current will occur at maximum MOSFET junction temperature and $V_{OC\text{-}THL}$ = 63 mV: MOSFET Junction Temperature for 10 A at 60°C can be estimated using the graph in Figure 14 as illustrated in Figure 20. Draw a vertical line from 10 A to intersect the 60°C ambient temperature line. At the intersection draw a horizontal line towards the Y-axis (Junction Temperature). The Junction Temperature at maximum load current (10 A) and 60°C ambient is 133°C.

$$R_{DS(on)}(T_J) = R_{DS(on)}(25°C) \bullet \left(0.873 \bullet e^{3.75 \bullet Tj \bullet 10^{-3}} + 0.041\right)$$

$$R_{DS(on)}(133) = 11m\Omega \bullet \left(0.873 \bullet e^{3.75 \bullet 133 \bullet 10^{-3}} + 0.041\right)$$

$$R_{DS(on)}(133) = 16.26m\Omega$$

$$Rs = \frac{V_{OC\_THL} \bullet \left(144 \bullet R_{DS(on)} + 192.5\right)}{12 \bullet I_{TRIP} \bullet R_{DS(on)} - 11 \bullet V_{OC\_THL}}$$

$$Rs = \frac{63 \bullet \left(144 \bullet 16.26 + 192.5\right)}{12 \bullet 10 \bullet 16.26 - 11 \bullet 63} = 126.9m\Omega$$

The closest 1% resistor available off-the-shelf is 130 mΩ.

The minimum trip current is:

$$I_{TRIP} = \frac{V_{OC\_THL} \bullet \left(144 \bullet R_{DS(on)} + 11 \bullet (Rs + 17.5)\right)}{12 \bullet Rs \bullet R_{DS(on)}}$$

$$I_{TRIP} = \frac{63 \bullet \left(144 \bullet 16.26 + 11 \bullet (130 + 17.5)\right)}{12 \bullet 130 \bullet 16.26} = 9.85A$$

Layout Recommendation

Use the following general guidelines when designing printed circuit boards. An example of the typical land pattern for the PI2161 is shown in Figure 22.

- Use a solid ground (return) plane to reduce circuit parasitic.
- Connect Rs terminal at SN pin side and all S pads together with a wide trace to reduce trace parasitics and to accommodate the high current output, and also connect all D pads together with a wide trace to accommodate the high current input.
- Kelvin connect SP pin and SN pin to Rs terminals to the S pins.
- Connect SL pins together with a wide trace connect them to Rs.
- Place C_{VC} very close to PI2161 to have very short traces to PI2161 pins without any PCB via in between.
- Use 1oz of copper or thicker if possible to reduce trace resistance and reduce power dissipation.

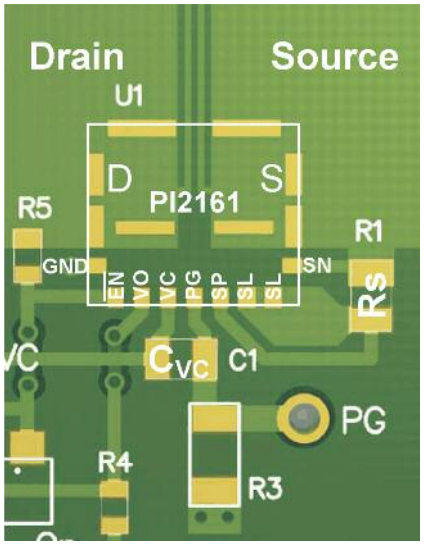
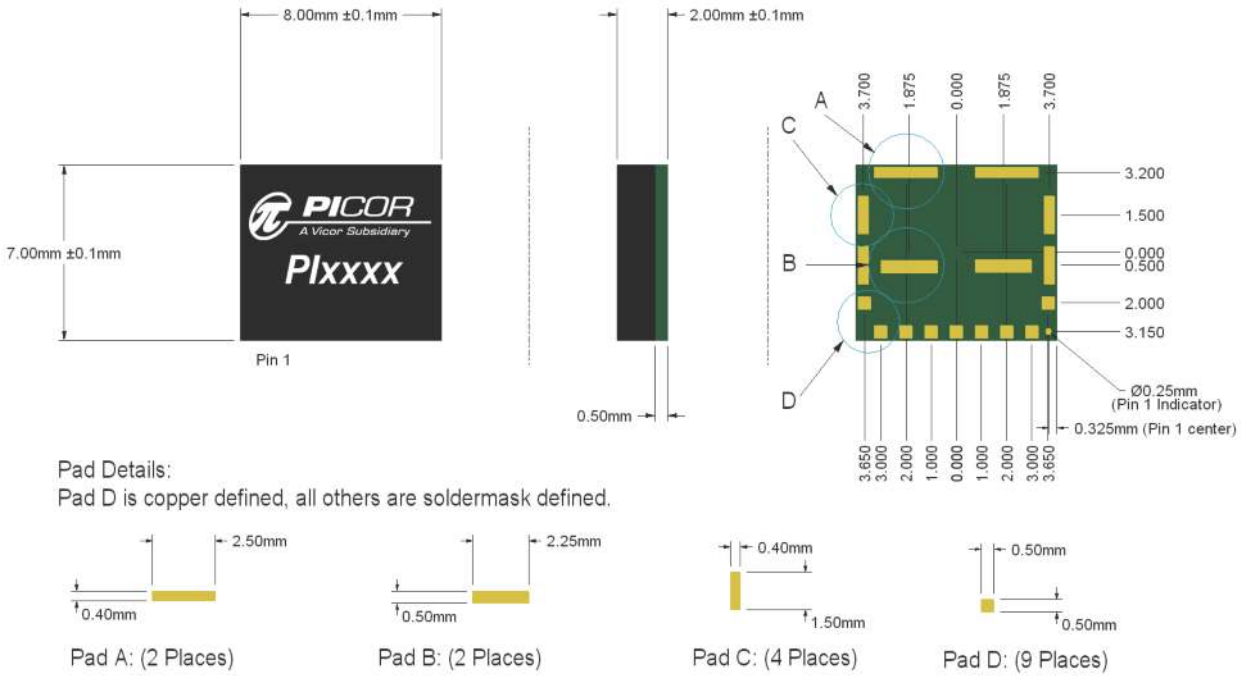
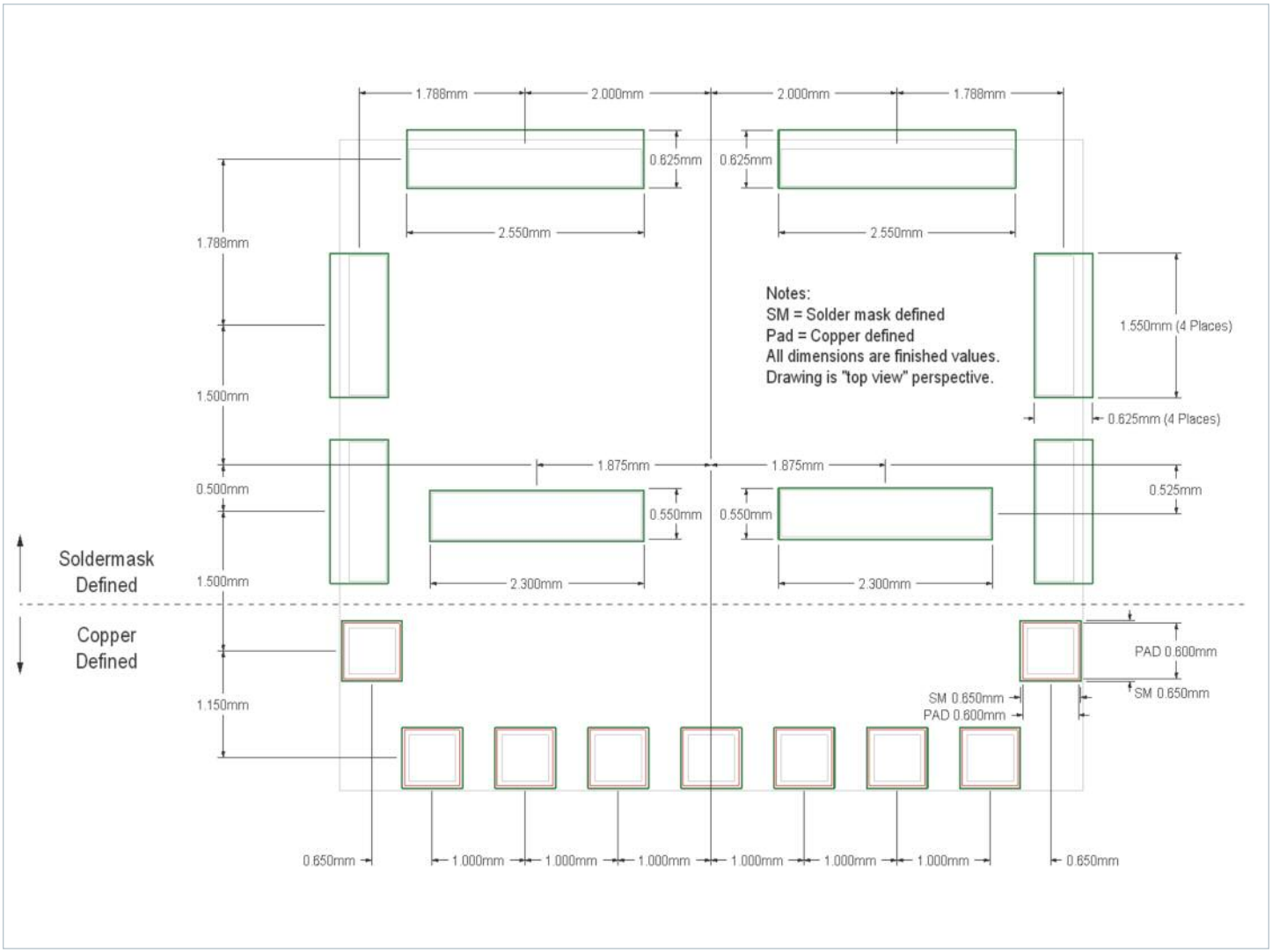


Figure 22 *— PI2161 layout recommendation*

Package Drawings



Footprint Recommendation



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