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# Preliminary User's Manual

# $\mu$ PD78F9510, 78F9511, 789512

## 8-bit Single-Chip Microcontrollers

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$\mu$ PD78F9510

$\mu$ PD78F9511

$\mu$ PD78F9512

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[MEMO]

## NOTES FOR CMOS DEVICES

### ① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).

### ② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

### ③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

### ④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

### ⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

### ⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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## INTRODUCTION

**Target Readers** This manual is intended for user engineers who wish to understand the functions of the  $\mu$ PD78F9510, 78F9511, 78F9512 in order to design and develop its application systems and programs.

**Purpose** This manual is intended to give users on understanding of the functions described in the **Organization** below.

**Organization** Two manuals are available for  $\mu$ PD78F9510, 78F9511, 78F9512: this manual and the Instruction Manual (common to the 78K0S microcontroller).

$\mu$ PD78F9510, 78F9511, 78F9512 User's Manual
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- Pin functions
- Internal block functions
- Interrupts
- Other internal peripheral functions
- Electrical specifications

78K/0S Series Instructions User's Manual
--

- CPU function
- Instruction set
- Instruction description

**How to Use This Manual** It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- ◇ To understand the overall functions of  $\mu$ PD78F9510, 78F9511, 78F9512  
→ Read this manual in the order of the **CONTENTS**.
- ◇ How to read register formats  
→ For a bit number enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0S, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0S.
- ◇ To learn the detailed functions of a register whose register name is known  
→ See **APPENDIX C REGISTER INDEX**.
- ◇ To learn the details of the instruction functions of the 78K0S microcontroller  
→ Refer to **78K/0S Series Instructions User's Manual (U11047E)** separately available.
- ◇ To learn the electrical specifications of the  $\mu$ PD78F9510, 78F9511, 78F9512  
→ See **CHAPTER 17 ELECTRICAL SPECIFICATIONS (TARGET)**.



**Conventions**

Data significance: Higher digits on the left and lower digits on the right  
Active low representation:  $\overline{\quad}$  (overscore over pin or signal name)  
**Note:** Footnote for item marked with **Note** in the text  
**Caution:** Information requiring particular attention  
**Remark:** Supplementary information  
Numerical representation: Binary ... or B  
Decimal ...  
Hexadecimal ... H

**Related Documents**

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

**Documents Related to Devices**

Document Name	Document No.
PD78F9510, 78F9511, 78F9512 User's Manual	This manual
78K/0S Series Instructions User's Manual	U11047E

**Documents Related to Development Software Tools (User's Manuals)**

Document Name	Document No.	
RA78K0S Assembler Package	Operation	U16656E
	Language	U14877E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U16654E
	Language	U14872E
ID78K0S-NS Ver. 2.52 Integrated Debugger	Operation	U16584E
ID78K0S-QB Ver. 2.81 Integrated Debugger	Operation	U17287E
PM plus Ver.5.20		U16934E

**Documents Related to Development Hardware Tools (User's Manuals)**

Document Name	Document No.
IE-78K0S-NS In-Circuit Emulator	U13549E
IE-78K0S-NS-A In-Circuit Emulator	U15207E
QB-78K0SKX1MINI In-Circuit Emulator	U17272E

**Caution** The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

### Documents Related to Flash Memory Writing

Document Name	Document No.
PG-FP4 Flash Memory Programmer User's Manual	U15260E
PG-FPL2 Flash Memory Programmer User's Manual	U17307E

### Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE - Products and Packages -	X13769X
Semiconductor Device Mount Manual	<b>Note</b>
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

**Note** See the "Semiconductor Device Mount Manual" website (<http://www.necel.com/pkg/en/mount/index.html>).

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## CHAPTER 1 OVERVIEW

### 1.1 Features

○ 78K0S CPU core

○ ROM and RAM capacities

Part number \ Item	Program Memory (Flash Memory)	Memory (Internal High-Speed RAM)
$\mu$ PD78F9510	1 KB	128 bytes
$\mu$ PD78F9511	2 KB	
$\mu$ PD78F9512	4 KB	

○ Minimum instruction execution time: 0.2  $\mu$ s (with 10 MHz@4.0 to 5.5 V operation)

○ Clock

- High-speed system clock ... Selected from the following two sources
  - Ceramic/crystal resonator: 1 to 10 MHz
  - High-speed internal oscillator: 8 MHz  $\pm$ 3% (-10 to +70°C), 8 MHz  $\pm$ 5% (-40 to +85°C)
- Low-speed internal oscillator 240 kHz (TYP.) ... Watchdog timer, timer clock in intermittent operation

○ I/O ports: 14 (CMOS I/O: 13, CMOS input: 1)

○ Timer: 3 channels

- 16-bit timer/event counter: 1 channel ... Timer output  $\times$  1, capture input  $\times$  2
- 8-bit timer: 1 channel ... PWM output  $\times$  1
- Watchdog timer: 1 channel ... Operable with low-speed internal oscillation clock

○ On-chip power-on-clear (POC) circuit (A reset is automatically generated when the voltage drops to 2.1 V  $\pm$ 0.1 V or below)

○ On-chip low voltage detector (LVI) circuit (An interrupt/reset (selectable) is generated when the detection voltage is reached)

- Detection voltage: Selectable from ten levels between 2.35 and 4.3 V

○ Single-power-supply flash memory

- Flash self programming enabled
- Software protection function: Protected from outside party copying (no flash reading command)
- Time required for writing by dedicated flash memory programmer: Approximately 3 seconds (4 KB)
  - \* Write operations on mass production lines supported

○ Safety function

- Watchdog timer operated by clock independent from CPU
  - ... A hang-up can be detected even if the system clock stops
- Supply voltage drop detectable by LVI
  - ... Appropriate processing can be executed before the supply voltage drops below the operation voltage
- Equipped with option byte function
  - ... Important system operation settings set in hardware

○ Assembly and C language supported

○ Enhanced development environment

- Support for full-function emulator (IECUBE), simplified emulator (MINICUBE2), and simulator

○ Supply voltage:  $V_{DD} = 2.0$  to 5.5 V

- \* Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage ( $V_{POC}$ ) of the power-on-clear (POC) circuit is 2.1 V  $\pm$ 0.1 V.

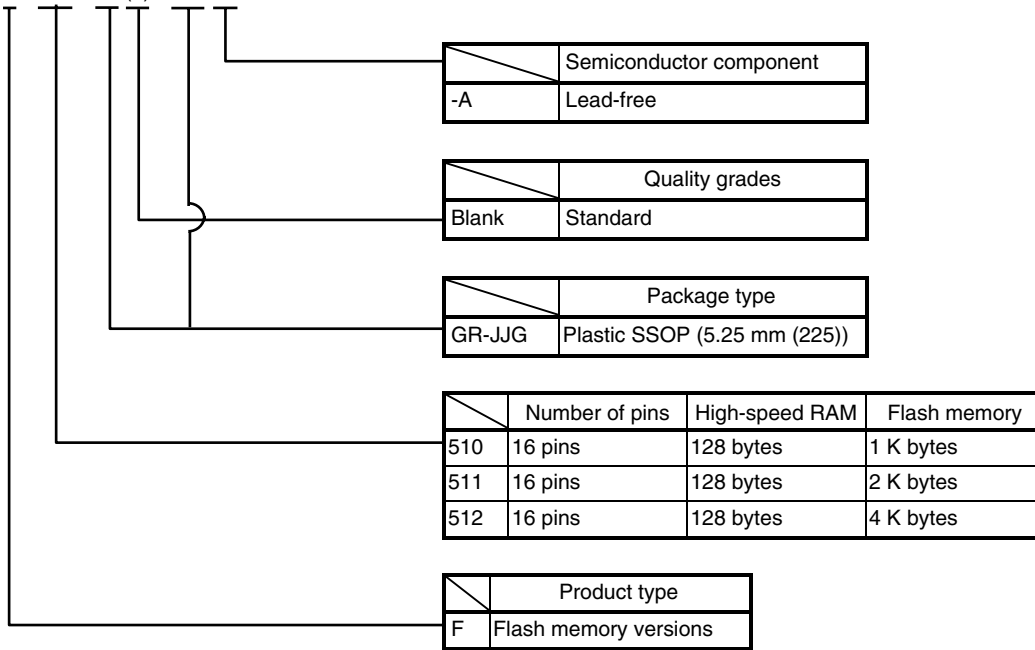
○ Operating temperature range:  $T_A = -40$  to +85°C



## 1.2 Ordering Information

Part Number

$\mu$ PD78F9 xxx - xx (x) - xxx -A



**[Part number list]**

$\mu$ PD78F9510GR-JJG-A<sup>Note</sup>

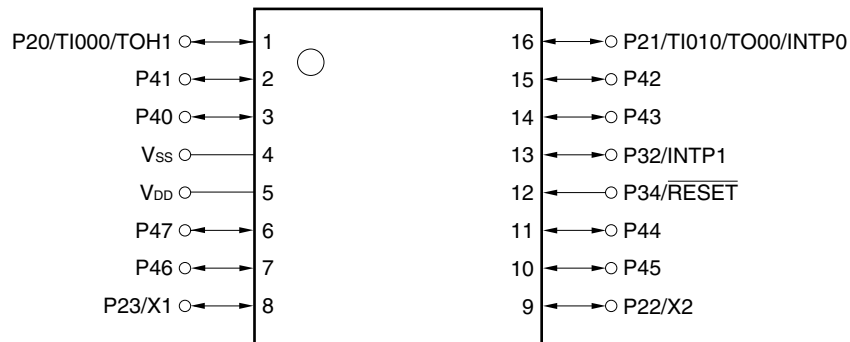
$\mu$ PD78F9511GR-JJG-A<sup>Note</sup>

$\mu$ PD78F9512GR-JJG-A<sup>Note</sup>

**Note** Under development

### 1.3 Pin Configuration (Top View)

16-pin plastic SSOP



INTP0, INTP1:	External interrupt input	TI000, TI010:	Timer input
P20 to P23:	Port 2	TO00, TOH1:	Timer output
P32, P34:	Port 3	V <sub>DD</sub> :	Power supply
P40 to P47:	Port 4	V <sub>SS</sub> :	Ground
$\overline{\text{RESET}}$ :	Reset	X1, X2:	Crystal oscillator (X1 input clock)

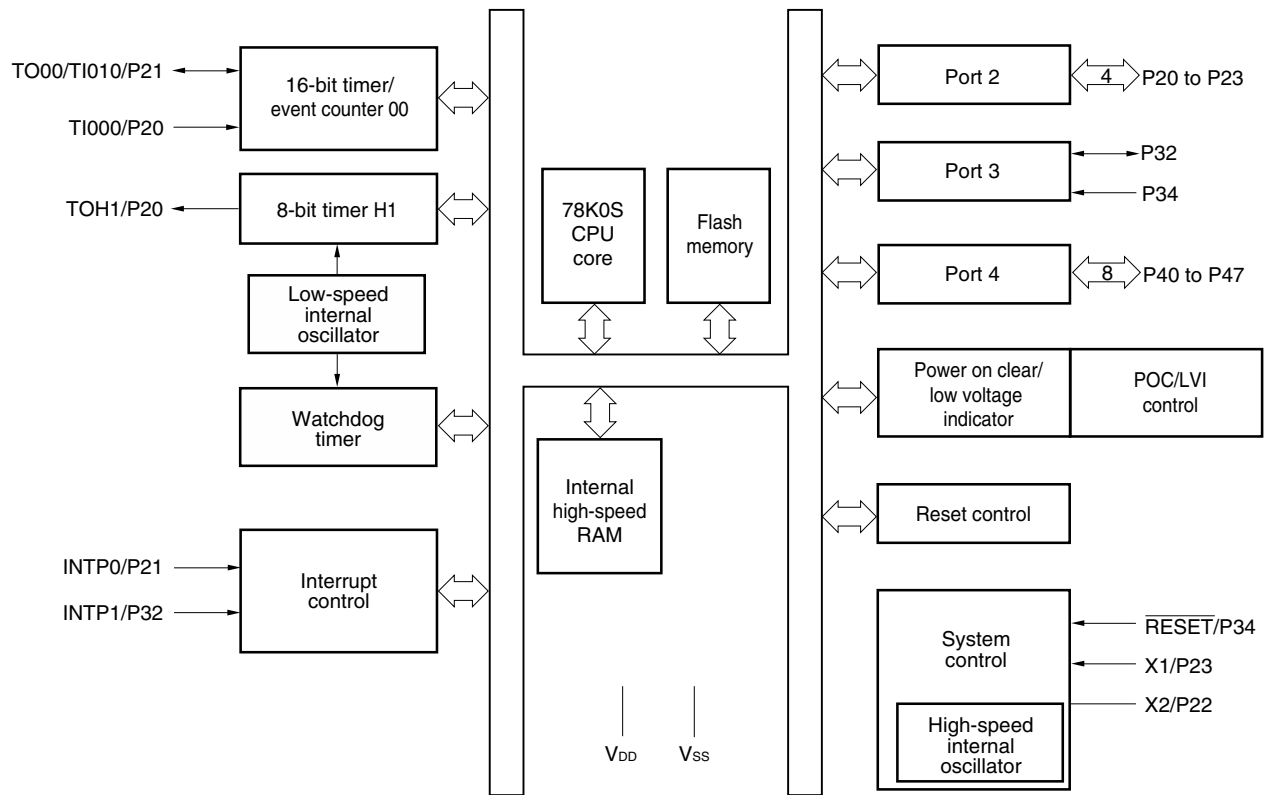
## 1.4 78K0S/Kx1+ Product Lineup

The following table shows the product lineup of the 78K0S/Kx1+.

Part Number		78K0S/KU1+	78K0S/KY1+	78K0S/KA1+	78K0S/KB1+
Item					
Number of pins		10 pins	16 pins	20 pins	30 pins
Internal memory	Flash memory	1 KB, 2 KB, 4 KB		2 KB	4 KB, 8 KB
	RAM	128 bytes		128 bytes	256 bytes
Supply voltage		$V_{DD} = 2.0$ to $5.5$ V <sup>Note 1</sup>			
Minimum instruction execution time		$0.20 \mu\text{s}$ (10 MHz, $V_{DD} = 4.0$ to $5.5$ V) $0.33 \mu\text{s}$ (6 MHz, $V_{DD} = 3.0$ to $5.5$ V) $0.40 \mu\text{s}$ (5 MHz, $V_{DD} = 2.7$ to $5.5$ V) $1.0 \mu\text{s}$ (2 MHz, $V_{DD} = 2.0$ to $5.5$ V)			
System clock (oscillation frequency)		High-speed internal oscillation (8 MHz (TYP.)) Crystal/ceramic oscillation (1 to 10 MHz) <sup>Note 4</sup> External clock input oscillation (1 to 10 MHz)			
Clock for TMH1 and WDT (oscillation frequency)		Low-speed internal oscillation (240 kHz (TYP.))			
Port	CMOS I/O	7	13	15	24
	CMOS input	1	1	1	1
	CMOS output	–	–	1	1
Timer	16-bit (TM0)	1 ch <sup>Note 4</sup>			
	8-bit (TMH)	1 ch			
	8-bit (TM8)	–	–	1 ch	
	WDT	1 ch			
Serial interface		–	–	LIN-Bus-supporting UART: 1 ch	
A/D converter <sup>Note 2</sup>		10 bits: 4 ch (2.7 to 5.5 V) <sup>Note 2</sup>			
Multiplier (8 bits × 8 bits)		–	–	–	Provided
Interrupts	External	2		4	
	Internal	5 <sup>Note 3</sup>		9	
Reset	RESET pin	Provided			
	POC	2.1 V ±0.1 V			
	LVI	Provided (selectable by software)			
	WDT	Provided			
Operating temperature range		Standard products: –40 to +85°C	Standard products, (A) grade products: –40 to +85°C (A2) grade products: –40 to +125°C		

- Note 1.** Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage ( $V_{POC}$ ) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.
- 2.** The product without A/D converter ( $\mu$  PD78F95xx) is provided for the 78K0S/KU1+ (under development) and 78K0S/KY1+ respectively. This product has no A/D converter.
- 3.** 4 factors for products without A/D converter
- 4.** The product without A/D converter ( $\mu$  PD78F950x) in the 78K0S/KU1+ (under development) is not supported.

1.5 Block Diagram



## 1.6 Functional Outline

Item		$\mu$ PD78F9510	$\mu$ PD78F9511	$\mu$ PD78F9512
Internal memory	Flash memory	1 KB	2 KB	4 KB
	High-speed RAM	128 bytes		
Memory space		64 KB		
X1 input clock (oscillation frequency)		Crystal/ceramic/external clock input: 10 MHz ( $V_{DD} = 2.0$ to $5.5$ V)		
Internal oscillation clock	High speed (oscillation frequency)	Internal oscillation: 8 MHz (TYP.)		
	Low speed (for TMH1 and WDT)	Internal oscillation: 240 kHz (TYP.)		
General-purpose registers		8 bits $\times$ 8 registers		
Instruction execution time		0.2 $\mu$ s/0.4 $\mu$ s/0.8 $\mu$ s/1.6 $\mu$ s/3.2 $\mu$ s (X1 input clock: $f_x = 10$ MHz)		
I/O port		Total: 14 pins CMOS I/O: 13 pins CMOS input: 1 pin		
Timer		<ul style="list-style-type: none"> <li>• 16-bit timer/event counter: 1 channel</li> <li>• 8-bit timer (timer H1): 1 channel</li> <li>• Watchdog timer: 1 channel</li> </ul>		
	Timer output	2 pins (PWM: 1 pin)		
Vectored interrupt sources	External	2		
	Internal	4		
Reset		<ul style="list-style-type: none"> <li>• Reset by RESET pin</li> <li>• Internal reset by watchdog timer</li> <li>• Internal reset by power-on-clear</li> <li>• Internal reset by low-voltage detector</li> </ul>		
Supply voltage		$V_{DD} = 2.0$ to $5.5$ V <sup>Note</sup>		
Operating temperature range		-40 to +85°C		
Package		16-pin plastic SSOP		

**Note** Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage ( $V_{POC}$ ) of the power-on-clear (POC) circuit is 2.1 V  $\pm$  0.1 V.

## CHAPTER 2 PIN FUNCTIONS

### 2.1 Pin Function List

#### (1) Port pins

Pin Name	I/O	Function		After Reset	Alternate-Function Pin
P20	I/O	Port 2. 4-bit I/O port. Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.		Input	TI000/TOH1
P21					TI010/TO00/ INTP0
P22 <sup>Note</sup>					X2 <sup>Note</sup>
P23 <sup>Note</sup>					X1 <sup>Note</sup>
P32	I/O	Port 3	Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.	Input	INTP1
P34 <sup>Note</sup>	Input		Input only	Input	RESET <sup>Note</sup>
P40 to P47	I/O	Port 4. 8-bit I/O port. Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.		Input	–

**Note** For the setting method for pin functions, see **CHAPTER 14 OPTION BYTE**.

**Caution** The P22/X2 and P23/X1 pins are pulled down during reset.

(2) Non-port pins

Pin Name	I/O	Function	After Reset	Alternate-Function Pin
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P21 /TI010/ TO00
INTP1				P32
TI000	Input	External count clock input to 16-bit timer/event counter 00. Capture trigger input to capture registers (CR000 and CR010) of 16-bit timer/event counter 00	Input	P20 /TOH1
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00		P21/TO00/ INTP0
TO00	Output	16-bit timer/event counter 00 output	Input	P21/TI010/ INTP0
TOH1	Output	8-bit timer H1 output	Input	P20/TI000
$\overline{\text{RESET}}$ <sup>Note</sup>	Input	System reset input	Input	P34 <sup>Note</sup>
X1 <sup>Note</sup>	Input	Connection of crystal/ceramic oscillator for system clock oscillation. External clock input	–	P23 <sup>Note</sup>
X2 <sup>Note</sup>	–	Connection of crystal/ceramic oscillator for system clock oscillation.	–	P22 <sup>Note</sup>
V <sub>DD</sub>	–	Positive power supply	–	–
V <sub>SS</sub>	–	Ground potential	–	–

**Note** For the setting method for pin functions, see **CHAPTER 14 OPTION BYTE**.

**Caution** The P22/X2 and P23/X1 pins are pulled down during reset.

## 2.2 Pin Functions

### 2.2.1 P20 to P23 (Port 2)

P20 to P23 constitute a 4-bit I/O port. In addition to the function as I/O port pins, these pins also have a function to input/output a timer signal, and input an external interrupt request signal.

P22 and P23 also function as the X2 and X1, respectively. For the setting method for pin functions, see **CHAPTER 14 OPTION BYTE**.

These pins can be set to the following operation modes in 1-bit units.

#### (1) Port mode

P20 to P23 function as a 4-bit I/O port. Each bit of this port can be set to the input or output mode by using port mode register 2 (PM2). In addition, an on-chip pull-up resistor can be connected to the port by using pull-up resistor option register 2 (PU2).

#### (2) Control mode

P20 to P23 function to input/output a timer signal, and input an external interrupt request signal.

##### (a) TI000

This pin inputs an external count clock to 16-bit timer/event counter 00, or a capture trigger signal to the capture registers (CR000 and CR010) of 16-bit timer/event counter 00.

##### (b) TI010

This pin inputs a capture trigger signal to the capture register (CR000) of 16-bit timer/event counter 00.

##### (c) TO00

This pin outputs a signal from 16-bit timer/event counter 00.

##### (d) TOH1

This pin outputs a signal from 8-bit timer H1.

##### (e) INTP0

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

**Caution** The P22/X2 and P23/X1 pins are pulled down during reset.



### 2.2.2 P32 and P34 (Port 3)

P32 is a 1-bit I/O port. In addition to the function as an I/O port pin, this pin also has a function to input an external interrupt request signal.

P34 is a 1-bit input-only port. This pin is also used as a  $\overline{\text{RESET}}$  pin, and when the power is turned on, this is the reset function.

For the setting method for pin functions, see **CHAPTER 14 OPTION BYTE**.

When P34 is used as an input port pin, connect the pull-up resistor.

P32 and P34 can be set to the following operation modes in 1-bit units.

#### (1) Port mode

P32 functions as a 1-bit I/O port. This pin can be set to the input or output mode by using port mode register 3 (PM3). In addition, an on-chip pull-up resistor can be connected to the port by using pull-up resistor option register 3 (PU3).

P34 functions as a 1-bit input-only port.

#### (2) Control mode

P32 functions as an external interrupt request input pin (INTP1) for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

### 2.2.3 P40 to P47 (Port 4)

P40 to P47 constitute an 8-bit I/O port. Each bit of this port can be set to the input or output mode by using port mode register 4 (PM4). In addition, an on-chip pull-up resistor can be connected to the port by using pull-up resistor option register 4 (PU4).

### 2.2.4 $\overline{\text{RESET}}$

This pin inputs an active-low system reset signal. When the power is turned on, this is the reset function, regardless of the option byte setting.

### 2.2.5 X1 and X2

These pins connect an oscillator to oscillate the X1 input clock.

X1 and X2 also function as the P23 and P22, respectively. For the setting method for pin functions, see **CHAPTER 14 OPTION BYTE**.

Supply an external clock to X1.

**Caution** The P22/X2 and P23/X1 pins are pulled down during reset.

### 2.2.6 V<sub>DD</sub>

This is the positive power supply pin.

### 2.2.7 V<sub>SS</sub>

This is the ground pin.

Be sure to connect V<sub>SS</sub> to a stabilized GND (= 0 V).

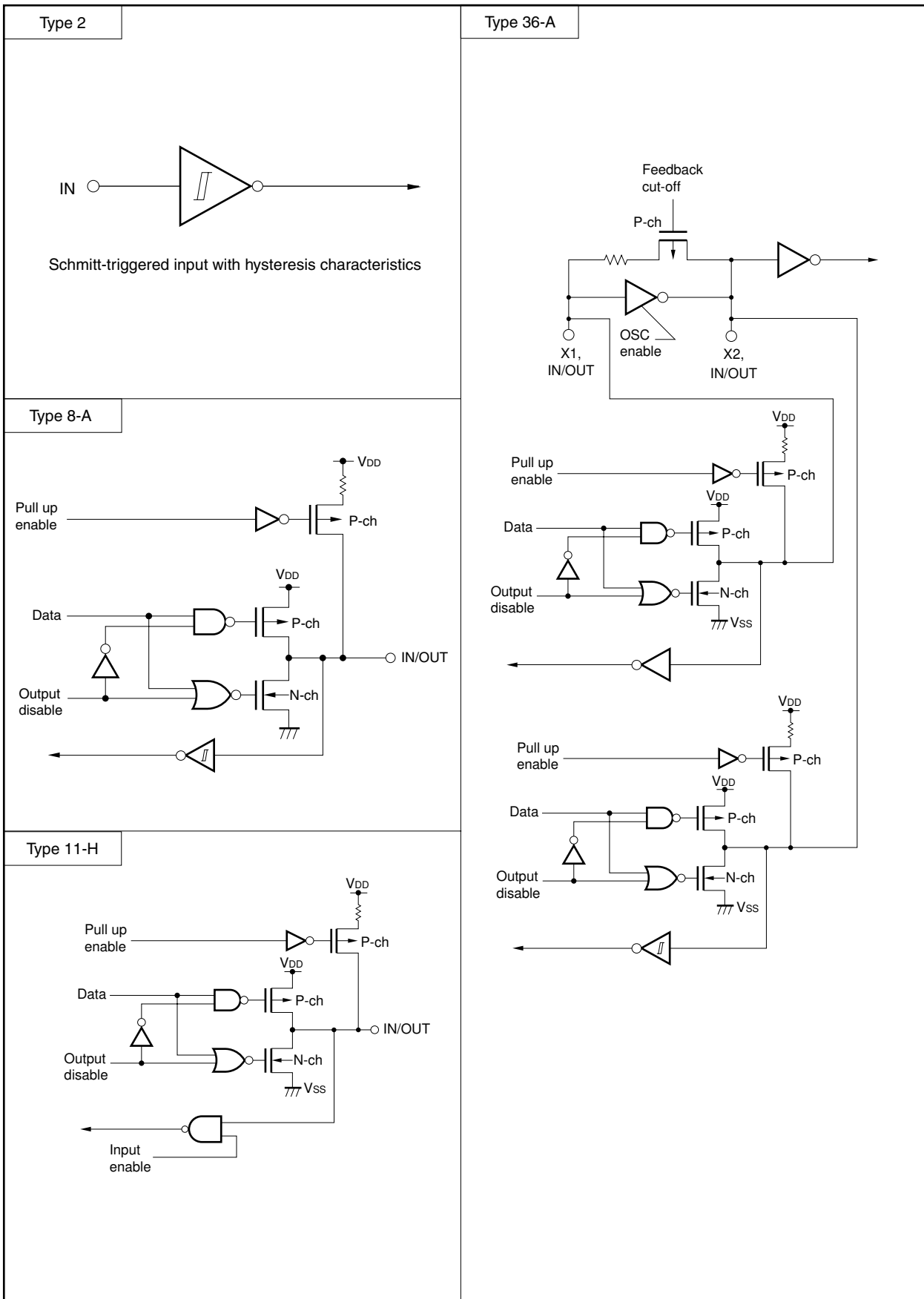
### 2.3 Pin I/O Circuits and Connection of Unused Pins

Table 2-1 shows I/O circuit type of each pin and the connections of unused pins.  
For the configuration of the I/O circuit of each type, refer to **Figure 2-1**.

**Table 2-1. Types of Pin I/O Circuits and Connection of Unused Pins**

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pin
P20/TI000/TOH1	11-H	I/O	Input: Individually connect to $V_{DD}$ or $V_{SS}$ via resistor. Output: Leave open.
P21/TI010/TO00/INTP0			
P22/X2	36-A		Input: Individually connect to $V_{SS}$ via resistor. Output: Leave open.
P23/X1			
P32/INTP1	8-A		Input: Individually connect to $V_{DD}$ or $V_{SS}$ via resistor. Output: Leave open.
P34/ $\overline{\text{RESET}}$	2		Input
P40 to P47	8-A	I/O	Input: Individually connect to $V_{DD}$ or $V_{SS}$ via resistor. Output: Leave open.

Figure 2-1. Pin I/O Circuits

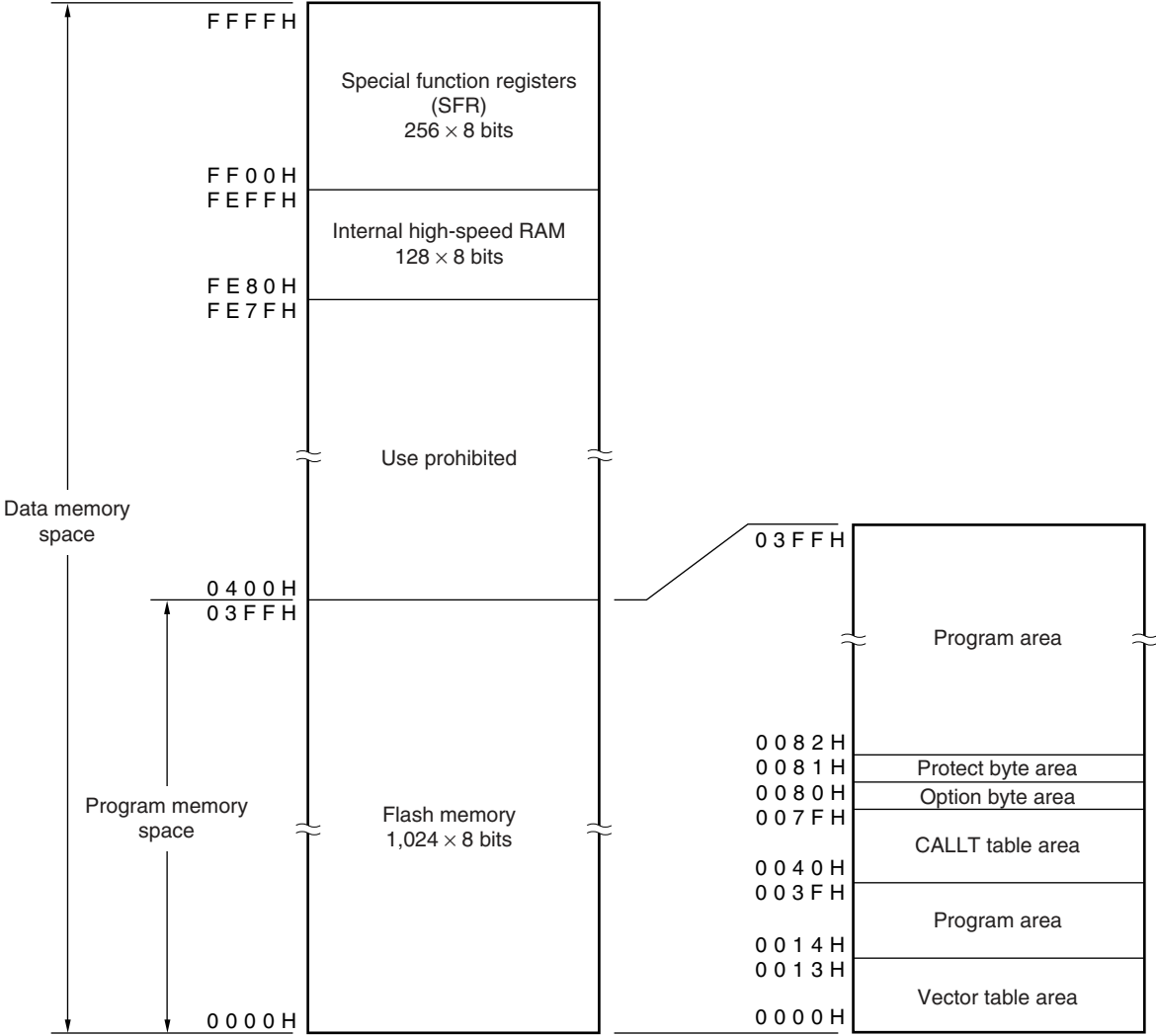


# CHAPTER 3 CPU ARCHITECTURE

## 3.1 Memory Space

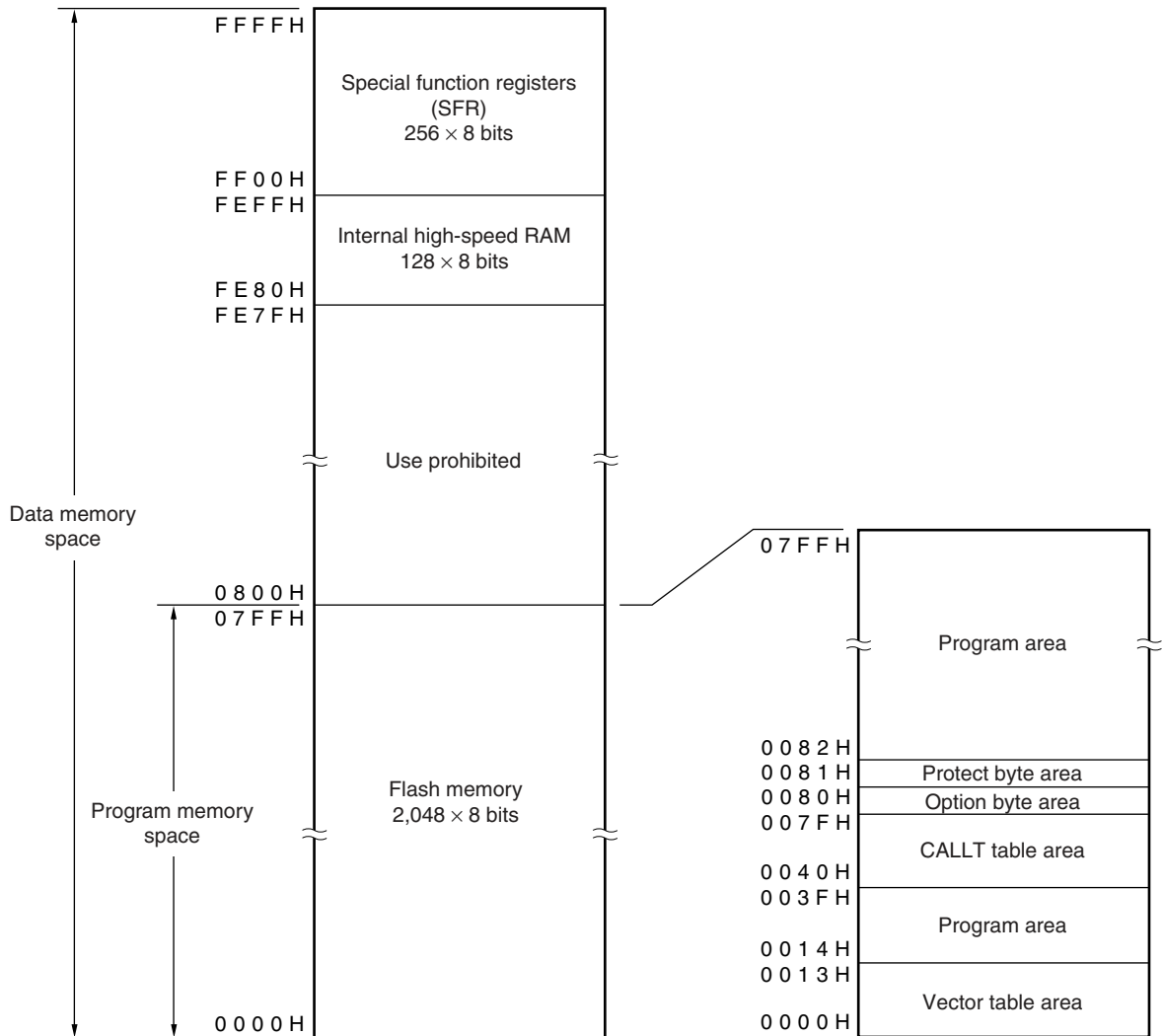
The  $\mu$ PD78F9510, 78F9511, 78F9512 can access up to 64 KB of memory space. Figures 3-1 to 3-3 show the memory maps.

**Figure 3-1. Memory Map ( $\mu$ PD78F9510)**



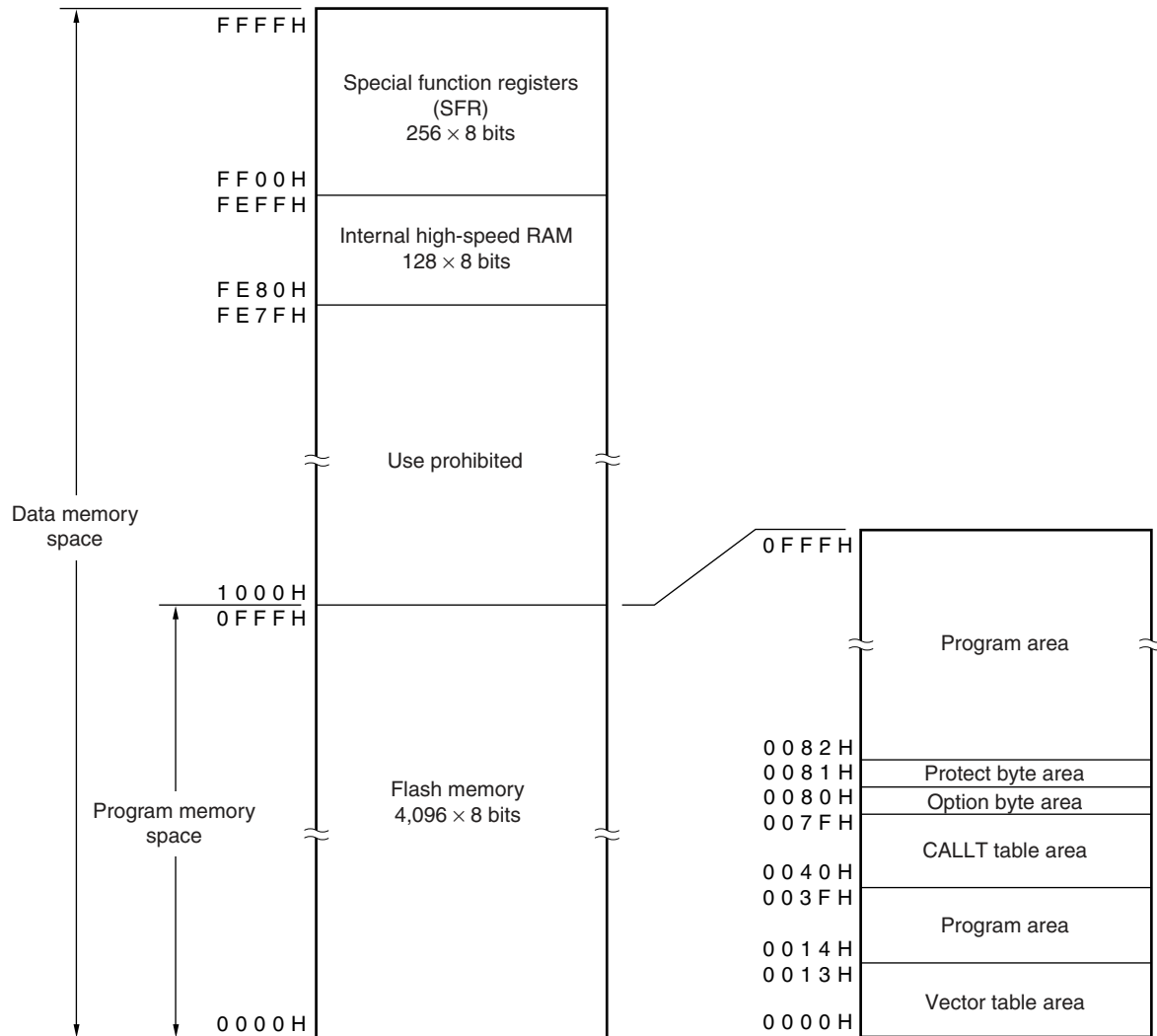
**Remark** The option byte and protect byte are 1 byte each.

Figure 3-2. Memory Map ( $\mu$ PD78F9511)



**Remark** The option byte and protect byte are 1 byte each.

Figure 3-3. Memory Map ( $\mu$ PD78F9512)



**Remark** The option byte and protect byte are 1 byte each.

### 3.1.1 Internal program memory space

The internal program memory space stores programs and table data. This space is usually addressed by the program counter (PC).

The  $\mu$ PD78F9510, 78F9511, 78F9512 provide the following internal ROMs (or flash memory) containing the following capacities.

**Table 3-1. Internal ROM Capacity**

Part Number	Internal ROM	
	Structure	Capacity
$\mu$ PD78F9510	Flash memory	1,024 $\times$ 8 bits
$\mu$ PD78F9511		2,048 $\times$ 8 bits
$\mu$ PD78F9512		4,096 $\times$ 8 bits

The following areas are allocated to the internal program memory space.

#### (1) Vector table area

The 20-byte area of addresses 0000H to 0013H is reserved as a vector table area. This area stores program start addresses to be used when branching by RESET or interrupt request generation. Of a 16-bit address, the lower 8 bits are stored in an even address, and the higher 8 bits are stored in an odd address.

**Table 3-2. Vector Table**

Vector Table Address	Interrupt Request	Vector Table Address	Interrupt Request
0000H	Reset	000CH	INTTMH1
0006H	INTLVI	000EH	INTTM000
0008H	INTP0	0010H	INTTM010
000AH	INTP1		

#### (2) CALLT instruction table area

The subroutine entry address of a 1-byte call instruction (CALLT) can be stored in the 64-byte area of addresses 0040H to 007FH.

#### (3) Option byte area

The option byte area is the 1-byte area of address 0080H. For details, refer to **CHAPTER 14 OPTION BYTE**.

#### (4) Protect byte area

The protect byte area is the 1-byte area of address 0081H. For details, refer to **CHAPTER 15 FLASH MEMORY**.

### 3.1.2 Internal data memory space

128-byte internal high-speed RAM is provided in the  $\mu$ PD78F9510, 78F9511, 78F9512. The internal high-speed RAM can also be used as a stack memory.

### 3.1.3 Special function register (SFR) area

Special function registers (SFRs) of on-chip peripheral hardware are allocated to the area of FF00H to FFFFH (see **Table 3-3**).

### 3.1.4 Data memory addressing

The  $\mu$ PD78F9510, 78F9511, 78F9512 are provided with a wide range of addressing modes to make memory manipulation as efficient as possible. The area (FE80H to FFFFH) which contains a data memory and the special function register (SFR) area can be accessed using a unique addressing mode in accordance with each function. Figures 3-4 to 3-6 illustrate the data memory addressing.

**Figure 3-4. Data Memory Addressing ( $\mu$ PD78F9510)**

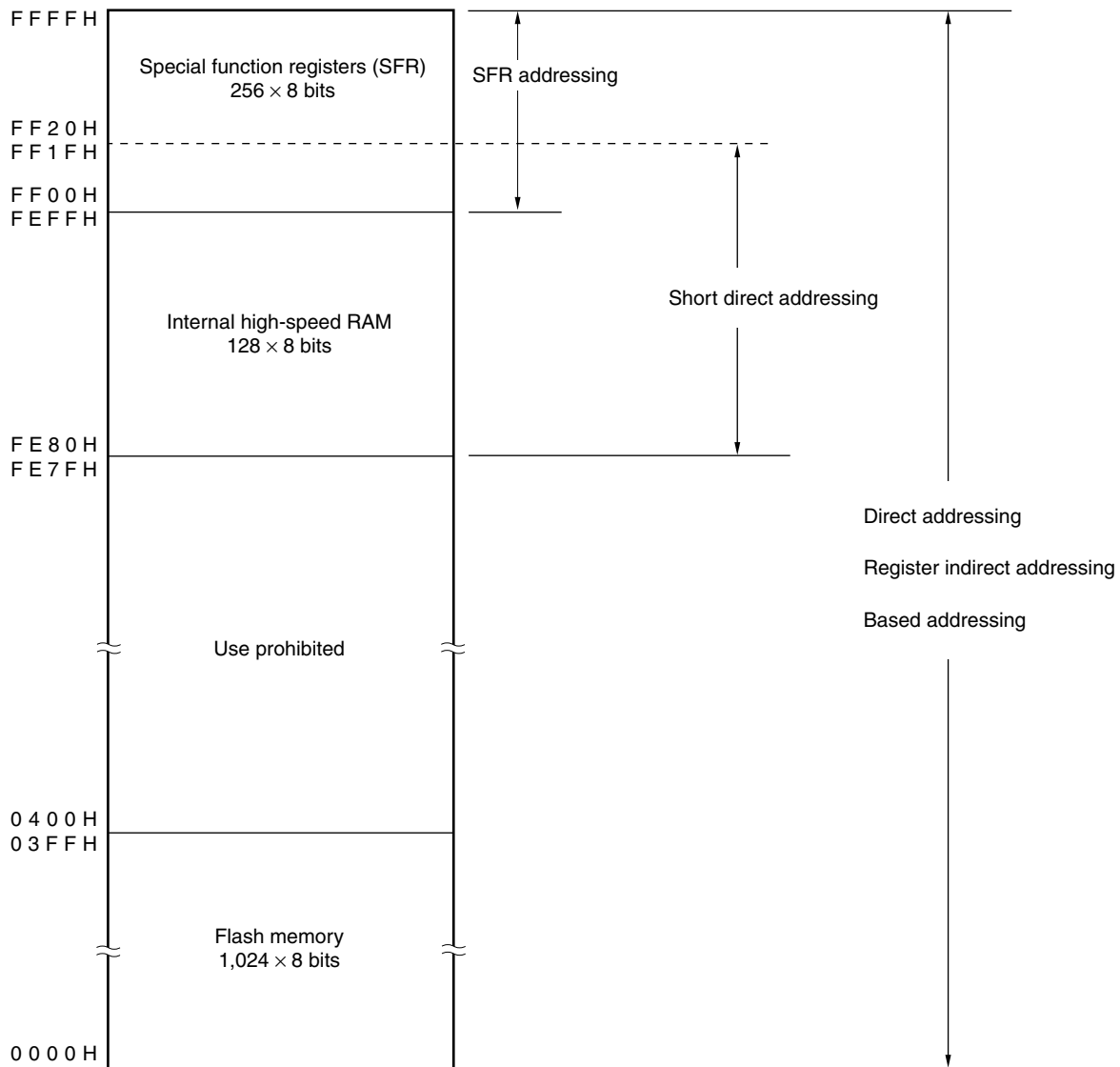




Figure 3-5. Data Memory Addressing ( $\mu$ PD78F9511)

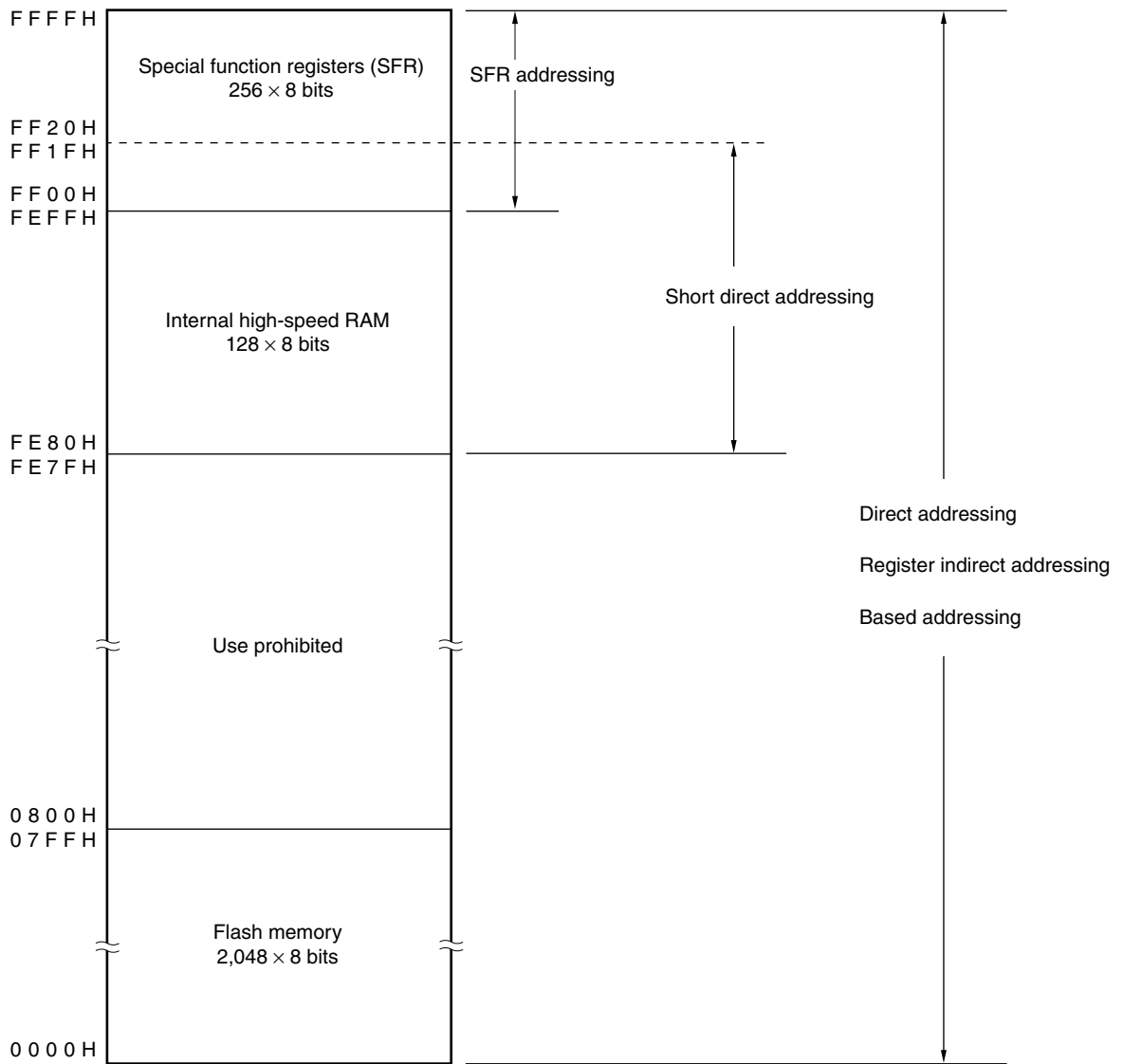
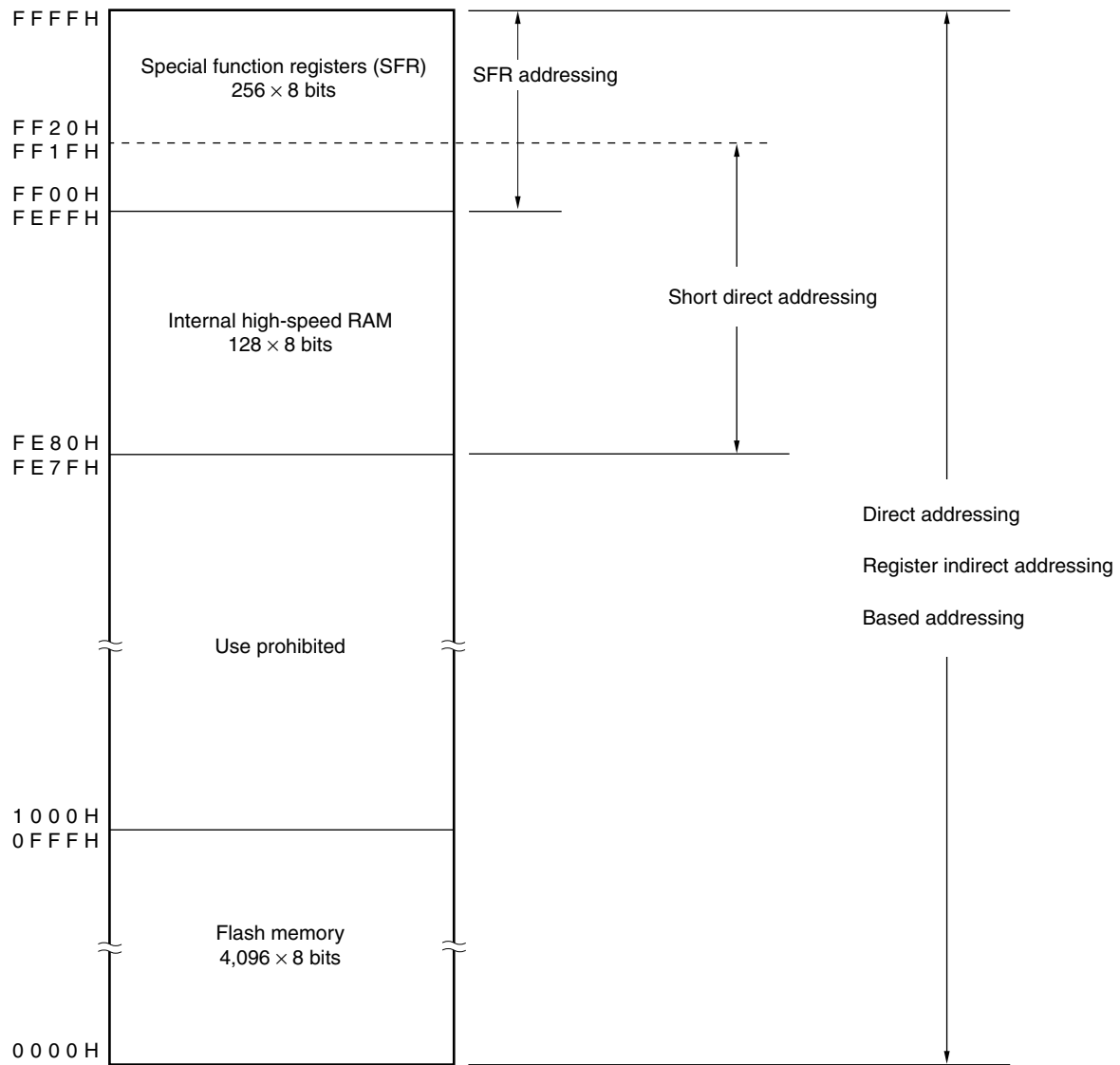


Figure 3-6. Data Memory Addressing ( $\mu$ PD78F9512)



### 3.2 Processor Registers

The  $\mu$ PD78F9510, 78F9511, 78F9512 provide the following on-chip processor registers.

#### 3.2.1 Control registers

The control registers have special functions to control the program sequence statuses and stack memory. The control registers include a program counter, a program status word, and a stack pointer.

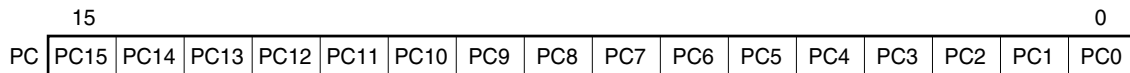
##### (1) Program counter (PC)

The program counter is a 16-bit register which holds the address information of the next program to be executed.

In normal operation, the PC is automatically incremented according to the number of bytes of the instruction to be fetched. When a branch instruction is executed, immediate data or register contents are set.

Reset signal generation sets the reset vector table values at addresses 0000H and 0001H to the program counter.

**Figure 3-7. Program Counter Configuration**



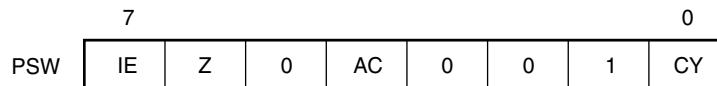
##### (2) Program status word (PSW)

The program status word is an 8-bit register consisting of various flags to be set/reset by instruction execution.

Program status word contents are stored in stack area upon interrupt request generation or PUSH PSW instruction execution and are restored upon execution of the RETI and POP PSW instructions.

Reset signal generation sets PSW to 02H.

**Figure 3-8. Program Status Word Configuration**



**(a) Interrupt enable flag (IE)**

This flag controls interrupt request acknowledge operations of the CPU.

When IE = 0, the interrupt disabled (DI) status is set. All interrupt requests are disabled.

When IE = 1, the interrupt enabled (EI) status is set. Interrupt request acknowledgment is controlled with an interrupt mask flag for various interrupt sources.

This flag is reset to 0 upon DI instruction execution or interrupt acknowledgment and is set to 1 upon EI instruction execution.

**(b) Zero flag (Z)**

When the operation result is zero, this flag is set to 1. It is reset to 0 in all other cases.

**(c) Auxiliary carry flag (AC)**

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set to 1. It is reset to 0 in all other cases.

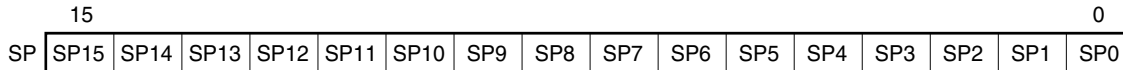
**(d) Carry flag (CY)**

This flag stores overflow and underflow that have occurred upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit operation instruction execution.

**(3) Stack pointer (SP)**

This is a 16-bit register to hold the start address of the memory stack area. Only the internal high-speed RAM area can be set as the stack area (Other than the internal high-speed RAM area cannot be set as the stack area).

**Figure 3-9. Stack Pointer Configuration**



The SP is decremented before writing (saving) to the stack memory and is incremented after reading (restoring) from the stack memory.

Each stack operation saves/restores data as shown in Figures 3-10 and 3-11.

**Cautions 1. Since reset signal generation makes the SP contents undefined, be sure to initialize the SP before using the stack memory.**

**2. Stack pointers can be set only to the high-speed RAM area, and only the lower 10 bits can be actually set.**

**Thus, if the stack pointer is specified to 0FF00H, it is converted to 0FB00H in the high-speed RAM area, since 0FF00H is in the SFR area and not in the high-speed RAM area.**

**When the value is actually pushed onto the stack, 1 is subtracted from 0FB00H to become 0FAFFH, but since that value is not in the high-speed RAM area, it is converted to 0FEFFH, which is the same value as when 0FF00H is set to the stack pointer.**

Figure 3-10. Data to Be Saved to Stack Memory

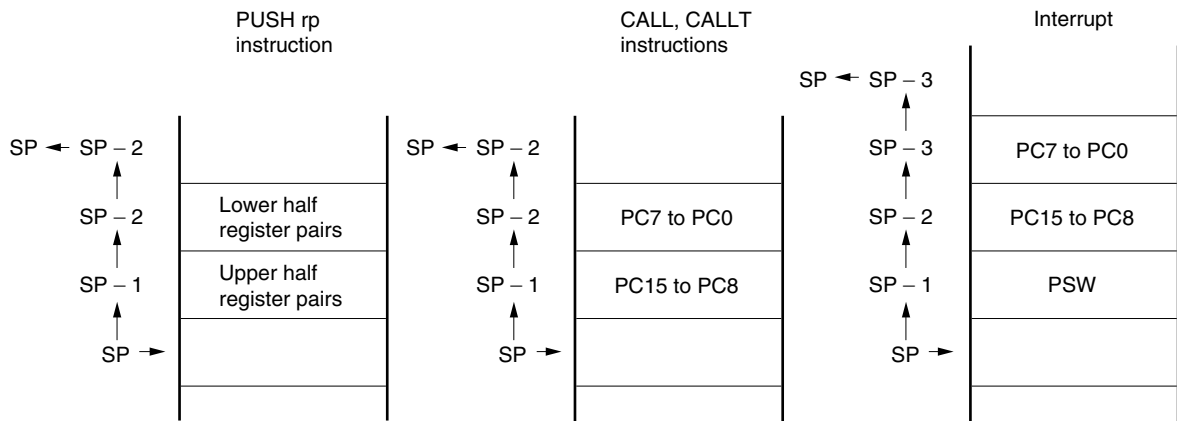
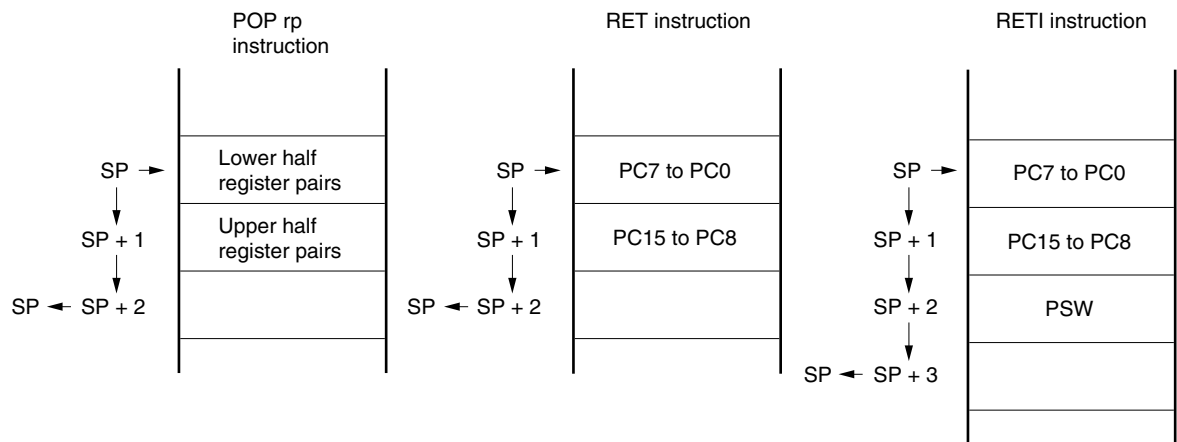


Figure 3-11. Data to Be Restored from Stack Memory



### 3.2.2 General-purpose registers

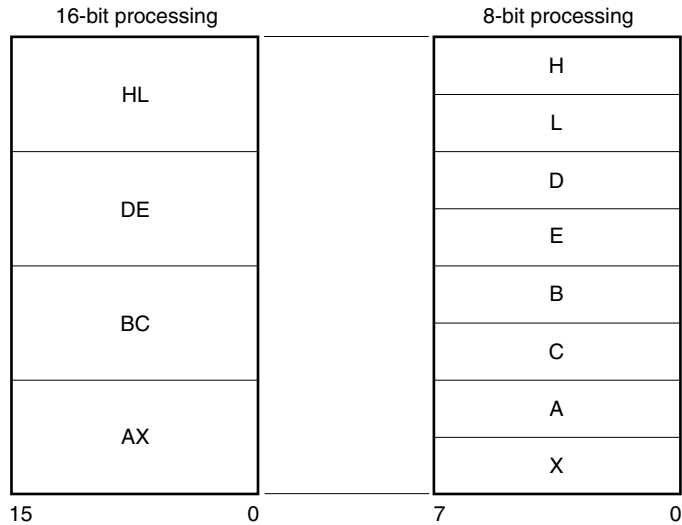
A general-purpose register consists of eight 8-bit registers (X, A, C, B, E, D, L, and H).

In addition each register being used as an 8-bit register, two 8-bit registers in pairs can be used as a 16-bit register (AX, BC, DE, and HL).

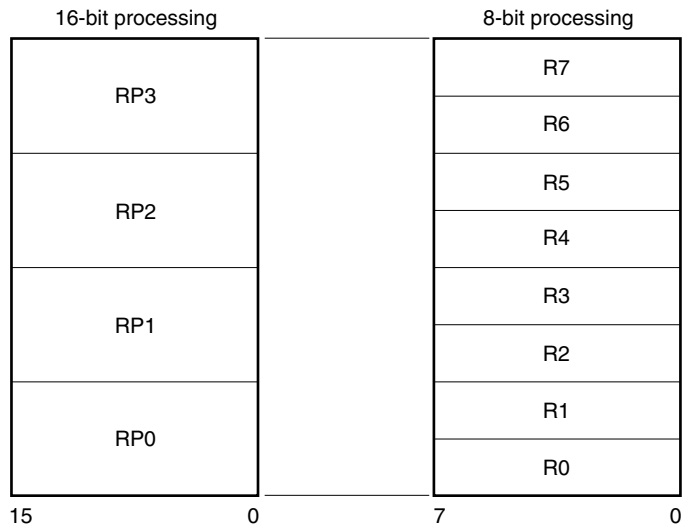
Registers can be described in terms of function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) and absolute names (R0 to R7 and RP0 to RP3).

**Figure 3-12. General-Purpose Register Configuration**

**(a) Function names**



**(b) Absolute names**



### 3.2.3 Special function registers (SFRs)

Unlike the general-purpose registers, each special function register has a special function.

The special function registers are allocated to the 256-byte area FF00H to FFFFH.

The special function registers can be manipulated, like the general-purpose registers, with operation, transfer, and bit manipulation instructions. Manipulatable bit units (1, 8, and 16) differ depending on the special function register type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation  
Describes a symbol reserved by the assembler for the 1-bit manipulation instruction operand (sfr.bit). This manipulation can also be specified with an address and bit.
  
- 8-bit manipulation  
Describes a symbol reserved by the assembler for the 8-bit manipulation instruction operand (sfr). This manipulation can also be specified with an address.
  
- 16-bit manipulation  
Describes a symbol reserved by the assembler for the 16-bit manipulation instruction operand. When specifying an address, describe an even address.

Table 3-3 lists the special function registers. The meanings of the symbols in this table are as follows:

- Symbol  
Indicates the addresses of the implemented special function registers. It is defined as a reserved word in the RA78K0S, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0S. Therefore, these symbols can be used as instruction operands if an assembler or integrated debugger is used.
  
- R/W  
Indicates whether the special function register can be read or written.  
R/W: Read/write  
R: Read only  
W: Write only
  
- Number of bits manipulated simultaneously  
Indicates the bit units (1, 8, and 16) in which the special function register can be manipulated.
  
- After reset  
Indicates the status of the special function register when a reset is input.

Table 3-3. Special Function Registers (1/3)

Address	Symbol	Special Function Register (SFR) Name								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FF00H, FF01H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF02H	P2	0	0	0	0	P23	P22	P21	P20	R/W Note 1	√	√	–	00H	60
FF03H	P3	0	0	0	P34	0	P32	0	0		√	√	–	00H	60
FF04H	P4	P47	P46	P45	P44	P43	P42	P41	P40		√	√	–	00H	60
FF05H to FF0DH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF0EH	CMP01	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	123
FF0FH	CMP11	–	–	–	–	–	–	–	–		–	√	–	00H	123
FF10H, FF11H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF12H	TM00	–	–	–	–	–	–	–	–	R	–	–	√	0000H	82
FF13H		–	–	–	–	–	–	–	–		Note 2				
FF14H	CR000	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	82
FF15H		–	–	–	–	–	–	–	–		Note 2				
FF16H	CR010	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	84
FF17H		–	–	–	–	–	–	–	–		Note 2				
FF18H to FF21H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF22H	PM2	1	1	1	1	PM23	PM22	PM21	PM20	R/W	√	√	–	FFH	59
FF23H	PM3	1	1	1	1	1	PM32	1	1		√	√	–	FFH	59
FF24H	PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40		√	√	–	FFH	59
FF25H to FF31H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF32H	PU2	0	0	0	0	PU23	PU22	PU21	PU20	R/W	√	√	–	00H	61
FF33H	PU3	0	0	0	0	0	PU32	0	0		√	√	–	00H	61
FF34H	PU4	PU47	PU46	PU45	PU44	PU43	PU42	PU41	PU40		√	√	–	00H	61
FF35H to FF47H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF48H	WDTM	0	1	1	WDC S4	WDC S3	WDC S2	WDC S1	WDC S0	R/W	–	√	–	67H	138
FF49H	WDTE	–	–	–	–	–	–	–	–		–	√	–	9AH	139

Notes 1. Only P34 is an input-only port.

2. A 16-bit access is possible only by the short direction addressing.



Table 3-3. Special Function Registers (2/3)

Address	Symbol	Special Function Register (SFR) Name								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FF50H	LVIM	<LVI ON>	0	0	0	0	0	<LVI MD>	<LVI F>	R/W	√	√	–	00H <sup>Note 1</sup>	179
FF51H	LVIS	0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0		–	√	–	00H <sup>Note 1</sup>	180
FF52H, FF53H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF54H	RESF	0	0	0	WDT RF	0	0	0	LVIRF	R	–	√	–	00H <sup>Note 2</sup>	173
FF55H to FF57H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF58H	LSRCM	0	0	0	0	0	0	0	<LSR STOP>	R/W	√	√	–	00H	67
FF59H to FF5FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF60H	TMC00	0	0	0	0	TMC 003	TMC 002	TMC 001	<OVF 00>	R/W	√	√	–	00H	86
FF61H	PRM00	ES 110	ES 100	ES 010	ES 000	0	0	PRM 001	PRM 000		√	√	–	00H	89
FF62H	CRC00	0	0	0	0	0	CRC 002	CRC 001	CRC 000		√	√	–	00H	87
FF63H	TOC00	0	<OSPT 00>	<OSPE 00>	TOC 004	<LVS 00>	<LVR 00>	TOC 001	<TOE 00>		√	√	–	00H	88
FF64H to FF6FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF70H	TMHMD1	<TMHE 1>	CKS1 2	CKS1 1	CKS1 0	TMM D11	TMM D10	<TOLE V1>	<TOEN 1>	R/W	√	√	–	00H	125
FF71H to FF9FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFA0H	PFCMD	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0	W	–	√	–	Undefined	206
FFA1H	PFS	0	0	0	0	0	WEP RERR	VCER R	FPRE RR	R/W	√	√	–	00H	207
FFA2H	FLPMC	0	PRSE LF4	PRSE LF3	PRSE LF2	PRSE LF1	PRSE LF0	0	FLSP M		–	√	–	Undefined	205
FFA3H	FLCMD	0	0	0	0	0	FLCM D2	FLCM D1	FLCM D0		√	√	–	00H	208
FFA4H	FLAPL	FLA P7	FLA P6	FLA P5	FLA P4	FLA P3	FLA P2	FLA P1	FLA P0		√	√	–	Undefined	209

- Notes 1.** Retained only after a reset by LVI.  
**2.** Varies depending on the reset cause.

**Remark** For a bit name enclosed in angle brackets (<->), the bit name is defined as a reserved word in the RA78K0S, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0S.

Table 3-3. Special Function Registers (3/3)

Address	Symbol	Special Function Register (SFR) Name								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FFA5H	FLAPH	0	0	0	0	FLA P11	FLA P10	FLA P9	FLA P8	R/W	√	√	–	Undefined	209
FFA6H	FLAPH C	0	0	0	0	FLAP C11	FLAP C10	FLAP C9	FLAP C8		√	√	–	00H	209
FFA7H	FLAPLC	FLAP C7	FLAP C6	FLAP C5	FLAP C4	FLAP C3	FLAP C2	FLAP C1	FLAP C0		√	√	–	00H	209
FFA8H	FLW	FLW7	FLW6	FLW5	FLW4	FLW3	FLW2	FLW1	FLW0		–	√	–	00H	210
FFA9H to FFDFH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFE0H	IF0	0	<TMIF 010>	<TMIF 000>	<TMIF H1>	<PIF 1>	<PIF 0>	<LVI IF>	0	R/W	√	√	–	00H	149
FFE1H to FFE3H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFE4H	MK0	1	<TMM K010>	<TMM K000>	<TMM KH1>	<PMK 1>	<PMK 0>	<LVIM K>	1	R/W	√	√	–	FFH	150
FFE5H to FFEBH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFECH	INTM0	0	0	ES11	ES10	ES01	ES00	0	0	R/W	–	√	–	00H	150
FFEDH to FFF2H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFF3H	PPCC	0	0	0	0	0	0	PPCC 1	PPCC 0	R/W	√	√	–	02H	66
FFF4H	OSTS	0	0	0	0	0	0	OSTS 1	OSTS 0		–	√	–	Undefined	68
FFF5H to FFFAH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFFBH	PCC	0	0	0	0	0	0	PCC1	0	R/W	√	√	–	02H	66

**Remark** For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0S, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0S.

### 3.3 Instruction Address Addressing

An instruction address is determined by the program counter (PC) contents. The PC contents are normally incremented (+1 for each byte) automatically according to the number of bytes of an instruction to be fetched each time another instruction is executed. When a branch instruction is executed, the branch destination address information is set to the PC to branch by the following addressing (for details of each instruction, refer to **78K/0S Series Instructions User's Manual (U11047E)**).

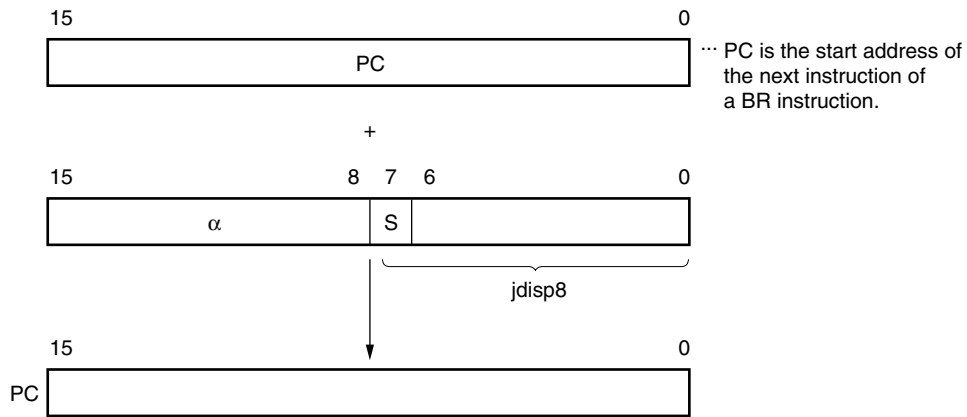
#### 3.3.1 Relative addressing

**[Function]**

The value obtained by adding 8-bit immediate data (displacement value: *jdisp8*) of an instruction code to the start address of the following instruction is transferred to the program counter (PC) to branch. The displacement value is treated as signed two's complement data (−128 to +127) and bit 7 becomes the sign bit. In other words, the range of branch in relative addressing is between −128 and +127 of the start address of the following instruction.

This function is carried out when the BR \$addr16 instruction or a conditional branch instruction is executed.

**[Illustration]**



When S = 0, α indicates that all bits are "0".  
 When S = 1, α indicates that all bits are "1".

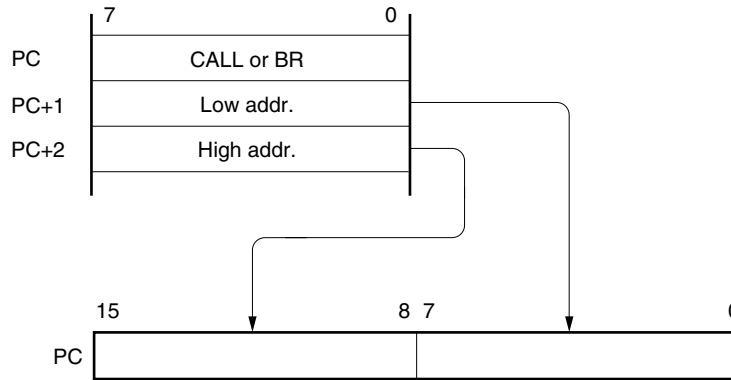
### 3.3.2 Immediate addressing

**[Function]**

Immediate data in the instruction word is transferred to the program counter (PC) to branch. This function is carried out when the CALL !addr16 and BR !addr16 instructions are executed. CALL !addr16 and BR !addr16 instructions can be used to branch to all the memory spaces.

**[Illustration]**

In case of CALL !addr16 and BR !addr16 instructions

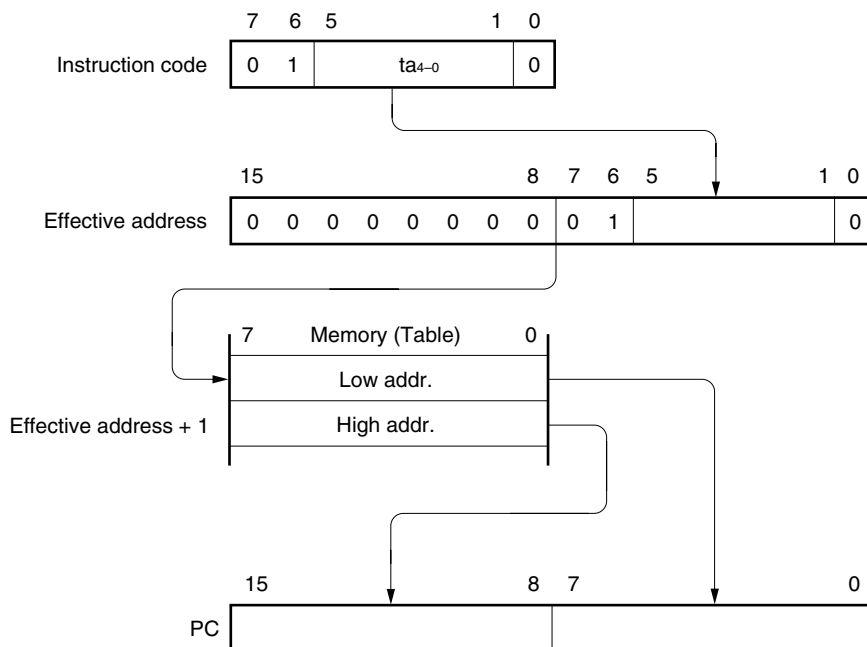


### 3.3.3 Table indirect addressing

**[Function]**

The table contents (branch destination address) of the particular location to be addressed by the immediate data of an instruction code from bit 1 to bit 5 are transferred to the program counter (PC) to branch. Table indirect addressing is carried out when the CALLT [addr5] instruction is executed. This instruction can be used to branch to all the memory spaces according to the address stored in the memory table 40H to 7FH.

**[Illustration]**

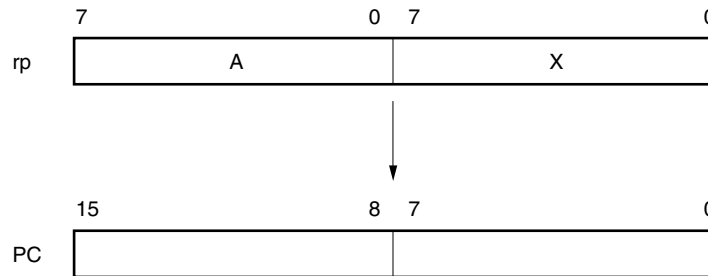


### 3.3.4 Register addressing

**[Function]**

The register pair (AX) contents to be specified with an instruction word are transferred to the program counter (PC) to branch.

This function is carried out when the BR AX instruction is executed.

**[Illustration]**

### 3.4 Operand Address Addressing

The following methods (addressing) are available to specify the register and memory to undergo manipulation during instruction execution.

#### 3.4.1 Direct addressing

**[Function]**

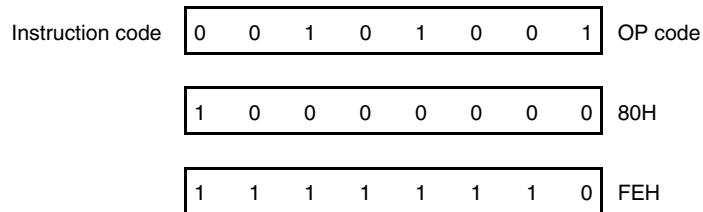
The memory indicated by immediate data in an instruction word is directly addressed.

**[Operand format]**

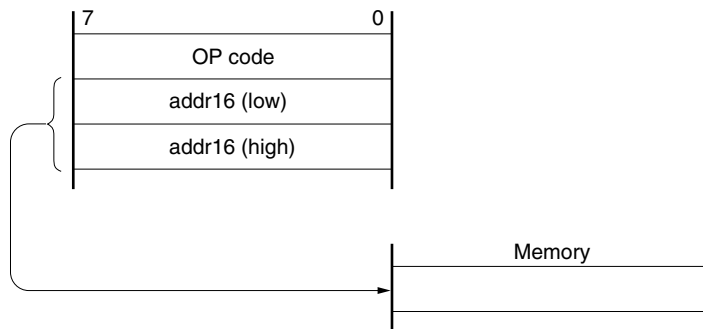
Identifier	Description
addr16	Label or 16-bit immediate data

**[Description example]**

MOV A, !FE80H; When setting !addr16 to FE80H



**[Illustration]**



3.4.2 Short direct addressing

[Function]

The memory to be manipulated in the fixed space is directly addressed with the 8-bit data in an instruction word. The fixed space where this addressing is applied is the 160-byte space FE80H to FF1FH (FE80H to FEFFH (internal high-speed RAM) + FF00H to FF1FH (special function registers)).

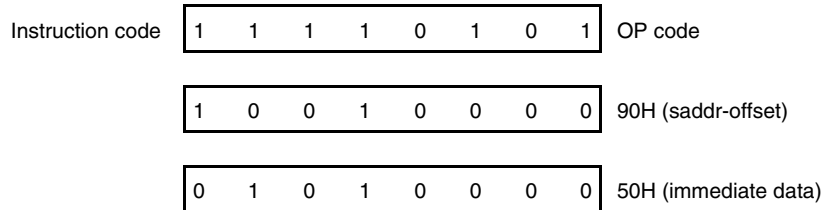
The SFR area where short direct addressing is applied (FF00H to FF1FH) is a part of the total SFR area. In this area, ports which are frequently accessed in a program and a compare register of the timer counter are mapped, and these SFRs can be manipulated with a small number of bytes and clocks.

When 8-bit immediate data is at 80H to FFH, bit 8 of an effective address is cleared to 0. When it is at 00H to 1FH, bit 8 is set to 1. See [Illustration] below.

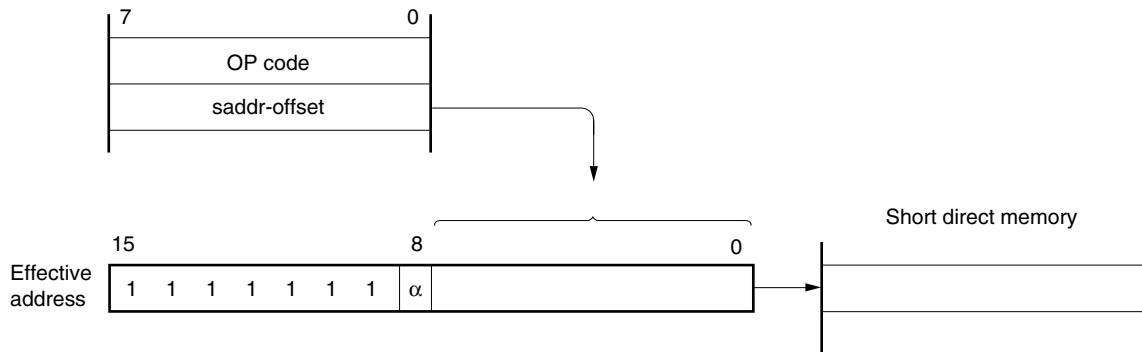
Identifier	Description
saddr	Label or FE80H to FF1FH immediate data
saddrp	Label or FE80H to FF1FH immediate data (even address only)

[Description example]

EQU DATA1 0FE90H ; DATA1 shows FE90H of a saddr area,  
 MOV DATA1, #50H ; When setting the immediate data to 50H



[Illustration]



When 8-bit immediate data is 20H to FFH,  $\alpha = 0$ .  
 When 8-bit immediate data is 00H to 1FH,  $\alpha = 1$ .

### 3.4.3 Special function register (SFR) addressing

**[Function]**

A memory-mapped special function register (SFR) is addressed with the 8-bit immediate data in an instruction word.

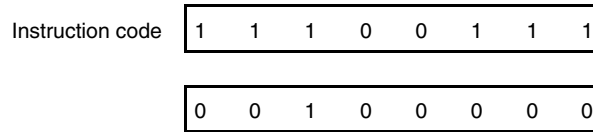
This addressing is applied to the 256-byte space FF00H to FFFFH. However, SFRs mapped at FF00H to FF1FH are accessed with short direct addressing.

**[Operand format]**

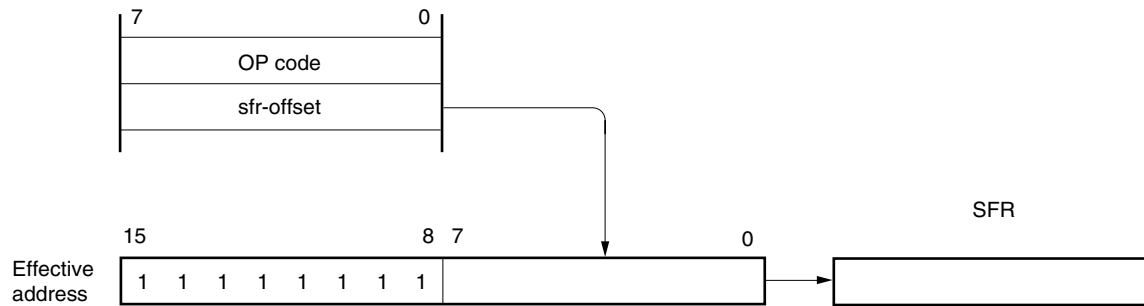
Identifier	Description
sfr	Special function register name

**[Description example]**

MOV PM0, A; When selecting PM0 for sfr



**[Illustration]**





### 3.4.4 Register addressing

**[Function]**

A general-purpose register is accessed as an operand.

The general-purpose register to be accessed is specified with the register specify code and functional name in the instruction code.

Register addressing is carried out when an instruction with the following operand format is executed. When an 8-bit register is specified, one of the eight registers is specified with 3 bits in the instruction code.

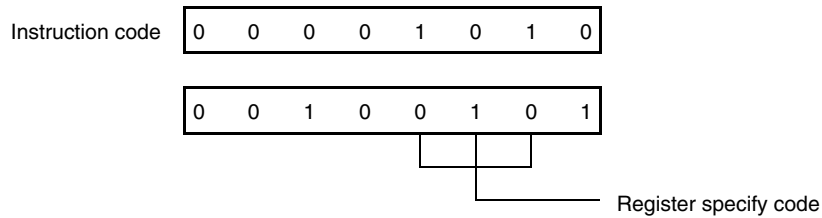
**[Operand format]**

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

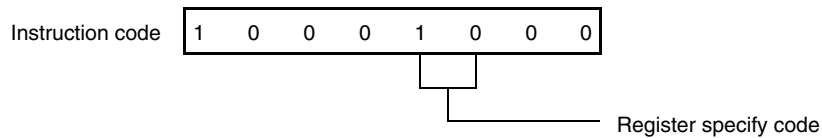
'r' and 'rp' can be described with absolute names (R0 to R7 and RP0 to RP3) as well as function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL).

**[Description example]**

MOV A, C; When selecting the C register for r



INCW DE; When selecting the DE register pair for rp



### 3.4.5 Register indirect addressing

**[Function]**

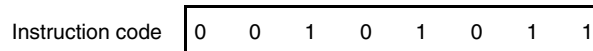
The memory is addressed with the contents of the register pair specified as an operand. The register pair to be accessed is specified with the register pair specify code in the instruction code. This addressing can be carried out for all the memory spaces.

**[Operand format]**

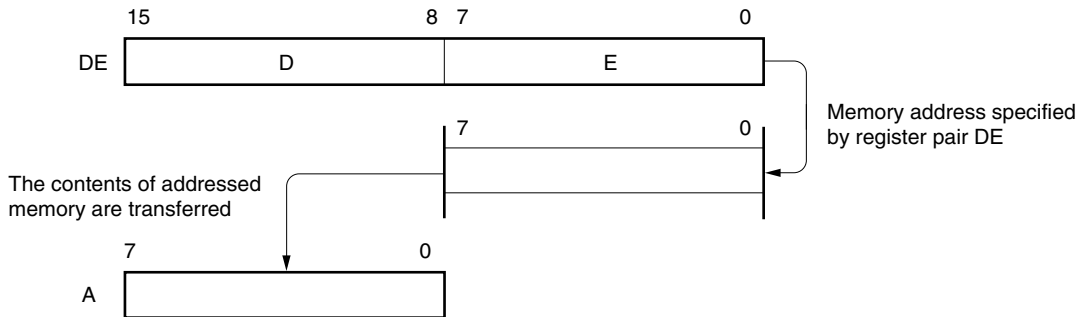
Identifier	Description
–	[DE], [HL]

**[Description example]**

MOV A, [DE]; When selecting register pair [DE]



**[Illustration]**



### 3.4.6 Based addressing

**[Function]**

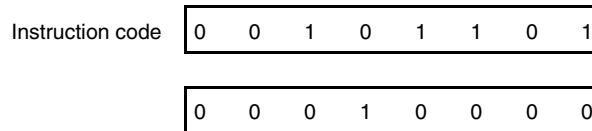
8-bit immediate data is added to the contents of the base register, that is, the HL register pair, and the sum is used to address the memory. Addition is performed by expanding the offset data as a positive number to 16 bits. A carry from the 16th bit is ignored. This addressing can be carried out for all the memory spaces.

**[Operand format]**

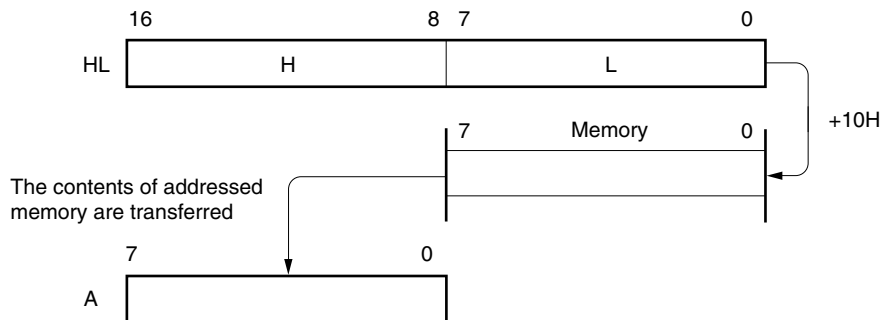
Identifier	Description
-	[HL+byte]

**[Description example]**

MOV A, [HL+10H]; When setting byte to 10H



**[Illustration]**



3.4.7 Stack addressing

[Function]

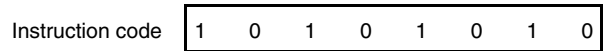
The stack area is indirectly addressed with the stack pointer (SP) contents.

This addressing method is automatically employed when the PUSH, POP, subroutine call, and return instructions are executed or the register is saved/restored upon interrupt request generation.

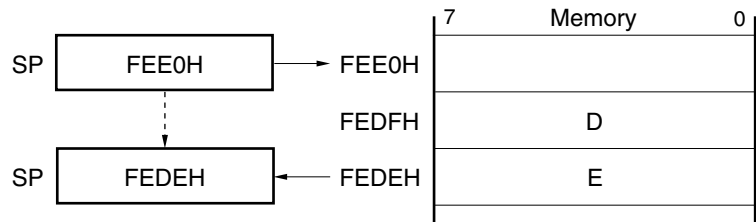
Stack addressing can be used to access the internal high-speed RAM area only.

[Description example]

In the case of PUSH DE



[Illustration]



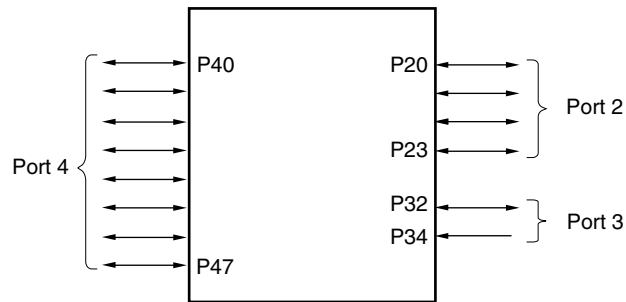
## CHAPTER 4 PORT FUNCTIONS

### 4.1 Functions of Ports

The  $\mu$ PD78F9510, 78F9511, 78F9512 has the ports shown in Figure 4-1, which can be used for various control operations. Table 4-1 shows the functions of each port.

In addition to digital I/O port functions, each of these ports has an alternate function. For details, refer to **CHAPTER 2 PIN FUNCTIONS**.

**Figure 4-1. Port Functions**



**Table 4-1. Port Functions**

Pin Name	I/O	Function		After Reset	Alternate-Function Pin
P20	I/O	Port 2. 4-bit I/O port. Can be set to input or output mode in 1-bit units. On-chip pull-up resistor can be connected by setting software.		Input	TI000/TOH1
P21					TI010/TO00/ INTP0
P22 <sup>Note</sup>					X2 <sup>Note</sup>
P23 <sup>Note</sup>					X1 <sup>Note</sup>
P32	I/O	Port 3	Can be set to input or output mode in 1-bit units. On-chip pull-up resistor can be connected by setting software.	Input	INTP1
P34 <sup>Note</sup>					
P40 to P47	I/O	Port 4. 8-bit I/O port. Can be set to input or output mode in 1-bit units. On-chip pull-up resistor can be connected setting software.		Input	–

**Note** For the setting method for pin functions, see **CHAPTER 14 OPTION BYTE**.

**Caution** The P22/X2 and P23/X1 pins are pulled down during reset.

**Remarks**

1. P22 and P23 can be allocated when the high-speed internal oscillation is selected as the system clock.
2. P22 can be allocated when an external clock input is selected as the system clock.

## 4.2 Port Configuration

Ports consist of the following hardware units.

**Table 4-2. Configuration of Ports**

Item	Configuration
Control registers	Port mode registers (PM2 to PM4) Port registers (P2 to P4) Pull-up resistor option registers (PU2 to PU4)
Ports	Total: 14 (CMOS I/O: 13, CMOS input: 1)
Pull-up resistor	Total: 13

### 4.2.1 Port 2

Port 2 is a 4-bit I/O port with an output latch. Each bit of this port can be set to the input or output mode by using port mode register 2 (PM2). When the P20 to P23 pins are used as an input port, an on-chip pull-up resistor can be connected in 1-bit units by using pull-up resistor option register 2 (PU2).

The P22 and P23 pins are also used as the X2 and X1 pins of the system clock oscillator. The functions of the P22 and P23 pins differ, therefore, depending on the selected system clock oscillator. The following three system clock oscillators can be used.

#### (1) High-speed internal oscillator

The P22 and P23 pins can be used as I/O port pins.

#### (2) Crystal/ceramic oscillator

The P22 and P23 pins cannot be used as I/O port pins because they are used as the X2 and X1 pins.

#### (3) External clock input

The P22 pin can be used as an I/O port pin.

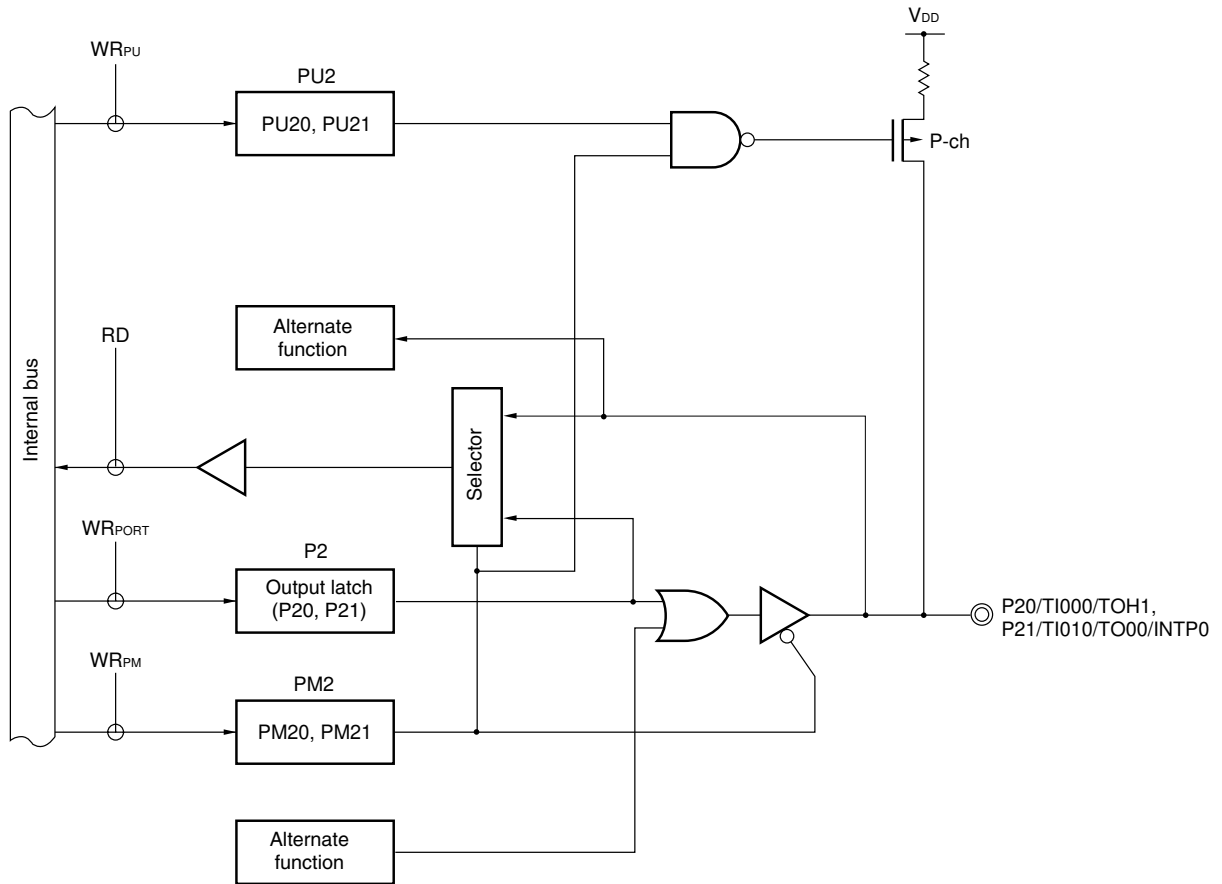
The P23 pin is used as the X1 pin to input an external clock, and therefore it cannot be used as an I/O port pin.

The system clock oscillation is selected by the option byte. For details, refer to **CHAPTER 14 OPTION BYTE**.

Reset signal generation sets port 2 to the input mode.

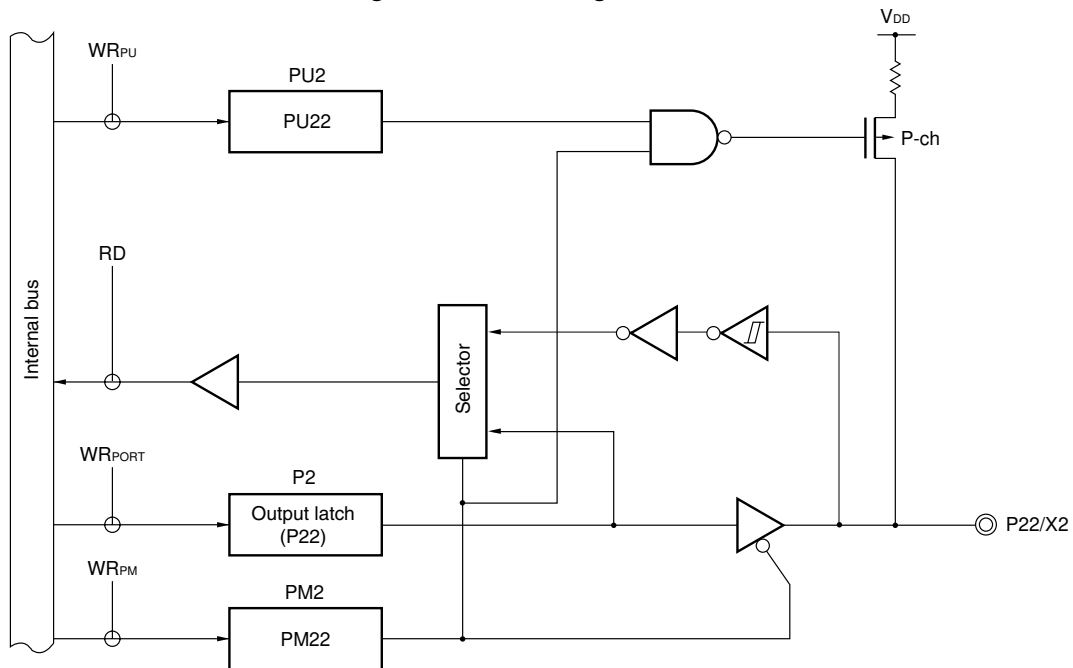
Figures 4-2 to 4-4 show the block diagrams of port 2.

Figure 4-2. Block Diagram of P20 and P21



- P2: Port register 2
- PU2: Pull-up resistor option register 2
- PM2: Port mode register 2
- RD: Read signal
- $WR_{xx}$ : Write signal

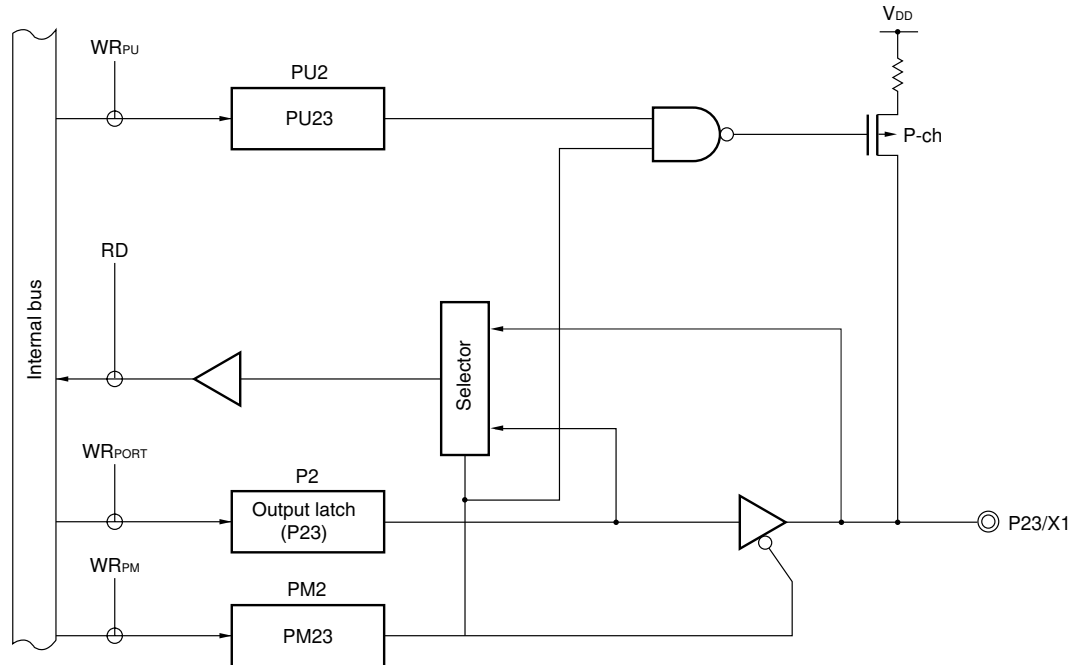
Figure 4-3. Block Diagram of P22



- P2: Port register 2
- PU2: Pull-up resistor option register 2
- PM2: Port mode register 2
- RD: Read signal
- $WR_{xx}$ : Write signal



Figure 4-4. Block Diagram of P23



- P2: Port register 2
- PU2: Pull-up resistor option register 2
- PM2: Port mode register 2
- RD: Read signal
- WR<sub>xx</sub>: Write signal

4.2.2 Port 3

The P32 pin is a 1-bit I/O port with an output latch. This pin can be set to the input or output mode by using port mode register 3 (PM3). When this pin is used as an input port, an on-chip pull-up resistor can be connected in 1-bit units by using pull-up resistor option register 3 (PU3). This pin can also be used for external interrupt request input.

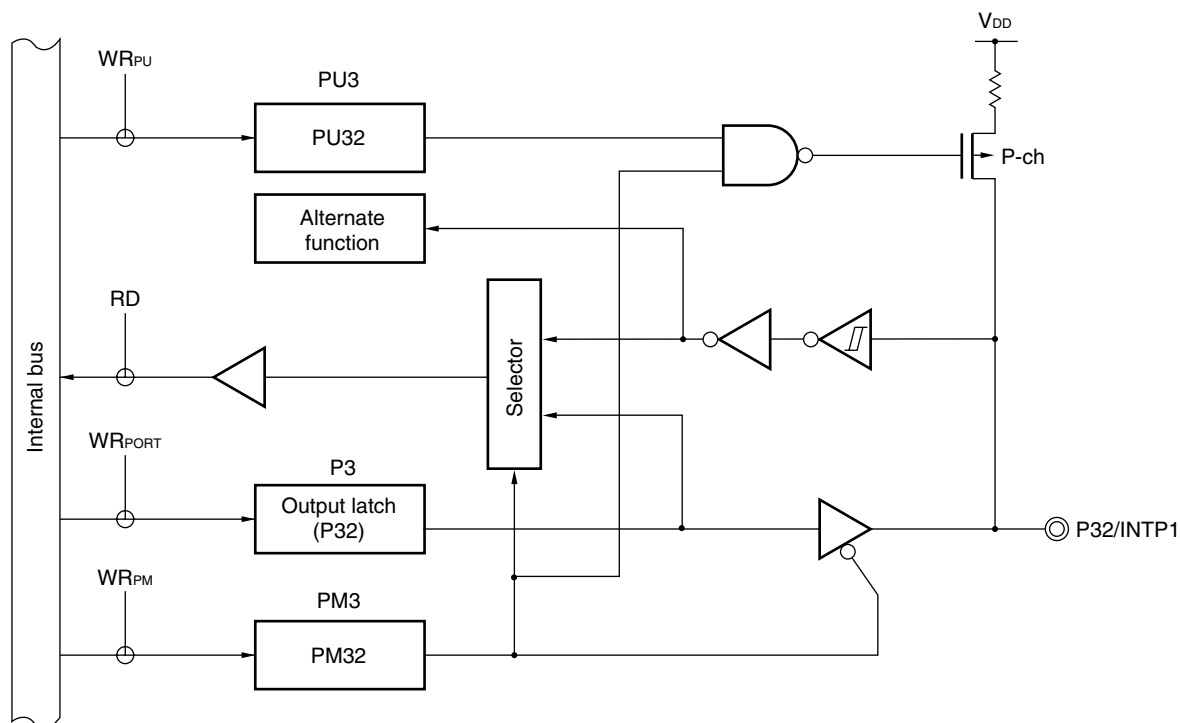
The P32 pin is a Reset signal generation sets port 3 to the input mode.

The P34 pin is a 1-bit input-only port. This pin is also used as a  $\overline{\text{RESET}}$  pin, and when the power is turned on, this is the reset function. For the setting method for pin functions, see **CHAPTER 14 OPTION BYTE**.

When P34 is used as an input port pin, connect the pull-up resistor.

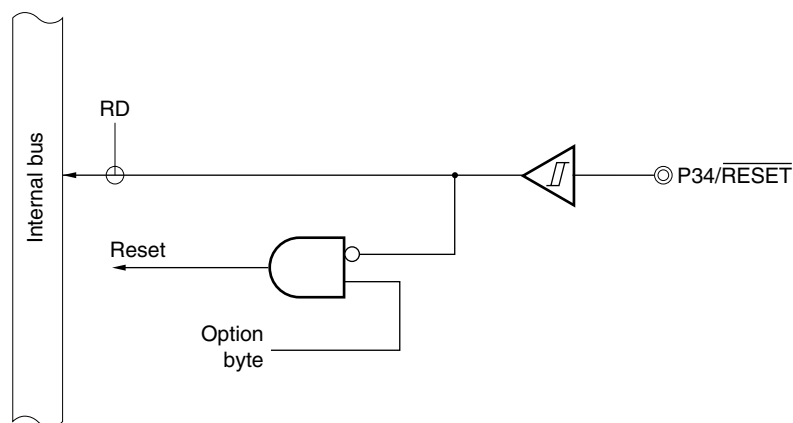
Figures 4-5 and 4-6 show the block diagrams of port 3.

Figure 4-5. Block Diagram of P32



- P3: Port register 3
- PU3: Pull-up resistor option register 3
- PM3: Port mode register 3
- RD: Read signal
- WR<sub>xx</sub>: Write signal

Figure 4-6. Block Diagram of P34



RD: Read signal

**Caution** Because the P34 pin functions alternately as the  $\overline{\text{RESET}}$  pin, if it is used as an input port pin, the function to input an external reset signal to the  $\overline{\text{RESET}}$  pin cannot be used. The function of the port is selected by the option byte. For details, refer to CHAPTER 14 OPTION BYTE.

Also, since the option byte is referenced after the reset release, if low level is input to the  $\overline{\text{RESET}}$  pin before the referencing, then the reset state is not released. When it is used as an input port pin, connect the pull-up resistor.

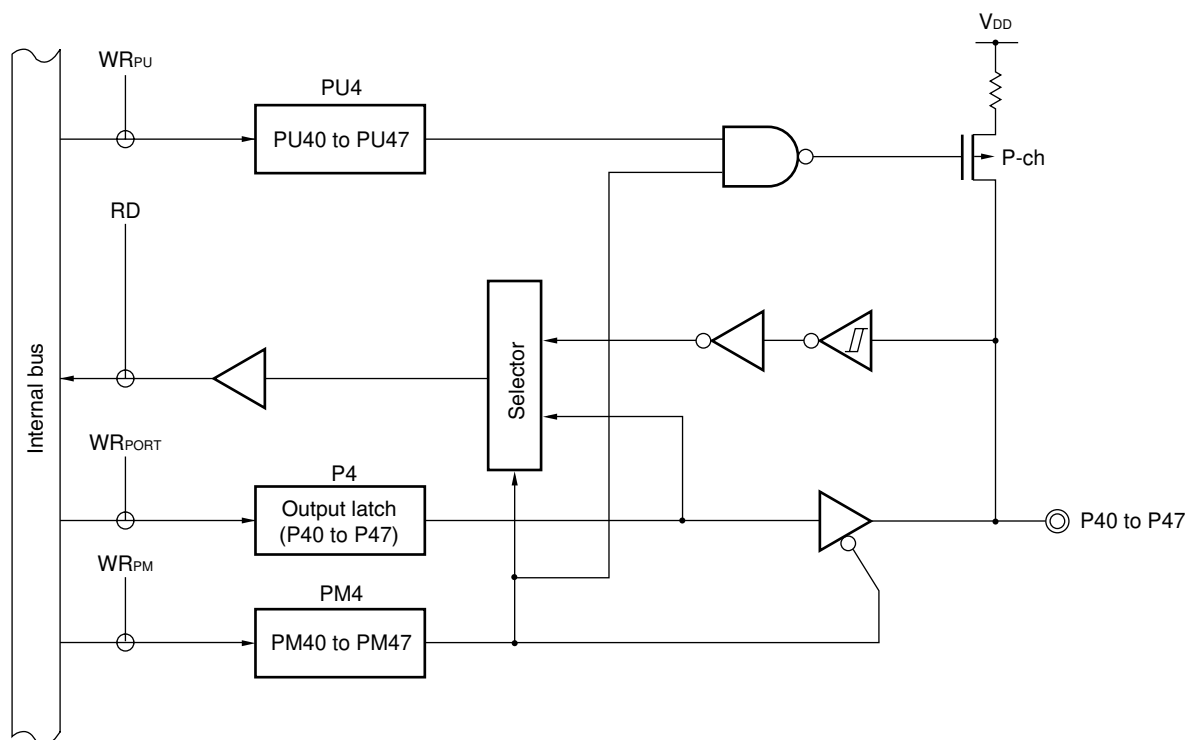
#### 4.2.3 Port 4

Port 4 is an 8-bit I/O port with an output latch. Each bit of this port can be set to the input or output mode by using port mode register 4 (PM4). When the P40 to P47 pins are used as an input port, an on-chip pull-up resistor can be connected in 1-bit units by using pull-up resistor option register 4 (PU4).

Reset signal generation sets port 4 to the input mode.

Figure 4-7 shows the block diagram of port 4.

Figure 4-7. Block Diagram of P40 to P47



- P4: Port register 4
- PU4: Pull-up resistor option register 4
- PM4: Port mode register 4
- RD: Read signal
- WR<sub>xx</sub>: Write signal

### 4.3 Registers Controlling Port Functions

The ports are controlled by the following four types of registers.

- Port mode registers (PM2 to PM4)
- Port registers (P2 to P4)
- Pull-up resistor option registers (PU2 to PU4)

**(1) Port mode registers (PM2 to PM4)**

These registers are used to set the corresponding port to the input or output mode in 1-bit units.

Each port mode register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

When a port pin is used as an alternate-function pin, set its port mode register and output latch as shown in Table 4-3.

**Caution** Because P21 and P32 are also used as external interrupt pins, the corresponding interrupt request flag is set if each of these pins is set to the output mode and its output level is changed. To use the port pin in the output mode, therefore, set the corresponding interrupt mask flag to 1 in advance.

**Figure 4-8. Format of Port Mode Register**

Address: FF22H, After reset: FFH, R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	1	1	PM23	PM22	PM21	PM20

Address: FF23H, After reset: FFH, R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	1	1	PM32	1	1

Address: FF24H, After reset: FFH, R/W

Symbol	7	6	5	4	3	2	1	0
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40

PMmn	Selection of I/O mode of Pmn pin (m = 2 to 4; n = 0 to 7)
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

**(2) Port registers (P2 to P4)**

These registers are used to write data to be output from the corresponding port pin to an external device connected to the chip.

When a port register is read, the pin level is read in the input mode, and the value of the output latch of the port is read in the output mode.

P20 to P23, P32, and P40 to P47 are set by using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to 00H.

**Figure 4-9. Format of Port Register**

Address: FF02H, After reset: 00H (Output latch) R/W

Symbol	7	6	5	4	3	2	1	0
P2	0	0	0	0	P23	P22	P21	P20

Address: FF03H, After reset: 00H<sup>Note</sup> (Output latch) R/W<sup>Note</sup>

Symbol	7	6	5	4	3	2	1	0
P3	0	0	0	P34	0	P32	0	0

Address: FF04H, After reset: 00H (Output latch) R/W

Symbol	7	6	5	4	3	2	1	0
P4	P47	P46	P45	P44	P43	P42	P41	P40

Pmn	m = 2 to 4; n = 0 to 7	
	Controls of output data (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

**Note** Because P34 is read-only, its reset value is undefined.

**(3) Pull-up resistor option registers (PU2 to PU4)**

These registers are used to specify whether an on-chip pull-up resistor is connected to P20 to P23, P32, and P40 to P47. By setting PU2 to PU4, an on-chip pull-up resistor can be connected to the port pin corresponding to the bit of PU2 to PU4.

PU2 to PU4 are set by using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation set these registers to 00H.

**Figure 4-11. Format of Pull-up Resistor Option Register**

Address: FF32H, After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PU2	0	0	0	0	PU23	PU22	PU21	PU20

Address: FF33H, After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PU3	0	0	0	0	0	PU32	0	0

Address: FF34H, After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PU4	PU47	PU46	PU45	PU44	PU43	PU42	PU41	PU40

PU <sub>m</sub> <sub>n</sub>	Selection of connection of on-chip pull-up resistor of P <sub>m</sub> <sub>n</sub> (m = 2 to 4; n = 0 to 7)
0	Does not connect on-chip pull-up resistor
1	Connects on-chip pull-up resistor

## 4.4 Operation of Port Function

The operation of a port differs, as follows, depending on the setting of the I/O mode.

**Caution** Although a 1-bit memory manipulation instruction manipulates 1 bit, it accesses a port in 8-bit units. Therefore, the contents of the output latch of a pin in the input mode, even if it is not subject to manipulation by the instruction, are undefined in a port with a mixture of inputs and outputs.

### 4.4.1 Writing to I/O port

#### (1) In output mode

A value can be written to the output latch by a transfer instruction. In addition, the contents of the output latch are output from the pin. Once data is written to the output latch, it is retained until new data is written to the output latch.

When a reset signal is generated, cleans the data in the output latch.

#### (2) In input mode

A value can be written to the output latch by a transfer instruction. Because the output buffer is off, however, the pin status remains unchanged.

Once data is written to the output latch, it is retained until new data is written to the output latch.

When a reset signal is generated, cleans the data in the output latch.

### 4.4.2 Reading from I/O port

#### (1) In output mode

The contents of the output latch can be read by a transfer instruction. The contents of the output latch remain unchanged.

#### (2) In input mode

The pin status can be read by a transfer instruction. The contents of the output latch remain unchanged.

### 4.4.3 Operations on I/O port

#### (1) In output mode

An operation is performed on the contents of the output latch and the result is written to the output latch. The contents of the output latch are output from the pin.

Once data is written to the output latch, it is retained until new data is written to the output latch.

Reset signal generation clears the data in the output latch.

#### (2) In input mode

The pin level is read and an operation is performed on its contents. The operation result is written to the output latch. However, the pin status remains unchanged because the output buffer is off.

When a reset signal is generated, cleans the data in the output latch.



## CHAPTER 5 CLOCK GENERATORS

### 5.1 Functions of Clock Generators

The clock generators include a circuit that generates a clock (system clock) to be supplied to the CPU and peripheral hardware, and a circuit that generates a clock (interval time generation clock) to be supplied to the watchdog timer and 8-bit timer H1 (TMH1).

#### 5.1.1 System clock oscillators

The following three types of system clock oscillators are used.

- High-speed internal oscillator  
This circuit internally oscillates a clock of 8 MHz (TYP.). Its oscillation can be stopped by execution of the STOP instruction.  
If the High-speed internal oscillator is selected to supply the system clock, the X1 and X2 pins can be used as I/O port pins.
- Crystal/ceramic oscillator  
This circuit oscillates a clock with a crystal/ceramic oscillator connected across the X1 and X2 pins. It can oscillate a clock of 1 MHz to 10 MHz. Oscillation of this circuit can be stopped by execution of the STOP instruction.
- External clock input circuit  
This circuit supplies a clock from an external IC to the X1 pin. A clock of 1 MHz to 10 MHz can be supplied. Internal clock supply can be stopped by execution of the STOP instruction.  
If the external clock input is selected as the system clock, the X2 pin can be used as an I/O port pin.

The system clock source is selected by using the option byte. For details, refer to **CHAPTER 14 OPTION BYTE**.  
When using the X1 and X2 pins as I/O port pins, refer to **CHAPTER 4 PORT FUNCTIONS** for details.

#### 5.1.2 Clock oscillator for interval time generation

The following circuit is used as a clock oscillator for interval time generation.

- Low-speed internal oscillator  
This circuit oscillates a clock of 240 kHz (TYP.). Its oscillation can be stopped by using the low-speed internal oscillation mode register (LSRCM) when it is specified by the option byte that its oscillation can be stopped by software.

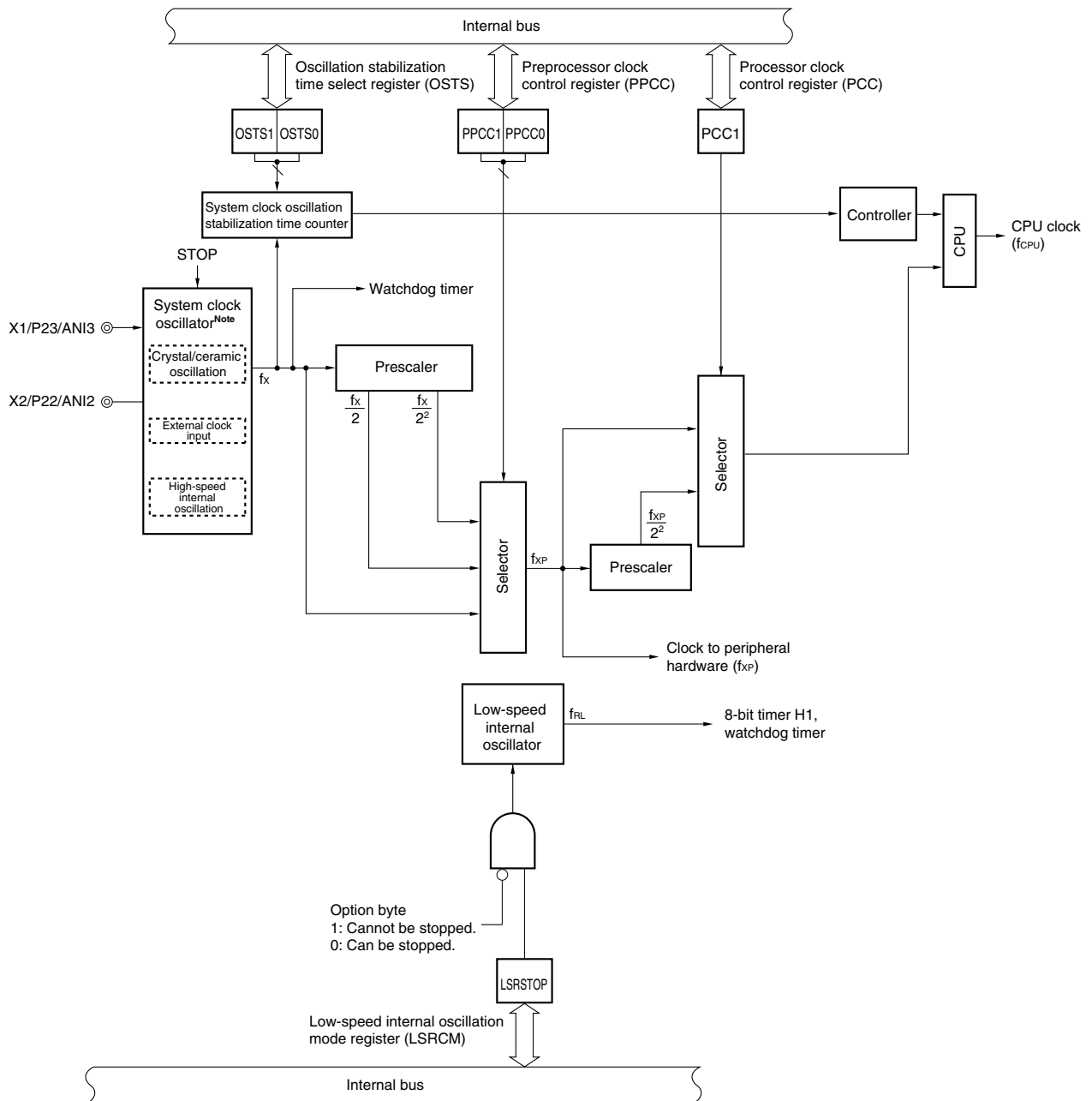
## 5.2 Configuration of Clock Generators

The clock generators consist of the following hardware.

**Table 5-1. Configuration of Clock Generators**

Item	Configuration
Control registers	Processor clock control register (PCC) Preprocessor clock control register (PPCC) Low-speed internal oscillation mode register (LSRCM) Oscillation stabilization time select register (OSTS)
Oscillators	Crystal/ceramic oscillator High-speed internal oscillator External clock input circuit Low-speed internal oscillator

Figure 5-1. Block Diagram of Clock Generators



**Note** Select the high-speed internal oscillator, crystal/ceramic oscillator, or external clock input circuit as the system clock source by using the option byte.

### 5.3 Registers Controlling Clock Generators

The clock generators are controlled by the following four registers.

- Processor clock control register (PCC)
- Preprocessor clock control register (PPCC)
- Low-speed internal oscillation mode register (LSRCM)
- Oscillation stabilization time select register (OSTS)

#### (1) Processor clock control register (PCC) and preprocessor clock control register (PPCC)

These registers are used to specify the division ratio of the system clock.

PCC and PPCC are set by using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PCC and PPCC to 02H.

**Figure 5-2. Format of Processor Clock Control Register (PCC)**

Address: FFFBH, After reset: 02H, R/W

Symbol	7	6	5	4	3	2	1	0
PCC	0	0	0	0	0	0	PCC1	0

**Figure 5-3. Format of Preprocessor Clock Control Register (PPCC)**

Address: FFF3H, After reset: 02H, R/W

Symbol	7	6	5	4	3	2	1	0
PPCC	0	0	0	0	0	0	PPCC1	PPCC0

PPCC1	PPCC0	PCC1	Selection of CPU clock ( $f_{CPU}$ )
0	0	0	$f_x$
0	1	0	$f_x/2$ <sup>Note 1</sup>
0	0	1	$f_x/2^2$
1	0	0	$f_x/2^2$ <sup>Note 2</sup>
0	1	1	$f_x/2^3$ <sup>Note 1</sup>
1	0	1	$f_x/2^4$ <sup>Note 2</sup>
Other than above			Setting prohibited

- Notes**
1. If PPCC = 01H, the clock ( $f_{XP}$ ) supplied to the peripheral hardware is  $f_x/2$ .
  2. If PPCC = 02H, the clock ( $f_{XP}$ ) supplied to the peripheral hardware is  $f_x/2^2$ .

The fastest instruction of the  $\mu$ PD78F9510, 78F9511, 78F9512 is executed in two CPU clocks. Therefore, the relationship between the CPU clock ( $f_{CPU}$ ) and the minimum instruction execution time is as shown in Table 5-2.

**Table 5-2. Relationship between CPU Clock and Minimum Instruction Execution Time**

CPU Clock ( $f_{CPU}$ ) <sup>Note</sup>	Minimum Instruction Execution Time: $2/f_{CPU}$	
	High-speed internal oscillation clock (at 8.0 MHz (TYP.))	Crystal/ceramic oscillation clock or external clock input (at 10.0 MHz)
$f_x$	0.25 $\mu s$	0.2 $\mu s$
$f_x/2$	0.5 $\mu s$	0.4 $\mu s$
$f_x/2^2$	1.0 $\mu s$	0.8 $\mu s$
$f_x/2^3$	2.0 $\mu s$	1.6 $\mu s$
$f_x/2^4$	4.0 $\mu s$	3.2 $\mu s$

**Note** The CPU clock (high-speed internal oscillation clock, crystal/ceramic oscillation clock, or external clock input) is selected by the option byte.

**(2) Low-speed internal oscillation mode register (LSRCM)**

This register is used to select the operation mode of the low-speed internal oscillator (240 kHz (TYP.)).

This register is valid when it is specified by the option byte that the low-speed internal oscillator can be stopped by software. If it is specified by the option byte that the low-speed internal oscillator cannot be stopped by software, setting of this register is invalid, and the low-speed internal oscillator continues oscillating. In addition, the source clock of WDT is fixed to the low-speed internal oscillator. For details, refer to **CHAPTER 8 WATCHDOG TIMER**.

LSRCM can be set by using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets LSRCM to 00H.

**Figure 5-4. Format of Low-Speed internal oscillation Mode Register (LSRCM)**

Address: FF58H, After reset: 00H, R/W

Symbol	7	6	5	4	3	2	1	<0>
LSRCM	0	0	0	0	0	0	0	LSRSTOP

LSRSTOP	Oscillation/stop of low-speed internal oscillator
0	Low-speed internal oscillates
1	Low-speed internal oscillator stops

**(3) Oscillation stabilization time select register (OSTS)**

This register is used to select oscillation stabilization time of the clock supplied from the oscillator when the STOP mode is released. The wait time set by OSTS is valid only when the crystal/ceramic oscillation clock is selected as the system clock and after the STOP mode is released. If the high-speed internal oscillator or external clock input is selected as the system clock source, no wait time elapses.

The system clock oscillator and the oscillation stabilization time that elapses after power application or release of reset are selected by the option byte. For details, refer to **CHAPTER 14 OPTION BYTE**.

OSTS is set by using an 8-bit memory manipulation instruction.

**Figure 5-5. Format of Oscillation Stabilization Time Select Register (OSTS)**

Address: FFF4H, After reset: Undefined, R/W

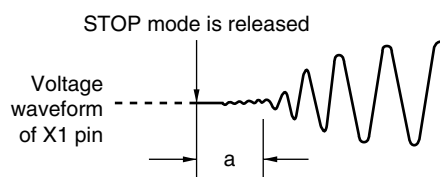
Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	0	OSTS1	OSTS0

OSTS1	OSTS0	Selection of oscillation stabilization time
0	0	$2^{10}/f_x$ (102.4 $\mu$ s)
0	1	$2^{12}/f_x$ (409.6 $\mu$ s)
1	0	$2^{15}/f_x$ (3.27 ms)
1	1	$2^{17}/f_x$ (13.1 ms)

**Cautions 1.** To set and then release the STOP mode, set the oscillation stabilization time as follows.

**Expected oscillation stabilization time of resonator  $\leq$  Oscillation stabilization time set by OSTS**

**2.** The wait time after the STOP mode is released does not include the time from the release of the STOP mode to the start of clock oscillation (“a” in the figure below), regardless of whether STOP mode was released by reset signal generation or interrupt generation.



**3.** The oscillation stabilization time that elapses on power application or after release of reset is selected by the option byte. For details, refer to **CHAPTER 14 OPTION BYTE**.

**Remarks 1.** ( ):  $f_x = 10$  MHz

**2.** Determine the oscillation stabilization time of the resonator by checking the characteristics of the resonator to be used.

## 5.4 System Clock Oscillators

The following three types of system clock oscillators are available.

- High-speed internal oscillator: Internally oscillates a clock of 8 MHz (TYP.).
- Crystal/ceramic oscillator: Oscillates a clock of 1 MHz to 10 MHz.
- External clock input circuit: Supplies a clock of 1 MHz to 10 MHz to the X1 pin.

### 5.4.1 High-speed internal oscillator

The  $\mu$ PD78F9510, 78F9511, 78F9512 include a high-speed internal oscillator (8 MHz (TYP.)).

If the high-speed internal oscillation is selected by the option byte as the clock source, the X1 and X2 pins can be used as I/O port pins.

For details of the option byte, refer to **CHAPTER 14 OPTION BYTE**. For details of I/O ports, refer to **CHAPTER 4 PORT FUNCTIONS**.

### 5.4.2 Crystal/ceramic oscillator

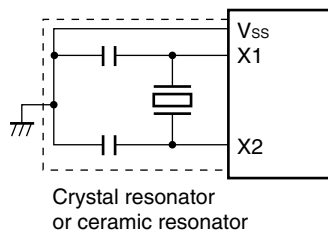
The crystal/ceramic oscillator oscillates using a crystal or ceramic resonator connected between the X1 and X2 pins.

If the crystal/ceramic oscillator is selected by the option byte as the system clock source, the X1 and X2 pins are used as crystal or ceramic resonator connection pins.

For details of the option byte, refer to **CHAPTER 14 OPTION BYTE**. For details of I/O ports, refer to **CHAPTER 4 PORT FUNCTIONS**.

Figure 5-6 shows the external circuit of the crystal/ceramic oscillator.

**Figure 5-6. External Circuit of Crystal/Ceramic Oscillator**



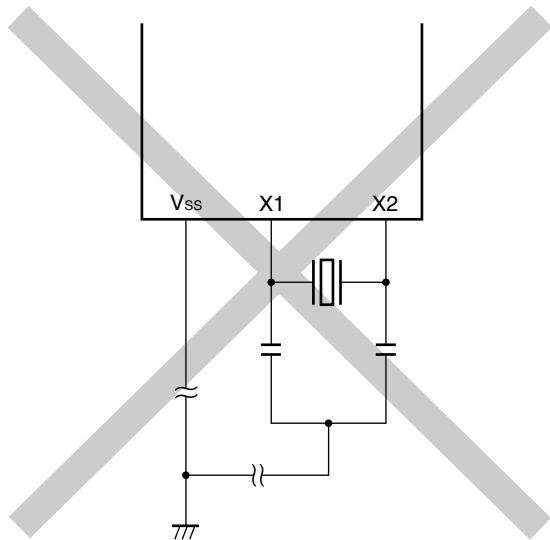
**Caution** When using the crystal/ceramic oscillator, wire as follows in the area enclosed by the broken lines in Figure 5-6 to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V<sub>SS</sub>. Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

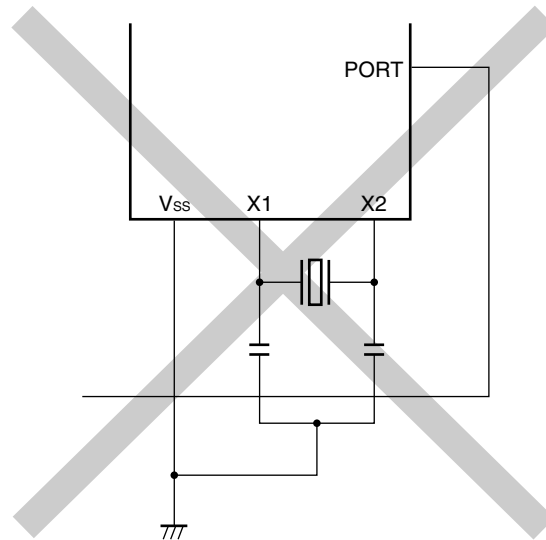
Figure 5-7 shows examples of incorrect resonator connection.

**Figure 5-7. Examples of Incorrect Resonator Connection (1/2)**

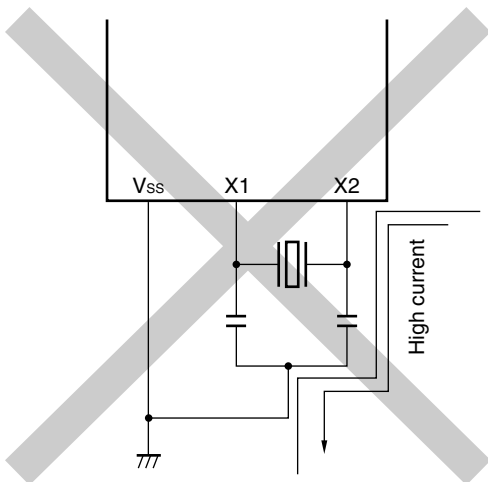
(a) Too long wiring of connected circuit



(b) Crossed signal lines



(c) Wiring near high fluctuating current



(d) Current flowing through ground line of oscillator (Potential at points A, B, and C fluctuates.)

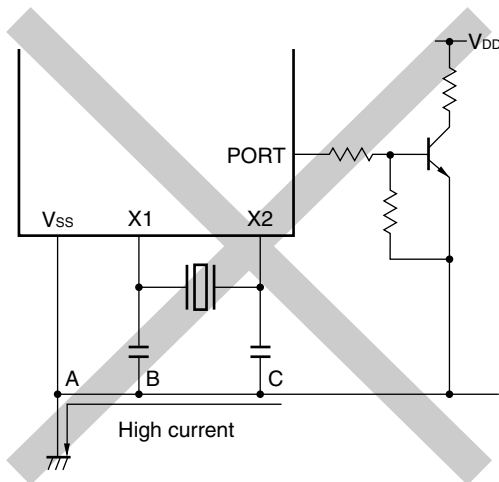
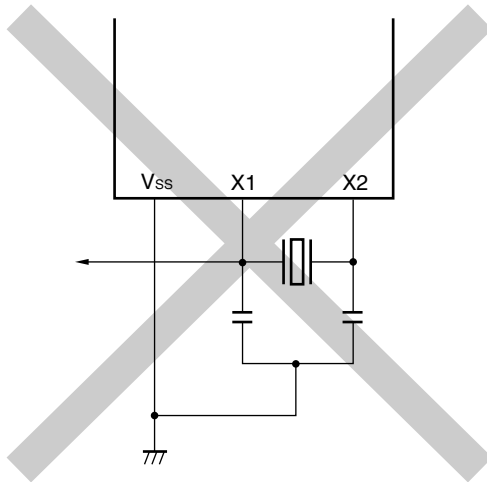




Figure 5-7. Examples of Incorrect Resonator Connection (2/2)

(e) Signals are fetched



#### 5.4.3 External clock input circuit

This circuit supplies a clock from an external IC to the X1 pin.

If external clock input is selected by the option byte as the system clock source, the X2 pin can be used as an I/O port pin.

For details of the option byte, refer to **CHAPTER 14 OPTION BYTE**. For details of I/O ports, refer to **CHAPTER 4 PORT FUNCTIONS**.

#### 5.4.4 Prescaler

The prescaler divides the clock ( $f_x$ ) output by the system clock oscillator to generate a clock ( $f_{xP}$ ) to be supplied to the peripheral hardware. It also divides the clock to peripheral hardware ( $f_{xP}$ ) to generate a clock to be supplied to the CPU.

**Remark** The clock output by the oscillator selected by the option byte (high-speed internal oscillator, crystal/ceramic oscillator, or external clock input circuit) is divided. For details of the option byte, refer to **CHAPTER 14 OPTION BYTE**.

## 5.5 Operation of CPU Clock Generator

A clock ( $f_{CPU}$ ) is supplied to the CPU from the system clock ( $f_x$ ) oscillated by one of the following three types of oscillators.

- High-speed internal oscillator: Internally oscillates a clock of 8 MHz (TYP.).
- Crystal/ceramic oscillator: Oscillates a clock of 1 MHz to 10 MHz.
- External clock input circuit: Supplies a clock of 1 MHz to 10 MHz to X1 pin.

The system clock oscillator is selected by the option byte. For details of the option byte, refer to **CHAPTER 14 OPTION BYTE**.

### (1) High-speed internal oscillator

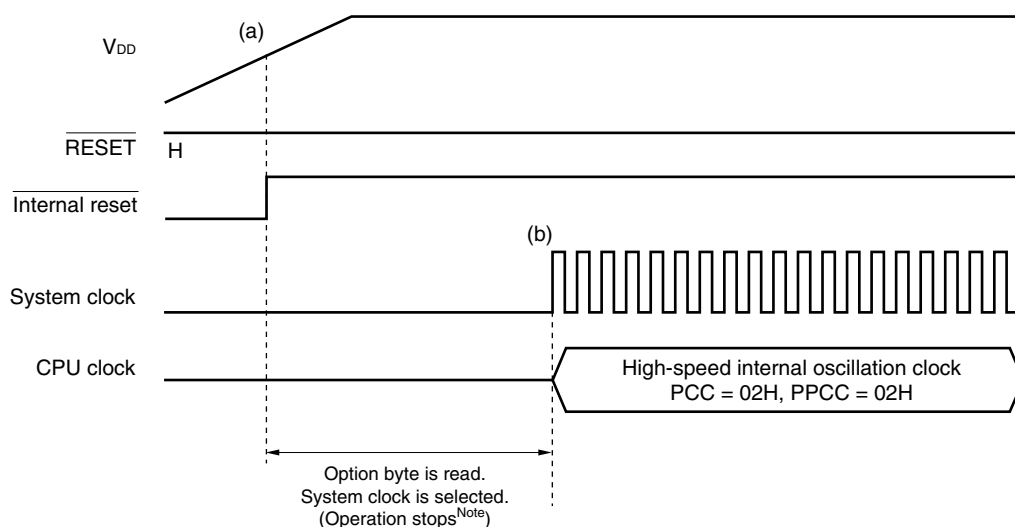
When the high-speed internal oscillation is selected by the option byte, the following is possible.

- Shortening of start time  
If the high-speed internal oscillator is selected as the oscillator, the CPU can be started without having to wait for the oscillation stabilization time of the system clock. Therefore, the start time can be shortened.
- Improvement of expandability  
If the high-speed internal oscillator is selected as the oscillator, the X1 and X2 pins can be used as I/O port pins. For details, refer to **CHAPTER 4 PORT FUNCTIONS**.

Figures 5-8 and 5-9 show the timing chart and status transition diagram of the default start by the high-speed internal oscillation.

**Remark** When the high-speed internal oscillation is used, the clock accuracy is  $\pm 5\%$ .

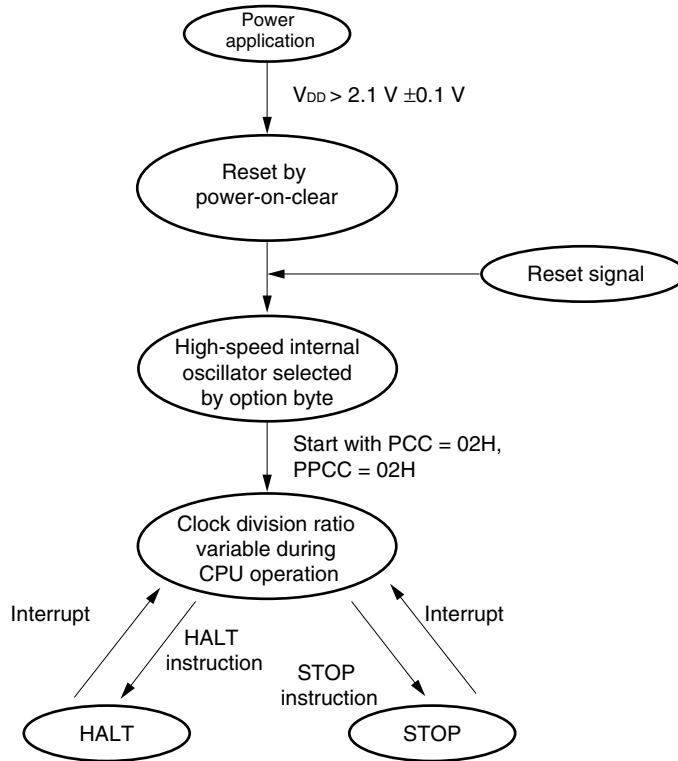
**Figure 5-8. Timing Chart of Default Start by High-Speed Internal Oscillation**



**Note** Operation stop time is 277  $\mu$ s (MIN.), 544  $\mu$ s (TYP.), and 1.075 ms (MAX.).

- (a) The internal reset signal is generated by the power-on-clear function on power application, the option byte is referenced after reset, and the system clock is selected.
- (b) The option byte is referenced and the system clock is selected. Then the high-speed internal oscillation clock operates as the system clock.

**Figure 5-9. Status Transition of Default Start by High-Speed internal oscillation**



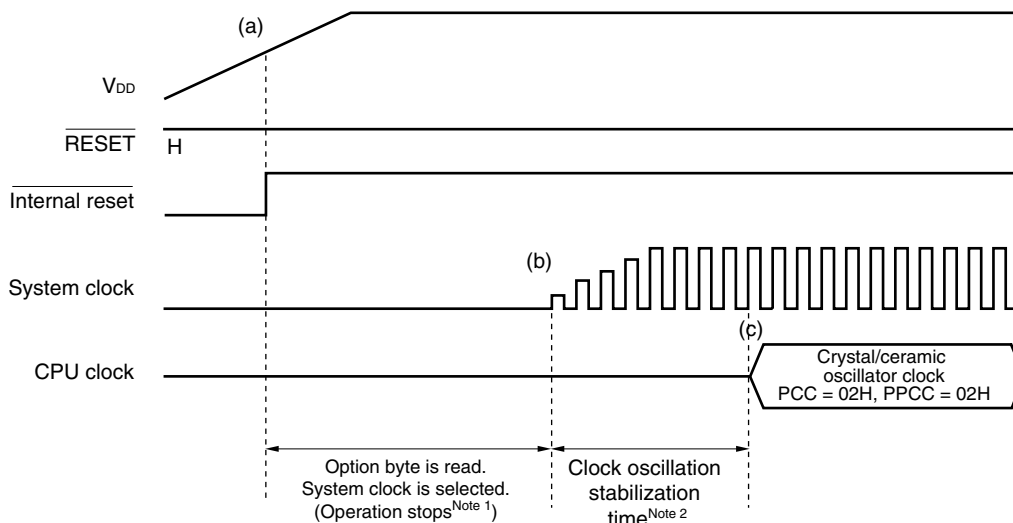
**Remark** PCC: Processor clock control register  
 PPCC: Preprocessor clock control register

**(2) Crystal/ceramic oscillator**

If crystal/ceramic oscillation is selected by the option byte, a clock frequency of 1 MHz to 10 MHz can be selected and the accuracy of processing is improved because the frequency deviation is small, as compared with high-speed internal oscillation (8 MHz (TYP.)).

Figures 5-10 and 5-11 show the timing chart and status transition diagram of default start by the crystal/ceramic oscillator.

**Figure 5-10. Timing Chart of Default Start by Crystal/Ceramic Oscillator**

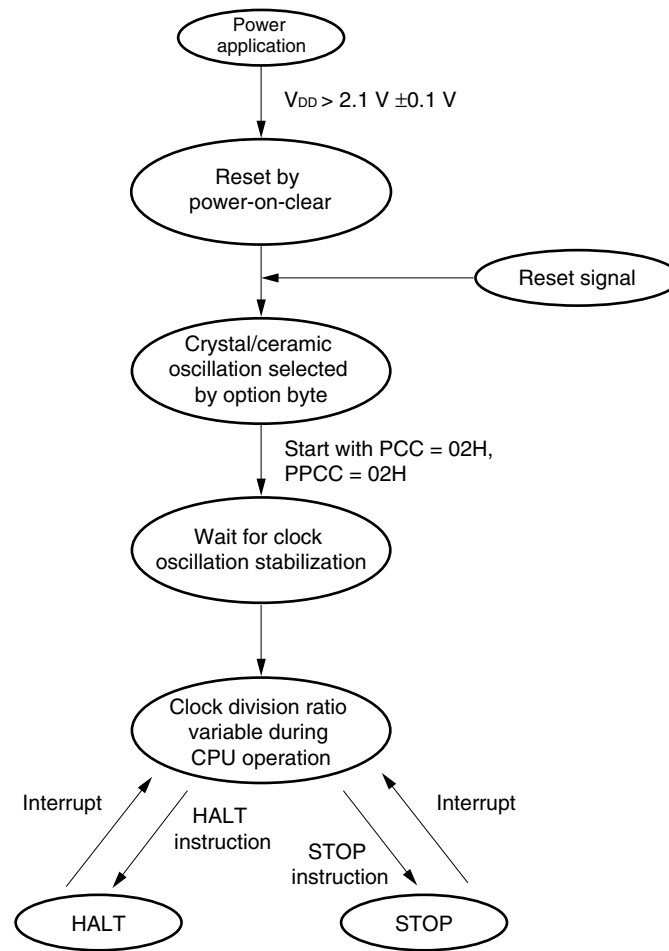


**Notes** 1. Operation stop time is 276  $\mu\text{s}$  (MIN.), 544  $\mu\text{s}$  (TYP.), and 1.074 ms (MAX.).

2. The clock oscillation stabilization time for default start is selected by the option byte. For details, refer to **CHAPTER 14 OPTION BYTE**. The oscillation stabilization time that elapses after the STOP mode is released is selected by the oscillation stabilization time select register (OSTS).

- (a) The internal reset signal is generated by the power-on-clear function on power application, the option byte is referenced after reset, and the system clock is selected.
- (b) After high-speed internal oscillation clock is generated, the option byte is referenced and the system clock is selected. In this case, the crystal/ceramic oscillator clock is selected as the system clock.
- (c) If the system clock is the crystal/ceramic oscillator clock, it starts operating as the CPU clock after clock oscillation is stabilized. The wait time is selected by the option byte. For details, refer to **CHAPTER 14 OPTION BYTE**.

Figure 5-11. Status Transition of Default Start by Crystal/Ceramic Oscillation



**Remark** PCC: Processor clock control register  
 PPCC: Preprocessor clock control register

**(3) External clock input circuit**

If external clock input is selected by the option byte, the following is possible.

- High-speed operation

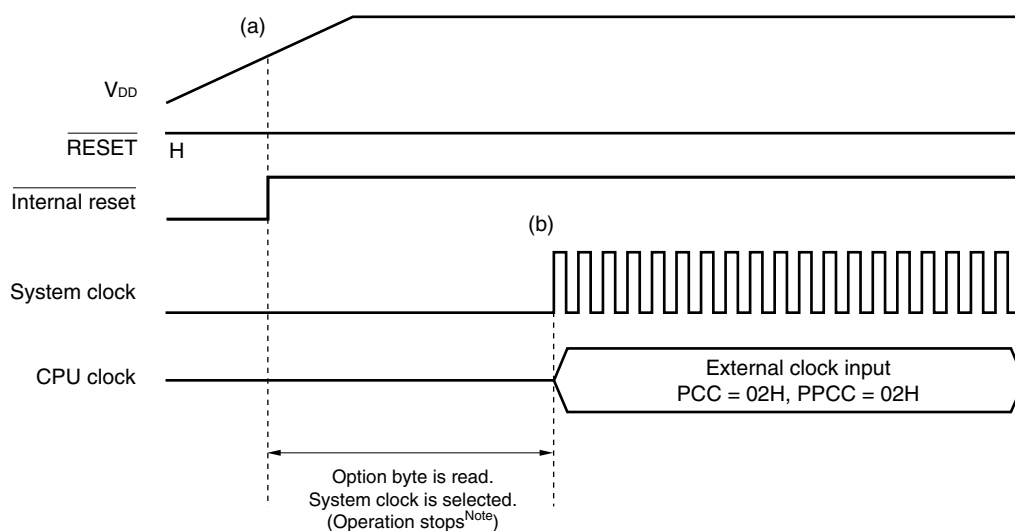
The accuracy of processing is improved as compared with high-speed internal oscillation (8 MHz (TYP.)) because an oscillation frequency of 1 MHz to 10 MHz can be selected and an external clock with a small frequency deviation can be supplied.

- Improvement of expandability

If the external clock input circuit is selected as the oscillator, the X2 pin can be used as an I/O port pin. For details, refer to **CHAPTER 4 PORT FUNCTIONS**.

Figures 5-12 and 5-13 show the timing chart and status transition diagram of default start by external clock input.

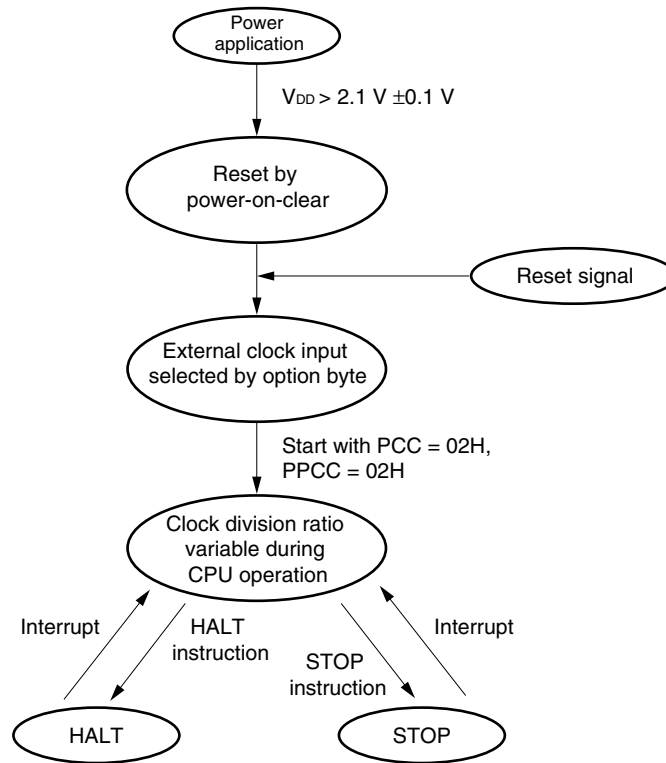
**Figure 5-12. Timing of Default Start by External Clock Input**



**Note** Operation stop time is 277  $\mu$ s (MIN.), 544  $\mu$ s (TYP.), and 1.075 ms (MAX.).

- The internal reset signal is generated by the power-on-clear function on power application, the option byte is referenced after reset, and the system clock is selected.
- The option byte is referenced and the system clock is selected. Then the external clock operates as the system clock.

Figure 5-13. Status Transition of Default Start by External Clock Input



**Remark** PCC: Processor clock control register  
 PPCC: Preprocessor clock control register

## 5.6 Operation of Clock Generator Supplying Clock to Peripheral Hardware

The following two types of clocks are supplied to the peripheral hardware.

- Clock to peripheral hardware ( $f_{XP}$ )
- Low-speed internal oscillation clock ( $f_{RL}$ )

### (1) Clock to peripheral hardware

The clock to the peripheral hardware is supplied by dividing the system clock ( $f_x$ ). The division ratio is selected by the pre-processor clock control register (PPCC).

Three types of frequencies are selectable: " $f_x$ ", " $f_x/2$ ", and " $f_x/2^2$ ". Table 5-3 lists the clocks supplied to the peripheral hardware.

**Table 5-3. Clocks to Peripheral Hardware**

PPCC1	PPCC0	Selection of clock to peripheral hardware ( $f_{XP}$ )
0	0	$f_x$
0	1	$f_x/2$
1	0	$f_x/2^2$
1	1	Setting prohibited

### (2) Low-speed internal oscillation clock

The low-speed internal oscillator of the clock oscillator for interval time generation is always started after release of reset, and oscillates at 240 kHz (TYP.).

It can be specified by the option byte whether the low-speed internal oscillator can or cannot be stopped by software. If it is specified that the low-speed internal oscillator can be stopped by software, oscillation can be started or stopped by using the low-speed internal oscillation mode register (LSRCM). If it is specified that it cannot be stopped by software, the clock source of WDT is fixed to the low-speed internal oscillation clock ( $f_{RL}$ ).

The low-speed internal oscillator is independent of the CPU clock. If it is used as the source clock of WDT, therefore, a hang-up can be detected even if the CPU clock is stopped. If the low-speed internal oscillator is used as a count clock source of 8-bit timer H1, 8-bit timer H1 can operate even in the standby status.

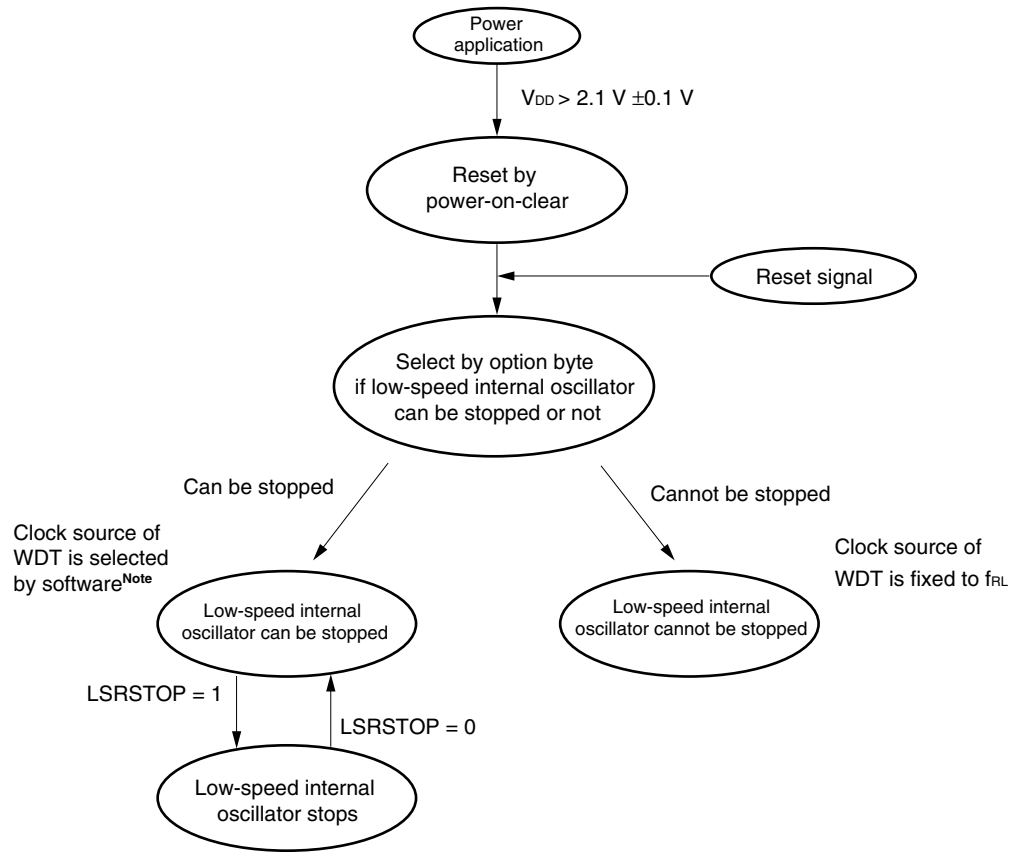
Table 5-4 shows the operation status of the low-speed internal oscillator when it is selected as the source clock of WDT and the count clock of 8-bit timer H1. Figure 5-14 shows the status transition of the low-speed internal oscillator.

**Table 5-4. Operation Status of Low-Speed Internal Oscillator**

Option Byte Setting		CPU Status	WDT Status	TMH1 Status
Can be stopped by software	LSRSTOP = 1	Operation mode	Stopped	Stopped
	LSRSTOP = 0		Operates	Operates
	LSRSTOP = 1	Standby	Stopped	Stopped
	LSRSTOP = 0		Stopped	Operates
Cannot be stopped		Operation mode	Operates	
		Standby		



Figure 5-14. Status Transition of Low-Speed Internal Oscillator



**Note** The clock source of the watchdog timer (WDT) is selected from  $f_x$  or  $f_{RL}$ , or it may be stopped. For details, refer to **CHAPTER 8 WATCHDOG TIMER**.

## CHAPTER 6 16-BIT TIMER/EVENT COUNTER 00

### 6.1 Functions of 16-bit Timer/Event Counter 00

16-bit timer/event counter 00 has the following functions.

#### (1) Interval timer

16-bit timer/event counter 00 generates interrupt requests at the preset time interval.

- Number of counts: 2 to 65536

#### (2) External event counter

16-bit timer/event counter 00 can measure the number of pulses with a high-/low-level width of valid level pulse width or more of a signal input externally.

- Valid level pulse width:  $2/f_{XP}$  or more

#### (3) Pulse width measurement

16-bit timer/event counter 00 can measure the pulse width of an externally input signal.

- Valid level pulse width:  $2/f_{XP}$  or more

#### (4) Square-wave output

16-bit timer/event counter 00 can output a square wave with any selected frequency.

- Cycle:  $(2 \text{ to } 65536) \times 2 \times \text{count clock cycle}$

#### (5) PPG output

16-bit timer/event counter 00 can output a square wave that have arbitrary cycle and pulse width.

- $1 < \text{Pulse width} < \text{Cycle} \leq 65536$

#### (6) One-shot pulse output

16-bit timer/event counter 00 can output a one-shot pulse for which output pulse width can be set to any desired value.

## 6.2 Configuration of 16-bit Timer/Event Counter 00

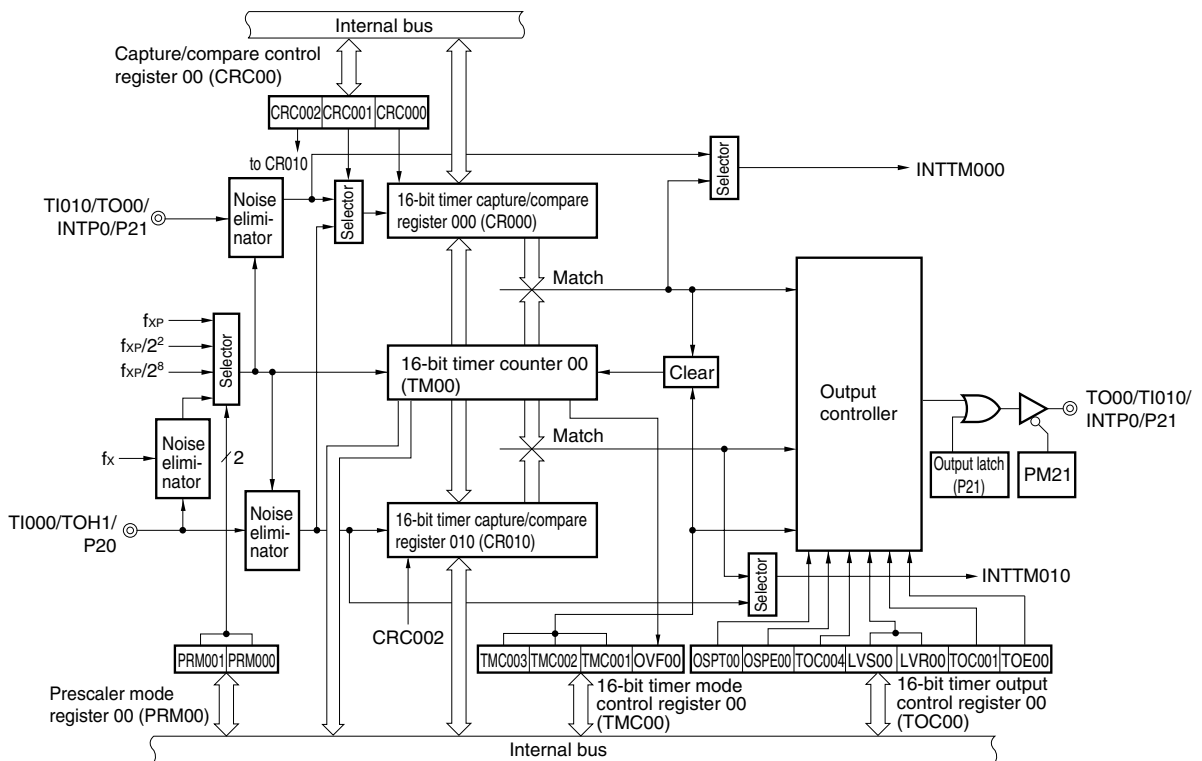
16-bit timer/event counter 00 consists of the following hardware.

**Table 6-1. Configuration of 16-bit Timer/Event Counter 00**

Item	Configuration
Timer counter	16-bit timer counter 00 (TM00)
Register	16-bit timer capture/compare registers 000, 010 (CR000, CR010)
Timer input	TI000, TI010
Timer output	TO00, output controller
Control registers	16-bit timer mode control register 00 (TMC00) Capture/compare control register 00 (CRC00) 16-bit timer output control register 00 (TOC00) Prescaler mode register 00 (PRM00) Port mode register 2 (PM2) Port register 2 (P2)

Figures 6-1 shows a block diagram of these counters.

**Figure 6-1. Block Diagram of 16-bit Timer/Event Counter 00**

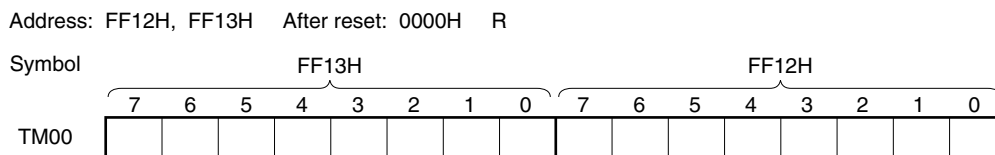


**(1) 16-bit timer counter 00 (TM00)**

TM00 is a 16-bit read-only register that counts count pulses.

The counter is incremented in synchronization with the rising edge of the count clock. If the count value is read during operation, input of the count clock is temporarily stopped, and the count value at that point is read.

**Figure 6-2. Format of 16-bit Timer Counter 00 (TM00)**



The count value is reset to 0000H in the following cases.

- <1> If a reset signal is generated
- <2> If TMC003 and TMC002 are cleared
- <3> If the valid edge of TI000 is input in the clear & start mode entered by inputting the valid edge of TI000
- <4> If TM00 and CR000 match in the clear & start mode entered on a match between TM00 and CR000
- <5> If OSPT00 is set to 1 in the one-shot pulse output mode

**Cautions 1. Even if TM00 is read, the value is not captured by CR010.**

**2. If TM00 is referred to during a timer count, a timer count will be stopped during reference processing, and a timer count is resumed after reference processing is finished.**

**Therefore, if processing which refers to TM00 is performed, an error will arise at a timer count.**

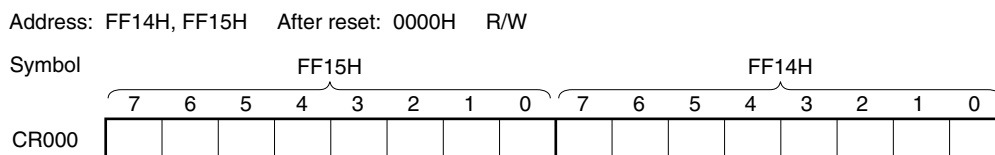
**(2) 16-bit timer capture/compare register 000 (CR000)**

CR000 is a 16-bit register which has the functions of both a capture register and a compare register. Whether it is used as a capture register or as a compare register is set by bit 0 (CRC000) of capture/compare control register 00 (CRC00).

CR000 is set by 16-bit memory manipulation instruction.

A reset signal generation clears CR000 to 0000H.

**Figure 6-3. Format of 16-bit Timer Capture/Compare Register 000 (CR000)**



- **When CR000 is used as a compare register**

The value set in CR000 is constantly compared with the 16-bit timer/counter 00 (TM00) count value, and an interrupt request (INTTM000) is generated if they match. It can also be used as the register that holds the interval time then TM00 is set to interval timer operation.

- **When CR000 is used as a capture register**

It is possible to select the valid edge of the TI000 pin or the TI010 pin as the capture trigger. Setting of the TI000 or TI010 valid edge is performed by means of prescaler mode register 00 (PRM00) (refer to **Table 6-2**).

**Table 6-2. CR000 Capture Trigger and Valid Edges of TI000 and TI010 Pins**

**(1) TI000 pin valid edge selected as capture trigger (CRC001 = 1, CRC000 = 1)**

CR000 Capture Trigger	TI000 Pin Valid Edge		
	ES010	ES000	
Falling edge	Rising edge	0	1
Rising edge	Falling edge	0	0
No capture operation	Both rising and falling edges	1	1

**(2) TI010 pin valid edge selected as capture trigger (CRC001 = 0, CRC000 = 1)**

CR000 Capture Trigger	TI010 Pin Valid Edge		
	ES110	ES100	
Falling edge	Falling edge	0	0
Rising edge	Rising edge	0	1
Both rising and falling edges	Both rising and falling edges	1	1

**Remarks 1.** Setting ES010, ES000 = 1, 0 and ES110, ES100 = 1, 0 is prohibited.

- 2.** ES010, ES000: Bits 5 and 4 of prescaler mode register 00 (PRM00)  
 ES110, ES100: Bits 7 and 6 of prescaler mode register 00 (PRM00)  
 CRC001, CRC000: Bits 1 and 0 of capture/compare control register 00 (CRC00)

- Cautions 1.** Set CR000 to other than 0000H in the clear & start mode entered on match between TM00 and CR000. This means a 1-pulse count operation cannot be performed when this register is used as an external event counter. However, in the free-running mode and in the clear & start mode using the valid edge of the TI000 pin, if CR000 is set to 0000H, an interrupt request (INTTM00) is generated when CR000 changes from 0000H to 0001H after an overflow (FFFFH).
- 2.** If the new value of CR000 is less than the value of 16-bit timer counter 0 (TM00), TM00 continues counting, overflows, and then starts counting from 0 again. If the new value of CR000 is less than the old value, therefore, the timer must be reset to be restarted after the value of CR000 is changed.
- 3.** The value of CR000 after 16-bit timer/event counter 00 has stopped is not guaranteed.
- 4.** The capture operation may not be performed for CR000 set in compare mode even if a capture trigger is input.
- 5.** When using P21 as the input pin (TI010) of the valid edge, it cannot be used as a timer output pin (TO00). When using P21 as the timer output pin (TO00), it cannot be used as the input pin (TI010) of the valid edge.
- 6.** If the register read period and the input of the capture trigger conflict when CR000 is used as a capture register, the capture trigger input takes precedence and the read data is undefined. Also, if the count stop of the timer and the input of the capture trigger conflict, the capture trigger is undefined.
- 7.** Changing the CR000 setting may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-bit Timer/Event Counter 00 (17) Changing compare register during timer operation.

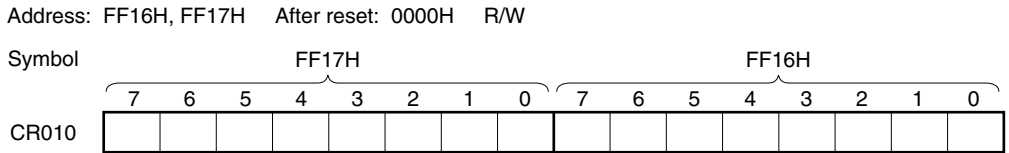
**(3) 16-bit timer capture/compare register 010 (CR010)**

CR010 is a 16-bit register which has the functions of both a capture register and a compare register. Whether it is used as a capture register or a compare register is set by bit 2 (CRC002) of capture/compare control register 00 (CRC00).

CR010 is set by 16-bit memory manipulation instruction.

Reset signal generation clears CR010 to 0000H.

**Figure 6-4. Format of 16-bit Timer Capture/Compare Register 010 (CR010)**



- **When CR010 is used as a compare register**

The value set in CR010 is constantly compared with the 16-bit timer counter 00 (TM00) count value, and an interrupt request (INTTM010) is generated if they match.

- **When CR010 is used as a capture register**

It is possible to select the valid edge of the TI000 pin as the capture trigger. The TI000 valid edge is set by means of prescaler mode register 00 (PRM00) (refer to **Table 6-3**).

**Table 6-3. CR010 Capture Trigger and Valid Edge of TI000 Pin (CRC002 = 1)**

CR010 Capture Trigger	TI000 Pin Valid Edge		
	ES010	ES000	
Falling edge	Falling edge	0	0
Rising edge	Rising edge	0	1
Both rising and falling edges	Both rising and falling edges	1	1

**Remarks** 1. Setting ES010, ES000 = 1, 0 is prohibited.

2. ES010, ES000: Bits 5 and 4 of prescaler mode register 00 (PRM00)

CRC002: Bit 2 of capture/compare control register 00 (CRC00)

**Cautions** 1. In the free-running mode and in the clear & start mode using the valid edge of the TI000 pin, if CR010 is set to 0000H, an interrupt request (INTTM010) is generated when CR010 changes from 0000H to 0001H after an overflow (FFFFH).

2. If the new value of CR010 is less than the value of 16-bit timer counter 00 (TM00), TM00 continues counting, overflows, and then starts counting from 0 again. If the new value of CR010 is less than the old value, therefore, the timer must be reset to be restarted after the value of CR010 is changed.

3. The value of CR010 after 16-bit timer/event counter 00 has stopped is not guaranteed.

4. The capture operation may not be performed for CR010 set in compare mode even if a capture trigger is input.

5. If the register read period and the input of the capture trigger conflict when CR010 is used as a capture register, the capture trigger input takes precedence and the read data is undefined. Also, if the timer count stop and the input of the capture trigger conflict, the capture data is undefined.

**Caution 6.** Changing the CR010 setting during TM00 operation may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-bit Timer/Event Counter 00 (17) Changing compare register during timer operation.

### 6.3 Registers to Control 16-bit Timer/Event Counter 00

The following seven types of registers are used to control 16-bit timer/event counter 00.

- 16-bit timer mode control register 00 (TMC00)
- Capture/compare control register 00 (CRC00)
- 16-bit timer output control register 00 (TOC00)
- Prescaler mode register 00 (PRM00)
- Port mode register 2 (PM2)
- Port register 2 (P2)

#### (1) 16-bit timer mode control register 00 (TMC00)

This register sets the 16-bit timer operating mode, the 16-bit timer counter 00 (TM00) clear mode, and output timing, and detects an overflow.

TMC00 is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets the value of TMC00 to 00H.

**Caution** 16-bit timer counter 00 (TM00) starts operating as soon as values other than 0 and 0 (operation stop mode) are set to TMC002 and TMC003, respectively. Set TMC002 and TMC003 to 0 and 0 to stop operation.

Figure 6-5. Format of 16-bit Timer Mode Control Register 00 (TMC00)

Address: FF60H After reset: 00H R/W

Symbol 7 6 5 4 3 2 1 &lt;0&gt;

TMC00	0	0	0	0	TMC003	TMC002	TMC001	OVF00
-------	---	---	---	---	--------	--------	--------	-------

TMC003	TMC002	TMC001	Operating mode and clear mode selection	TO00 inversion timing selection	Interrupt request generation
0	0	0	Operation stop (TM00 cleared to 0)	No change	Not generated
0	0	1			
0	1	0	Free-running mode	Match between TM00 and CR000 or match between TM00 and CR010	< When operating as compare register > Generated on match between TM00 and CR000, or match between TM00 and CR010 < When operating as capture register >
0	1	1		Match between TM00 and CR000, match between TM00 and CR010 or TI000 pin valid edge	
1	0	0	Clear & start occurs on valid edge of TI000 pin	-	Generated on TI000 pin and TI010 pin valid edge
1	0	1			
1	1	0	Clear & start occurs on match between TM00 and CR000	Match between TM00 and CR000 or match between TM00 and CR010	
1	1	1		Match between TM00 and CR000, match between TM00 and CR010 or TI000 pin valid edge	

OVF00	Overflow detection of 16-bit timer counter 00 (TM00)
0	Overflow not detected
1	Overflow detected

- Cautions**
1. The timer operation must be stopped before writing to bits other than the OVF00 flag.
  2. If the timer is stopped, timer counts and timer interrupts do not occur, even if a signal is input to the TI000/TI010 pins.
  3. Except when the valid edge of the TI000 pin is selected as the count clock, stop the timer operation before setting STOP mode or system clock stop mode; otherwise the timer may malfunction when the system clock starts.
  4. Set the valid edge of the TI000 pin with bits 4 and 5 of prescaler mode register 00 (PRM00) after stopping the timer operation.
  5. If the clear & start mode entered on a match between TM00 and CR000, clear & start mode at the valid edge of the TI000 pin, or free-running mode is selected, when the set value of CR000 is FFFFH and the TM00 value changes from FFFFH to 0000H, the OVF00 flag is set to 1.
  6. Even if the OVF00 flag is cleared before the next count clock is counted (before TM00 becomes 0001H) after the occurrence of a TM00 overflow, the OVF00 flag is re-set and clearance becomes invalid.
  7. The capture operation is performed at the fall of the count clock. An interrupt request input (INTTM0n0), however, occurs at the rise of the next count clock.



**Remark** TM00: 16-bit timer counter 00  
 CR000: 16-bit timer capture/compare register 000  
 CR010: 16-bit timer capture/compare register 010

**(2) Capture/compare control register 00 (CRC00)**

This register controls the operation of the 16-bit capture/compare registers (CR000, CR010).

CRC00 is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets the value of CRC00 to 00H.

**Figure 6-6. Format of Capture/Compare Control Register 00 (CRC00)**

Address: FF62H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CRC00	0	0	0	0	0	CRC002	CRC001	CRC000

CRC002	CR010 operating mode selection
0	Operate as compare register
1	Operate as capture register

CRC001	CR000 capture trigger selection
0	Capture on valid edge of TI010 pin
1	Capture on valid edge of TI000 pin by reverse phase <sup>Note</sup>

CRC000	CR000 operating mode selection
0	Operate as compare register
1	Operate as capture register

**Note** When the CRC001 bit value is 1, capture is not performed if both the rising and falling edges have been selected as the valid edges of the TI000 pin.

- Cautions**
1. The timer operation must be stopped before setting CRC00.
  2. When the clear & start mode entered on a match between TM00 and CR000 is selected by 16-bit timer mode control register 00 (TMC00), CR000 should not be specified as a capture register.
  3. To ensure the reliability of the capture operation, the capture trigger requires a pulse longer than two cycles of the count clock selected by prescaler mode register 00 (PRM00) (refer to Figure 6-17).

**(3) 16-bit timer output control register 00 (TOC00)**

This register controls the operation of the 16-bit timer/event counter output controller. It sets timer output F/F set/reset, output inversion enable/disable, 16-bit timer/event counter 00 timer output enable/disable, one-shot pulse output operation enable/disable, and output trigger of one-shot pulse by software.

TOC00 is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets the value of TOC00 to 00H.

**Figure 6-7. Format of 16-bit Timer Output Control Register 00 (TOC00)**

Address: FF63H After reset: 00H R/W

Symbol	7	<6>	<5>	4	<3>	<2>	1	<0>
TOC00	0	OSPT00	OSPE00	TOC004	LVS00	LVR00	TOC001	TOE00
OSPT00	One-shot pulse output trigger control via software							
0	No one-shot pulse output trigger							
1	One-shot pulse output trigger							
OSPE00	One-shot pulse output operation control							
0	Successive pulse output mode							
1	One-shot pulse output mode <sup>Note</sup>							
TOC004	Timer output F/F control using match of CR010 and TM00							
0	Disables inversion operation							
1	Enables inversion operation							
LVS00	LVR00	Timer output F/F status setting						
0	0	No change						
0	1	Timer output F/F reset (0)						
1	0	Timer output F/F set (1)						
1	1	Setting prohibited						
TOC001	Timer output F/F control using match of CR000 and TM00							
0	Disables inversion operation							
1	Enables inversion operation							
TOE00	Timer output control							
0	Disables output (output fixed to level 0)							
1	Enables output							

**Note** The one-shot pulse output mode operates correctly only in the free-running mode and the mode in which clear & start occurs at the TI000 pin valid edge. In the mode in which clear & start occurs on a match between TM00 and CR000, one-shot pulse output is not possible because an overflow does not occur.

- Cautions**
1. Timer operation must be stopped before setting other than OSPT00.
  2. If LVS00 and LVR00 are read, 0 is read.
  3. OSPT00 is automatically cleared after data is set, so 0 is read.
  4. Do not set OSPT00 to 1 other than in one-shot pulse output mode.
  5. A write interval of two cycles or more of the count clock selected by prescaler mode register 00 (PRM00) is required, when OSPT00 is set to 1 successively.

**Caution 6.** When TOE00 is 0, set TOE00, LVS00, and LVR00 at the same time with the 8-bit memory manipulation instruction. When TOE00 is 1, LVS00 and LVR00 can be set with the 1-bit memory manipulation instruction.

**(4) Prescaler mode register 00 (PRM00)**

This register is used to set the 16-bit timer counter 00 (TM00) count clock and the TI000, TI010 pin input valid edges.

PRM00 is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets the value of PRM00 to 00H.

**Figure 6-8. Format of Prescaler Mode Register 00 (PRM00)**

Address: FF61H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PRM00	ES110	ES100	ES010	ES000	0	0	PRM001	PRM000

ES110	ES100	TI010 pin valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES010	ES000	TI000 pin valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

PRM001	PRM000	Count clock selection
0	0	$f_{XP}$ (10 MHz)
0	1	$f_{XP}/2^2$ (2.5 MHz)
1	0	$f_{XP}/2^3$ (39.06 kHz)
1	1	TI000 pin valid edge <sup>Note</sup>

**Remarks 1.**  $f_{XP}$ : Oscillation frequency of clock supplied to peripheral hardware

**2.** ( ):  $f_{XP} = 10$  MHz

**Note** The external clock requires a pulse longer than two cycles of the internal count clock ( $f_{XP}$ ).

**Cautions 1.** Always set data to PRM00 after stopping the timer operation.

**2.** If the valid edge of the TI000 pin is to be set as the count clock, do not set the clear/start mode and the capture trigger at the valid edge of the TI000 pin.

- Cautions 3.** In the following cases, note with caution that the valid edge of the TI0n0 pin is detected.
- <1> Immediately after a system reset, if a high level is input to the TI0n0 pin, the operation of 16-bit timer counter 00 (TM00) is enabled
    - If the rising edge or both rising and falling edges are specified as the valid edge of the TI0n0 pin, a rising edge is detected immediately after the TM00 operation is enabled.
  - <2> If the TM00 operation is stopped while the TI0n0 pin is at high level, TM00 operation is then enabled after a low level is input to the TI0n0 pin
    - If the falling edge or both rising and falling edges are specified as the valid edge of the TI0n0 pin, a falling edge is detected immediately after the TM00 operation is enabled.
  - <3> If the TM00 operation is stopped while the TI0n0 pin is at low level, TM00 operation is then enabled after a high level is input to the TI0n0 pin
    - If the rising edge or both rising and falling edges are specified as the valid edge of the TI0n0 pin, a rising edge is detected immediately after the TM00 operation is enabled.
4. The sampling clock used to eliminate noise differs when the valid edge of TI000 is used as the count clock and when it is used as a capture trigger. In the former case, the count clock is  $f_{XP}$ , and in the latter case the count clock is selected by prescaler mode register 00 (PRM00). The capture operation is not performed until the valid edge is sampled and the valid level is detected twice, thus eliminating noise with a short pulse width.
5. When using P21 as the input pin (TI010) of the valid edge, it cannot be used as a timer output pin (TO00). When using P21 as the timer output pin (TO00), it cannot be used as the input pin (TI010) of the valid edge.

**Remark** n = 0, 1

**(5) Port mode register 2 (PM2)**

When using the P21/TO00/TI010/INTP0 pin for timer output, clear PM21, the output latch of P21.  
 When using the P20/TI000/TOH1 and P21/TO00/TI010/INTP0 pins as a timer input, set PM20 and PM21 to 1.  
 At this time, the output latches of P20 and P21 can be either 0 or 1.  
 PM2 is set by a 1-bit or 8-bit memory manipulation instruction.  
 Reset signal generation sets the value of PM2 to FFH.

**Figure 6-9. Format of Port Mode Register 2 (PM2)**

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	1	1	PM23	PM22	PM21	PM20

PM2n	P2n pin I/O mode selection (n = 0 to 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

## 6.4 Operation of 16-bit Timer/Event Counter 00

### 6.4.1 Interval timer operation

Setting 16-bit timer mode control register 00 (TMC00) and capture/compare control register 00 (CRC00) as shown in Figure 6-11 allows operation as an interval timer.

#### Setting

The basic operation setting procedure is as follows.

- <1> Set the CRC00 register (see **Figure 6-10** for the set value).
- <2> Set any value to the CR000 register.
- <3> Set the count clock by using the PRM00 register.
- <4> Set the TMC00 register to start the operation (see **Figure 6-10** for the set value).

**Caution** Changing the CR000 setting during TM00 operation may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-bit Timer/Event Counter 00 (17) Changing compare register during timer operation.

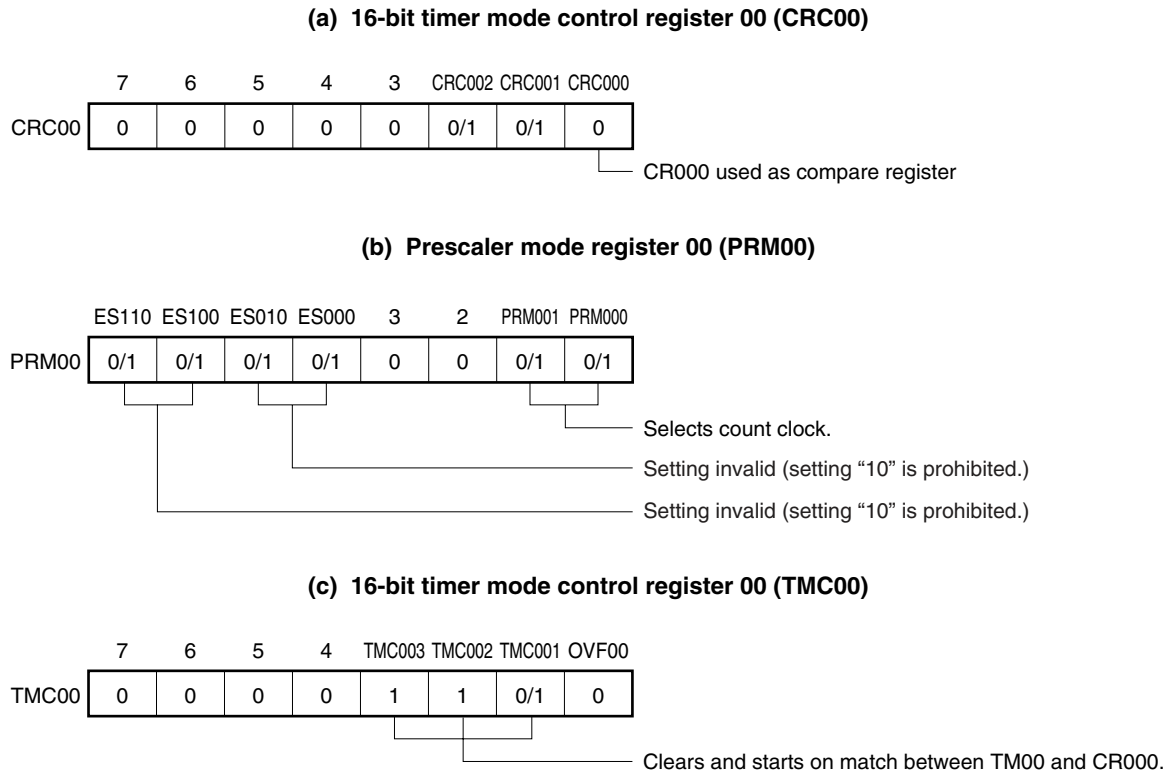
**Remark** For how to enable the INTTM000 interrupt, see **CHAPTER 9 INTERRUPT FUNCTIONS**.

Interrupt requests are generated repeatedly using the count value set in 16-bit timer capture/compare register 000 (CR000) beforehand as the interval.

When the count value of 16-bit timer counter 00 (TM00) matches the value set to CR000, counting continues with the TM00 value cleared to 0 and the interrupt request signal (INTTM000) is generated.

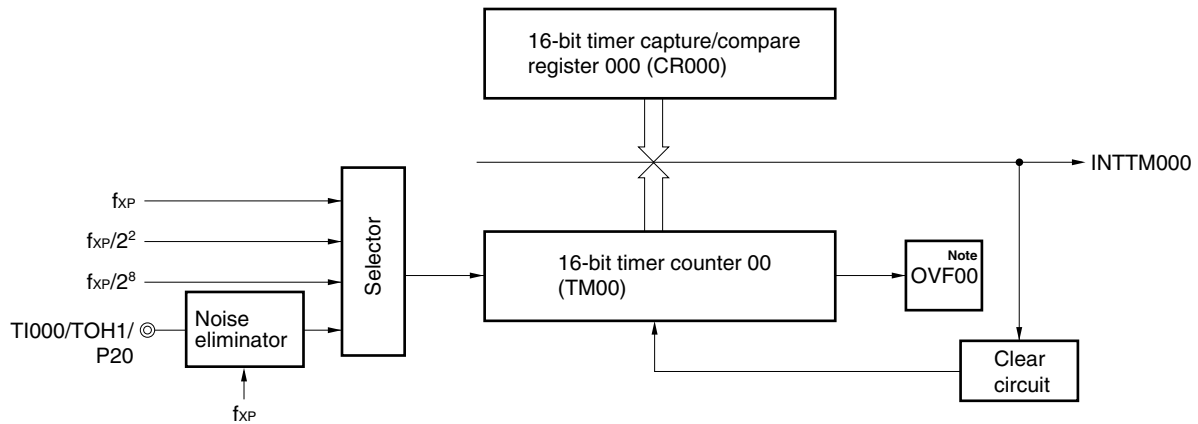
The count clock of the 16-bit timer/event counter can be selected using bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00).

Figure 6-10. Control Register Settings for Interval Timer Operation



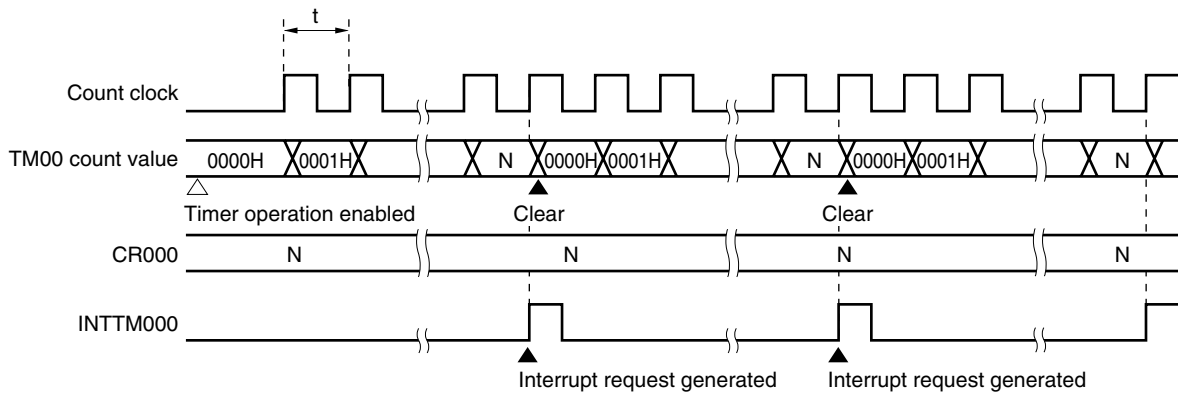
**Remark** 0/1: Setting 0 or 1 allows another function to be used simultaneously with the interval timer. See the description of the respective control registers for details.

Figure 6-11. Interval Timer Configuration Diagram



**Note** OVF00 is set to 1 only when 16-bit timer capture/compare register 000 is set to FFFFH.

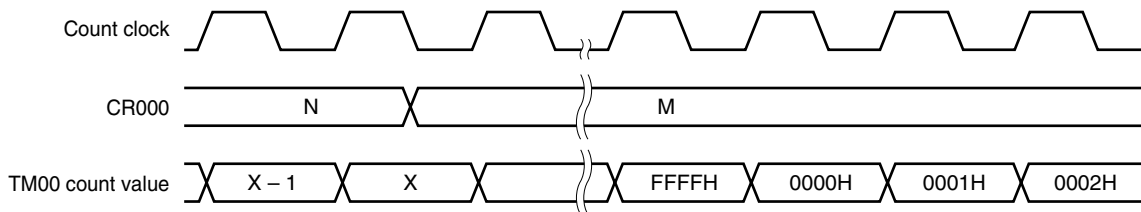
Figure 6-12. Timing of Interval Timer Operation



**Remark** Interval time =  $(N + 1) \times t$   
 $N = 0001H$  to  $FFFFH$  (settable range)

When the compare register is changed during timer count operation, if the value after 16-bit timer capture/compare register 000 (CR000) is changed is smaller than that of 16-bit timer counter 00 (TM00), TM00 continues counting, overflows and then restarts counting from 0. Thus, if the value (M) after the CR000 change is smaller than that (N) before the change, it is necessary to restart the timer after changing CR000.

Figure 6-13. Timing After Change of Compare Register During Timer Count Operation (N → M: N > M)



**Remark**  $N > X > M$

### 6.4.2 External event counter operation

#### Setting

The basic operation setting procedure is as follows.

- <1> Set the CRC00 register (see **Figure 6-14** for the set value).
- <2> Set the count clock by using the PRM00 register.
- <3> Set any value to the CR000 register (0000H cannot be set).
- <4> Set the TMC00 register to start the operation (see **Figure 6-14** for the set value).

- Remarks**
1. For the setting of the TI000 pin, see **6.3 (5) Port mode register 2 (PM2)**.
  2. For how to enable the INTTM000 interrupt, see **CHAPTER 9 INTERRUPT FUNCTIONS**.

The external event counter counts the number of external clock pulses to be input to the TI000 pin with using 16-bit timer counter 00 (TM00).

TM00 is incremented each time the valid edge specified by prescaler mode register 00 (PRM00) is input.

When the TM00 count value matches the 16-bit timer capture/compare register 000 (CR000) value, TM00 is cleared to 0 and the interrupt request signal (INTTM000) is generated.

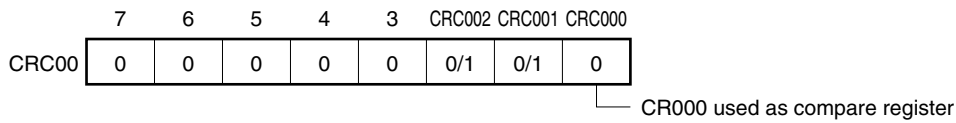
Input a value other than 0000H to CR000. (A count operation with a pulse cannot be carried out.)

The rising edge, the falling edge, or both edges can be selected using bits 4 and 5 (ES000 and ES010) of prescaler mode register 00 (PRM00).

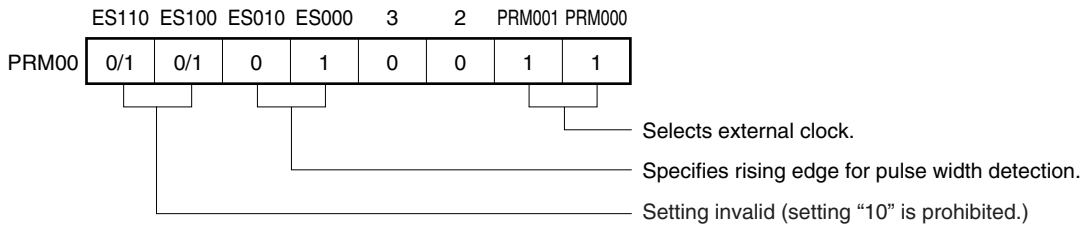
Because an operation is carried out only when the valid edge of the TI000 pin is detected twice after sampling with the internal clock ( $f_{XP}$ ), noise with a short pulse width can be removed.

**Figure 6-14. Control Register Settings in External Event Counter Mode (with Rising Edge Specified)**

**(a) Capture/compare control register 00 (CRC00)**



**(b) Prescaler mode register 00 (PRM00)**



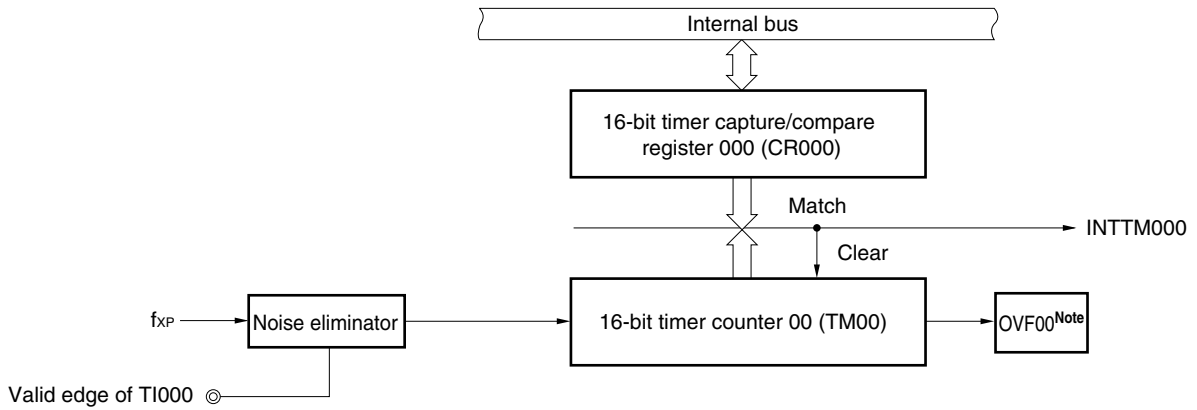
**(c) 16-bit timer mode control register 00 (TMC00)**



**Remark** 0/1: Setting 0 or 1 allows another function to be used simultaneously with the external event counter. See the description of the respective control registers for details.



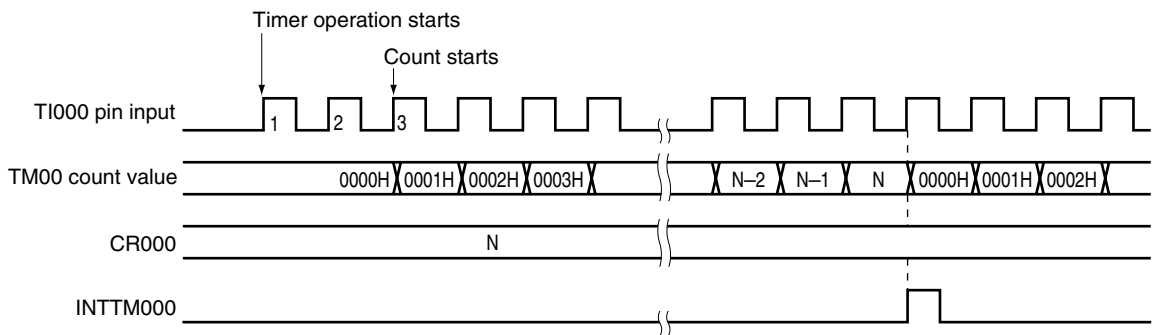
Figure 6-15. External Event Counter Configuration Diagram



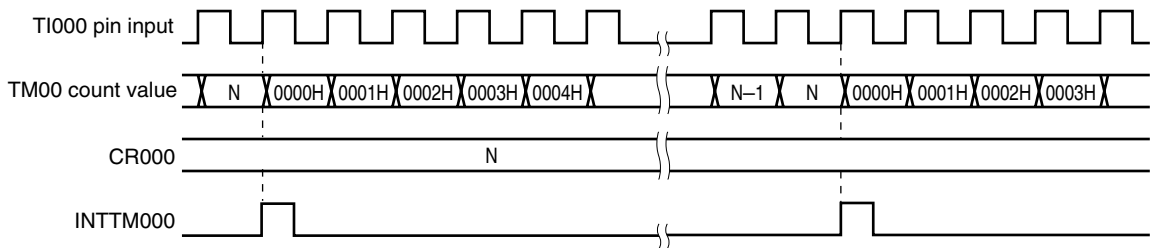
**Note** OVF00 is 1 only when 16-bit timer capture/compare register 000 is set to FFFFH.

Figure 6-16. External Event Counter Operation Timing (with Rising Edge Specified)

(1) INTTM000 generation timing immediately after operation starts  
Counting is started after a valid edge is detected twice.



(2) INTTM000 generation timing after INTTM000 has been generated twice



**Caution** When reading the external event counter count value, TM00 should be read.

### 6.4.3 Pulse width measurement operations

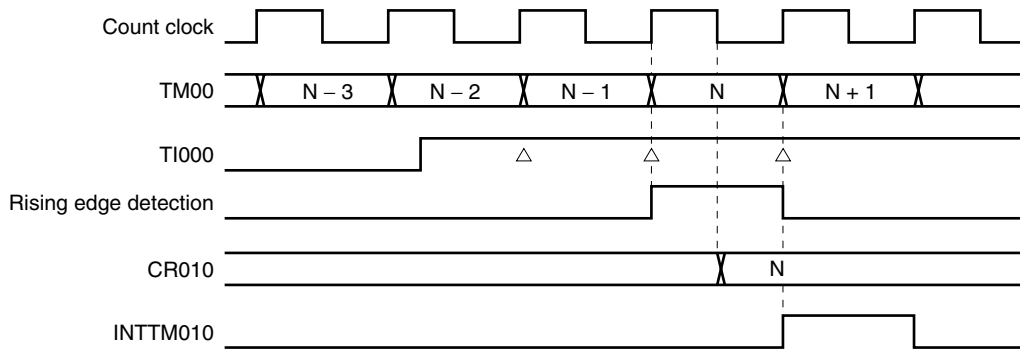
It is possible to measure the pulse width of the signals input to the TI000 pin and TI010 pin using 16-bit timer counter 00 (TM00).

There are two measurement methods: measuring with TM00 used in free-running mode, and measuring by restarting the timer in synchronization with the edge of the signal input to the TI000 pin.

When an interrupt occurs, necessary pulse width is calculable by reading the valid value of the capture register.

The capture operation is not performed until the signal pulse width is sampled in the count clock cycle selected by prescaler mode register 00 (PRM00) and the valid level of the TI000 or TI010 pin is detected twice, thus eliminating noise with a short pulse width (see **Figure 6-17**).

**Figure 6-17. CR010 Capture Operation with Rising Edge Specified**



#### Setting

The basic operation setting procedure is as follows.

- <1> Set the CRC00 register (see **Figures 6-18, 6-21, 6-23, and 6-25** for the set value).
- <2> Set the count clock by using the PRM00 register.
- <3> Set the TMC00 register to start the operation (see **Figures 6-18, 6-21, 6-23, and 6-25** for the set value).

**Caution** To use two capture registers, set the TI000 and TI010 pins.

**Remarks 1.** For the setting of the TI000 (or TI010) pin, see **6.3 (5) Port mode register 2 (PM2)**.

- 2. For how to enable the INTTM000 (or INTTM010) interrupt, see **CHAPTER 9 INTERRUPT FUNCTIONS**.

#### (1) Pulse width measurement with free-running counter and one capture register

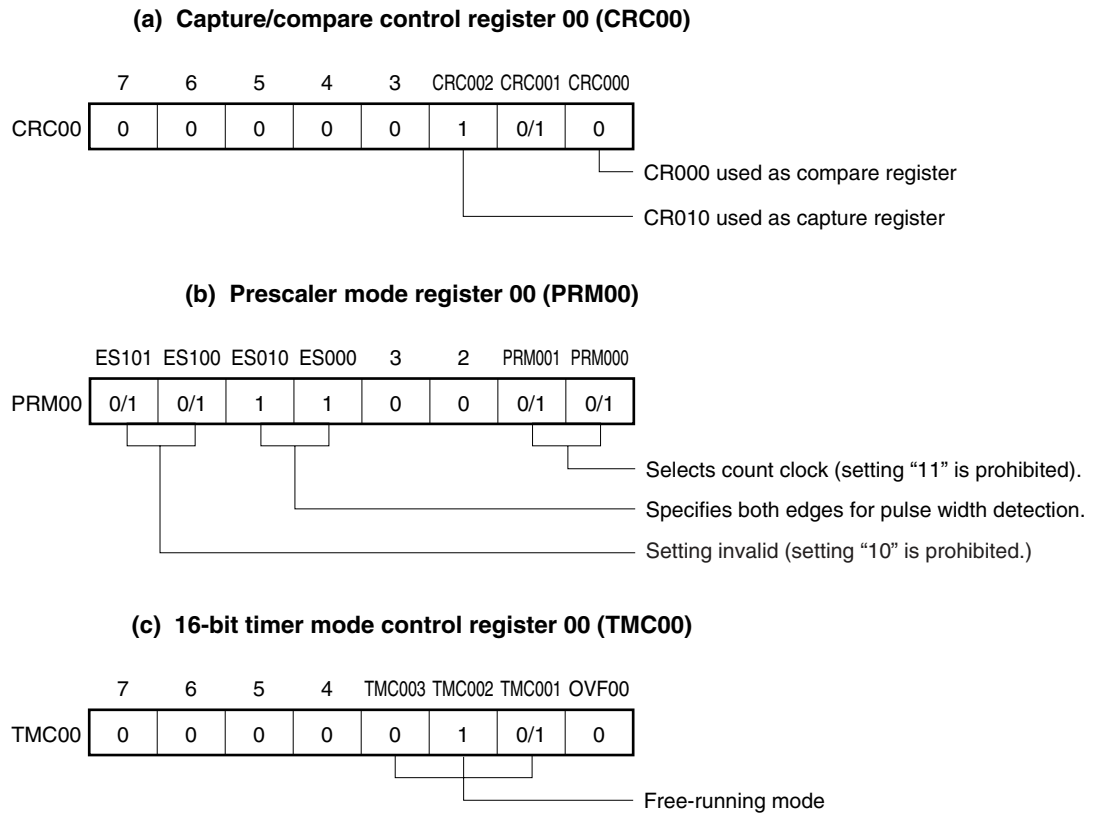
Specify both the rising and falling edges as the valid edges of the TI000 pin, by using bits 4 and 5 (ES000 and ES010) of PRM00.

When 16-bit timer counter 00 (TM00) is operated in free-running mode, and the valid edge specified by PRM00 is input, the value of TM00 is taken into 16-bit timer capture/compare register 010 (CR010) and an external interrupt request signal (INTTM010) is set.

Sampling is performed using the count clock selected by PRM00, and a capture operation is only performed when a valid level of the TI000 pin is detected twice, thus eliminating noise with a short pulse width.

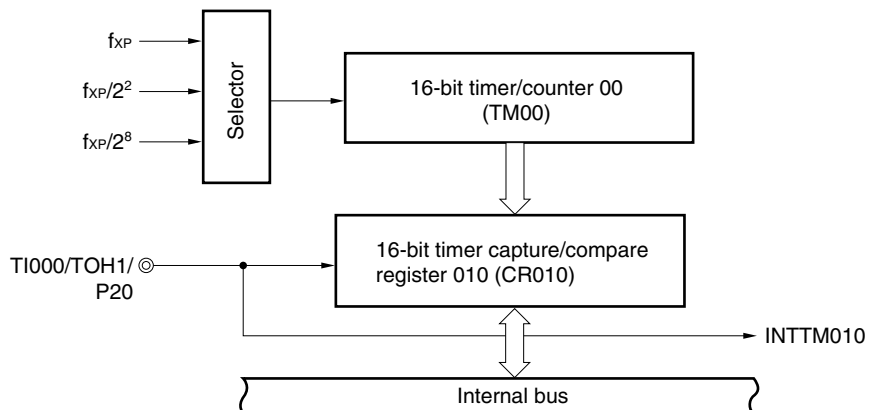
**Caution** The measurable pulse width in this operation example is up to 1 cycle of the timer counter.

**Figure 6-18. Control Register Settings for Pulse Width Measurement with Free-Running Counter and One Capture Register (When TI000 and CR010 Are Used)**

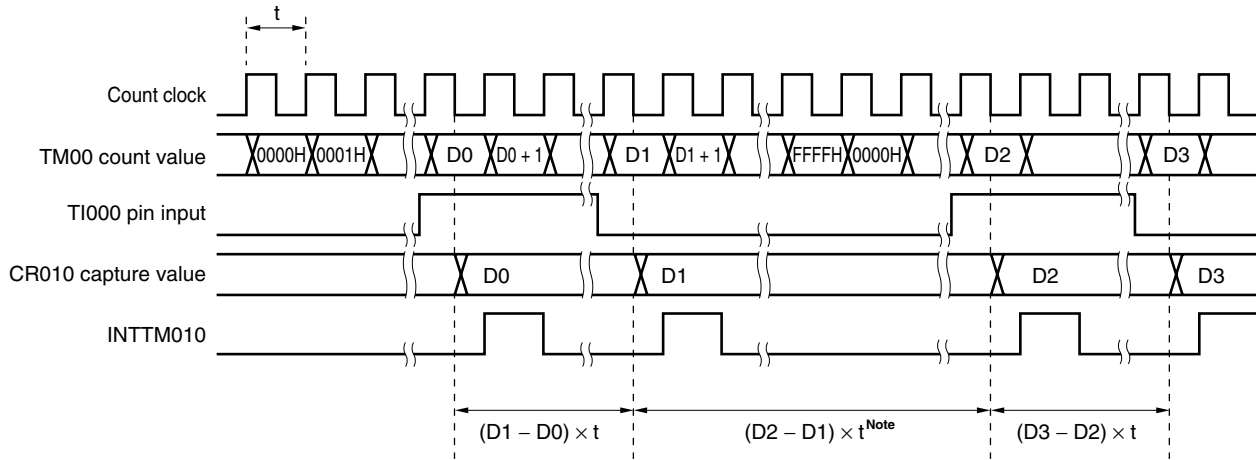


**Remark** 0/1: Setting 0 or 1 allows another function to be used simultaneously with pulse width measurement. See the description of the respective control registers for details.

**Figure 6-19. Configuration Diagram for Pulse Width Measurement by Free-Running Counter**



**Figure 6-20. Timing of Pulse Width Measurement Operation by Free-Running Counter and One Capture Register (with Both Edges Specified)**



**Note** The carry flag is set to 1. Ignore this setting.

## (2) Measurement of two pulse widths with free-running counter

When 16-bit timer counter 00 (TM00) is operated in free-running mode, it is possible to simultaneously measure the pulse widths of the two signals input to the TI000 pin and the TI010 pin.

Specify both the rising and falling edges as the valid edges of the TI000 and TI010 pins, by using bits 4 and 5 (ES000 and ES010) and bits 6 and 7 (ES100 and ES110) of PRM00.

When the valid edge specified by bits 4 and 5 (ES000 and ES010) of prescaler mode register 00 (PRM00) is input to the TI000 pin, the value of TM00 is taken into 16-bit timer capture/compare register 010 (CR010) and an interrupt request signal (INTTM010) is set.

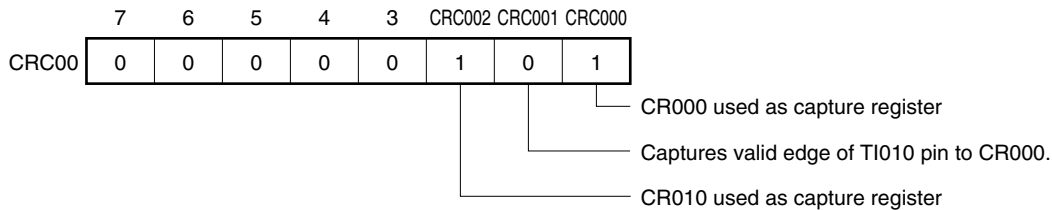
Also, when the valid edge specified by bits 6 and 7 (ES100 and ES110) of PRM00 is input to the TI010 pin, the value of TM00 is taken into 16-bit timer capture/compare register 000 (CR000) and an interrupt request signal (INTTM000) is set.

Sampling is performed using the count clock cycle selected by prescaler mode register 00 (PRM00), and a capture operation is only performed when a valid level of the TI000 or TI010 pin is detected twice, thus eliminating noise with a short pulse width.

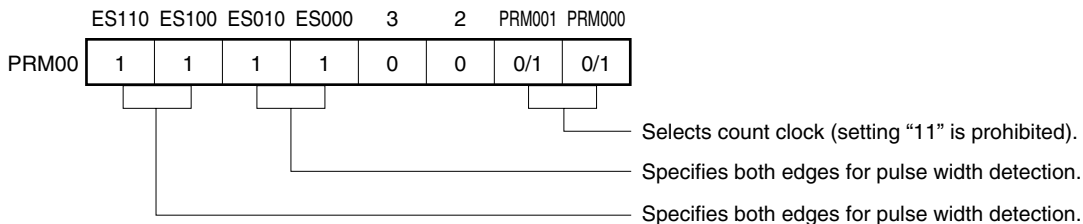
**Caution** The measurable pulse width in this operation example is up to 1 cycle of the timer counter.

Figure 6-21. Control Register Settings for Measurement of Two Pulse Widths with Free-Running Counter

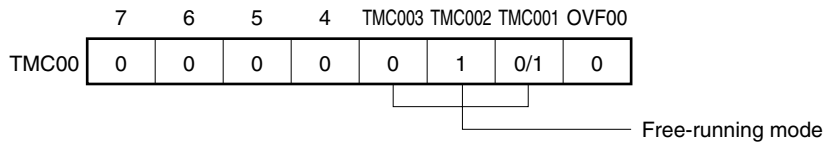
(a) Capture/compare control register 00 (CRC00)



(b) Prescaler mode register 00 (PRM00)

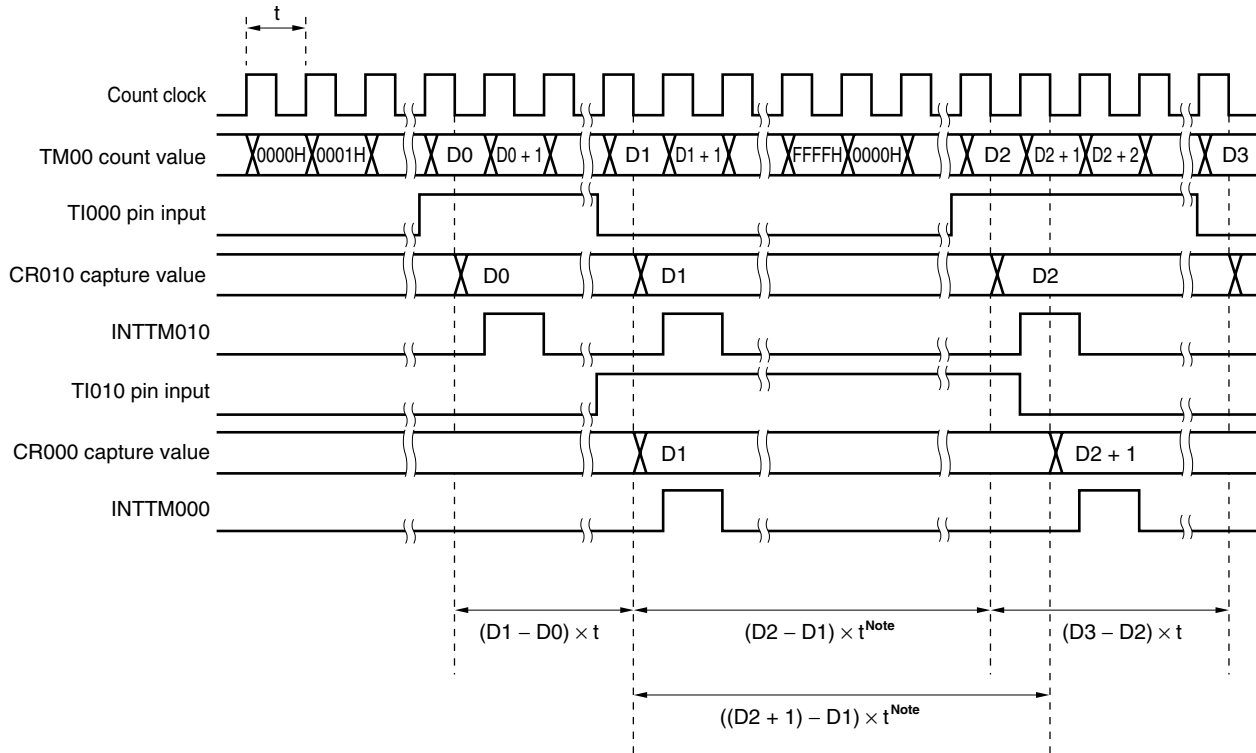


(c) 16-bit timer mode control register 00 (TMC00)



**Remark** 0/1: Setting 0 or 1 allows another function to be used simultaneously with pulse width measurement. See the description of the respective control registers for details.

**Figure 6-22. Timing of Pulse Width Measurement Operation with Free-Running Counter  
(with Both Edges Specified)**



**Note** The carry flag is set to 1. Ignore this setting.

### (3) Pulse width measurement with free-running counter and two capture registers

When 16-bit timer counter 00 (TM00) is operated in free-running mode, it is possible to measure the pulse width of the signal input to the TI000 pin.

Specify both the rising and falling edges as the valid edges of the TI000 pin, by using bits 4 and 5 (ES000 and ES010) of PRM00.

When the rising or falling edge specified by bits 4 and 5 (ES000 and ES010) of prescaler mode register 00 (PRM00) is input to the TI000 pin, the value of TM00 is taken into 16-bit timer capture/compare register 010 (CR010) and an interrupt request signal (INTTM010) is set.

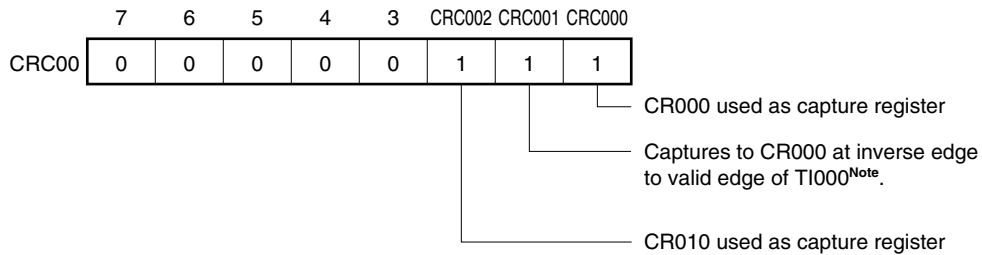
Also, when the inverse edge to that of the capture operation is input into CR010, the value of TM00 is taken into 16-bit timer capture/compare register 000 (CR000).

Sampling is performed using the count clock cycle selected by prescaler mode register 00 (PRM00), and a capture operation is only performed when a valid level of the TI000 pin is detected twice, thus eliminating noise with a short pulse width.

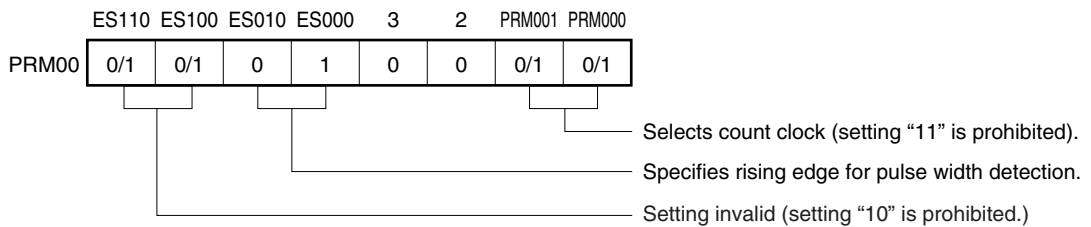
**Caution** The measurable pulse width in this operation example is up to 1 cycle of the timer counter.

**Figure 6-23. Control Register Settings for Pulse Width Measurement with Free-Running Counter and Two Capture Registers (with Rising Edge Specified)**

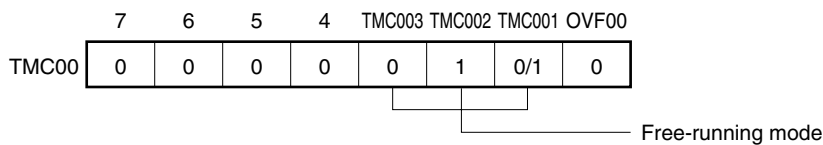
**(a) Capture/compare control register 00 (CRC00)**



**(b) Prescaler mode register 00 (PRM00)**



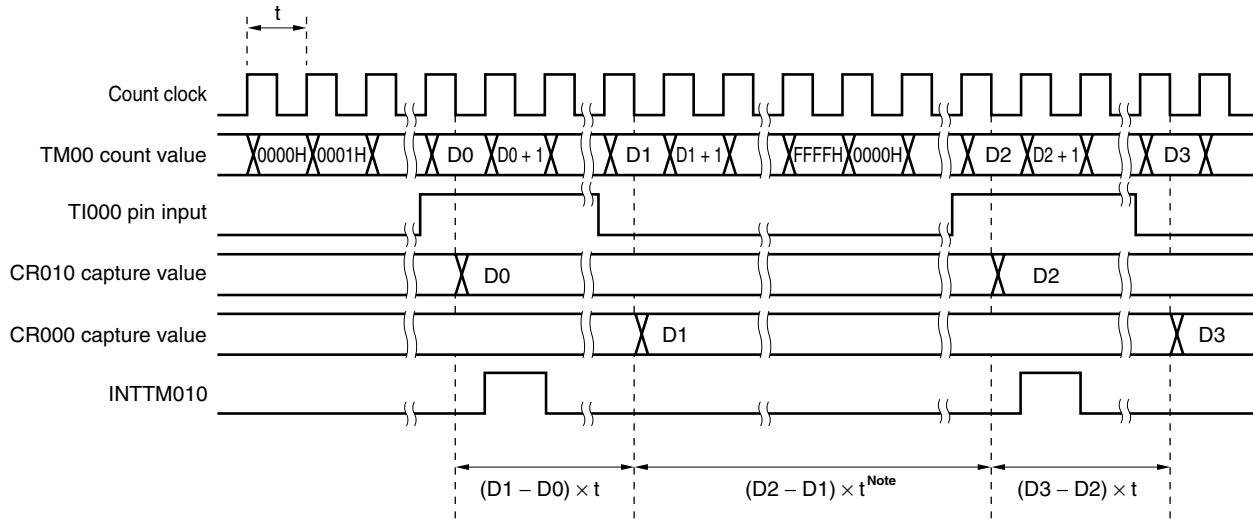
**(c) 16-bit timer mode control register 00 (TMC00)**



**Note** If the valid edge of TI000 is specified to be both the rising and falling edges, 16-bit timer capture/compare register 000 (CR000) cannot perform the capture operation. When the CRC001 bit value is 1, the TM00 count value is not captured in the CR000 register when a valid edge of the TI010 pin is detected, but the input from the TI010 pin can be used as an external interrupt source because INTTM000 is generated at that timing.

**Remark** 0/1: Setting 0 or 1 allows another function to be used simultaneously with pulse width measurement. See the description of the respective control registers for details.

**Figure 6-24. Timing of Pulse Width Measurement Operation by Free-Running Counter and Two Capture Registers (with Rising Edge Specified)**



**Note** The carry flag is set to 1. Ignore this setting.

**(4) Pulse width measurement by means of restart**

Specify both the rising and falling edges as the valid edges of the TI000 pin, by using bits 4 and 5 (ES000 and ES010) of PRM00.

When input of a valid edge to the TI000 pin is detected, the count value of 16-bit timer/counter 00 (TM00) is taken into 16-bit timer capture/compare register 010 (CR010), and then the pulse width of the signal input to the TI000 pin is measured by clearing TM00 and restarting the count.

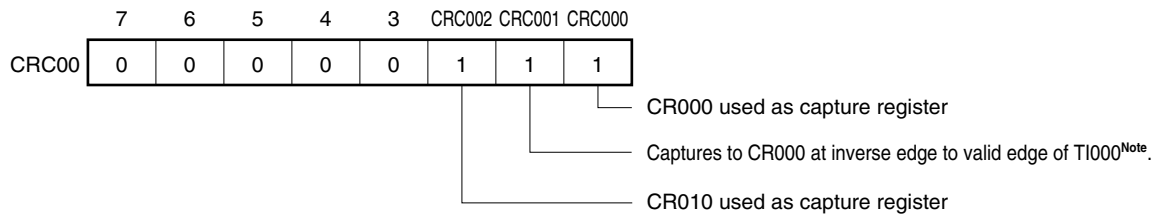
The edge specification can be selected from two types, rising or falling edges, by bits 4 and 5 (ES000 and ES010) of prescaler mode register 00 (PRM00)

Sampling is performed at the interval selected by prescaler mode register 00 (PRM00) and a capture operation is only performed when a valid level of the TI000 pin is detected twice, thus eliminating noise with a short pulse width.

**Caution** The measurable pulse width in this operation example is up to 1 cycle of the timer counter.

**Figure 6-25. Control Register Settings for Pulse Width Measurement by Means of Restart (with Rising Edge Specified) (1/2)**

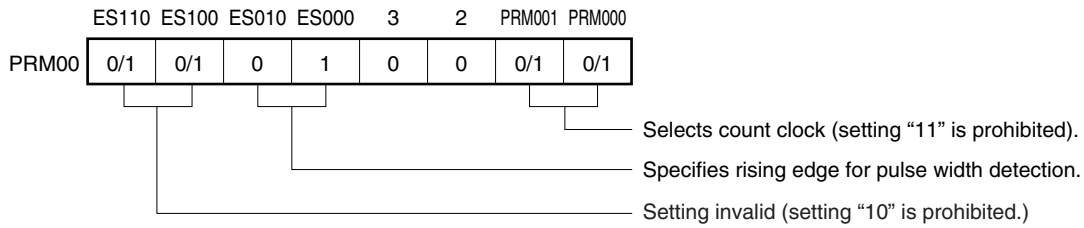
**(a) Capture/compare control register 00 (CRC00)**



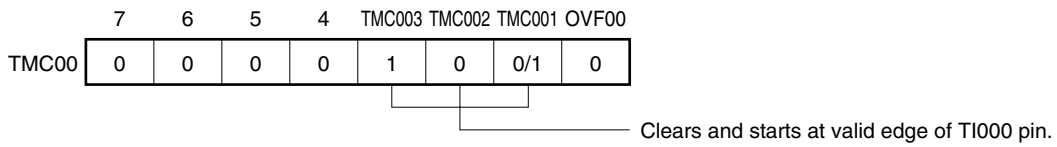


**Figure 6-25. Control Register Settings for Pulse Width Measurement by Means of Restart (with Rising Edge Specified) (2/2)**

**(b) Prescaler mode register 00 (PRM00)**

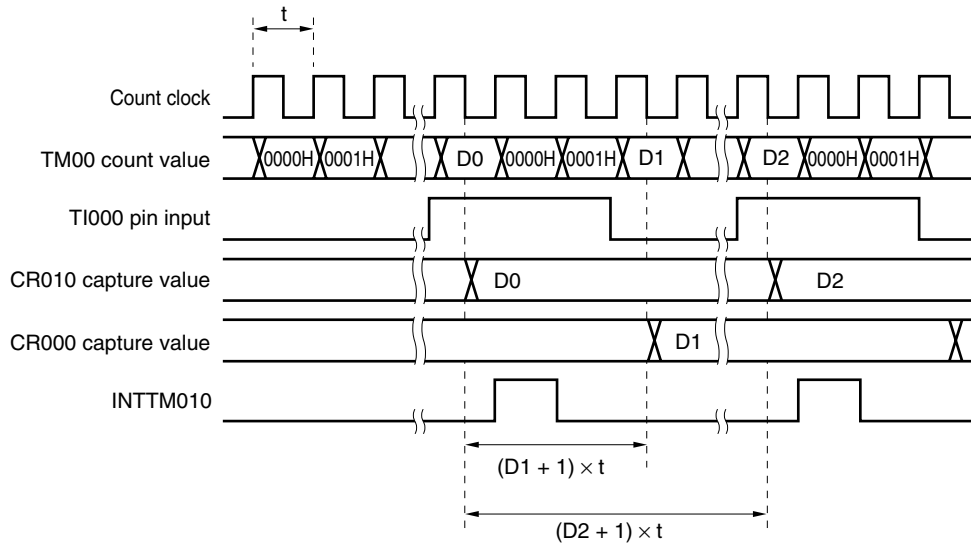


**(c) 16-bit timer mode control register 00 (TMC00)**



**Note** If the valid edge of TI000 is specified to be both the rising and falling edges, 16-bit timer capture/compare register 000 (CR000) cannot perform the capture operation.

**Figure 6-26. Timing of Pulse Width Measurement Operation by Means of Restart (with Rising Edge Specified)**



### 6.4.4 Square-wave output operation

#### Setting

The basic operation setting procedure is as follows.

- <1> Set the count clock by using the PRM00 register.
- <2> Set the CRC00 register (see **Figure 6-27** for the set value).
- <3> Set the TOC00 register (see **Figure 6-27** for the set value).
- <4> Set any value to the CR000 register (0000H cannot be set).
- <5> Set the TMC00 register to start the operation (see **Figure 6-27** for the set value).

**Caution** Changing the CR000 setting during TM00 operation may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-bit Timer/Event Counter 00 (17) Changing compare register during timer operation.

- Remarks 1.** For the setting of the TO00 pin, see 6.3 (5) Port mode register 2 (PM2).  
**2.** For how to enable the INTTM000 interrupt, see CHAPTER 9 INTERRUPT FUNCTIONS.

A square wave with any selected frequency can be output at intervals determined by the count value preset to 16-bit timer capture/compare register 000 (CR000).

The TO00 pin output status is reversed at intervals determined by the count value preset to CR000 + 1 by setting bit 0 (TOE00) and bit 1 (TOC001) of 16-bit timer output control register 00 (TOC00) to 1. This enables a square wave with any selected frequency to be output.

**Figure 6-27. Control Register Settings in Square-Wave Output Mode (1/2)**

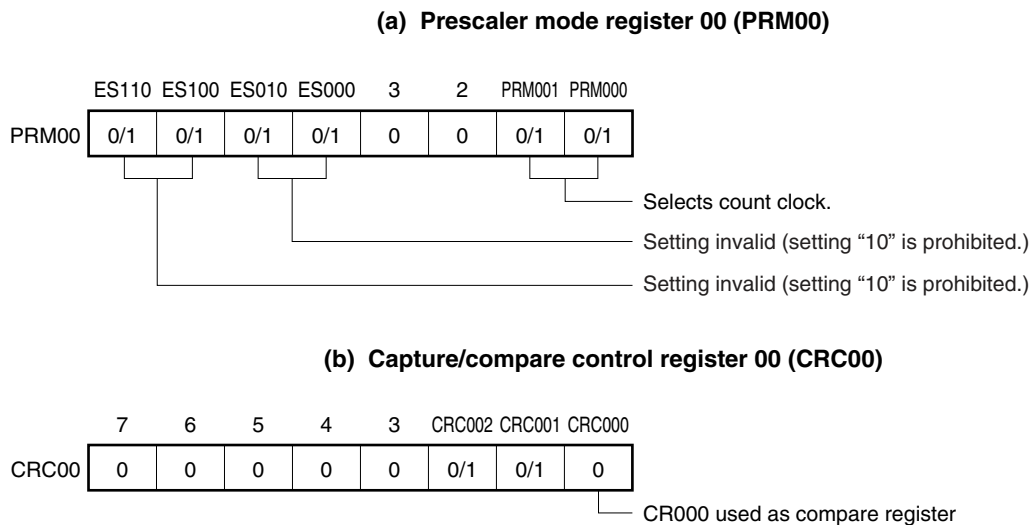
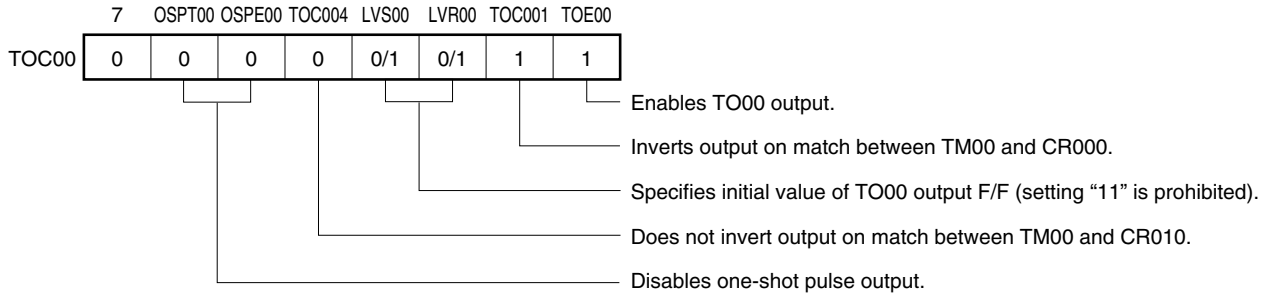
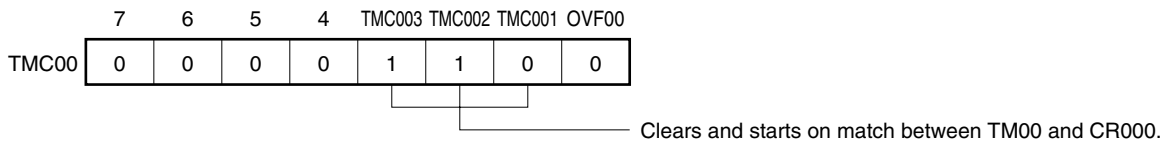


Figure 6-27. Control Register Settings in Square-Wave Output Mode (2/2)

(c) 16-bit timer output control register 00 (TOC00)

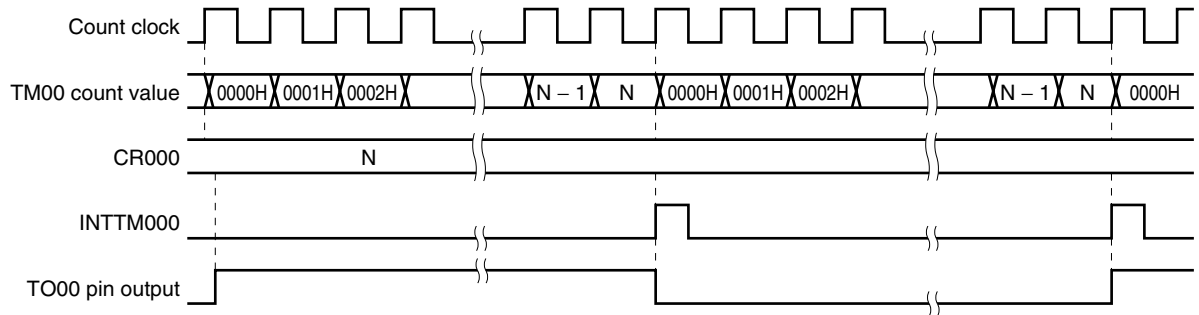


(d) 16-bit timer mode control register 00 (TMC00)



**Remark** 0/1: Setting 0 or 1 allows another function to be used simultaneously with square-wave output. See the description of the respective control registers for details.

Figure 6-28. Square-Wave Output Operation Timing



### 6.4.5 PPG output operations

Setting 16-bit timer mode control register 00 (TMC00) and capture/compare control register 00 (CRC00) as shown in Figure 6-30 allows operation as PPG (Programmable Pulse Generator) output.

#### Setting

The basic operation setting procedure is as follows.

- <1> Set the CRC00 register (see **Figure 6-29** for the set value).
- <2> Set any value to the CR000 register as the cycle.
- <3> Set any value to the CR010 register as the duty factor.
- <4> Set the TOC00 register (see **Figure 6-29** for the set value).
- <5> Set the count clock by using the PRM00 register.
- <6> Set the TMC00 register to start the operation (see **Figure 6-29** for the set value).

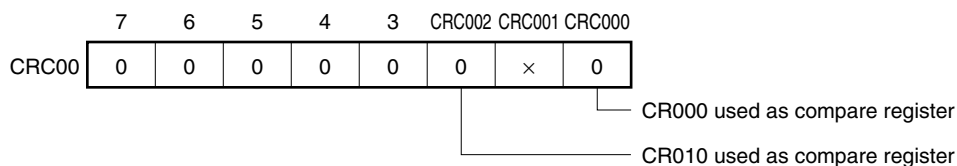
**Caution** Changing the CRC0n0 setting during TM00 operation may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-bit Timer/Event Counter 00 (17) Changing compare register during timer operation.

- Remarks**
1. For the setting of the TO00 pin, see 6.3 (5) Port mode register 2 (PM2).
  2. For how to enable the INTTM000 interrupt, see CHAPTER 9 INTERRUPT FUNCTIONS.
  3. n = 0 or 1

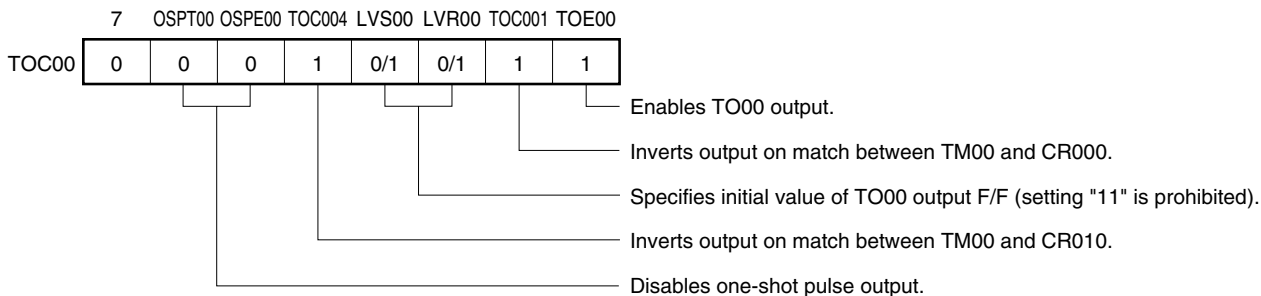
In the PPG output operation, rectangular waves are output from the TO00 pin with the pulse width and the cycle that correspond to the count values preset in 16-bit timer capture/compare register 010 (CR010) and in 16-bit timer capture/compare register 000 (CR000), respectively.

Figure 6-29. Control Register Settings for PPG Output Operation

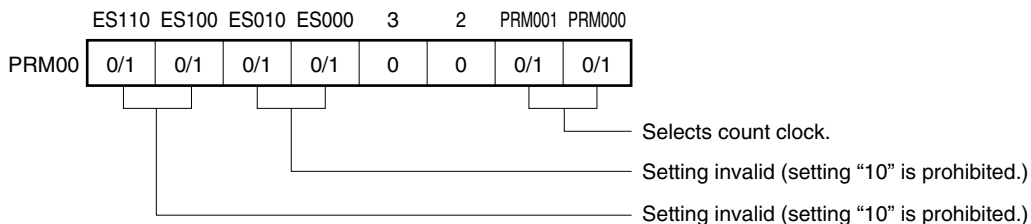
(a) Capture/compare control register 00 (CRC00)



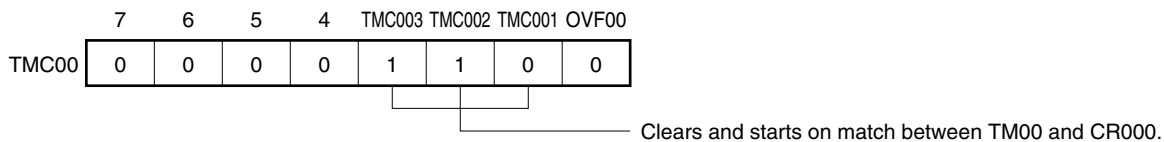
(b) 16-bit timer output control register 00 (TOC00)



(c) Prescaler mode register 00 (PRM00)



(d) 16-bit timer mode control register 00 (TMC00)



- Cautions**
1. Values in the following range should be set to CR000 and CR010:  
 $0000H < CR010 < CR000 \leq FFFFH$
  2. The cycle of the pulse generated through PPG output (CR000 setting value + 1) has a duty of (CR010 setting value + 1)/(CR000 setting value + 1).

**Remark** ×: Don't care

Figure 6-30. Configuration Diagram of PPG Output

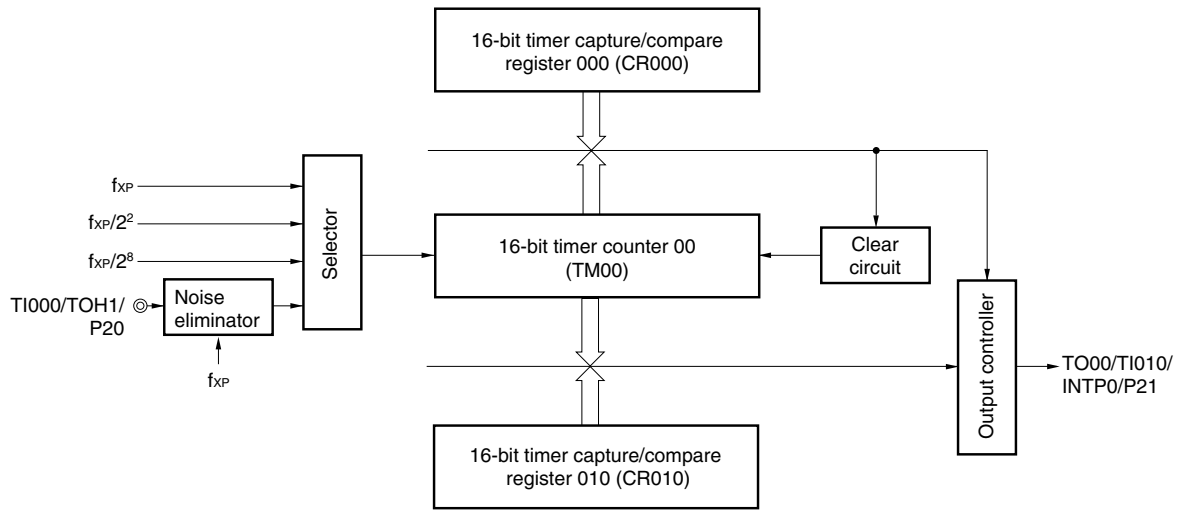
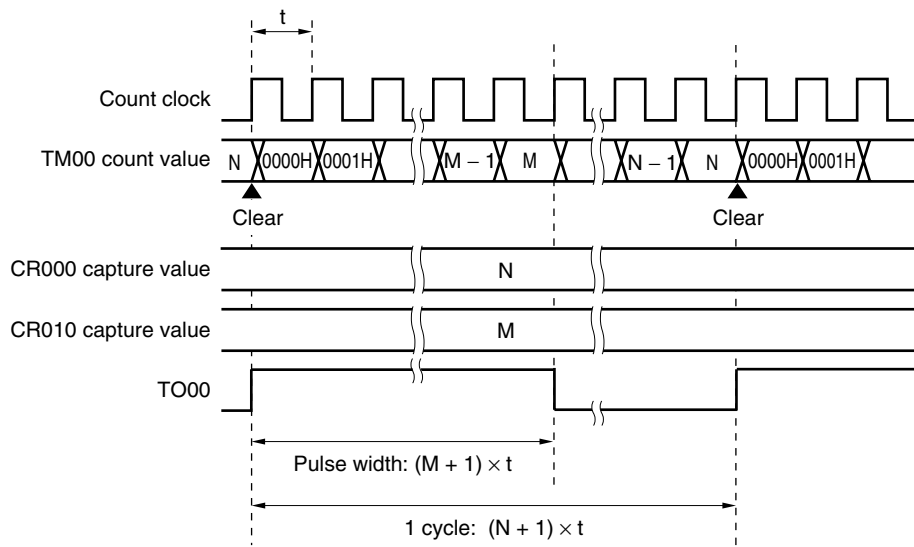


Figure 6-31. PPG Output Operation Timing



**Remark**  $0000H < M < N \leq FFFFH$

### 6.4.6 One-shot pulse output operation

16-bit timer/event counter 00 can output a one-shot pulse in synchronization with a software trigger or an external trigger (TI000 pin input).

#### Setting

The basic operation setting procedure is as follows.

- <1> Set the count clock by using the PRM00 register.
- <2> Set the CRC00 register (see **Figures 6-32** and **6-34** for the set value).
- <3> Set the TOC00 register (see **Figures 6-32** and **6-34** for the set value).
- <4> Set any value to the CR000 and CR010 registers (0000H cannot be set).
- <5> Set the TMC00 register to start the operation (see **Figures 6-32** and **6-34** for the set value).

- Remarks**
1. For the setting of the TO00 pin, see **6.3 (5) Port mode register 2 (PM2)**.
  2. For how to enable the INTTM000 (if necessary, INTTM010) interrupt, see **CHAPTER 9 INTERRUPT FUNCTIONS**.

#### (1) One-shot pulse output with software trigger

A one-shot pulse can be output from the TO00 pin by setting 16-bit timer mode control register 00 (TMC00), capture/compare control register 00 (CRC00), and 16-bit timer output control register 00 (TOC00) as shown in Figure 6-33, and by setting bit 6 (OSPT00) of the TOC00 register to 1 by software.

By setting the OSPT00 bit to 1, 16-bit timer/event counter 00 is cleared and started, and its output becomes active at the count value (N) set in advance to 16-bit timer capture/compare register 010 (CR010). After that, the output becomes inactive at the count value (M) set in advance to 16-bit timer capture/compare register 000 (CR000)<sup>Note</sup>.

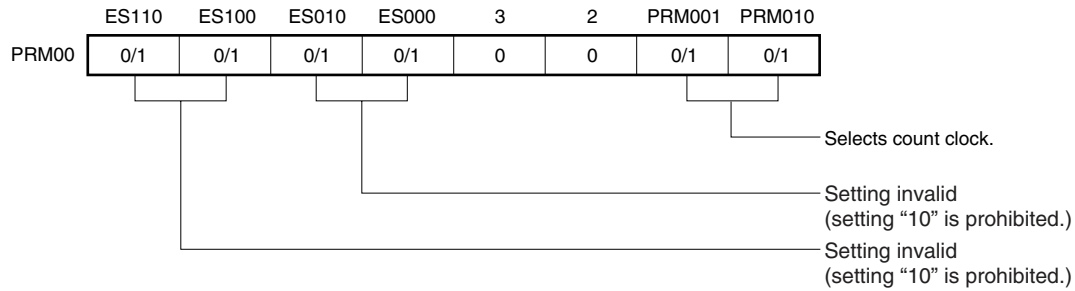
Even after the one-shot pulse has been output, the TM00 register continues its operation. To stop the TM00 register, the TMC003 and TMC002 bits of the TMC00 register must be cleared to 00.

**Note** The case where  $N < M$  is described here. When  $N > M$ , the output becomes active with the CR000 register and inactive with the CR010 register. Do not set  $N$  to  $M$ .

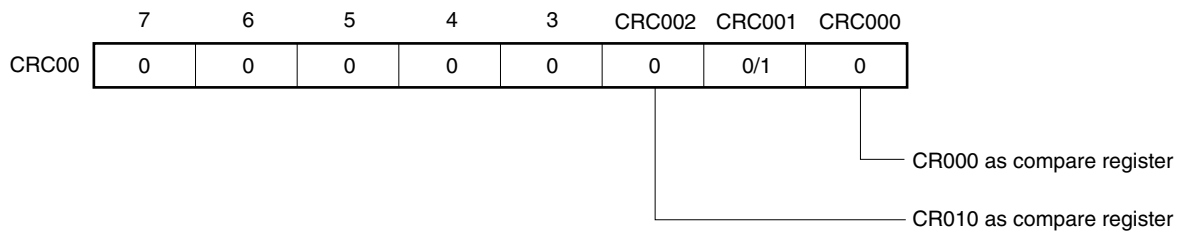
- Cautions**
1. **Do not set the OSPT00 bit to 1 again while the one-shot pulse is being output. To output the one-shot pulse again, wait until the current one-shot pulse output is completed.**
  2. **When using the one-shot pulse output of 16-bit timer/event counter 00 with a software trigger, do not change the level of the TI000 pin or its alternate-function port pin. Because the external trigger is valid even in this case, the timer is cleared and started even at the level of the TI000 pin or its alternate-function port pin, resulting in the output of a pulse at an undesired timing.**

Figure 6-32. Control Register Settings for One-Shot Pulse Output with Software Trigger

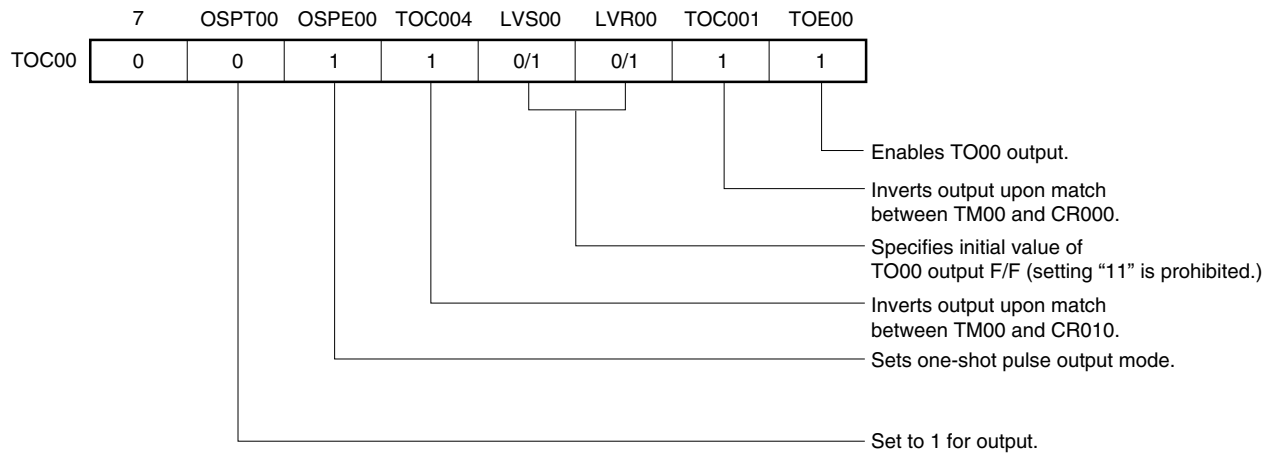
(a) Prescaler mode register 00 (PRM00)



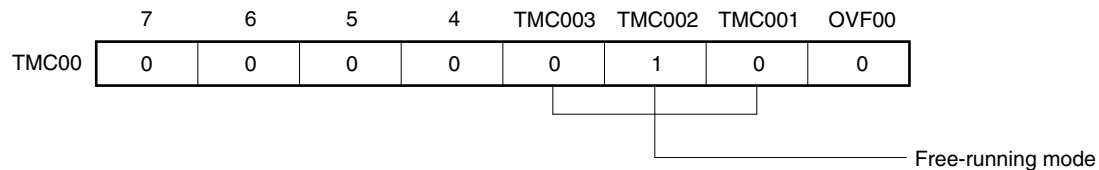
(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)



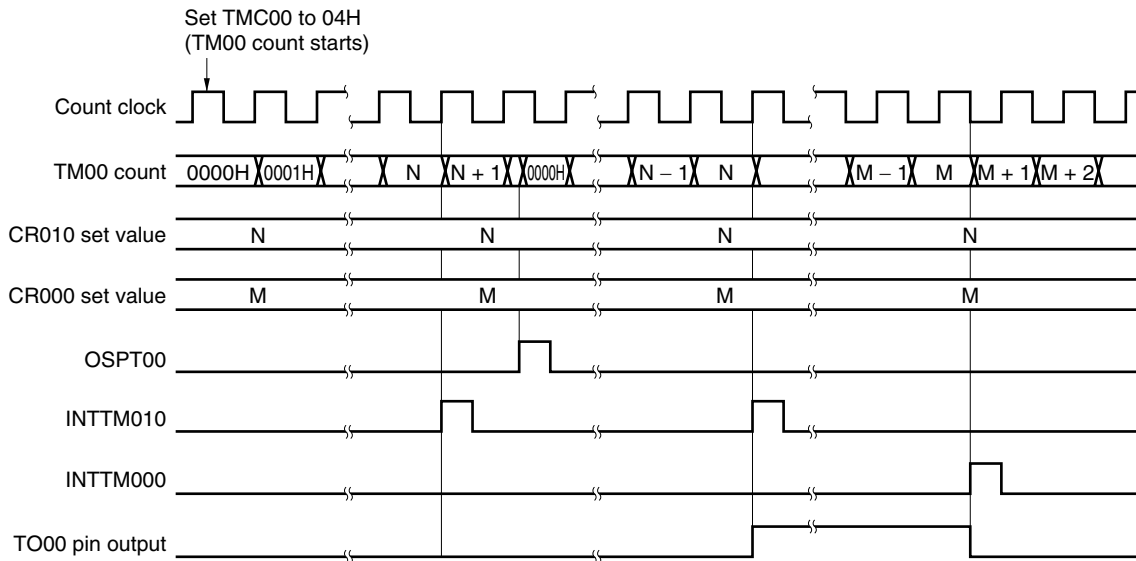
(d) 16-bit timer mode control register 00 (TMC00)



**Caution** Do not set 0000H to the CR000 and CR010 registers.



Figure 6-33. Timing of One-Shot Pulse Output Operation with Software Trigger



**Caution** 16-bit timer counter 00 starts operating as soon as a value other than 00 (operation stop mode) is set to the TMC003 and TMC002 bits.

**Remark**  $N < M$

## (2) One-shot pulse output with external trigger

A one-shot pulse can be output from the TO00 pin by setting 16-bit timer mode control register 00 (TMC00), capture/compare control register 00 (CRC00), and 16-bit timer output control register 00 (TOC00) as shown in Figure 6-35, and by using the valid edge of the TI000 pin as an external trigger.

The valid edge of the TI000 pin is specified by bits 4 and 5 (ES000, ES010) of prescaler mode register 00 (PRM00). The rising, falling, or both the rising and falling edges can be specified.

When the valid edge of the TI000 pin is detected, the 16-bit timer/event counter is cleared and started, and the output becomes active at the count value set in advance to 16-bit timer capture/compare register 010 (CR010). After that, the output becomes inactive at the count value set in advance to 16-bit timer capture/compare register 000 (CR000)<sup>Note</sup>.

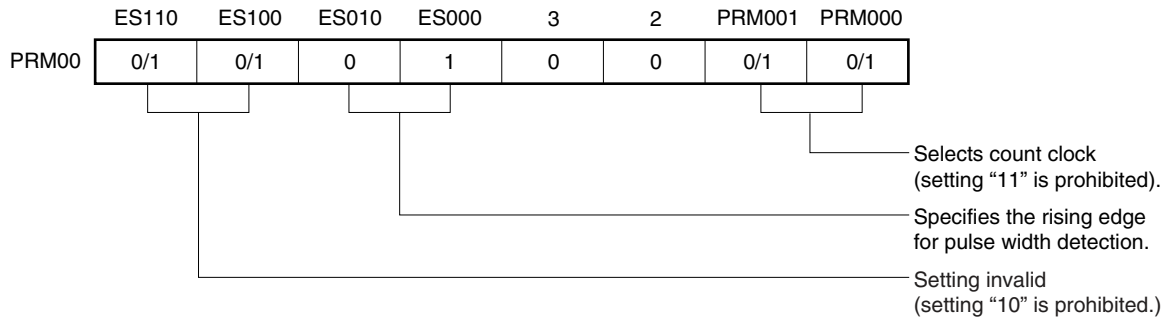
**Note** The case where  $N < M$  is described here. When  $N > M$ , the output becomes active with the CR000 register and inactive with the CR010 register. Do not set  $N$  to  $M$ .

**Caution** Do not input the external trigger again while the one-shot pulse is output.

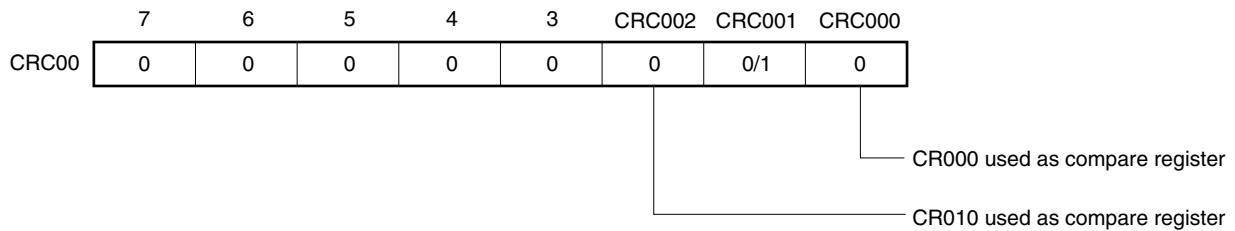
To output the one-shot pulse again, wait until the current one-shot pulse output is completed.

**Figure 6-34. Control Register Settings for One-Shot Pulse Output with External Trigger  
(with Rising Edge Specified)**

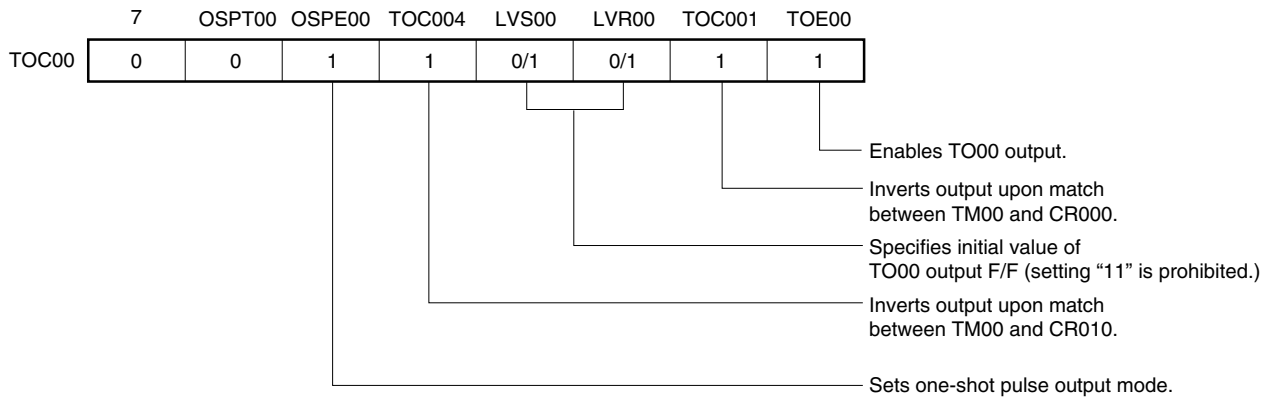
**(a) Prescaler mode register 00 (PRM00)**



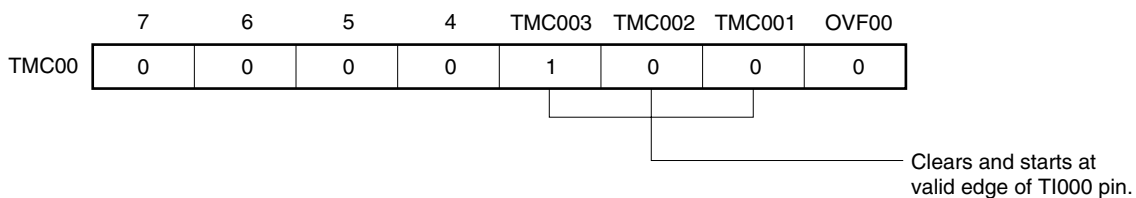
**(b) Capture/compare control register 00 (CRC00)**



**(c) 16-bit timer output control register 00 (TOC00)**

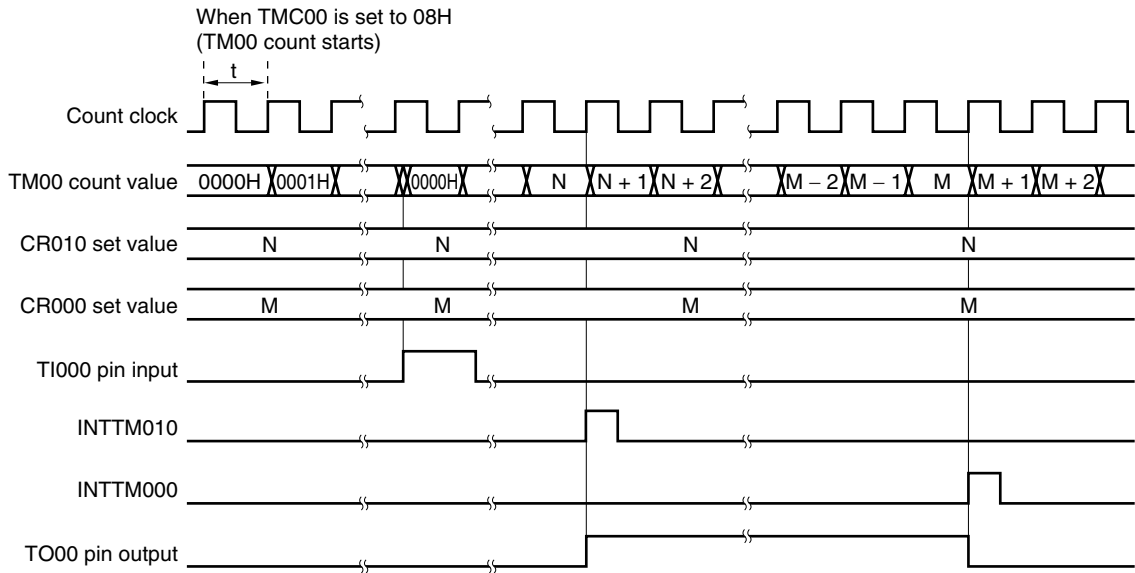


**(d) 16-bit timer mode control register 00 (TMC00)**



**Caution** Do not set 0000H to the CR000 and CR010 registers.

Figure 6-35. Timing of One-Shot Pulse Output Operation with External Trigger (with Rising Edge Specified)



**Caution** 16-bit timer counter 00 starts operating as soon as a value other than 00 (operation stop mode) is set to the TMC002 and TMC003 bits.

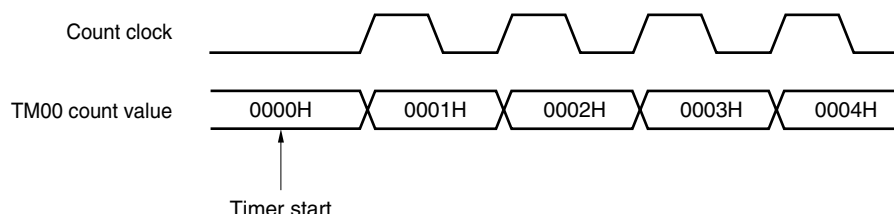
**Remark**  $N < M$

## 6.5 Cautions Related to 16-bit Timer/Event Counter 00

### (1) Timer start errors

An error of up to one clock may occur in the time required for a match signal to be generated after timer start. This is because 16-bit timer counter 00 (TM00) is started asynchronously to the count clock.

**Figure 6-36. Start Timing of 16-bit Timer Counter 00 (TM00)**



### (2) 16-bit timer counter 00 (TM00) operation

- <1> 16-bit timer counter 00 (TM00) starts operating as soon as values other than 0 and 0 (operation stop mode) are set to TMC002 and TMC003, respectively. Set TMC002 and TMC003 to 0 and 0 to stop operation.
- <2> Even if TM00 is read, the value is not captured by 16-bit timer capture/compare register 010 (CR010).
- <3> If TM00 is referred to during a timer count, a timer count will be stopped during reference processing, and a timer count is resumed after reference processing is finished. Therefore, if processing which refers to TM00 is performed, an error will arise at a timer count.
- <4> If the timer is stopped, timer counts and timer interrupts do not occur, even if a signal is input to the TI000/TI010 pins.

### (3) Setting of 16-bit timer capture/compare registers 000, 010 (CR000, CR010)

- <1> Set 16-bit timer capture/compare register 000 (CR000) to other than 0000H in the clear & start mode entered on match between TM00 and CR000. This means a 1-pulse count operation cannot be performed when this register is used as an external event counter.
- <2> When the clear & start mode entered on a match between TM00 and CR000 is selected, CR000 should not be specified as a capture register.
- <3> In the free-running mode and in the clear & start mode using the valid edge of the TI000 pin, if CR0n0 is set to 0000H, an interrupt request (INTTM0n0) is generated when CR0n0 changes from 0000H to 0001H after an overflow (FFFFH).
- <4> If the new value of CR0n0 is less than the value of TM00, TM00 continues counting, overflows, and then starts counting from 0 again. If the new value of CR0n0 is less than the old value, therefore, the timer must be reset to be restarted after the value of CR0n0 is changed.

**(4) Capture register data retention**

The values of 16-bit timer capture/compare registers 0n0 (CR0n0) after 16-bit timer/event counter 00 has stopped are not guaranteed.

**Remark** n = 0, 1

**(5) Setting of 16-bit timer mode control register 00 (TMC00)**

The timer operation must be stopped before writing to bits other than the OVF00 flag.

**(6) Setting of capture/compare control register 00 (CRC00)**

The timer operation must be stopped before setting CRC00.

**(7) Setting of 16-bit timer output control register 00 (TOC00)**

<1> Timer operation must be stopped before setting other than OSPT00.

<2> If LVS00 and LVR00 are read, 0 is read.

<3> OSPT00 is automatically cleared after data is set, so 0 is read.

<4> Do not set OSPT00 to 1 other than in one-shot pulse output mode.

<5> A write interval of two cycles or more of the count clock selected by prescaler mode register 00 (PRM00) is required, when OSPT00 is set to 1 successively.

**(8) Setting of prescaler mode register 00 (PRM00)**

Always set data to PRM00 after stopping the timer operation.

**(9) Valid edge setting**

Set the valid edge of the TI000 pin with bits 4 and 5 (ES000 and ES010) of prescaler mode register 00 (PRM00) after stopping the timer operation.

**(10) One-shot pulse output**

One-shot pulse output normally operates only in the free-running mode or in the clear & start mode at the valid edge of the TI000 pin. Because an overflow does not occur in the clear & start mode on a match between TM00 and CR000, one-shot pulse output is not possible.

**(11) One-shot pulse output by software**

<1> Do not set the OSPT00 bit to 1 again while the one-shot pulse is being output. To output the one-shot pulse again, wait until the current one-shot pulse output is completed.

<2> When using the one-shot pulse output of 16-bit timer/event counter 00 with a software trigger, do not change the level of the TI000 pin or its alternate function port pin.

Because the external trigger is valid even in this case, the timer is cleared and started even at the level of the TI000 pin or its alternate function port pin, resulting in the output of a pulse at an undesired timing.

<3> Do not set the 16-bit timer capture/compare registers 000 and 010 (CR000 and CR010) to 0000H.

**(12) One-shot pulse output with external trigger**

<1> Do not input the external trigger again while the one-shot pulse is output.  
To output the one-shot pulse again, wait until the current one-shot pulse output is completed.

<2> Do not set the 16-bit timer capture/compare registers 000 and 010 (CR000 and CR010) to 0000H.

**(13) Operation of OVF00 flag**

<1> The OVF00 flag is also set to 1 in the following case.  
Either of the clear & start mode entered on a match between TM00 and CR000, clear & start at the valid edge of the TI000 pin, or free-running mode is selected.

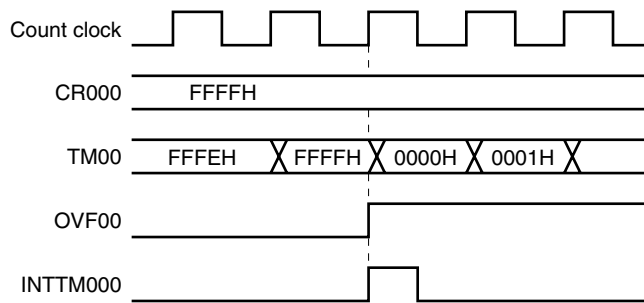
↓

CR000 is set to FFFFH.

↓

When TM00 is counted up from FFFFH to 0000H.

**Figure 6-37. Operation Timing of OVF00 Flag**

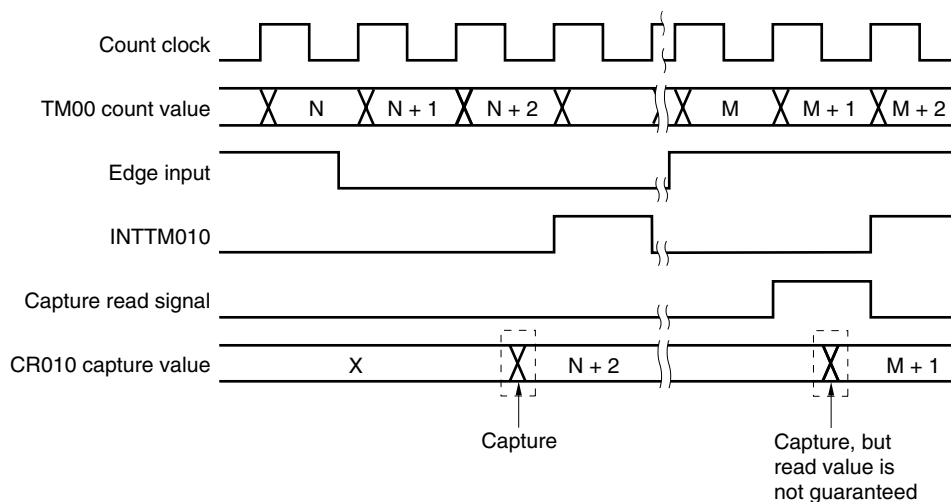


<2> Even if the OVF00 flag is cleared before the next count clock is counted (before TM00 becomes 0001H) after the occurrence of a TM00 overflow, the OVF00 flag is re-set and clearance becomes invalid.

**(14) Conflicting operations**

If the register read period and the input of the capture trigger conflict when CR000/CR010 is used as a capture register, the capture trigger input takes precedence and the read data is undefined. Also, if the count stop of the timer and the input of the capture trigger conflict, the captured data is undefined.

Figure 6-38. Capture Register Data Retention Timing

**(15) Capture operation**

- <1> If the valid edge of the TI000 pin is to be set as the count clock, do not set the clear/start mode and the capture trigger at the valid edge of the TI000 pin.
- <2> When the CRC001 bit value is 1, capture is not performed in the CR000 register if both the rising and falling edges have been selected as the valid edges of the TI000 pin.
- <3> When the CRC001 bit value is 1, the TM00 count value is not captured in the CR000 register when a valid edge of the TI010 pin is detected, but the input from the TI010 pin can be used as an external interrupt source because INTTM000 is generated at that timing.
- <4> To ensure the reliability of the capture operation, the capture trigger requires a pulse longer than two cycles of the count clock selected by prescaler mode register 00 (PRM00).
- <5> The capture operation is performed at the fall of the count clock. An interrupt request input (INTTM0n0), however, occurs at the rise of the next count clock.
- <6> To use two capture registers, set the TI000 and TI010 pins.

**Remark** n = 0, 1

**(16) Compare operation**

The capture operation may not be performed for CR0n0 set in compare mode even if a capture trigger is input.

**Remark** n = 0, 1

**(17) Changing compare register during timer operation**

<1> With the 16-bit timer capture/compare register 0n0 (CR0n0) used as a compare register, when changing CR0n0 around the timing of a match between 16-bit timer counter 00 (TM00) and 16-bit timer capture/compare register 0n0 (CR0n0) during timer counting, the change timing may conflict with the timing of the match, so the operation is not guaranteed in such cases. To change CR0n0 during timer counting, INTTM000 interrupt servicing performs the following operation.

<Changing cycle (CR000)>

1. Disable the timer output inversion operation at the match between TM00 and CR000 (TOC001 = 0).
2. Disable the INTTM000 interrupt (TMMK000 = 1).
3. Rewrite CR000.
4. Wait for 1 cycle of the TM00 count clock.
5. Enable the timer output inversion operation at the match between TM00 and CR000 (TOC001 = 1).
6. Clear the interrupt request flag of INTTM000 (TMIF000 = 0).
7. Enable the INTTM000 interrupt (TMMK000 = 0).

<Changing duty (CR010)>

1. Disable the timer output inversion operation at the match between TM00 and CR010 (TOC004 = 0).
2. Disable the INTTM000 interrupt (TMMK000 = 1).
3. Rewrite CR010.
4. Wait for 1 cycle of the TM00 count clock.
5. Enable the timer output inversion operation at the match between TM00 and CR010 (TOC004 = 1).
6. Clear the interrupt request flag of INTTM000 (TMIF000 = 0).
7. Enable the INTTM000 interrupt (TMMK000 = 0).

While interrupts and timer output inversion are disabled (1 to 4 above), timer counting is continued. If the value to be set in CR0n0 is small, the value of TM00 may exceed CR0n0. Therefore, set the value, considering the time lapse of the timer clock and CPU after an INTTM000 interrupt has been generated.

**Remark** n = 0 or 1

<2> If CR010 is changed during timer counting without performing processing <1> above, the value in CR010 may be rewritten twice or more, causing an inversion of the output level of the TO00 pin at each rewrite.



**(18) Edge detection**

- <1> In the following cases, note with caution that the valid edge of the TI0n0 pin is detected.
- (a) Immediately after a system reset, if a high level is input to the TI0n0 pin, the operation of 16-bit timer counter 00 (TM00) is enabled
    - If the rising edge or both rising and falling edges are specified as the valid edge of the TI0n0 pin, a rising edge is detected immediately after the TM00 operation is enabled.
  - (b) If the TM00 operation is stopped while the TI0n0 pin is at high level, TM00 operation is then enabled after a low level is input to the TI0n0 pin
    - If the falling edge or both rising and falling edges are specified as the valid edge of the TI0n0 pin, a falling edge is detected immediately after the TM00 operation is enabled.
  - (c) When the TM00 operation is stopped while the TI0n0 pin is at low level, TM00 operation is then enabled after a high level is input to the TI0n0 pin
    - If the rising edge or both rising and falling edges are specified as the valid edge, of the TI0n0 pin, a rising edge is detected immediately after the TM00 operation is enabled.

**Remark** n = 0, 1

- <2> The sampling clock used to remove noise differs when the valid edge of TI000 is used as the count clock and when it is used as a capture trigger. In the former case, the count clock is  $f_{XP}$ , and in the latter case the count clock is selected by prescaler mode register 00 (PRM00). The capture operation is not performed until the valid edge is sampled and the valid level is detected twice, thus eliminating noise with a short pulse width.

**(19) External event counter**

- <1> The timing of the count start is after two valid edge detections.
- <2> When reading the external event counter count value, TM00 should be read.

**(20) PPG output**

- <1> Values in the following range should be set to CR000 and CR010:  
 $0000H < CR010 < CR000 \leq FFFFH$
- <2> The cycle of the pulse generated through PPG output (CR000 setting value + 1) has a duty of (CR010 setting value + 1)/(CR000 setting value + 1).

**(21) STOP mode or system clock stop mode setting**

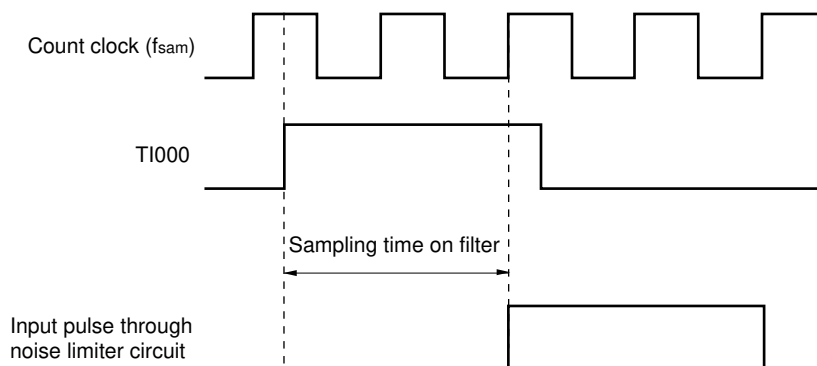
Except when the valid edge of the TI000 pin is selected as the count clock, stop the timer operation before setting STOP mode or system clock stop mode; otherwise the timer may malfunction when the system clock starts.

**(22) P21/TI010/TO00 pin**

When using P21 as the input pin (TI010) of the valid edge, it cannot be used as a timer output pin (TO00).  
 When using P21 as the timer output pin (TO00), it cannot be used as the input pin (TI010) of the valid edge.

**(23) External clock limitation**

- <1> When using an input pulse of the TI000 pin as a count clock (external trigger), be sure to input the pulse width which satisfies the AC characteristics. For the AC characteristics, refer to **CHAPTER 17 ELECTRICAL SPECIFICATIONS (TARGET)**.
- <2> When an external waveform is input to 16-bit timer/event counter 00, it is sampled by the noise limiter circuit and thus an error occurs on the timing to become valid inside the device.



**Remark** The count clock ( $f_{sam}$ ) can be selected using bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00).

## CHAPTER 7 8-BIT TIMER H1

### 7.1 Functions of 8-bit Timer H1

8-bit timer H1 has the following functions.

- Interval timer
- PWM output mode
- Square-wave output

### 7.2 Configuration of 8-bit Timer H1

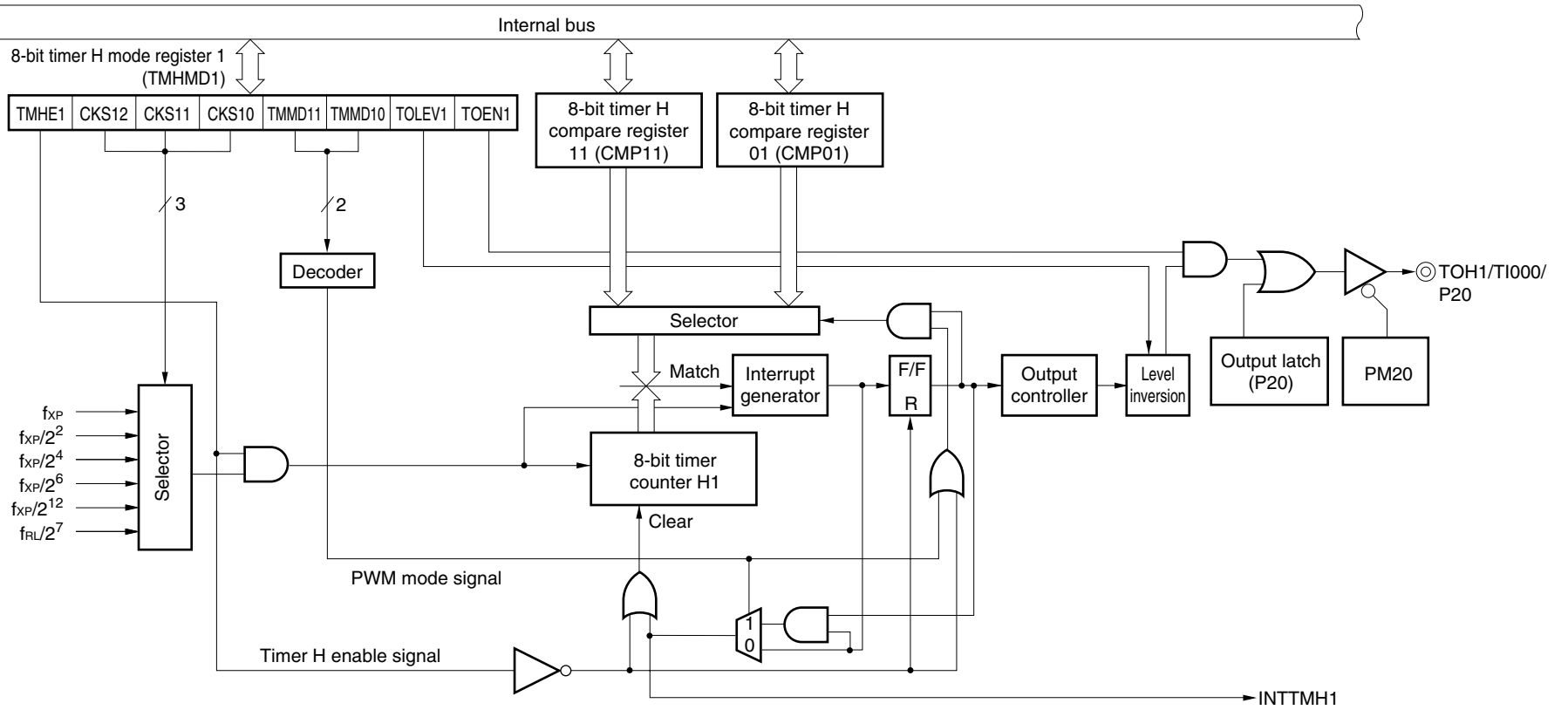
8-bit timer H1 consists of the following hardware.

**Table 7-1. Configuration of 8-bit Timer H1**

Item	Configuration
Timer register	8-bit timer counter H1
Registers	8-bit timer H compare register 01 (CMP01) 8-bit timer H compare register 11 (CMP11)
Timer output	TOH1
Control registers	8-bit timer H mode register 1 (TMHMD1) Port mode register 2 (PM2) Port register 2 (P2)

Figure 7-1 shows a block diagram.

Figure 7-1. Block Diagram of 8-bit Timer H1

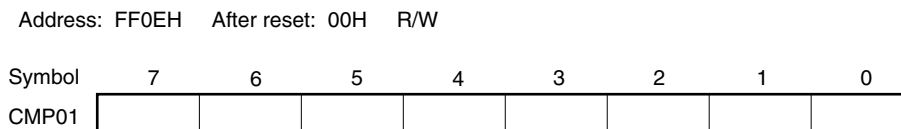


**(1) 8-bit timer H compare register 01 (CMP01)**

This register can be read or written by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 7-2. Format of 8-bit Timer H Compare Register 01 (CMP01)**



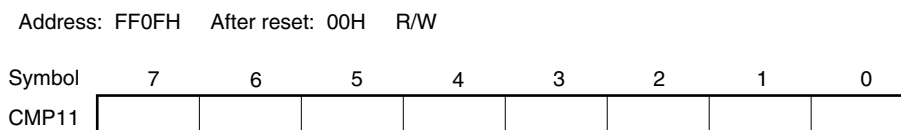
**Caution** CMP01 cannot be rewritten during timer count operation.

**(2) 8-bit timer H compare register 11 (CMP11)**

This register can be read or written by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 7-3. Format of 8-bit Timer H Compare Register 11 (CMP11)**



CMP11 can be rewritten during timer count operation.

If the CMP11 value is rewritten during timer operation, the compare value after the rewrite takes effect at the timing at which the count value and the compare value before the rewrite match. If the timing at which the count value and compare value match conflicts with the timing of the writing from the CPU to CMP11, the compare value after the rewrite takes effect at the timing at which the next count value and the compare value before the rewrite match.

**Caution** In the PWM output mode, be sure to set CMP11 when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to CMP11).

### 7.3 Registers Controlling 8-bit Timer H1

The following four registers are used to control 8-bit timer H1.

- 8-bit timer H mode register 1 (TMHMD1)
- Port mode register 2 (PM2)
- Port register 2 (P2)

#### (1) 8-bit timer H mode register 1 (TMHMD1)

This register controls the mode of timer H.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-4. Format of 8-bit Timer H Mode Register 1 (TMHMD1)

Address: FF70H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	<1>	<0>
TMHMD1	TMHE1	CKS12	CKS11	CKS10	TMMD11	TMMD10	TOLEV1	TOEN1

TMHE1	Timer operation enable
0	Stop timer count operation (counter is cleared to 0)
1	Enable timer count operation (count operation started by inputting clock)

CKS12	CKS11	CKS10	Count clock ( $f_{CNT}$ ) selection
0	0	0	$f_{XP}$ (10 MHz)
0	0	1	$f_{XP}/2^2$ (2.5 MHz)
0	1	0	$f_{XP}/2^4$ (625 kHz)
0	1	1	$f_{XP}/2^6$ (156.25 kHz)
1	0	0	$f_{XP}/2^{12}$ (2.44 kHz)
1	0	1	$f_{RL}/2^7$ (1.88 kHz (TYP.))
Other than above			Setting prohibited

TMMD11	TMMD10	Timer operation mode
0	0	Interval timer mode
1	0	PWM output mode
Other than above		Setting prohibited

TOLEV1	Timer output level control (in default mode)
0	Low level
1	High level

TOEN1	Timer output control
0	Disable output
1	Enable output

- Cautions**
1. When **TMHE1 = 1**, setting the other bits of the **TMHMD1** register is prohibited.
  2. In the **PWM output mode**, be sure to set **8-bit timer H compare register 11 (CMP11)** when starting the timer count operation (**TMHE1 = 1**) after the timer count operation was stopped (**TMHE1 = 0**) (be sure to set again even if setting the same value to the **CMP11** register).

- Remarks**
1.  $f_{XP}$ : Oscillation frequency of clock to peripheral hardware
  2.  $f_{RL}$ : Low-speed internal oscillation clock oscillation frequency
  3. Figures in parentheses apply to operation at  $f_{XP} = 10$  MHz,  $f_{RL} = 240$  kHz (TYP.).

## 7.4 Operation of 8-bit Timer H1

### 7.4.1 Operation as interval timer/square-wave output

When 8-bit timer counter H1 and compare register 01 (CMP01) match, an interrupt request signal (INTTMH1) is generated and 8-bit timer counter H1 is cleared to 00H.

Compare register 11 (CMP11) is not used in interval timer mode. Since a match of 8-bit timer counter H1 and the CMP11 register is not detected even if the CMP11 register is set, timer output is not affected.

By setting bit 0 (TOEN1) of timer H mode register 1 (TMHMD1) to 1, a square wave of any frequency (duty = 50%) is output from TOH1.

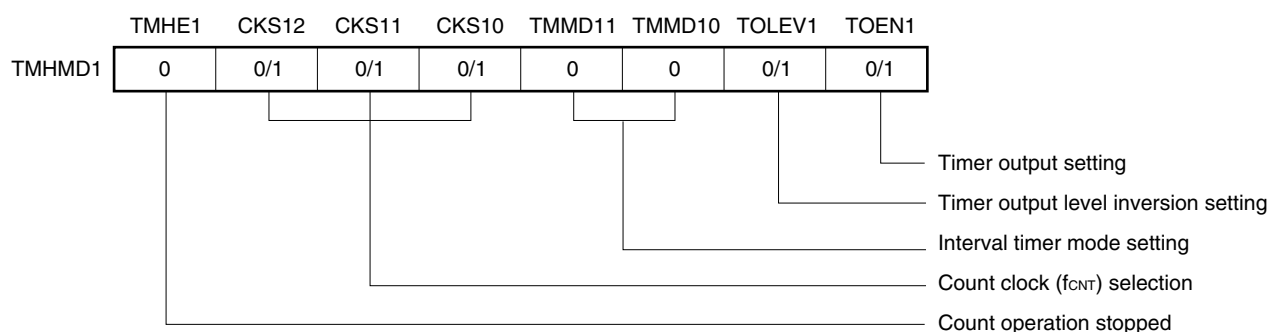
#### (1) Usage

Generates the INTTMH1 signal repeatedly at the same interval.

<1> Set each register.

Figure 7-5. Register Setting During Interval Timer/Square-Wave Output Operation

#### (i) Setting timer H mode register 1 (TMHMD1)



#### (ii) CMP01 register setting

- Compare value (N)

<2> Count operation starts when TMHE1 = 1.

<3> When the values of 8-bit timer counter H1 and the CMP01 register match, the INTTMH1 signal is generated and 8-bit timer counter H1 is cleared to 00H.

$\text{Interval time} = (N + 1)/f_{\text{CNT}}$
---

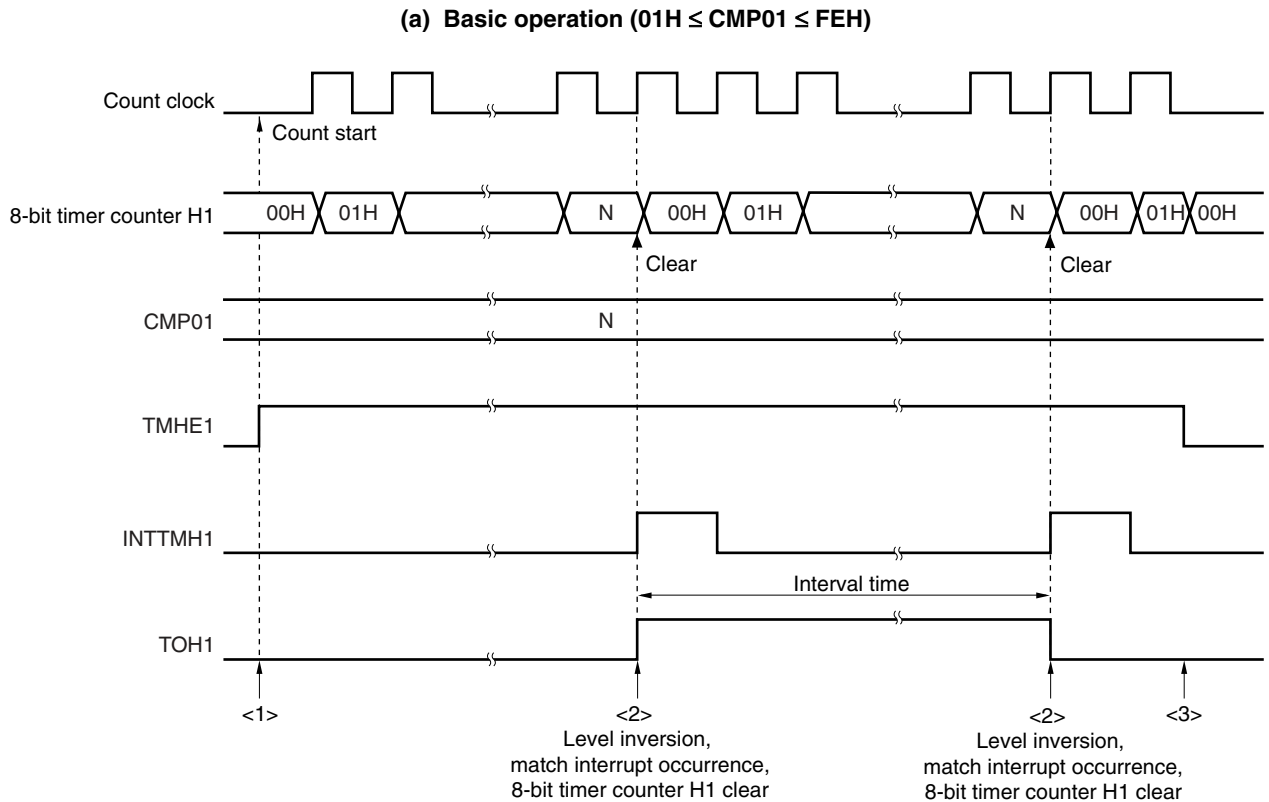
<4> Subsequently, the INTTMH1 signal is generated at the same interval. To stop the count operation, clear TMHE1 to 0.



## (2) Timing chart

The timing of the interval timer/square-wave output operation is shown below.

Figure 7-6. Timing of Interval Timer/Square-Wave Output Operation (1/2)

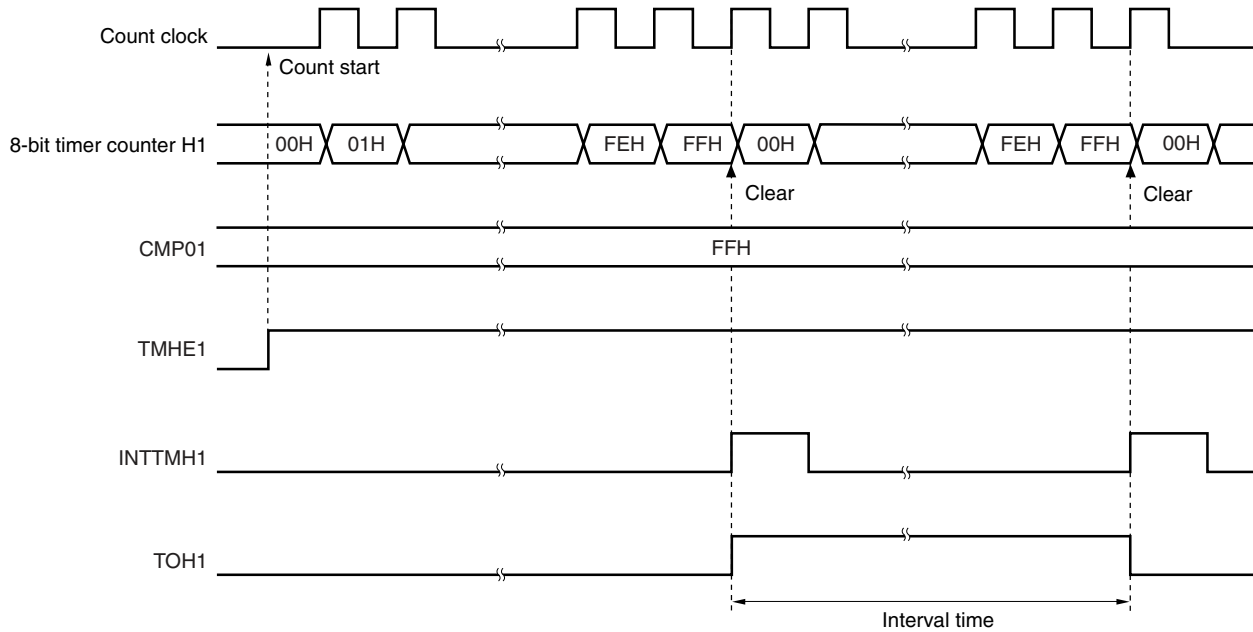


- <1> The count operation is enabled by setting the TMHE1 bit to 1. The count clock starts counting no more than 1 clock after the operation is enabled.
- <2> When the values of 8-bit timer counter H1 and the CMP01 register match, the value of 8-bit timer counter H1 is cleared, the TOH1 output level is inverted, and the INTTMH1 signal is output.
- <3> The INTTMH1 signal and TOH1 output become inactive by clearing the TMHE1 bit to 0 during timer H1 operation. If these are inactive from the first, the level is retained.

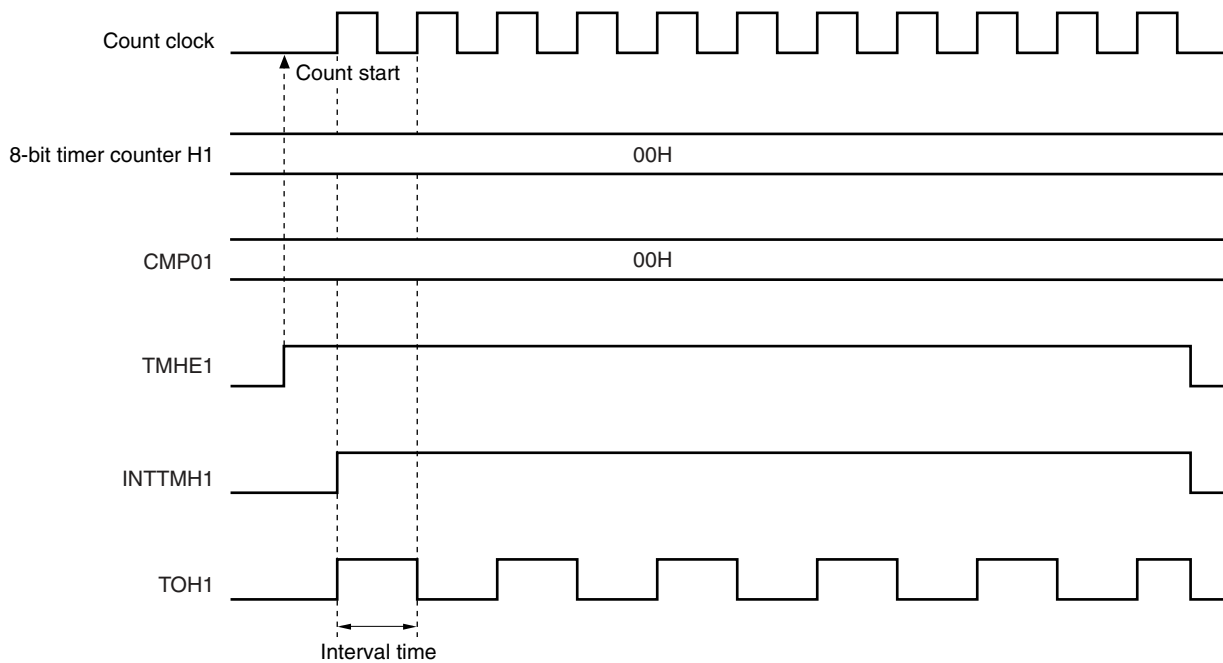
**Remark**  $01H \leq N \leq FEH$

Figure 7-6. Timing of Interval Timer/Square-Wave Output Operation (2/2)

(b) Operation when CMP01 = FFH



(c) Operation when CMP01 = 00H



### 7.4.2 Operation as PWM output mode

In PWM output mode, a pulse with an arbitrary duty and arbitrary cycle can be output.

8-bit timer compare register 01 (CMP01) controls the cycle of timer output (TOH1). Rewriting the CMP01 register during timer operation is prohibited.

8-bit timer compare register 11 (CMP11) controls the duty of timer output (TOH1). Rewriting the CMP11 register during timer operation is possible.

The operation in PWM output mode is as follows.

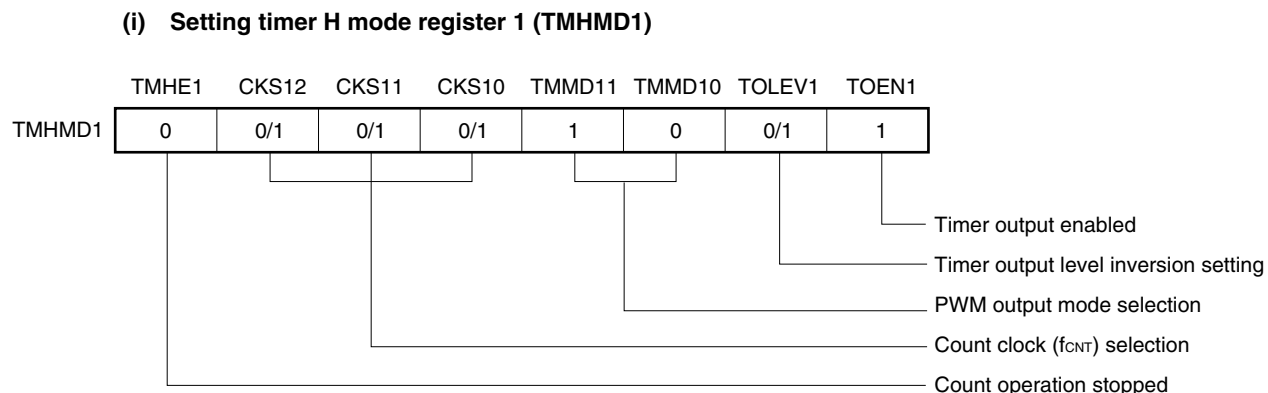
TOH1 output becomes active and 8-bit timer counter H1 is cleared to 0 when 8-bit timer counter H1 and the CMP01 register match after the timer count is started. TOH1 output becomes inactive when 8-bit timer counter H1 and the CMP11 register match.

#### (1) Usage

In PWM output mode, a pulse for which an arbitrary duty and arbitrary cycle can be set is output.

<1> Set each register.

Figure 7-7. Register Setting in PWM Output Mode



#### (ii) Setting CMP01 register

- Compare value (N): Cycle setting

#### (iii) Setting CMP11 register

- Compare value (M): Duty setting

**Remark**  $00H \leq \text{CMP11 (M)} < \text{CMP01 (N)} \leq \text{FFH}$

<2> The count operation starts when  $\text{TMHE1} = 1$ .

<3> The CMP01 register is the compare register that is to be compared first after count operation is enabled. When the values of 8-bit timer counter H1 and the CMP01 register match, 8-bit timer counter H1 is cleared, an interrupt request signal (INTTMH1) is generated, and TOH1 output becomes active. At the same time, the compare register to be compared with 8-bit timer counter H1 is changed from the CMP01 register to the CMP11 register.

- <4> When 8-bit timer counter H1 and the CMP11 register match, TOH1 output becomes inactive and the compare register to be compared with 8-bit timer counter H1 is changed from the CMP11 register to the CMP01 register. At this time, 8-bit timer counter H1 is not cleared and the INTTMH1 signal is not generated.
- <5> By performing procedures <3> and <4> repeatedly, a pulse with an arbitrary duty can be obtained.
- <6> To stop the count operation, set TMHE1 = 0.

If the setting value of the CMP01 register is N, the setting value of the CMP11 register is M, and the count clock frequency is  $f_{CNT}$ , the PWM pulse output cycle and duty are as follows.

$\text{PWM pulse output cycle} = (N+1)/f_{CNT}$ $\text{Duty} = \text{Active width} : \text{Total width of PWM} = (M + 1) : (N + 1)$
---

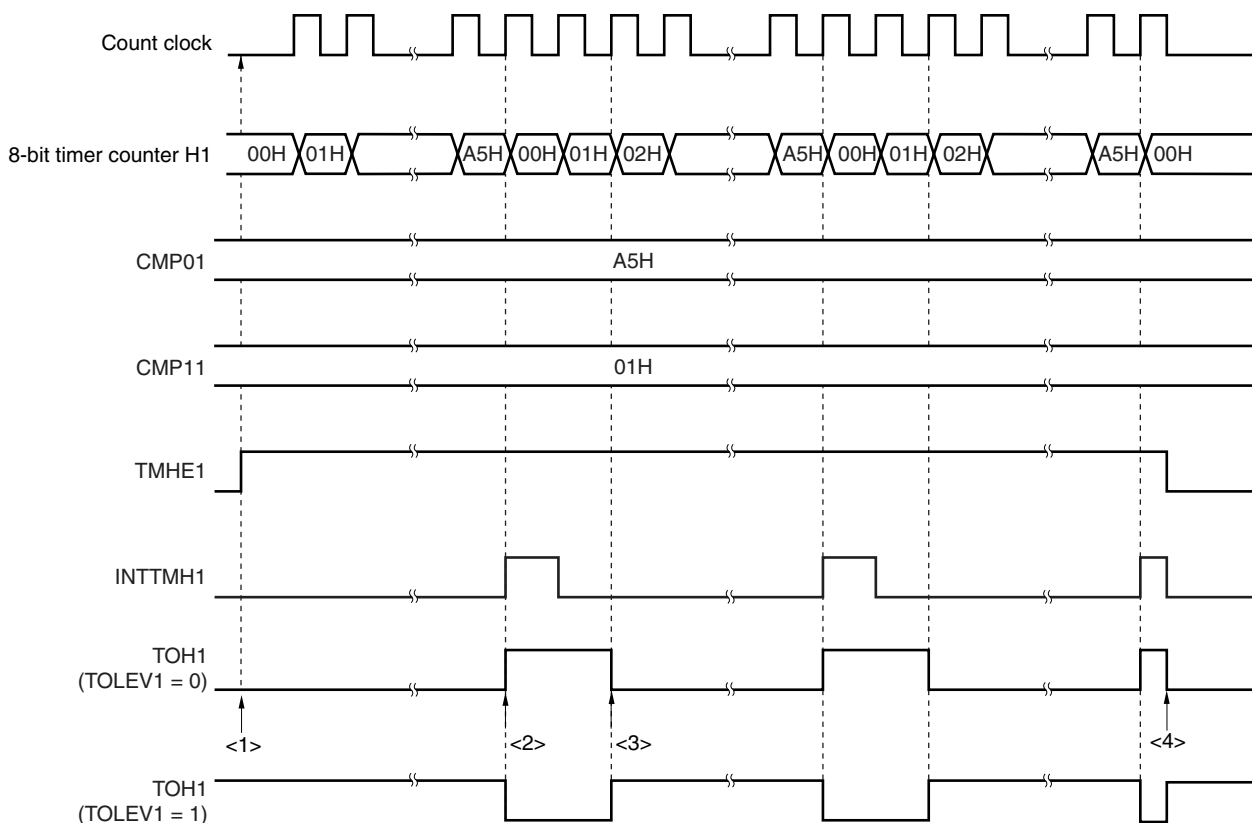
- Cautions**
1. In PWM output mode, the setting value for the CMP11 register can be changed during timer count operation. However, three operation clocks (signal selected using the CKS12 to CKS10 bits of the TMHMD1 register) or more are required to transfer the register value after rewriting the CMP11 register value.
  2. Be sure to set the CMP11 register when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to the CMP11 register).

## (2) Timing chart

The operation timing in PWM output mode is shown below.

- Caution** Make sure that the CMP11 register setting value (M) and CMP01 register setting value (N) are within the following range.
- $$00H \leq \text{CMP11 (M)} < \text{CMP01 (N)} \leq \text{FFH}$$

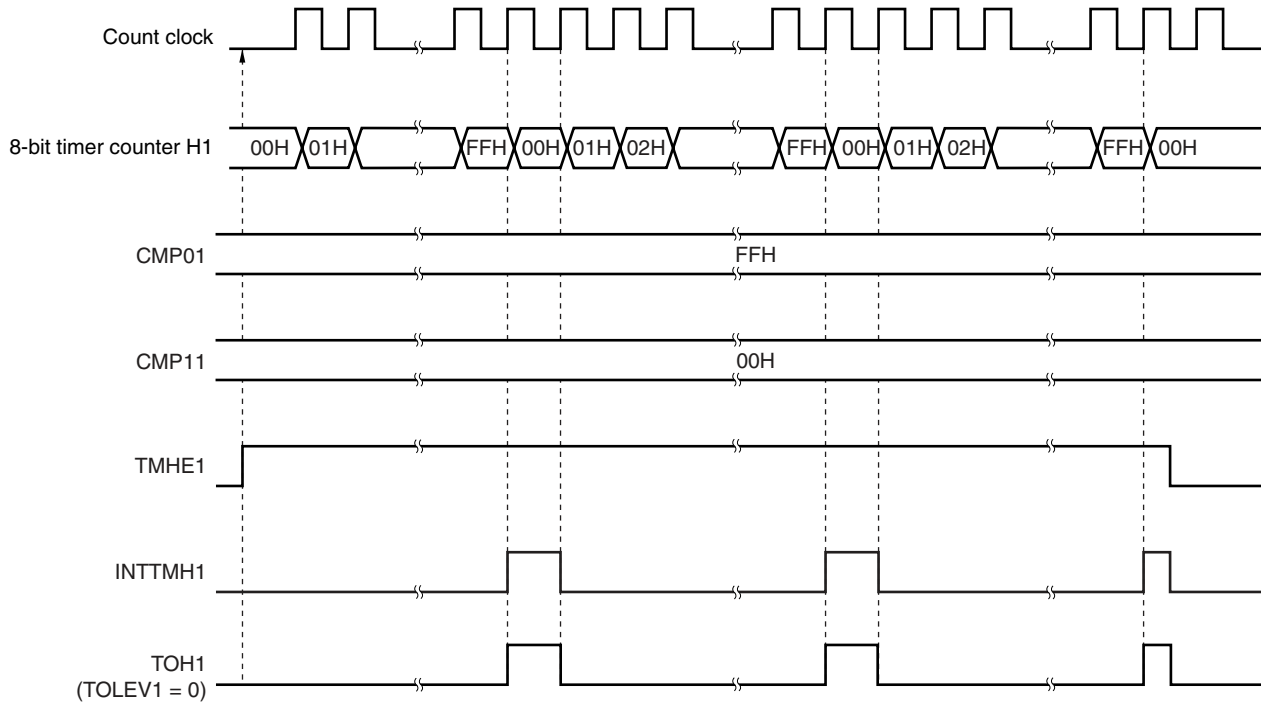
Figure 7-8. Operation Timing in PWM Output Mode (1/4)

(a) Basic operation ( $00H < CMP11 < CMP01 < FFH$ )

- <1> The count operation is enabled by setting the TMHE1 bit to 1. Start 8-bit timer counter H1 by masking one count clock to count up. At this time, TOH1 output remains inactive (when TOLEV1 = 0).
- <2> When the values of 8-bit timer counter H1 and the CMP01 register match, the TOH1 output level is inverted, the value of 8-bit timer counter H1 is cleared, and the INTTMH1 signal is output.
- <3> When the values of 8-bit timer counter H1 and the CMP11 register match, the level of the TOH1 output is returned. At this time, the 8-bit timer counter value is not cleared and the INTTMH1 signal is not output.
- <4> Clearing the TMHE1 bit to 0 during timer H1 operation makes the INTTMH1 signal and TOH1 output inactive.

Figure 7-8. Operation Timing in PWM Output Mode (2/4)

(b) Operation when CMP01 = FFH, CMP11 = 00H



(c) Operation when CMP01 = FFH, CMP11 = FEH

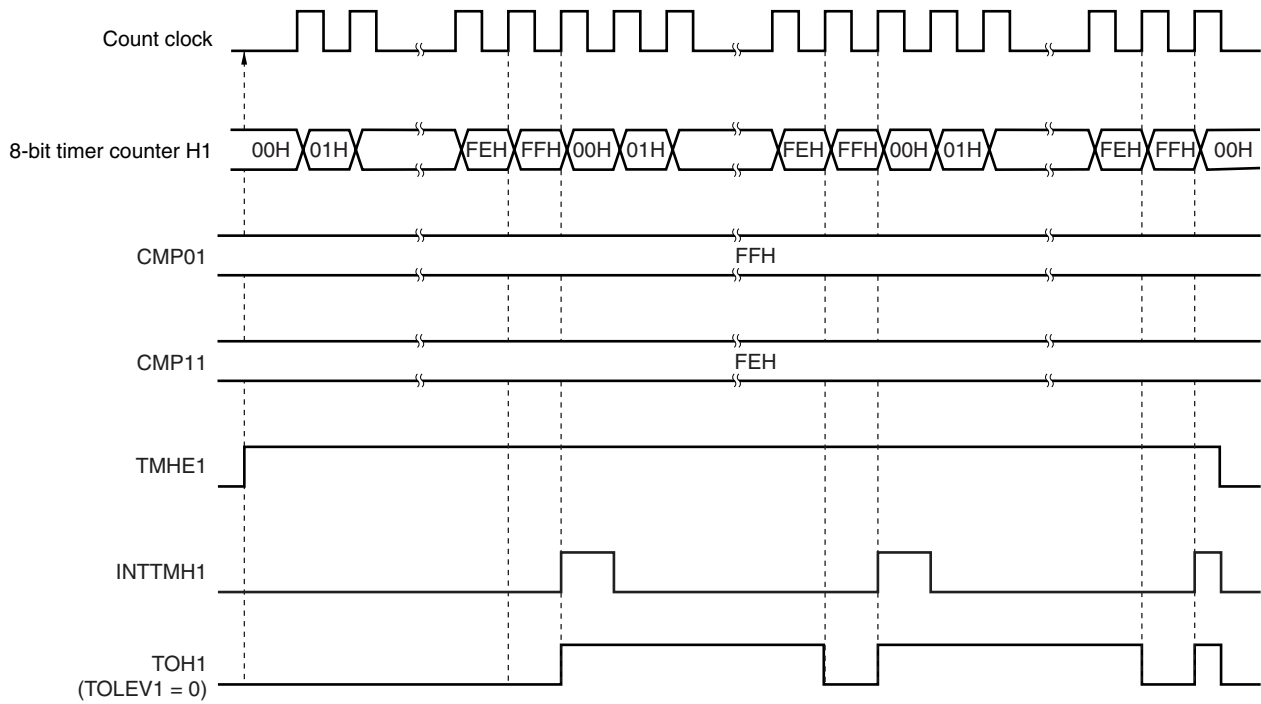


Figure 7-8. Operation Timing in PWM Output Mode (3/4)

(d) Operation when CMP01 = 01H, CMP11 = 00H

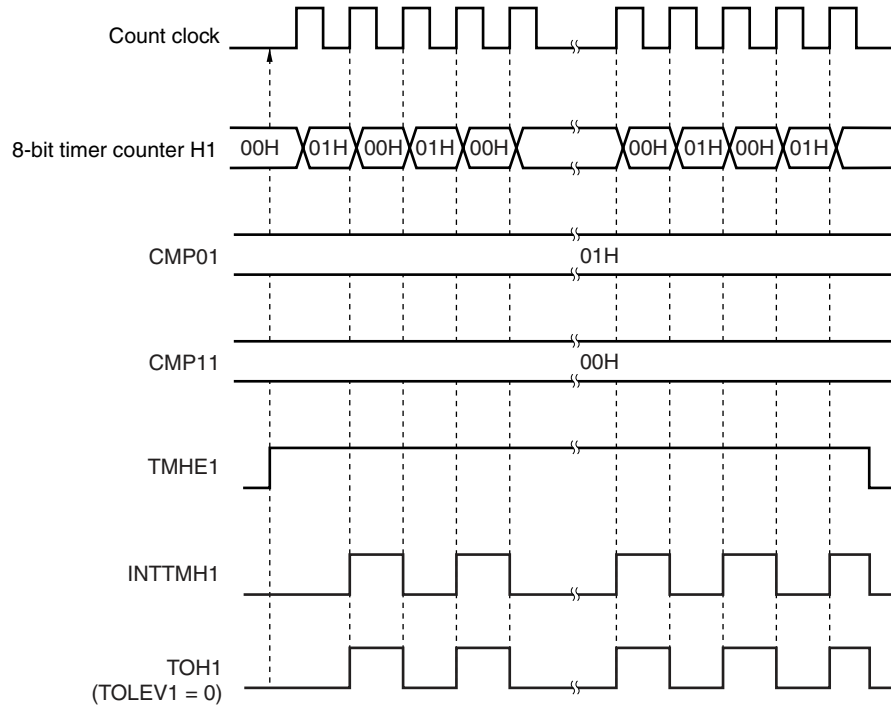
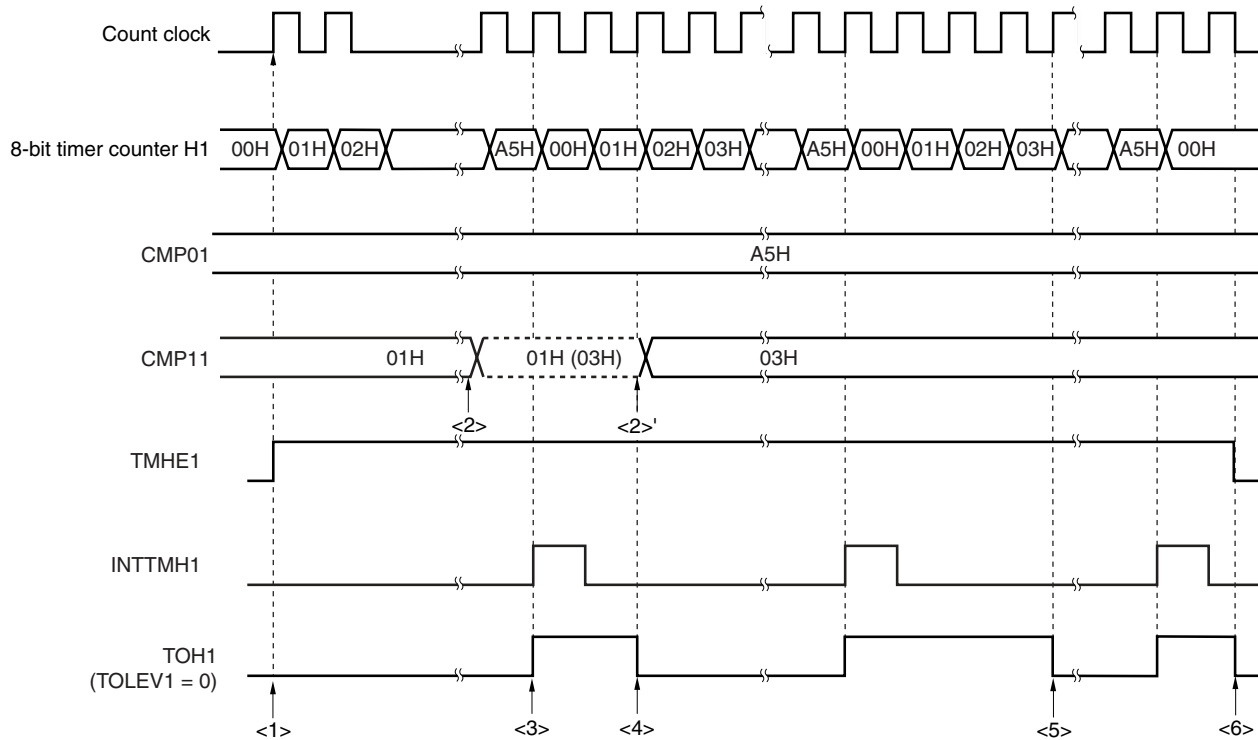


Figure 7-8. Operation Timing in PWM Output Mode (4/4)

## (e) Operation by changing CMP11 (CMP11 = 02H → 03H, CMP01 = A5H)



- <1> The count operation is enabled by setting TMHE1 = 1. Start 8-bit timer counter H1 by masking one count clock to count up. At this time, the TOH1 output remains inactive (when TOLEV1 = 0).
- <2> The CMP11 register value can be changed during timer counter operation. This operation is asynchronous to the count clock.
- <3> When the values of 8-bit timer counter H1 and the CMP01 register match, the value of 8-bit timer counter H1 is cleared, the TOH1 output becomes active, and the INTTMH1 signal is output.
- <4> If the CMP11 register value is changed, the value is latched and not transferred to the register. When the values of 8-bit timer counter H1 and the CMP11 register before the change match, the value is transferred to the CMP11 register and the CMP11 register value is changed (<2>').  
However, three count clocks or more are required from when the CMP11 register value is changed to when the value is transferred to the register. If a match signal is generated within three count clocks, the changed value cannot be transferred to the register.
- <5> When the values of 8-bit timer counter H1 and the CMP11 register after the change match, the TOH1 output becomes inactive. 8-bit timer counter H1 is not cleared and the INTTMH1 signal is not generated.
- <6> Clearing the TMHE1 bit to 0 during timer H1 operation makes the INTTMH1 signal and TOH1 output inactive.



## CHAPTER 8 WATCHDOG TIMER

### 8.1 Functions of Watchdog Timer

The watchdog timer is used to detect an inadvertent program loop. If a program loop is detected, an internal reset signal is generated.

When a reset occurs due to the watchdog timer, bit 4 (WDTRF) of the reset control flag register (RESF) is set to 1. For details of RESF, see **CHAPTER 11 RESET FUNCTION**.

**Table 8-1. Loop Detection Time of Watchdog Timer**

Loop Detection Time	
During Low-Speed Internal oscillation Clock Operation	During System Clock Operation
$2^{11}/f_{RL}$ (4.27 ms)	$2^{13}/f_x$ (819.2 $\mu$ s)
$2^{12}/f_{RL}$ (8.53 ms)	$2^{14}/f_x$ (1.64 ms)
$2^{13}/f_{RL}$ (17.07 ms)	$2^{15}/f_x$ (3.28 ms)
$2^{14}/f_{RL}$ (34.13 ms)	$2^{16}/f_x$ (6.55 ms)
$2^{15}/f_{RL}$ (68.27 ms)	$2^{17}/f_x$ (13.11 ms)
$2^{16}/f_{RL}$ (136.53 ms)	$2^{18}/f_x$ (26.21 ms)
$2^{17}/f_{RL}$ (273.07 ms)	$2^{19}/f_x$ (52.43 ms)
$2^{18}/f_{RL}$ (546.13 ms)	$2^{20}/f_x$ (104.86 ms)

- Remarks**
1.  $f_{RL}$ : Low-speed internal oscillation clock oscillation frequency
  2.  $f_x$ : System clock oscillation frequency
  3. Figures in parentheses apply to operation at  $f_{RL} = 480$  kHz (MAX.),  $f_x = 10$  MHz.

The operation mode of the watchdog timer (WDT) is switched according to the option byte setting of the on-chip low-speed internal oscillator as shown in Table 8-2.

Table 8-2. Option Byte Setting and Watchdog Timer Operation Mode

	Option Byte Setting	
	Low-Speed Internal Oscillator Cannot Be Stopped	Low-Speed Internal Oscillator Can Be Stopped by Software
Watchdog timer clock source	Fixed to $f_{RL}$ <sup>Note 1</sup> .	<ul style="list-style-type: none"> <li>• Selectable by software (<math>f_x</math>, <math>f_{RL}</math> or stopped)</li> <li>• When reset is released: <math>f_{RL}</math></li> </ul>
Operation after reset	Operation starts with the maximum interval ( $2^{16}/f_{RL}$ ).	Operation starts with the maximum interval ( $2^{16}/f_{RL}$ ).
Operation mode selection	The interval can be changed only once.	The clock selection/interval can be changed only once.
Features	The watchdog timer cannot be stopped.	The watchdog timer can be stopped <sup>Note 2</sup> .

**Notes** 1. As long as power is being supplied, low-speed internal oscillator cannot be stopped (except in the reset period).

2. The conditions under which clock supply to the watchdog timer is stopped differ depending on the clock source of the watchdog timer.

<1> If the clock source is  $f_x$ , clock supply to the watchdog timer is stopped under the following conditions.

- When  $f_x$  is stopped
- In HALT/STOP mode
- During oscillation stabilization time

<2> If the clock source is  $f_{RL}$ , clock supply to the watchdog timer is stopped under the following conditions.

- If the CPU clock is  $f_x$  and if  $f_{RL}$  is stopped by software before execution of the STOP instruction
- In HALT/STOP mode

**Remarks** 1.  $f_{RL}$ : Low-speed internal oscillation clock oscillation frequency

2.  $f_x$ : System clock oscillation frequency

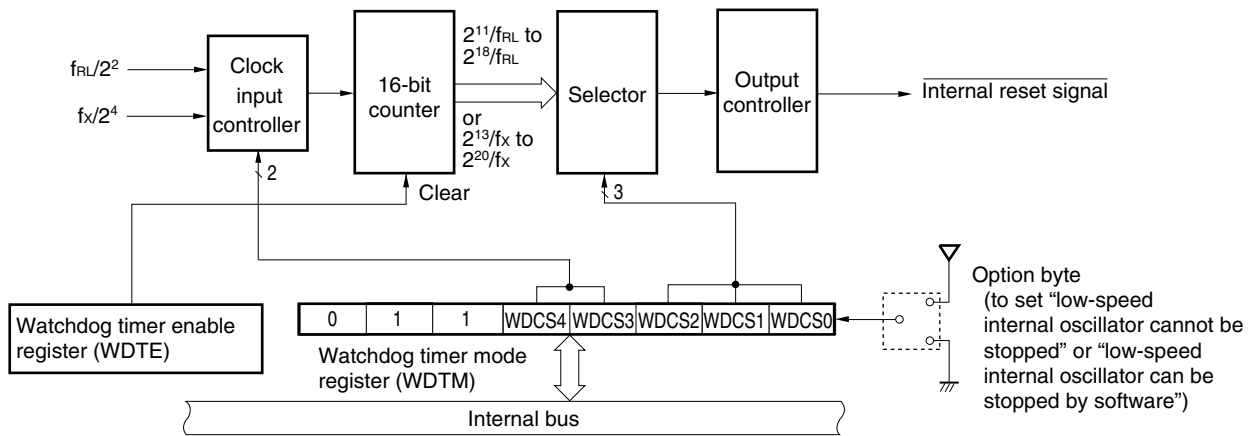
## 8.2 Configuration of Watchdog Timer

The watchdog timer consists of the following hardware.

**Table 8-3. Configuration of Watchdog Timer**

Item	Configuration
Control registers	Watchdog timer mode register (WDTM) Watchdog timer enable register (WDTE)

**Figure 8-1. Block Diagram of Watchdog Timer**



- Remarks**
1.  $f_{RL}$ : Low-speed internal oscillation clock oscillation frequency
  2.  $f_x$ : System clock oscillation frequency

### 8.3 Registers Controlling Watchdog Timer

The watchdog timer is controlled by the following two registers.

- Watchdog timer mode register (WDTM)
- Watchdog timer enable register (WDTE)

#### (1) Watchdog timer mode register (WDTM)

This register sets the overflow time and operation clock of the watchdog timer.

This register can be set by an 8-bit memory manipulation instruction and can be read many times, but can be written only once after reset is released.

Reset signal generation sets this register to 67H.

**Figure 8-2. Format of Watchdog Timer Mode Register (WDTM)**

Address: FF48H After reset: 67H R/W

Symbol	7	6	5	4	3	2	1	0
WDTM	0	1	1	WDCS4	WDCS3	WDCS2	WDCS1	WDCS0

WDCS4 <sup>Note 1</sup>	WDCS3 <sup>Note 1</sup>	Operation clock selection
0	0	Low-speed internal oscillation clock (f <sub>RL</sub> )
0	1	System Clock (f <sub>x</sub> )
1	×	Watchdog timer operation stopped

WDCS2 <sup>Note 2</sup>	WDCS1 <sup>Note 2</sup>	WDCS0 <sup>Note 2</sup>	Overflow time setting	
			During low-speed internal oscillation clock operation	During system clock operation
0	0	0	2 <sup>11</sup> /f <sub>RL</sub> (4.27 ms)	2 <sup>13</sup> /f <sub>x</sub> (819.2 μs)
0	0	1	2 <sup>12</sup> /f <sub>RL</sub> (8.53 ms)	2 <sup>14</sup> /f <sub>x</sub> (1.64 ms)
0	1	0	2 <sup>13</sup> /f <sub>RL</sub> (17.07 ms)	2 <sup>15</sup> /f <sub>x</sub> (3.28 ms)
0	1	1	2 <sup>14</sup> /f <sub>RL</sub> (34.13 ms)	2 <sup>16</sup> /f <sub>x</sub> (6.55 ms)
1	0	0	2 <sup>15</sup> /f <sub>RL</sub> (68.27 ms)	2 <sup>17</sup> /f <sub>x</sub> (13.11 ms)
1	0	1	2 <sup>16</sup> /f <sub>RL</sub> (136.53 ms)	2 <sup>18</sup> /f <sub>x</sub> (26.21 ms)
1	1	0	2 <sup>17</sup> /f <sub>RL</sub> (273.07 ms)	2 <sup>19</sup> /f <sub>x</sub> (52.43 ms)
1	1	1	2 <sup>18</sup> /f <sub>RL</sub> (546.13 ms)	2 <sup>20</sup> /f <sub>x</sub> (104.86 ms)

**Notes 1.** If “low-speed internal oscillator cannot be stopped” is specified by the option byte, this cannot be set. The low-speed internal oscillation clock will be selected no matter what value is written.

**2.** Reset is released at the maximum cycle (WDCS2, 1, 0 = 1, 1, 1).

**Caution 1.** Set bits 7, 6, and 5 to 0, 1, and 1, respectively. Do not set the other values.

**Cautions 2.** After reset is released, WDTM can be written only once by an 8-bit memory manipulation instruction. If writing is attempted a second time, an internal reset signal is generated. However, at the first write, if “1” and “x” are set for WDCS4 and WDCS3 respectively and the watchdog timer is stopped, then the internal reset signal does not occur even if the following are executed.

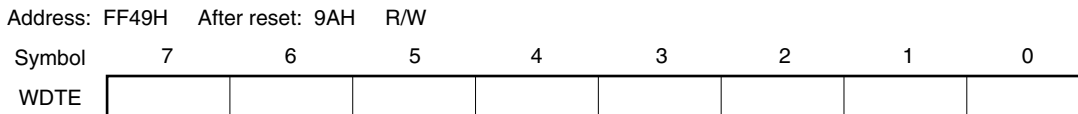
- Second write to WDTM
  - 1-bit memory manipulation instruction to WDTE
  - Writing of a value other than “ACH” to WDTE
3. WDTM cannot be set by a 1-bit memory manipulation instruction.
  4. When using the flash memory self programming by self writing, set the overflow time for the watchdog timer so that enough overflow time is secured (Example 1-byte writing: 200  $\mu$ s MIN., 1-block deletion: 10 ms MIN.).

- Remarks**
1.  $f_{RL}$ : Low-speed internal oscillation clock oscillation frequency
  2.  $f_x$ : System clock oscillation frequency
  3. x: Don't care
  4. Figures in parentheses apply to operation at  $f_{RL} = 480$  kHz (MAX.),  $f_x = 10$  MHz.

**(2) Watchdog timer enable register (WDTE)**

Writing ACH to WDTE clears the watchdog timer counter and starts counting again.  
 This register can be set by an 8-bit memory manipulation instruction.  
 Reset signal generation sets this register to 9AH.

**Figure 8-3. Format of Watchdog Timer Enable Register (WDTE)**



- Cautions**
1. If a value other than ACH is written to WDTE, an internal reset signal is generated.
  2. If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated.
  3. The value read from WDTE is 9AH (this differs from the written value (ACH)).

## 8.4 Operation of Watchdog Timer

### 8.4.1 Watchdog timer operation when “low-speed internal oscillator cannot be stopped” is selected by option byte

The operation clock of watchdog timer is fixed to low-speed internal oscillation clock.

After reset is released, operation is started at the maximum cycle (bits 2, 1, and 0 (WDCS2, WDCS1, WDCS0) of the watchdog timer mode register (WDTM) = 1, 1, 1). The watchdog timer operation cannot be stopped.

The following shows the watchdog timer operation after reset release.

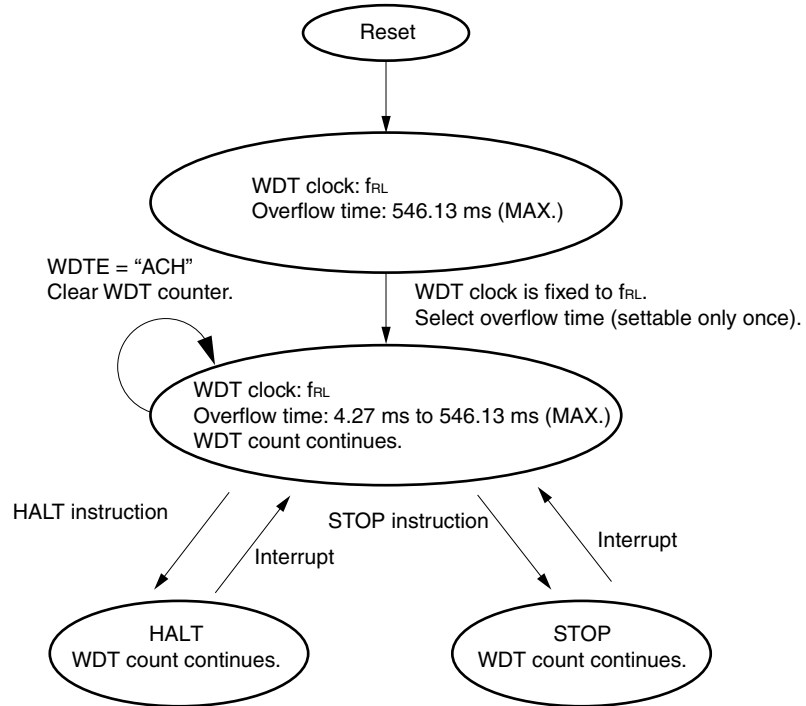
1. The status after reset release is as follows.
  - Operation clock: Low-speed internal oscillation clock
  - Cycle:  $2^{18}/f_{RL}$  (546.13 ms: At operation with  $f_{RL} = 480$  kHz (MAX.))
  - Counting starts
2. The following should be set in the watchdog timer mode register (WDTM) by an 8-bit memory manipulation instruction<sup>Notes 1, 2</sup>.
  - Cycle: Set using bits 2 to 0 (WDCS2 to WDCS0)
3. After the above procedures are executed, writing ACH to WDTE clears the count to 0, enabling recounting.

- Notes**
1. The operation clock (low-speed internal oscillation clock) cannot be changed. If any value is written to bits 3 and 4 (WDCS3, WDCS4) of WDTM, it is ignored.
  2. As soon as WDTM is written, the counter of the watchdog timer is cleared.

**Caution** In this mode, operation of the watchdog timer cannot be stopped even during STOP instruction execution. For 8-bit timer H1 (TMH1), a division of the low-speed internal oscillation clock can be selected as the count source, so clear the watchdog timer using the interrupt request of TMH1 before the watchdog timer overflows after STOP instruction execution. If this processing is not performed, an internal reset signal is generated when the watchdog timer overflows after STOP instruction execution.

A status transition diagram is shown below

Figure 8-4. Status Transition Diagram When “Low-Speed Internal Oscillator Cannot Be Stopped” Is Selected by Option Byte



### 8.4.2 Watchdog timer operation when “low-speed internal oscillator can be stopped by software” is selected by option byte

The operation clock of the watchdog timer can be selected as either the low-speed internal oscillation clock or system clock.

After reset is released, operation is started at the maximum cycle of the low-speed internal oscillation clock (bits 2, 1, and 0 (WDCS2, WDCS1, WDCS0) of the watchdog timer mode register (WDTM) = 1, 1, 1).

The following shows the watchdog timer operation after reset release.

1. The status after reset release is as follows.
  - Operation clock: Low-speed internal oscillation clock
  - Cycle:  $2^{19}/f_{RL}$  (546.13 ms: At operation with  $f_{RL} = 480$  kHz (MAX.))
  - Counting starts
2. The following should be set in the watchdog timer mode register (WDTM) by an 8-bit memory manipulation instruction<sup>Notes 1, 2, 3</sup>.
  - Operation clock: Any of the following can be selected using bits 3 and 4 (WDCS3 and WDCS4).
    - Low-speed internal oscillation clock
    - System clock (fx)
    - Watchdog timer operation stopped
  - Cycle: Set using bits 2 to 0 (WDCS2 to WDCS0)
3. After the above procedures are executed, writing ACH to WDTE clears the count to 0, enabling recounting.

- Notes**
1. As soon as WDTM is written, the counter of the watchdog timer is cleared.
  2. Set bits 7, 6, and 5 to 0, 1, 1, respectively. Do not set the other values.
  3. At the first write, If the watchdog timer is stopped by setting WDCS4 and WDCS3 to 1 and x, respectively, an internal reset signal is not generated even if the following processing is performed.
    - WDTM is written a second time.
    - A 1-bit memory manipulation instruction is executed to WDTE.
    - A value other than ACH is written to WDTE.

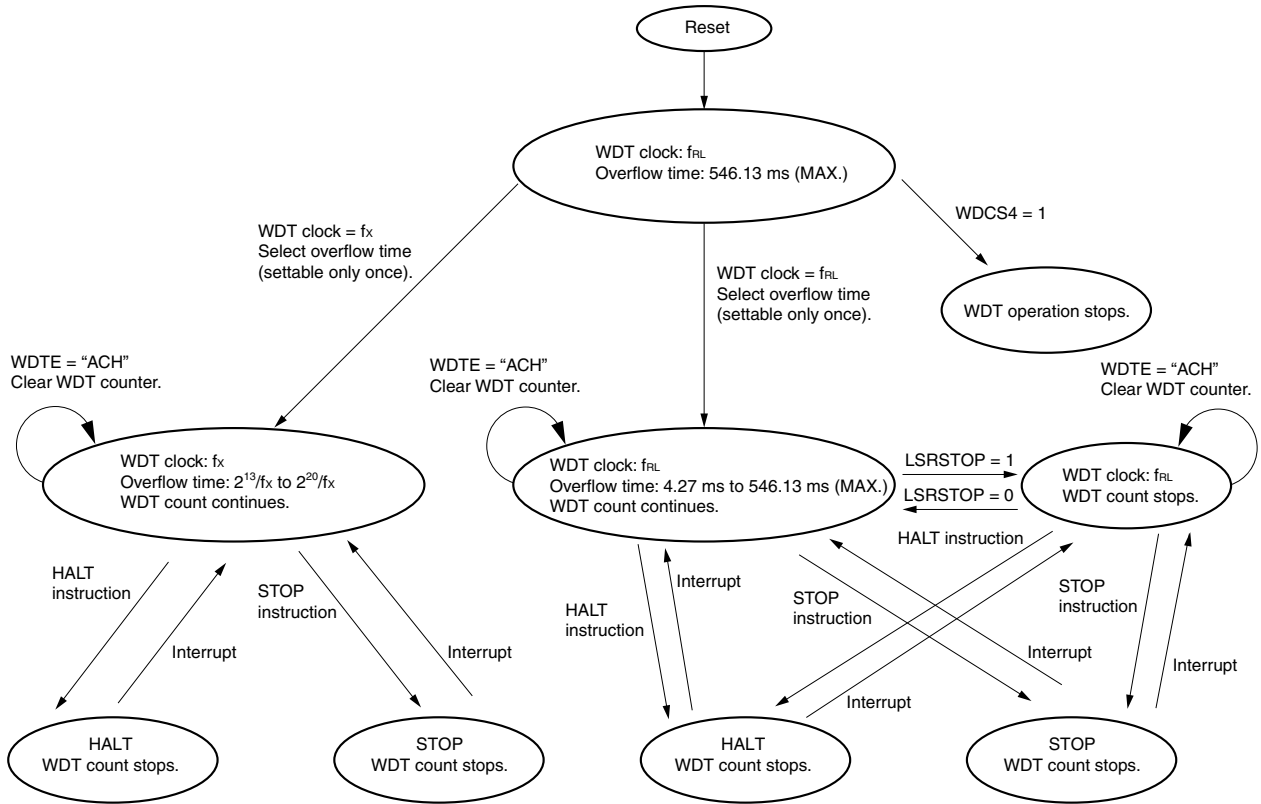
**Caution** In this mode, watchdog timer operation is stopped during HALT/STOP instruction execution. After HALT/STOP mode is released, counting is started again using the operation clock of the watchdog timer set before HALT/STOP instruction execution by WDTM. At this time, the counter is not cleared to 0 but holds its value.

For the watchdog timer operation during STOP mode and HALT mode in each status, see 8.4.3 Watchdog timer operation in STOP mode and 8.4.4 Watchdog timer operation in HALT mode.

A status transition diagram is shown below.



Figure 8-5. Status Transition Diagram When “Low-Speed Internal Oscillator Can Be Stopped by Software” Is Selected by Option Byte

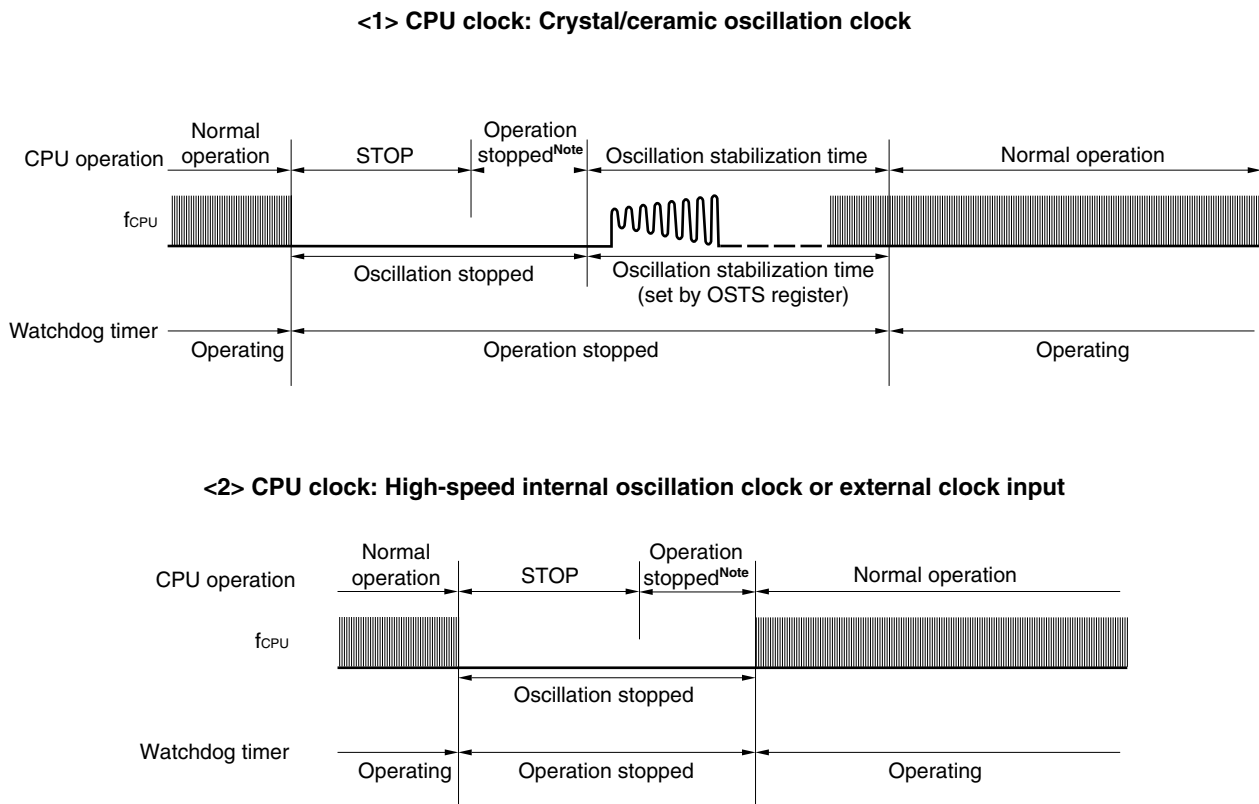


**8.4.3 Watchdog timer operation in STOP mode (when “low-speed internal oscillator can be stopped by software” is selected by option byte)**

The watchdog timer stops counting during STOP instruction execution regardless of whether the system clock or low-speed internal oscillation clock is being used.

- (1) **When the watchdog timer operation clock is the system clock (fx) when the STOP instruction is executed**  
 When STOP instruction is executed, operation of the watchdog timer is stopped. After STOP mode is released, operation stops for 34  $\mu$ s (TYP.) (after waiting for the oscillation stabilization time set by the oscillation stabilization time select register (OSTS) after operation stops in the case of crystal/ceramic oscillation) and then counting is started again using the operation clock before the operation was stopped. At this time, the counter is not cleared to 0 but holds its value.

**Figure 8-6. Operation in STOP Mode (WDT Operation Clock: Clock to Peripheral Hardware)**

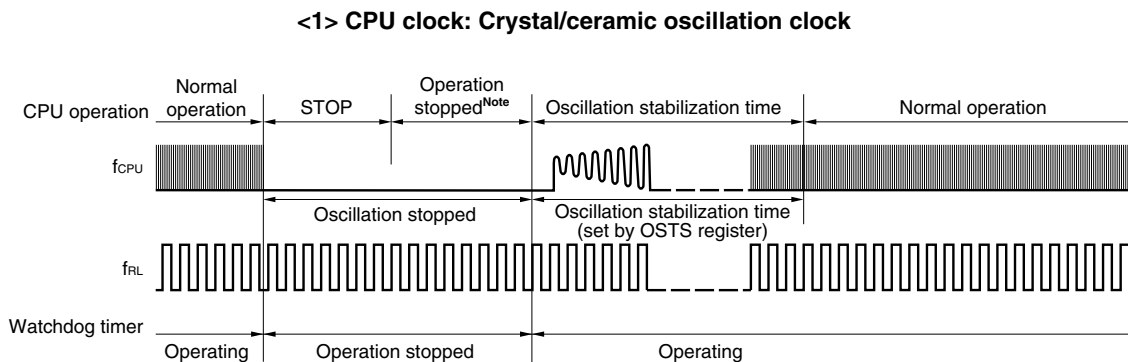


**Note** The operation stop time is 17  $\mu$ s (MIN.), 34  $\mu$ s (TYP.), and 67  $\mu$ s (MAX.).

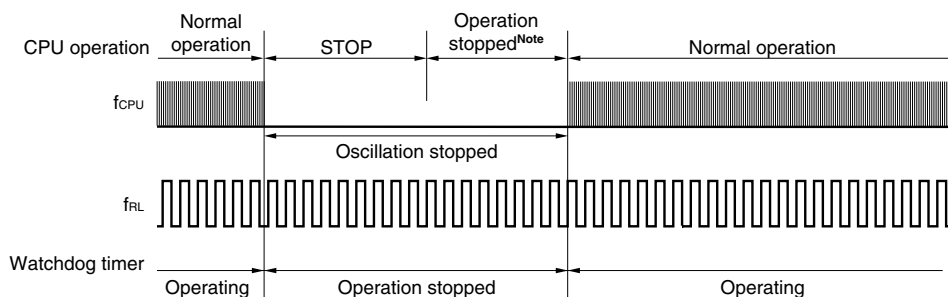
**(2) When the watchdog timer operation clock is the low-speed internal oscillation clock (f<sub>R</sub>L) when the STOP instruction is executed**

When the STOP instruction is executed, operation of the watchdog timer is stopped. After STOP mode is released, operation stops for 34 μs (TYP.) and then counting is started again using the operation clock before the operation was stopped. At this time, the counter is not cleared to 0 but holds its value.

**Figure 8-7. Operation in STOP Mode (WDT Operation Clock: Low-Speed Internal Oscillation Clock)**



**<2> CPU clock: High-speed internal oscillation clock or external clock input**

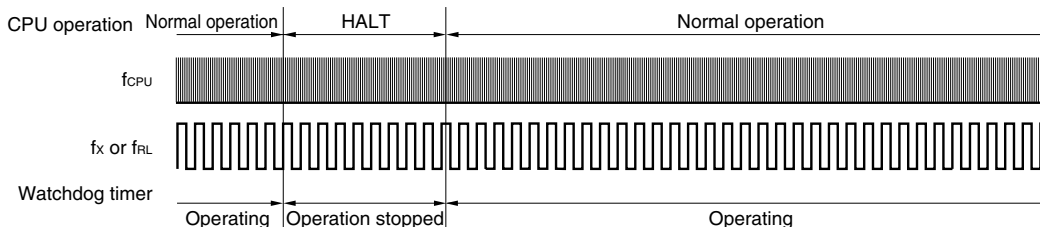


**Note** The operation stop time is 17 μs (MIN.), 34 μs (TYP.), and 67 μs (MAX.).

**8.4.4 Watchdog timer operation in HALT mode (when “low-speed internal oscillator can be stopped by software” is selected by option byte)**

The watchdog timer stops counting during HALT instruction execution regardless of whether the operation clock of the watchdog timer is the system clock (f<sub>x</sub>) or low-speed internal oscillation clock (f<sub>R</sub>L). After HALT mode is released, counting is started again using the operation clock before the operation was stopped. At this time, the counter is not cleared to 0 but holds its value.

**Figure 8-8. Operation in HALT Mode**



## CHAPTER 9 INTERRUPT FUNCTIONS

### 9.1 Interrupt Function Types

There are two types of interrupts: maskable interrupts and resets.

- **Maskable interrupts**

These interrupts undergo mask control. When an interrupt request occurs, the standby release signal occurs, and if an interrupt can be acknowledged then the program corresponding to the address written in the vector table address is executed (vector interrupt servicing). When several interrupt requests are generated at the same time, processing takes place in the priority order of the vector interrupt servicing. For details on the priority order, see Table 9-1.

There are four internal sources and two external sources of maskable interrupts.

- **Reset**

The CPU and SFR are returned to their initial states by the reset signal. The causes for reset signal occurrences are shown in Table 9-1.

When a reset signal occurs, program execution starts from the programs at the addresses written in addresses 0000H and 0001H.

### 9.2 Interrupt Sources and Configuration

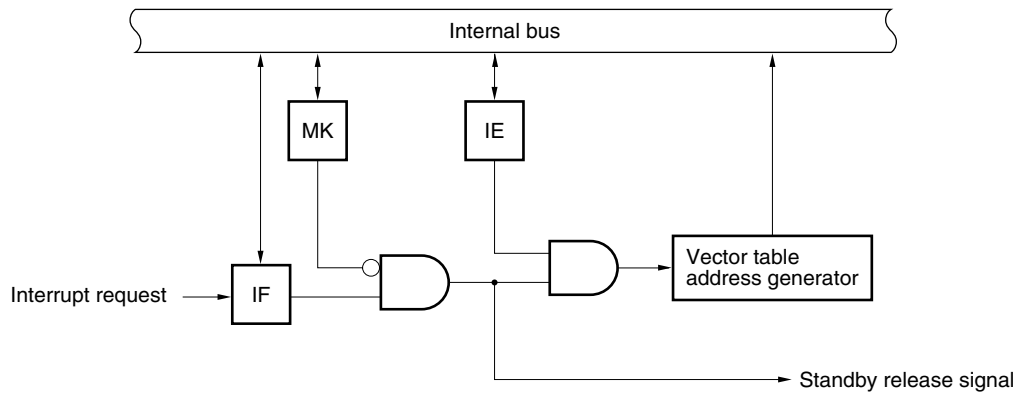
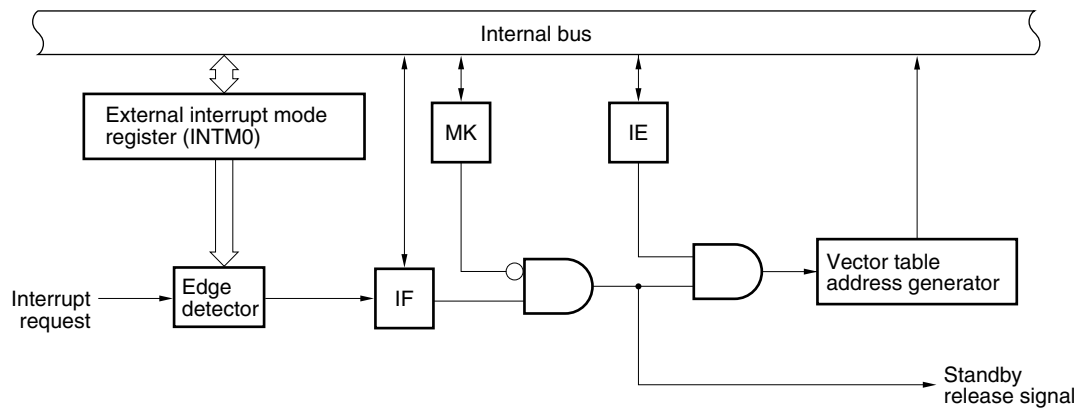
There are a total of six maskable interrupt sources, and up to four reset sources (see **Table 9-1**).

Table 9-1. Interrupt Sources

Interrupt Type	Priority <sup>Note 1</sup>	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type <sup>Note 2</sup>
		Name	Trigger			
Maskable	1	INTLVI	Low-voltage detection <sup>Note 3</sup>	Internal	0006H	(A)
	2	INTP0	Pin input edge detection	External	0008H	(B)
	3	INTP1			000AH	
	4	INTTMH1	Match between TMH1 and CMP01 (when compare register is specified)	Internal	000CH	(A)
	5	INTTM000	Match between TM00 and CR000 (when compare register is specified), TI010 pin valid edge detection (when capture register is specified)		000EH	
	6	INTTM010	Match between TM00 and CR010 (when compare register is specified), TI000 pin valid edge detection (when capture register is specified)		0010H	
Reset	–	RESET	Reset input	–	0000H	–
		POC	Power-on-clear			
		LVI	Low-voltage detection <sup>Note 4</sup>			
		WDT	WDT overflow			

- Notes**
1. Priority is the vector interrupt servicing priority order when several maskable interrupt requests are generated at the same time. 1 is the highest and 6 is the lowest.
  2. Basic configuration types (A) and (B) correspond to (A) and (B) in Figure 9-1.
  3. When bit 1 (LVIMD) of low-voltage detection register (LVIM) = 0 is selected.
  4. When bit 1 (LVIMD) of low-voltage detection register (LVIM) = 1 is selected.

Figure 9-1. Basic Configuration of Interrupt Function

**(A) Internal maskable interrupt****(B) External maskable interrupt**

IF: Interrupt request flag

IE: Interrupt enable flag

MK: Interrupt mask flag

### 9.3 Interrupt Function Control Registers

The interrupt functions are controlled by the following four types of registers.

- Interrupt request flag register 0 (IF0)
- Interrupt mask flag register 0 (MK0)
- External interrupt mode register 0 (INTM0)
- Program status word (PSW)

Table 9-2 lists interrupt requests, the corresponding interrupt request flags, and interrupt mask flags.

**Table 9-2. Interrupt Request Signals and Corresponding Flags**

Interrupt Request Signal	Interrupt Request Flag	Interrupt Mask Flag
INTLVI	LVIIIF	LVIMK
INTP0	PIF0	PMK0
INTP1	PIF1	PMK1
INTTMH1	TMIFH1	TMMKH1
INTTM000	TMIF000	TMMK000
INTTM010	TMIF010	TMMK010

**(1) Interrupt request flag register 0 (IF0)**

An interrupt request flag is set to 1 when the corresponding interrupt request is issued, or when the instruction is executed. It is cleared to 0 by executing an instruction when the interrupt request is acknowledged or when a reset signal is input.

IF0 is set with a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears IF0 to 00H.

**Figure 9-2. Format of Interrupt Request Flag Register 0 (IF0)**

Address: FFE0H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	0
IF0	0	TMIF010	TMIF000	TMIFH1	PIF1	PIF0	LVIIIF	0

××IF×	Interrupt request flag
0	No interrupt request signal has been issued.
1	An interrupt request signal has been issued; an interrupt request status.

**Caution** Because P21 and P32 have an alternate function as external interrupt inputs, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, the interrupt mask flag should be set to 1 before using the output mode.

**(2) Interrupt mask flag register 0 (MK0)**

The interrupt mask flag is used to enable and disable the corresponding maskable interrupts. MK0 is set with a 1-bit or 8-bit memory manipulation instruction. Reset signal generation sets MK0 to FFH.

**Figure 9-3. Format of Interrupt Mask Flag Register 0 (MK0)**

Address: FFE4H After reset: FFH R/W

Symbol	7	<6>	<5>	<4>	<3>	<2>	<1>	0
MK0	1	TMMK010	TMMK000	TMMKH1	PMK1	PMK0	LVIMK	1

xxMKx	Interrupt servicing control
0	Enables interrupt servicing.
1	Disables interrupt servicing.

**Caution** Because P21 and P32 have an alternate function as external interrupt inputs, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, the interrupt mask flag should be set to 1 before using the output mode.

**(3) External interrupt mode register 0 (INTM0)**

This register is used to set the valid edge of INTP0 and INTP1. INTM0 is set with an 8-bit memory manipulation instruction. Reset signal generation clears INTM0 to 00H.

**Figure 9-4. Format of External Interrupt Mode Register 0 (INTM0)**

Address: FFECH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
INTM0	0	0	ES11	ES10	ES01	ES00	0	0

ES11	ES10	INTP1 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES01	ES00	INTP0 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

**Caution** 1. Be sure to clear bits 0, 1, 6, and 7 to 0.



**Caution 2.** Before setting the INTM0 register, be sure to set the corresponding interrupt mask flag (××MK× = 1) to disable interrupts. After setting the INTM0 register, clear the interrupt request flag (××IF× = 0), then clear the interrupt mask flag (××MK× = 0), which will enable interrupts.

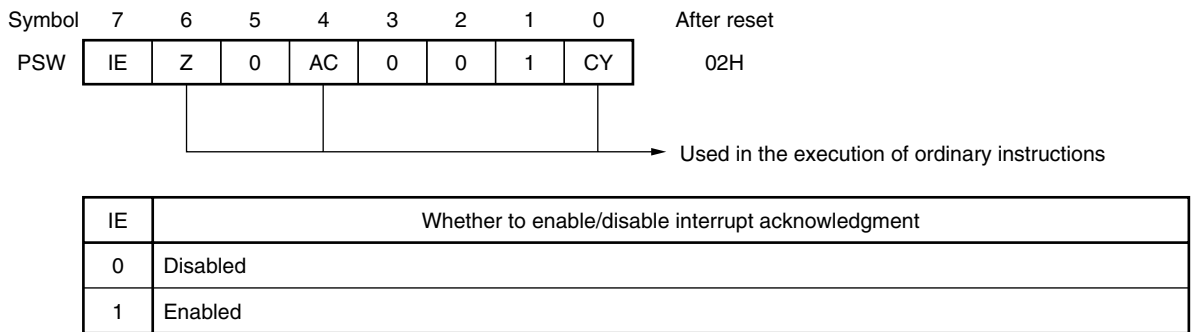
**(4) Program status word (PSW)**

The program status word is used to hold the instruction execution result and the current status of the interrupt requests. The IE flag, used to enable and disable maskable interrupts, is mapped to PSW.

PSW can be read- and write-accessed in 8-bit units, as well as using bit manipulation instructions and dedicated instructions (EI and DI). When a vectored interrupt is acknowledged, the PSW is automatically saved to a stack, and the IE flag is reset to 0.

Reset signal generation sets PSW to 02H.

**Figure 9-5. Program Status Word (PSW) Configuration**



**9.4 Interrupt Servicing Operation**

**9.4.1 Maskable interrupt request acknowledgment operation**

A maskable interrupt request can be acknowledged when the interrupt request flag is set to 1 and the corresponding interrupt mask flag is cleared to 0. If the interrupt enabled status is in effect (when the IE flag is set to 1), then the request is acknowledged as a vector interrupt.

The time required to start the vectored interrupt servicing after a maskable interrupt request has been generated is shown in Table 9-3.

See Figures 9-7 and 9-8 for the interrupt request acknowledgment timing.

**Table 9-3. Time from Generation of Maskable Interrupt Request to Servicing**

Minimum Time	Maximum Time <sup>Note</sup>
9 clocks	19 clocks

**Note** The wait time is maximum when an interrupt request is generated immediately before BT and BF instructions.

**Remark** 1 clock:  $\frac{1}{f_{CPU}}$  (f<sub>CPU</sub>: CPU clock)

When two or more maskable interrupt requests are generated at the same time, they are acknowledged starting from the interrupt request assigned the highest priority.

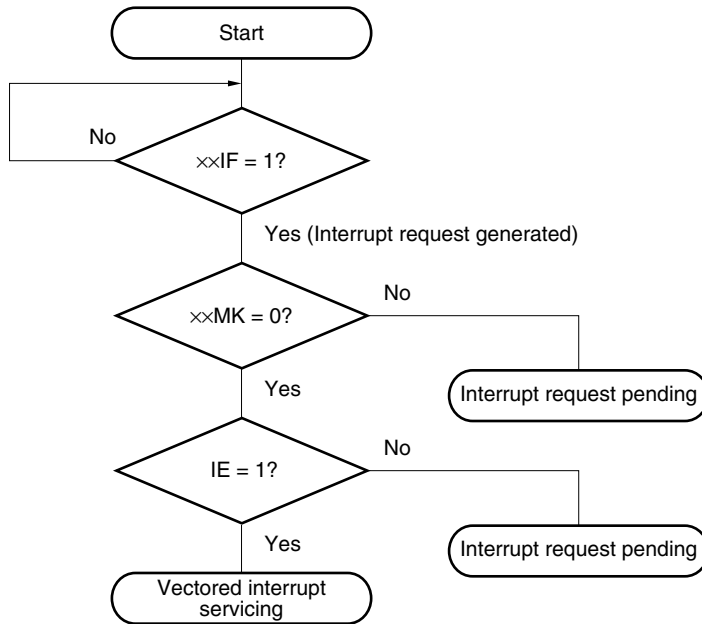
A pending interrupt is acknowledged when a status in which it can be acknowledged is set.

Figure 9-6 shows the algorithm of interrupt request acknowledgment.

When a maskable interrupt request is acknowledged, the contents of the PSW and PC are saved to the stack in that order, the IE flag is reset to 0, and the data in the vector table determined for each interrupt request is loaded to the PC, and execution branches.

To return from interrupt servicing, use the RETI instruction.

**Figure 9-6. Interrupt Request Acknowledgment Processing Algorithm**

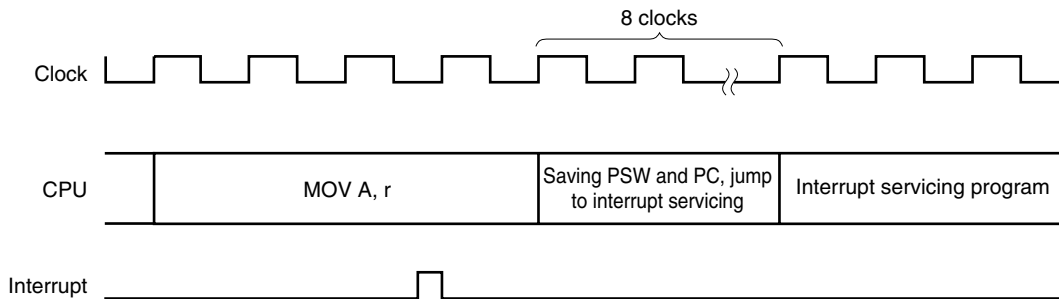


xxIF: Interrupt request flag

xxMK: Interrupt mask flag

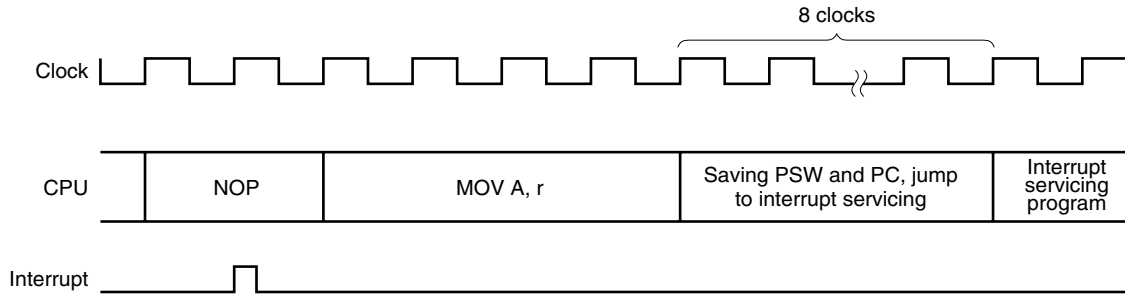
IE: Flag to control maskable interrupt request acknowledgment (1 = enable, 0 = disable)

**Figure 9-7. Interrupt Request Acknowledgment Timing (Example of MOV A, r)**



If an interrupt request flag (xxIF) is set before an instruction clock  $n$  ( $n = 4$  to  $10$ ) under execution becomes  $n - 1$ , the interrupt is acknowledged after the instruction under execution is complete. Figure 9-7 shows an example of the interrupt request acknowledgment timing for an 8-bit data transfer instruction MOV A, r. Since this instruction is executed for 4 clocks, if an interrupt occurs for 3 clocks after the instruction fetch starts, the interrupt acknowledgment processing is performed after the MOV A, r instruction is executed.

**Figure 9-8. Interrupt Request Acknowledgment Timing (When Interrupt Request Flag Is Set at Last Clock During Instruction Execution)**



If an interrupt request flag ( $\times\times IF$ ) is set at the last clock of the instruction, the interrupt acknowledgment processing starts after the next instruction is executed.

Figure 9-8 shows an example of the interrupt request acknowledgment timing for an interrupt request flag that is set at the second clock of NOP (2-clock instruction). In this case, the MOV A, r instruction after the NOP instruction is executed, and then the interrupt acknowledgment processing is performed.

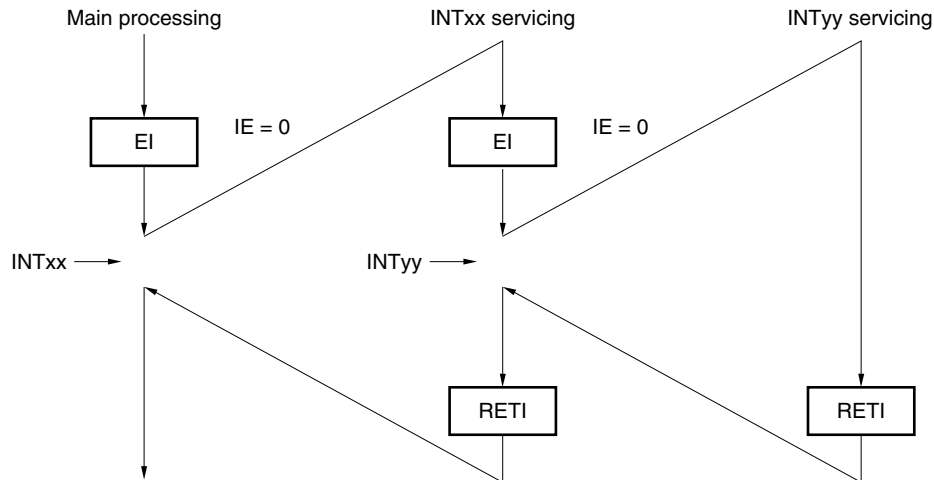
**Caution** Interrupt requests will be held pending while the interrupt request flag register 0 (IF0) or interrupt mask flag register 0 (MK0) are being accessed.

#### 9.4.2 Multiple interrupt servicing

In order to perform multiple interrupt servicing in which another interrupt is acknowledged while an interrupt is being serviced, the interrupt mask function must be used to mask interrupts for which a low priority is to be set.

Figure 9-9. Example of Multiple Interrupts (1/2)

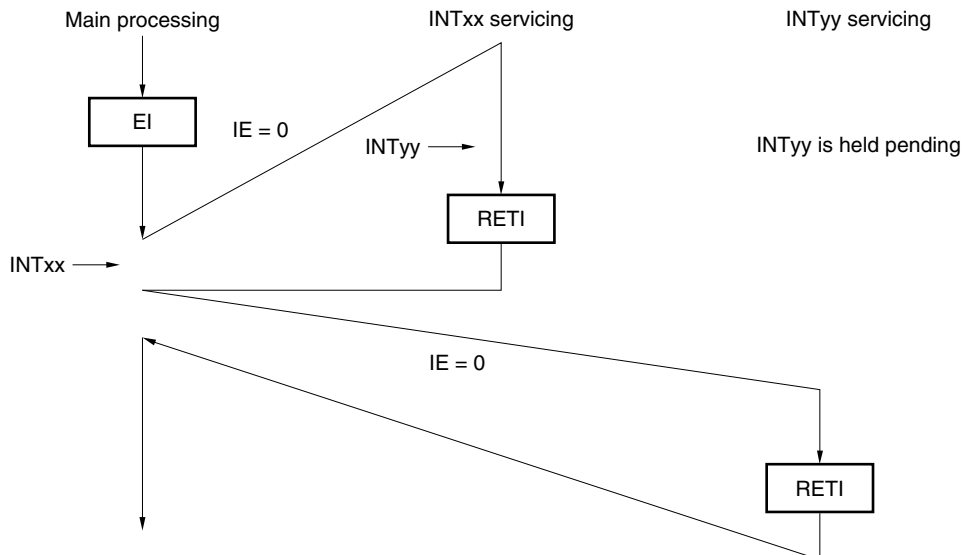
## Example 1. Multiple interrupts are acknowledged



During interrupt INTxx servicing, interrupt request INTyy is acknowledged, and multiple interrupts are generated. Before each interrupt request acknowledgment, the EI instruction is issued, the interrupt mask is released, and the interrupt request acknowledgment enable state is set.

**Caution** Multiple interrupts can be acknowledged even for low-priority interrupts.

## Example 2. Multiple interrupts are not generated because interrupts are not enabled



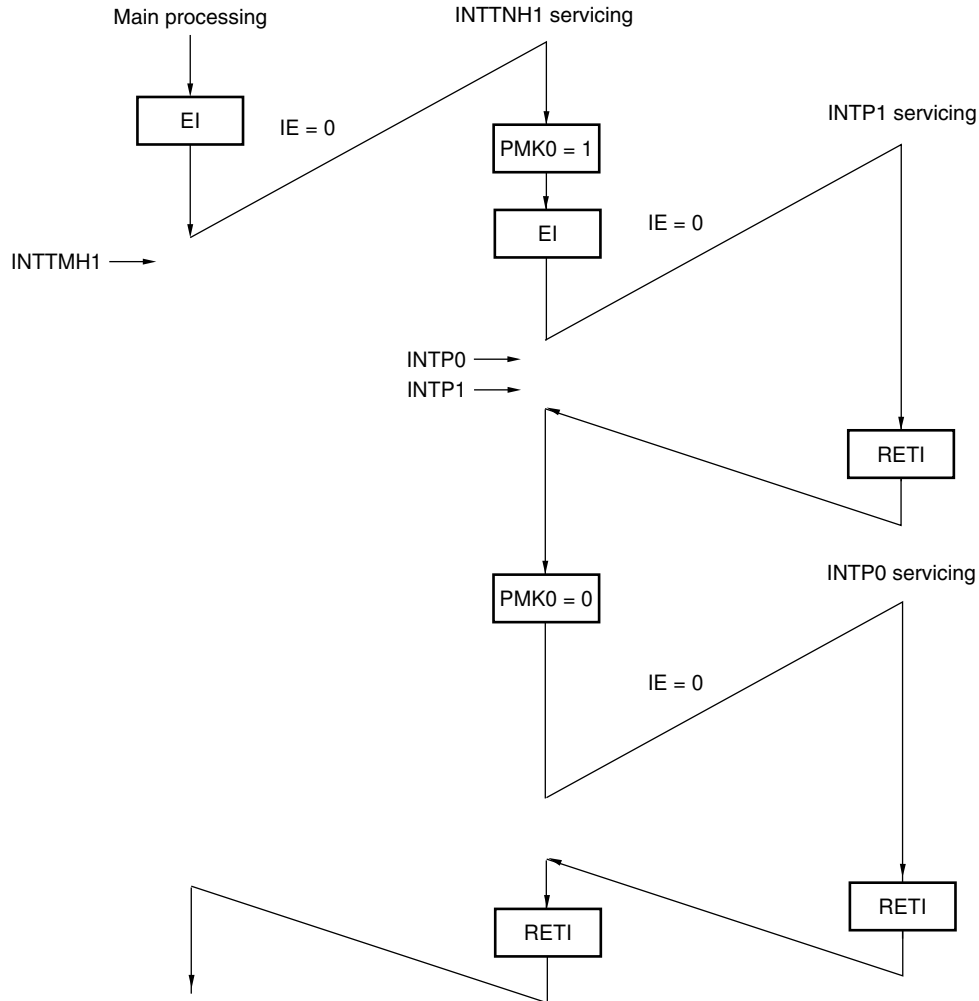
Because interrupts are not enabled in interrupt INTxx servicing (the EI instruction is not issued), interrupt request INTyy is not acknowledged, and multiple interrupts are not generated. The INTyy request is held pending and acknowledged after the INTxx servicing is performed.

IE = 0: Interrupt request acknowledgment disabled

Figure 9-9. Example of Multiple Interrupts (2/2)

## Example 3. A priority is controlled by the multiple interrupts

The vector interrupt enable state is set for INTPO, INTP1, and INTTMH1.  
(Interrupt priority INTPO > INTP1 > INTTMH1 (refer to Table 9-1))



In the interrupt INTTMH1 servicing, servicing is performed such that the INTP1 interrupt is given priority, since the INTPO interrupt was first masked.

Afterwards, once the interrupt mask for INTPO is released, INTPO processing through multiple interrupts is performed.

IE = 0: Interrupt request acknowledgment disabled

### 9.4.3 Interrupt request pending

Some instructions may keep pending the acknowledgment of an instruction request until the completion of the execution of the next instruction even if the interrupt request (maskable interrupt and external interrupt) is generated during the execution. The following shows such instructions (interrupt request pending instruction).

- Manipulation instruction for interrupt request flag register 0 (IF0)
- Manipulation instruction for interrupt mask flag register 0 (MK0)

## CHAPTER 10 STANDBY FUNCTION

### 10.1 Standby Function and Configuration

#### 10.1.1 Standby function

**Table 10-1. Relationship Between Operation Clocks in Each Operation Status**

Operation Mode \ Status	Low-Speed Internal Oscillator		System Clock	Clock Supplied to Peripheral Hardware
	Note 1	Note 2		
			LSRSTOP = 0	LSRSTOP = 1
Reset	Stopped		Stopped	Stopped
STOP	Oscillating	Oscillating <sup>Note 3</sup>	Stopped	
HALT			Oscillating	Oscillating

- Notes**
1. When “Cannot be stopped” is selected for low-speed internal oscillator by the option byte.
  2. When it is selected that the low-speed internal oscillator “can be stopped by software”, oscillation of the low-speed internal oscillator can be stopped by LSRSTOP.
  3. If the operating clock of the watchdog timer is the low-speed internal oscillation clock, the watchdog timer is stopped.

**Caution** The LSRSTOP setting is valid only when “Can be stopped by software” is set for the low-speed internal oscillator by the option byte.

**Remark** LSRSTOP: Bit 0 of the low-speed internal oscillation mode register (LSRCM)

The standby function is designed to reduce the operating current of the system. The following two modes are available.

#### (1) HALT mode

HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. Oscillation of the system clock oscillator continues. If the low-speed internal oscillator is operating before the HALT mode is set, oscillation of the clock of the low-speed internal oscillator continues (refer to **Table 10-1**. Oscillation of the low-speed internal oscillation clock (whether it cannot be stopped or can be stopped by software) is set by the option byte). In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and frequently carrying out intermittent operations.

**(2) STOP mode**

STOP instruction execution sets the STOP mode. In the STOP mode, the system clock oscillator stops, stopping the whole system, thereby considerably reducing the CPU operating current.

Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, select the HALT mode if processing must be immediately started by an interrupt request when the operation stop time<sup>Note</sup> is generated after the STOP mode is released (because an additional wait time for stabilizing oscillation elapses when crystal/ceramic oscillation is used).

**Note** The operation stop time is 17  $\mu$ s (MIN.), 34  $\mu$ s (TYP.), and 67  $\mu$ s (MAX.).

In either of these two modes, all the contents of registers, flags and data memory just before the standby mode is set are held. The I/O port output latches and output buffer statuses are also held.

- Cautions**
1. When shifting to the STOP mode, be sure to stop the peripheral hardware operation before executing STOP instruction (except the peripheral hardware that operates on the low-speed internal oscillation clock).
  2. If the low-speed internal oscillator is operating before the STOP mode is set, oscillation of the low-speed internal oscillation clock cannot be stopped in the STOP mode (refer to Table 10-1).

**10.1.2 Registers used during standby**

The oscillation stabilization time after the standby mode is released is controlled by the oscillation stabilization time select register (OSTS).

**Remark** For the registers that start, stop, or select the clock, see **CHAPTER 5 CLOCK GENERATORS**.

**(1) Oscillation stabilization time select register (OSTS)**

This register is used to select oscillation stabilization time of the clock supplied from the oscillator when the STOP mode is released. The wait time set by OSTO is valid only when the crystal/ceramic oscillation clock is selected as the system clock and after the STOP mode is released. If the high-speed internal oscillation or external clock input is selected as the system clock source, no wait time elapses.

The system clock oscillator and the oscillation stabilization time that elapses after power application or release of reset are selected by the option byte. For details, refer to **CHAPTER 14 OPTION BYTE**.

OSTS is set by using the 8-bit memory manipulation instruction.

**Figure 10-1. Format of Oscillation Stabilization Time Select Register (OSTS)**

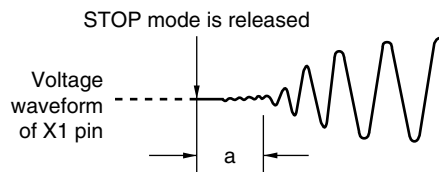
Address: FFF4H, After reset: Undefined, R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	0	OSTS1	OSTS0

OSTS1	OSTS0	Selection of oscillation stabilization time
0	0	$2^{10}/f_x$ (102.4 $\mu$ s)
0	1	$2^{12}/f_x$ (409.6 $\mu$ s)
1	0	$2^{15}/f_x$ (3.27 ms)
1	1	$2^{17}/f_x$ (13.1 ms)

**Cautions 1.** To set and then release the STOP mode, set the oscillation stabilization time as follows. **Expected oscillation stabilization time of resonator  $\leq$  Oscillation stabilization time set by OSTO**

**2.** The wait time after the STOP mode is released does not include the time from the release of the STOP mode to the start of clock oscillation (“a” in the figure below), regardless of whether STOP mode was released by reset signal generation or interrupt generation.



**3.** The oscillation stabilization time that elapses on power application or after release of reset is selected by the option byte. For details, refer to **CHAPTER 14 OPTION BYTE**.

**Remarks 1.** ( ):  $f_x = 10$  MHz

**2.** Determine the oscillation stabilization time of the resonator by checking the characteristics of the resonator to be used.



## 10.2 Standby Function Operation

### 10.2.1 HALT mode

#### (1) HALT mode

The HALT mode is set by executing the HALT instruction.

The operating statuses in the HALT mode are shown below.

**Caution** Because an interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag clear, the standby mode is immediately cleared if set.

**Table 10-2. Operating Statuses in HALT Mode**

Setting of HALT Mode		Low-Speed Internal Oscillator cannot be stopped <sup>Note</sup> .	Low-Speed Internal Oscillator can be stopped <sup>Note</sup> .	
			When Low-Speed Internal Oscillation Continues	When Low-Speed Internal Oscillation Stops
Item				
System clock		Clock supply to CPU is stopped.		
CPU		Operation stops.		
Port (latch)		Holds status before HALT mode was set.		
16-bit timer/event counter 00		Operable		
8-bit timer H1	Sets count clock to $f_{XP}$ to $f_{XP}/2^{12}$	Operable		
	Sets count clock to $f_{RL}/2^7$	Operable	Operable	Operation stops.
Watchdog timer	“System clock” selected as operating clock	Setting disabled.	Operation stops.	
	“Low-speed internal oscillation clock” selected as operating clock	Operable (Operation continues)	Operation stops.	
Power-on-clear circuit		Always operates.		
Low-voltage detector		Operable		
External interrupt		Operable		

**Note** “Cannot be stopped” or “Stopped by software” is selected for low-speed internal oscillator by the option byte (for the option byte, see **CHAPTER 14 OPTION BYTE**).

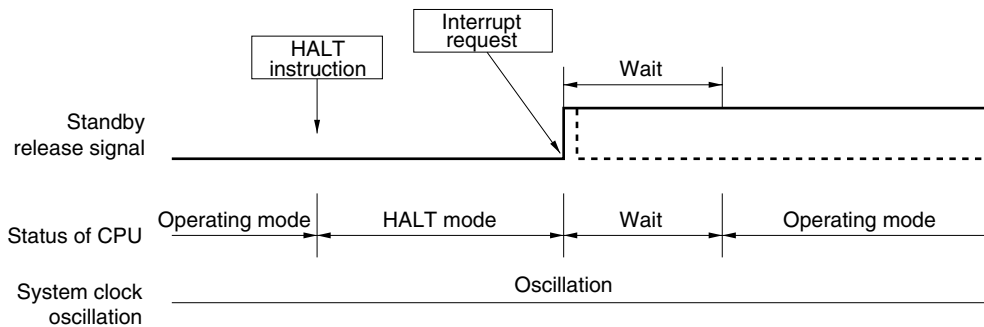
**(2) HALT mode release**

The HALT mode can be released by the following two sources.

**(a) Release by unmasked interrupt request**

When an unmasked interrupt request is generated, the HALT mode is released. If interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

**Figure 10-2. HALT Mode Release by Interrupt Request Generation**



**Remarks 1.** The broken lines indicate the case when the interrupt request which has released the standby mode is acknowledged.

**2.** The wait time is as follows:

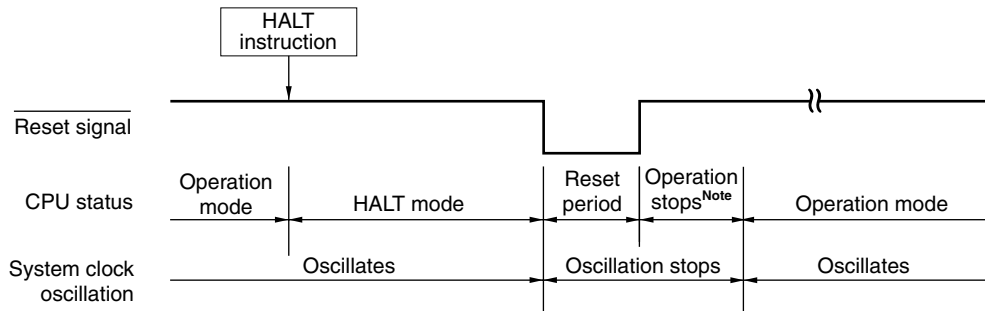
- When vectored interrupt servicing is carried out: 11 to 13 clocks
- When vectored interrupt servicing is not carried out: 3 to 5 clocks

**(b) Release by reset signal generation**

When the reset signal is input, HALT mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

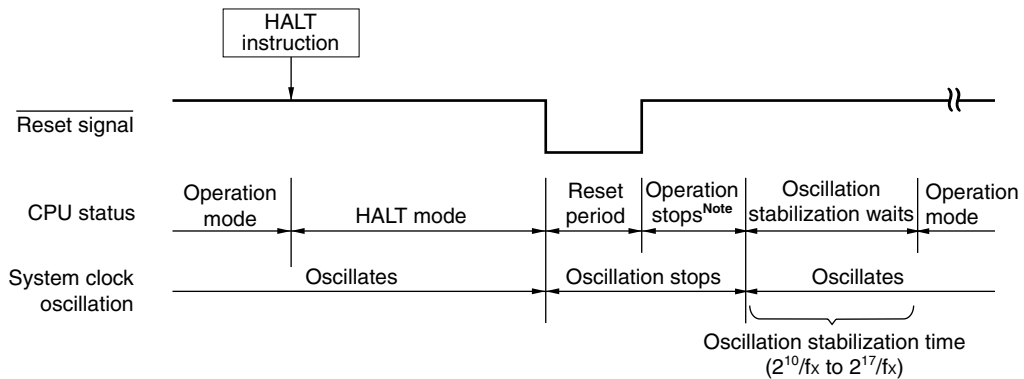
**Figure 10-3. HALT Mode Release by Reset Signal Generation**

**(1) When CPU clock is high-speed internal oscillation clock or external input clock**



**Note** Operation is stopped (277  $\mu$ s (MIN.), 544  $\mu$ s (TYP.), 1.075 ms (MAX.)) because the option byte is referenced.

**(2) When CPU clock is crystal/ceramic oscillation clock**



**Note** Operation is stopped (276  $\mu$ s (MIN.), 544  $\mu$ s (TYP.), 1.074 ms (MAX.)) because the option byte is referenced.

**Remark** fx: System clock oscillation frequency

**Table 10-3. Operation in Response to Interrupt Request in HALT Mode**

Release Source	MK $\times$	IE	Operation
Maskable interrupt request	0	0	Next address instruction execution
	0	1	Interrupt servicing execution
	1	$\times$	HALT mode held
Reset signal generation	-	$\times$	Reset processing

$\times$ : don't care

10.2.2 STOP mode

(1) STOP mode setting and operating statuses

The STOP mode is set by executing the STOP instruction.

**Caution** Because an interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set. Thus, in the STOP mode, the normal operation mode is restored after the STOP instruction is executed and then the operation is stopped for the duration of 34  $\mu$ s (TYP.) (after an additional wait time for stabilizing oscillation set by the oscillation stabilization time select register (OSTS) has elapsed when crystal/ceramic oscillation is used).

The operating statuses in the STOP mode are shown below.

Table 10-4. Operating Statuses in STOP Mode

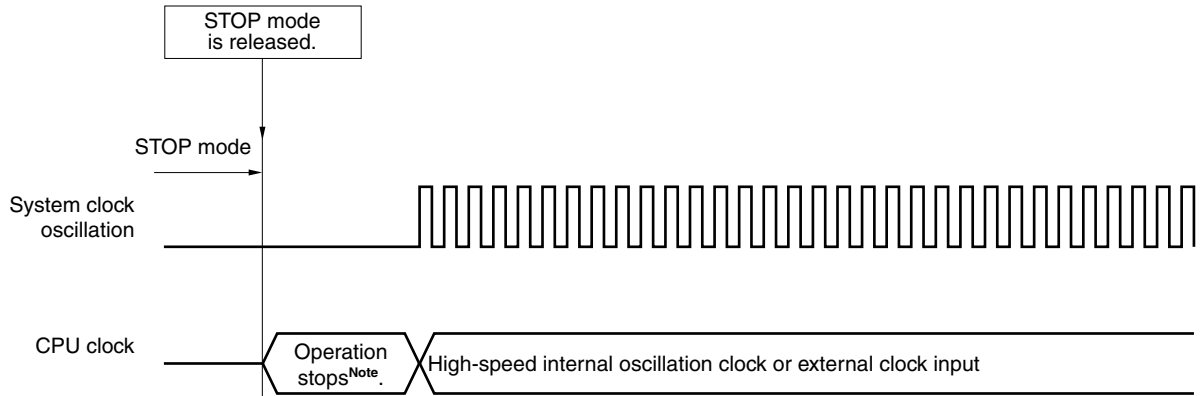
Setting of STOP Mode		Low-Speed Internal Oscillator cannot be stopped <sup>Note</sup> .	Low-Speed Internal Oscillator can be stopped <sup>Note</sup> .	
			When Low-Speed Internal Oscillation Continues	When Low-Speed Internal Oscillation Stops
Item				
System clock		Oscillation stops.		
CPU		Operation stops.		
Port (latch)		Holds status before STOP mode was set.		
16-bit timer/event counter 00		Operation stops.		
8-bit timer H1	Sets count clock to $f_{XP}$ to $f_{XP}/2^{12}$	Operation stops.		
	Sets count clock to $f_{RL}/2^7$	Operable	Operable	Operation stops.
Watchdog timer	“System clock” selected as operating clock	Setting disabled.	Operation stops.	
	“Low-speed internal oscillation clock” selected as operating clock	Operable (Operation continues)	Operation stops.	
Power-on-clear circuit		Always operates.		
Low-voltage detector		Operable		
External interrupt		Operable		

**Note** “Cannot be stopped” or “Stopped by software” is selected for low-speed internal oscillator by the option byte (for the option byte, see CHAPTER 14 OPTION BYTE).

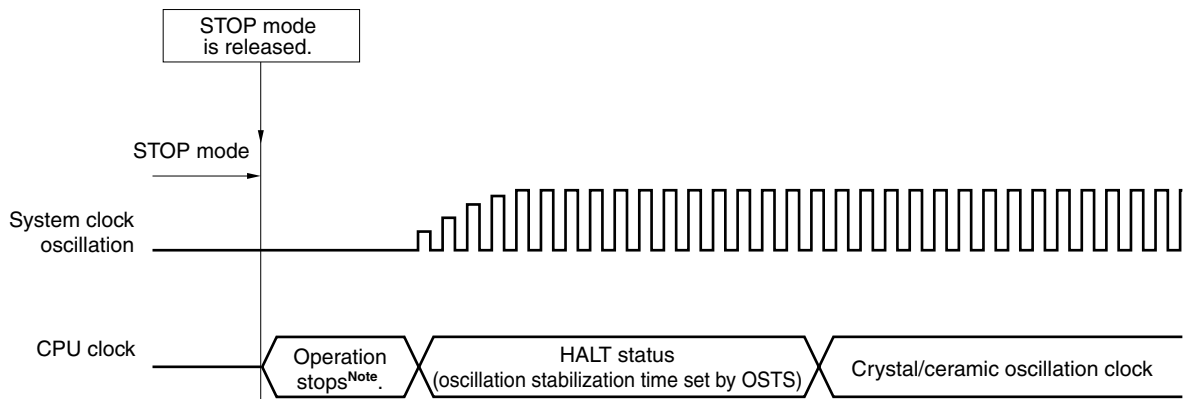
(2) STOP mode release

Figure 10-4. Operation Timing When STOP Mode Is Released

<1> If high-speed internal oscillation clock or external input clock is selected as system clock to be supplied



<2> If crystal/ceramic oscillation clock is selected as system clock to be supplied



**Note** The operation stop time is 17  $\mu$ s (MIN.), 34  $\mu$ s (TYP.), and 67  $\mu$ s (MAX.).

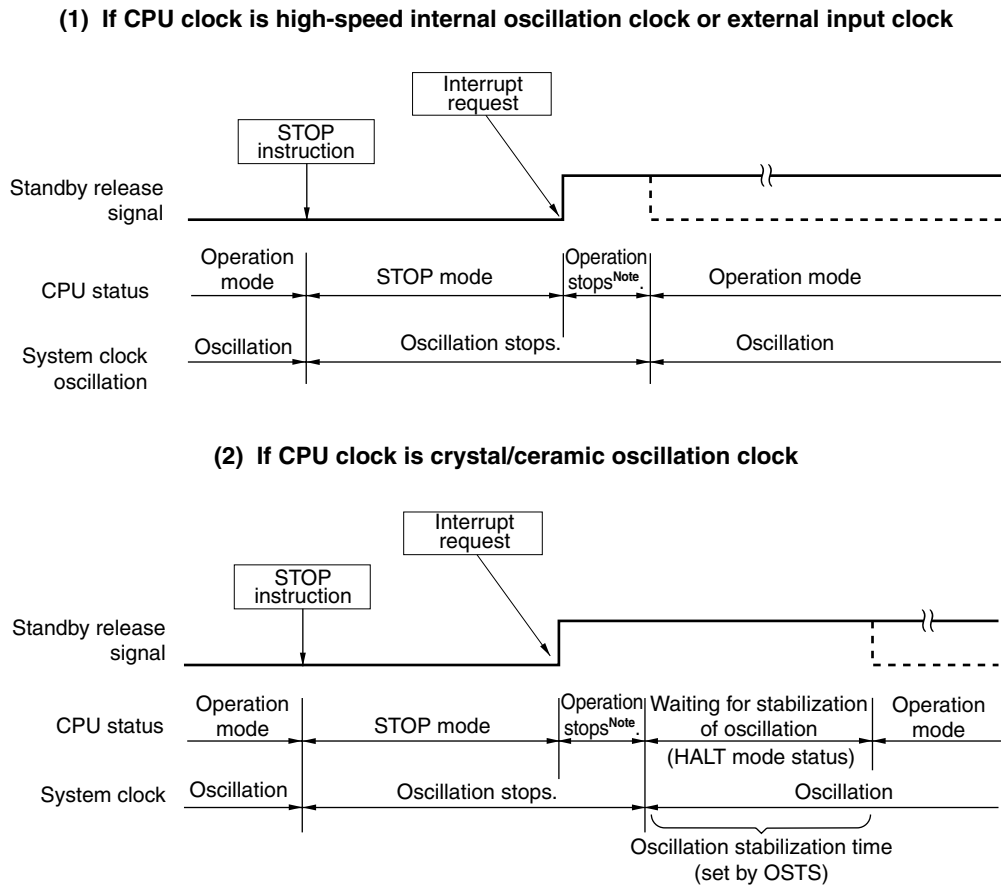
The STOP mode can be released by the following two sources.

**(a) Release by unmasked interrupt request**

When an unmasked interrupt request (8-bit timer H1<sup>Note</sup>, low-voltage detector, external interrupt request) is generated, the STOP mode is released. After the oscillation stabilization time has elapsed, if interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

**Note** Only when sets count clock to  $f_{RL}/2^7$

**Figure 10-5. STOP Mode Release by Interrupt Request Generation**



**Note** The operation stop time is 17  $\mu$ s (MIN.), 34  $\mu$ s (TYP.), and 67  $\mu$ s (MAX.).

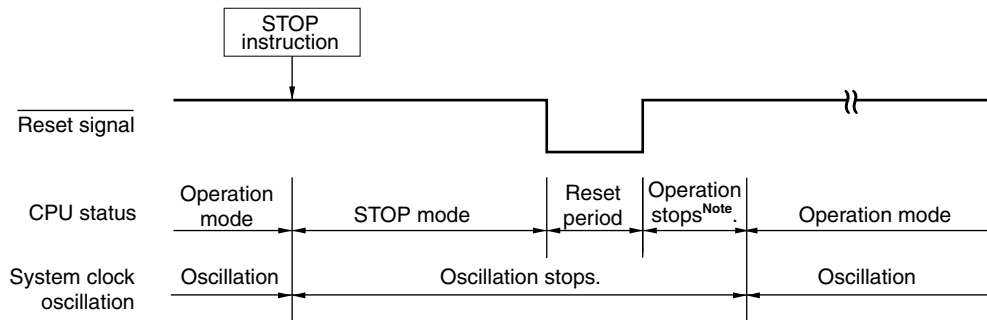
**Remark** The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

**(b) Release by reset signal generation**

When the reset signal is input, STOP mode is released and a reset operation is performed after the oscillation stabilization time has elapsed.

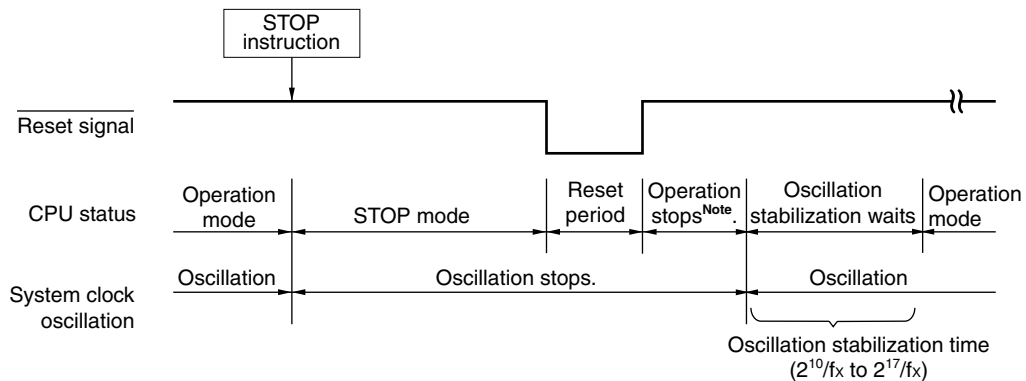
**Figure 10-6. STOP Mode Release by Reset signal generation**

**(1) If CPU clock is high-speed internal oscillation clock or external input clock**



**Note** Operation is stopped (277  $\mu$ s (MIN.), 544  $\mu$ s (TYP.), 1.075 ms (MAX.)) because the option byte is referenced.

**(2) If CPU clock is crystal/ceramic oscillation clock**



**Note** Operation is stopped (276  $\mu$ s (MIN.), 544  $\mu$ s (TYP.), 1.074 ms (MAX.)) because the option byte is referenced.

**Remark** fx: System clock oscillation frequency

**Table 10-5. Operation in Response to Interrupt Request in STOP Mode**

Release Source	MK $\times$	IE	Operation
Maskable interrupt request	0	0	Next address instruction execution
	0	1	Interrupt servicing execution
	1	$\times$	STOP mode held
Reset signal generation	–	$\times$	Reset processing

$\times$ : don't care

## CHAPTER 11 RESET FUNCTION

The following four operations are available to generate a reset signal.

- (1) External reset input via  $\overline{\text{RESET}}$  pin
- (2) Internal reset by watchdog timer overflows
- (3) Internal reset by comparison of supply voltage and detection voltage of power-on-clear (POC) circuit
- (4) Internal reset by comparison of supply voltage and detection voltage of low-power-supply detector (LVI)

External and internal resets have no functional differences. In both cases, program execution starts from the programs at the address written in addresses 0000H and 0001H when the reset signal is generated.

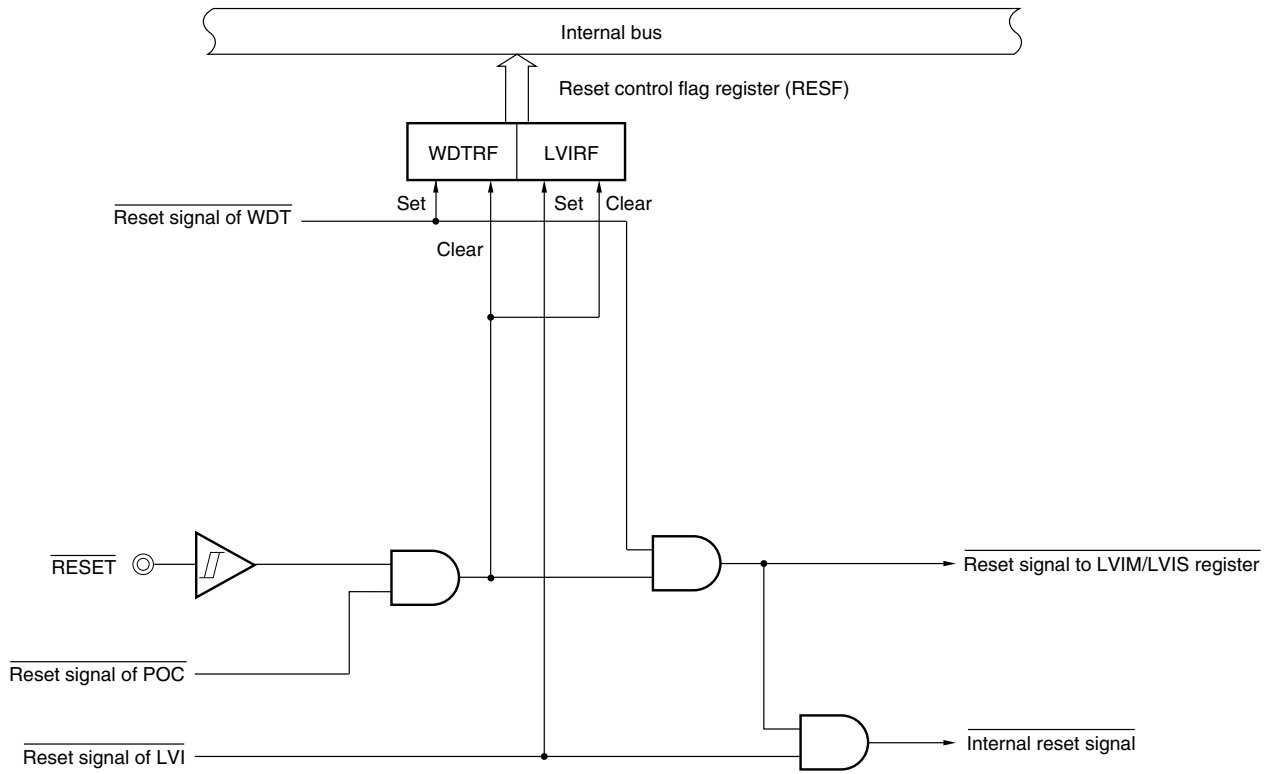
A reset is applied when a low level is input to the  $\overline{\text{RESET}}$  pin, the watchdog timer overflows, or by POC and LVI circuit voltage detection, and each item of hardware is set to the status shown in Table 14-1. Each pin is high impedance during reset signal generation or during the oscillation stabilization time just after reset release, except for P130, which is low-level output.

When a low level is input to the  $\overline{\text{RESET}}$  pin, a reset occurs, and when a high level is input to the  $\overline{\text{RESET}}$  pin, the reset is released and the CPU starts program execution after referencing the option byte (after the option byte is referenced and the clock oscillation stabilization time elapses if crystal/ceramic oscillation is selected). A reset generated by the watchdog timer source is automatically released after the reset, and the CPU starts program execution after referencing the option byte (after the option byte is referenced and the clock oscillation stabilization time elapses if crystal/ceramic oscillation is selected). (see **Figures 11-2 to 11-4**). Reset by POC and LVI circuit power supply detection is automatically released when  $V_{DD} > V_{POC}$  or  $V_{DD} > V_{LVI}$  after the reset, and the CPU starts program execution after referencing the option byte (after the option byte is referenced and the clock oscillation stabilization time elapses if crystal/ceramic oscillation is selected) (see **CHAPTER 12 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 13 LOW-VOLTAGE DETECTOR**).

- Cautions**
1. For an external reset, input a low level for 2  $\mu$ s or more to the  $\overline{\text{RESET}}$  pin.
  2. During reset signal generation, the system clock and low-speed internal oscillation clock stop oscillating.
  3. When the  $\overline{\text{RESET}}$  pin is used as an input-only port pin (P34), the PD78F9510, 78F9511, 78F9512 is reset if a low level is input to the  $\overline{\text{RESET}}$  pin after reset is released by the POC circuit and before the option byte is referenced again. The reset status is retained until a high level is input to the  $\overline{\text{RESET}}$  pin.



Figure 11-1. Block Diagram of Reset Function

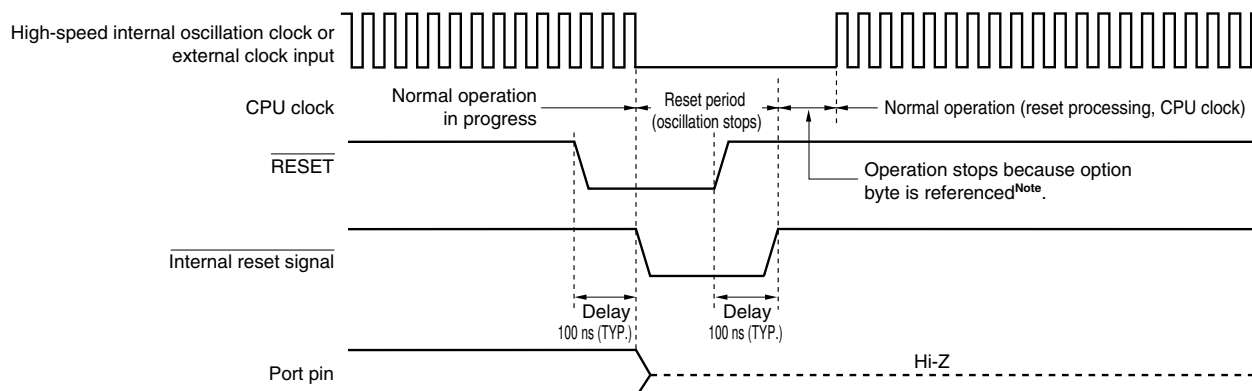


**Caution** The LVI circuit is not reset by the internal reset signal of the LVI circuit.

- Remarks**
1. LVIM: Low-voltage detect register
  2. LVIS: Low-voltage detection level select register

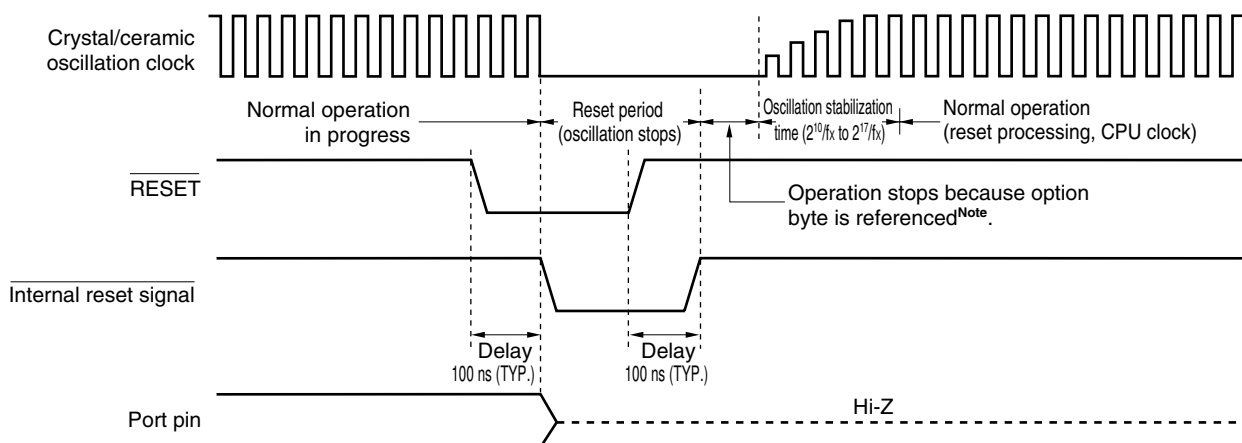
Figure 11-2. Timing of Reset by RESET Input

<1> With high-speed internal oscillation clock or external clock input



**Note** The operation stop time is 277 s (MIN.), 544 s (TYP.), and 1.075 ms (MAX.).

<2> With crystal/ceramic oscillation clock

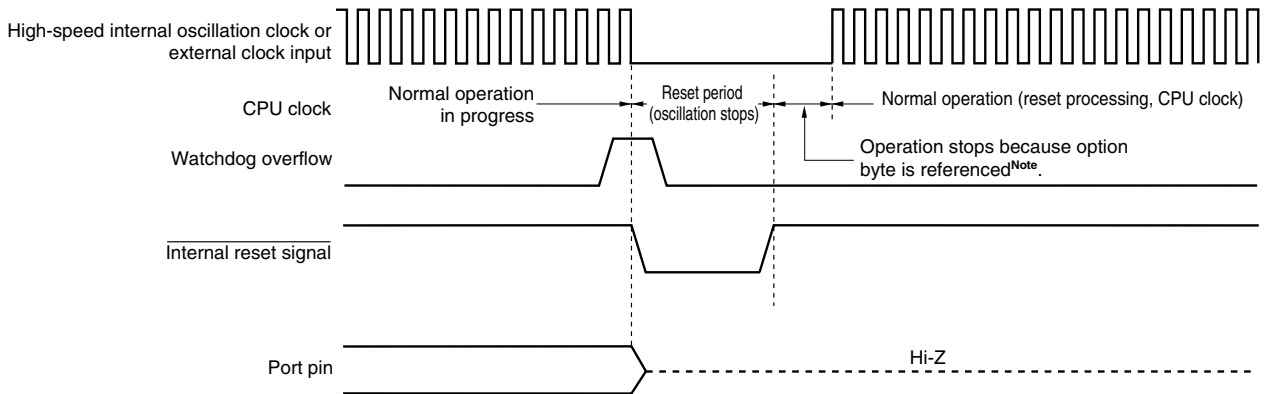


**Note** The operation stop time is 276 s (MIN.), 544 s (TYP.), and 1.074 ms (MAX.).

**Remark**  $f_x$ : System clock oscillation frequency

Figure 11-3. Timing of Reset by Overflow of Watchdog Timer

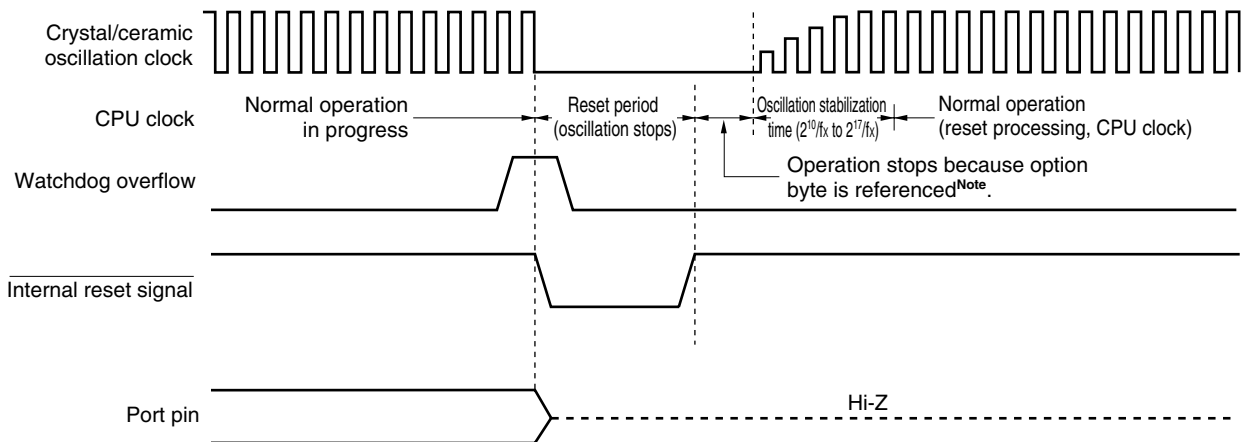
<1> With high-speed internal oscillation clock or external clock input



**Note** The operation stop time is 277  $\mu$ s (MIN.), 544  $\mu$ s (TYP.), and 1.075 ms (MAX.).

**Caution** The watchdog timer is also reset in the case of an internal reset of the watchdog timer.

<2> With crystal/ceramic oscillation clock



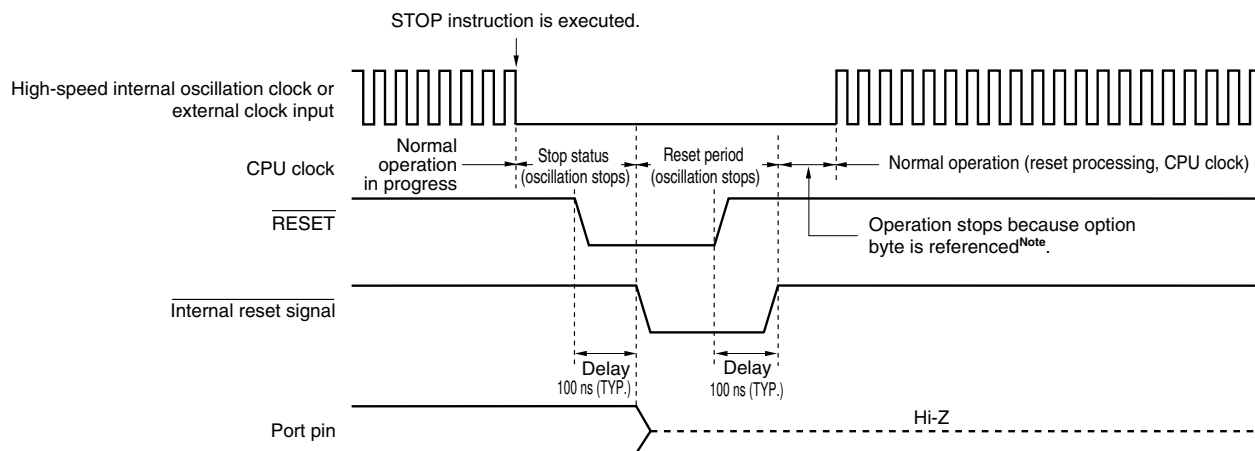
**Note** The operation stop time is 276  $\mu$ s (MIN.), 544  $\mu$ s (TYP.), and 1.074 ms (MAX.).

**Caution** The watchdog timer is also reset in the case of an internal reset of the watchdog timer.

**Remark** fx: System clock oscillation frequency

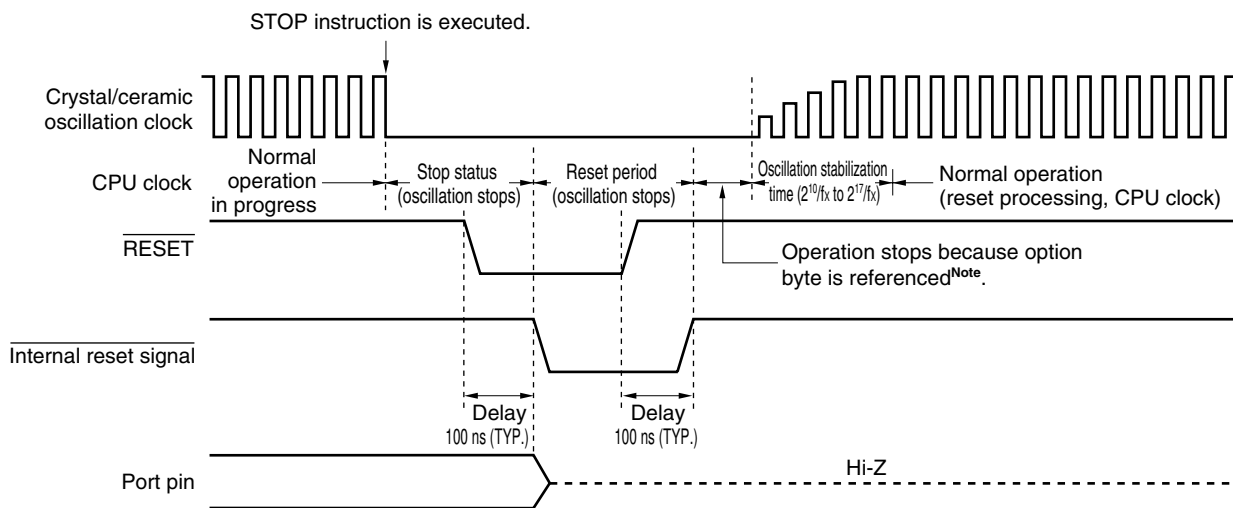
Figure 11-4. Reset Timing by RESET Input in STOP Mode

<1> With high-speed internal oscillation clock or external clock input



**Note** The operation stop time is 277  $\mu$ s (MIN.), 544  $\mu$ s (TYP.), and 1.075 ms (MAX.).

<2> With crystal/ceramic oscillation clock



**Note** The operation stop time is 276  $\mu$ s (MIN.), 544  $\mu$ s (TYP.), and 1.074 ms (MAX.).

**Remarks 1.** For the reset timing of the power-on-clear circuit and low-voltage detector, refer to **CHAPTER 12 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 13 LOW-VOLTAGE DETECTOR**.

**2.**  $f_x$ : System clock oscillation frequency

Table 11-1. Hardware Statuses After Reset Acknowledgment (1/2)

Hardware		Status After Reset
Program counter (PC) <sup>Note 1</sup>		Contents of reset vector table (0000H and 0001H) are set.
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined <sup>Note 2</sup>
	General-purpose registers	Undefined <sup>Note 2</sup>
Ports (P2 to P4) (output latches)		00H
Port mode registers (PM2 to PM4)		FFH
Pull-up resistor option registers (PU2 to PU4)		00H
Processor clock control register (PCC)		02H
Preprocessor clock control register (PPCC)		02H
Low-speed internal oscillation mode register (LSRCM)		00H
Oscillation stabilization time select register (OSTS)		Undefined
16-bit timer 00	Timer counter 00 (TM00)	0000H
	Capture/compare registers 000, 010 (CR000, CR010)	0000H
	Mode control register 00 (TMC00)	00H
	Prescaler mode register 00 (PRM00)	00H
	Capture/compare control register 00 (CRC00)	00H
	Timer output control register 00 (TOC00)	00H
8-bit timer H1	Compare registers (CMP01, CMP11)	00H
	Mode register 1 (TMHMD1)	00H
Watchdog timer	Mode register (WDTM)	67H
	Enable register (WDTE)	9AH

- Notes**
1. Only the contents of PC are undefined while reset signal generation and while the oscillation stabilization time elapses. The statuses of the other hardware units remain unchanged.
  2. The status after reset is held in the standby mode.

**Table 11-1. Hardware Statuses After Reset Acknowledgment (2/2)**

Hardware		Status After Reset
Reset function	Reset control flag register (RESF)	00H <sup>Note</sup>
Low-voltage detector	Low-voltage detection register (LVIM)	00H <sup>Note</sup>
	Low-voltage detection level select register (LVIS)	00H <sup>Note</sup>
Interrupt	Request flag registers (IF0)	00H
	Mask flag registers (MK0)	FFH
	External interrupt mode registers (INTM0)	00H
Flash memory	Flash protect command register (PFCMD)	Undefined
	Flash status register (PFS)	00H
	Flash programming mode control register (FLPMC)	Undefined
	Flash programming command register (FLCMD)	00H
	Flash address pointer L (FLAPL)	Undefined
	Flash address pointer H (FLAPH)	
	Flash address pointer H compare register (FLAPHC)	00H
	Flash address pointer L compare register (FLAPLC)	00H
	Flash write buffer register (FLW)	00H

**Note** These values change as follows depending on the reset source.

Reset Source		$\overline{\text{RESET}}$ Input	Reset by POC	Reset by WDT	Reset by LVI
Register	RESF	Cleared (0)	Cleared (0)	Set (1)	Held
	WDTRF			Held	Set (1)
	LVIRF				
	LVIM	Cleared (00H)	Cleared (00H)	Cleared (00H)	Held
	LVIS				

### 11.1 Register for Confirming Reset Source

Many internal reset generation sources exist in the PD78F9510, 78F9511, 78F9512. The reset control flag register (RESF) is used to store which source has generated the reset request.

RESF can be read by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$  input, reset signal generation by power-on-clear (POC) circuit, and reading RESF clear RESF to 00H.

**Figure 11-5. Format of Reset Control Flag Register (RESF)**

Address: FF54H    After reset: 00H<sup>Note</sup>    R

Symbol	7	6	5	4	3	2	1	0
RESF	0	0	0	WDTRF	0	0	0	LVIRF

WDTRF	Internal reset request by watchdog timer (WDT)
0	Internal reset request is not generated, or RESF is cleared.
1	Internal reset request is generated.

LVIRF	Internal reset request by low-voltage detector (LVI)
0	Internal reset request is not generated, or RESF is cleared.
1	Internal reset request is generated.

**Note** The value after reset varies depending on the reset source.

**Caution** Do not read data by a 1-bit memory manipulation instruction.

The status of RESF when a reset request is generated is shown in Table 11-2.

**Table 11-2. RESF Status When Reset Request Is Generated**

Reset Source	$\overline{\text{RESET}}$ Input	Reset by POC	Reset by WDT	Reset by LVI
WDTRF	Cleared (0)	Cleared (0)	Set (1)	Held
LVIRF			Held	Set (1)

## CHAPTER 12 POWER-ON-CLEAR CIRCUIT

### 12.1 Functions of Power-on-Clear Circuit

The power-on-clear circuit (POC) has the following functions.

- Generates internal reset signal at power on.
- Compares supply voltage ( $V_{DD}$ ) and detection voltage ( $V_{POC} = 2.1\text{ V} \pm 0.1\text{ V}$ ), and generates internal reset signal when  $V_{DD} < V_{POC}$ .
- Compares supply voltage ( $V_{DD}$ ) and detection voltage ( $V_{POC} = 2.1\text{ V} \pm 0.1\text{ V}$ ), and releases internal reset signal when  $V_{DD} \geq V_{POC}$ .

**Cautions** 1. If an internal reset signal is generated in the POC circuit, the reset control flag register (RESF) is cleared to 00H.

2. Because the detection voltage ( $V_{POC}$ ) of the POC circuit is in a range of  $2.1\text{ V} \pm 0.1\text{ V}$ , use a voltage in the range of 2.2 to 5.5 V.

**Remark** This product incorporates multiple hardware functions that generate an internal reset signal. A flag that indicates the reset cause is located in the reset control flag register (RESF) for when an internal reset signal is generated by the watchdog timer (WDT) or low-voltage-detection (LVI) circuit. RESF is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by WDT or LVI.

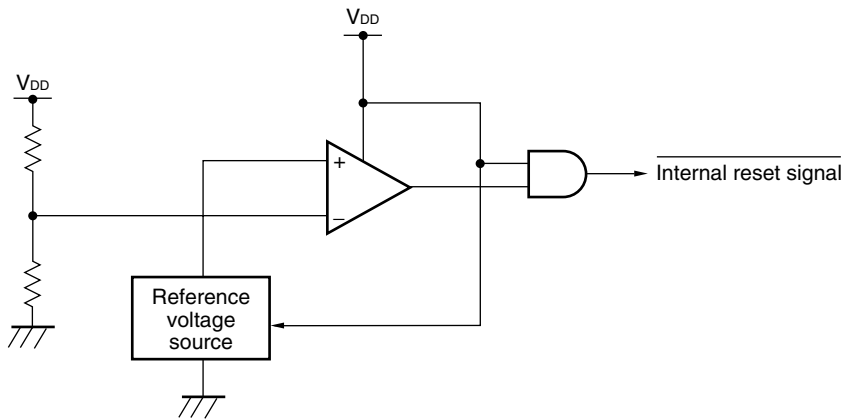
For details of RESF, see **CHAPTER 11 RESET FUNCTION**.



## 12.2 Configuration of Power-on-Clear Circuit

The block diagram of the power-on-clear circuit is shown in Figure 12-1.

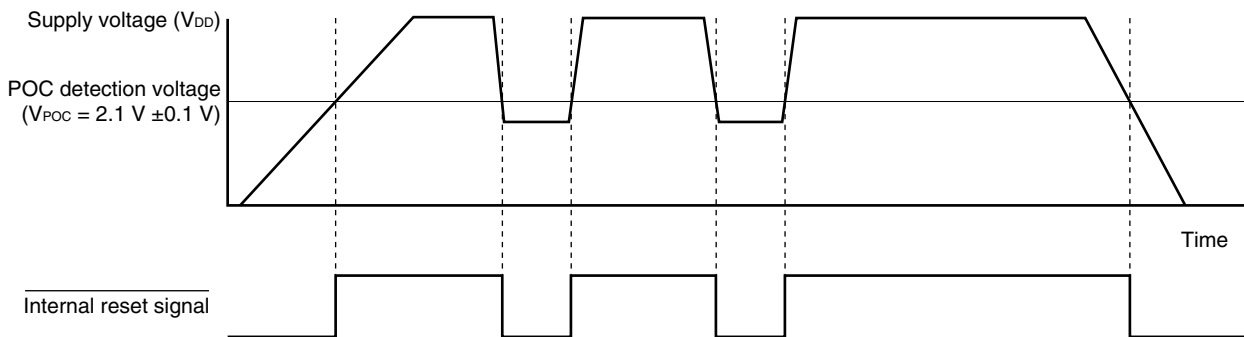
Figure 12-1. Block Diagram of Power-on-Clear Circuit



## 12.3 Operation of Power-on-Clear Circuit

In the power-on-clear circuit, the supply voltage ( $V_{DD}$ ) and detection voltage ( $V_{POC} = 2.1 \text{ V} \pm 0.1 \text{ V}$ ) are compared, and an internal reset signal is generated when  $V_{DD} < V_{POC}$ , and an internal reset is released when  $V_{DD} \geq V_{POC}$ .

Figure 12-2. Timing of Internal Reset Signal Generation in Power-on-Clear Circuit



### 12.4 Cautions for Power-on-Clear Circuit

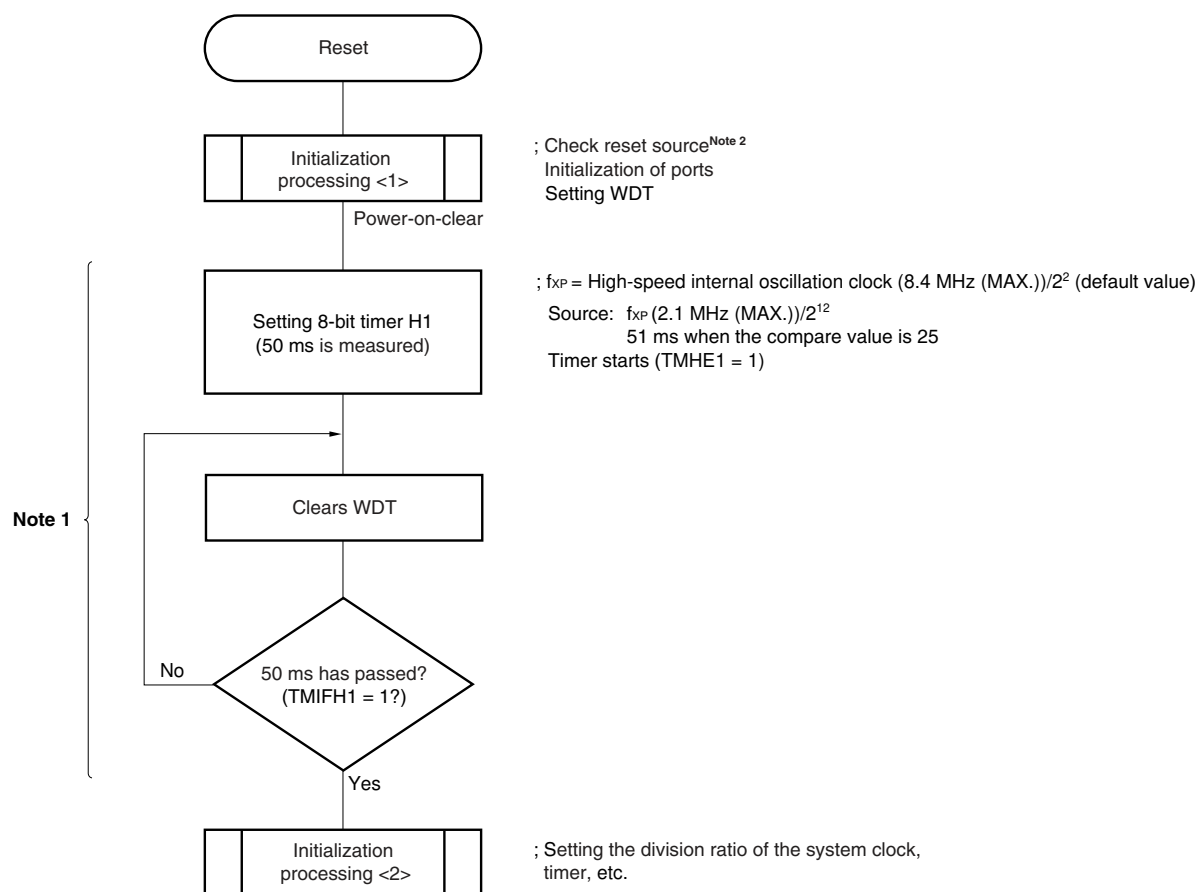
In a system where the supply voltage ( $V_{DD}$ ) fluctuates for a certain period in the vicinity of the POC detection voltage ( $V_{POC}$ ), the system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking the following action.

<Action>

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports.

**Figure 12-3. Example of Software Processing After Release of Reset (1/2)**

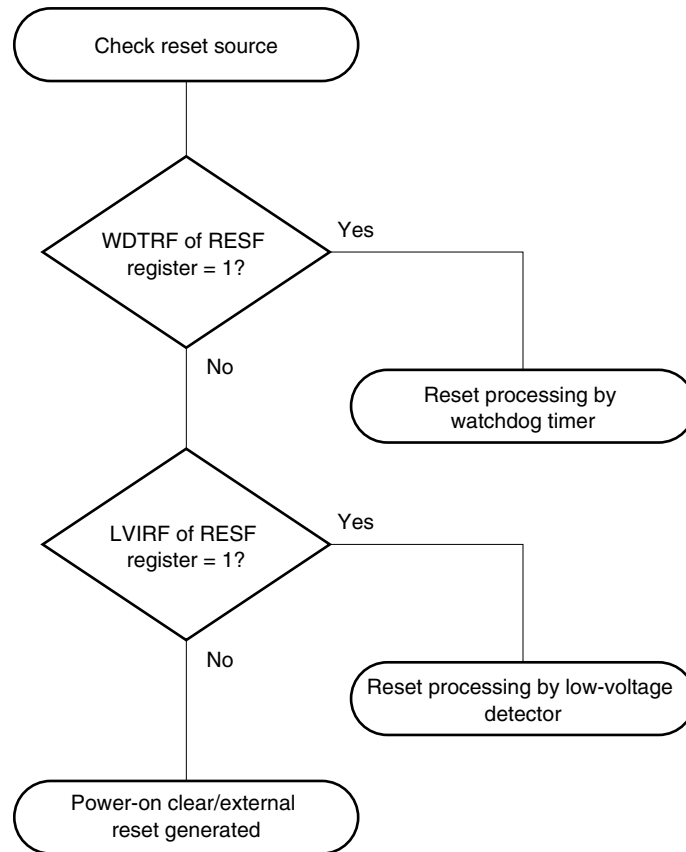
- If supply voltage fluctuation is 50 ms or less in vicinity of POC detection voltage



- Notes**
1. If reset is generated again during this period, initialization processing <2> is not started.
  2. A flowchart is shown on the next page.

Figure 12-3. Example of Software Processing After Release of Reset (2/2)

- Checking reset cause



## CHAPTER 13 LOW-VOLTAGE DETECTOR

### 13.1 Functions of Low-Voltage Detector

The low-voltage detector (LVI) has following functions.

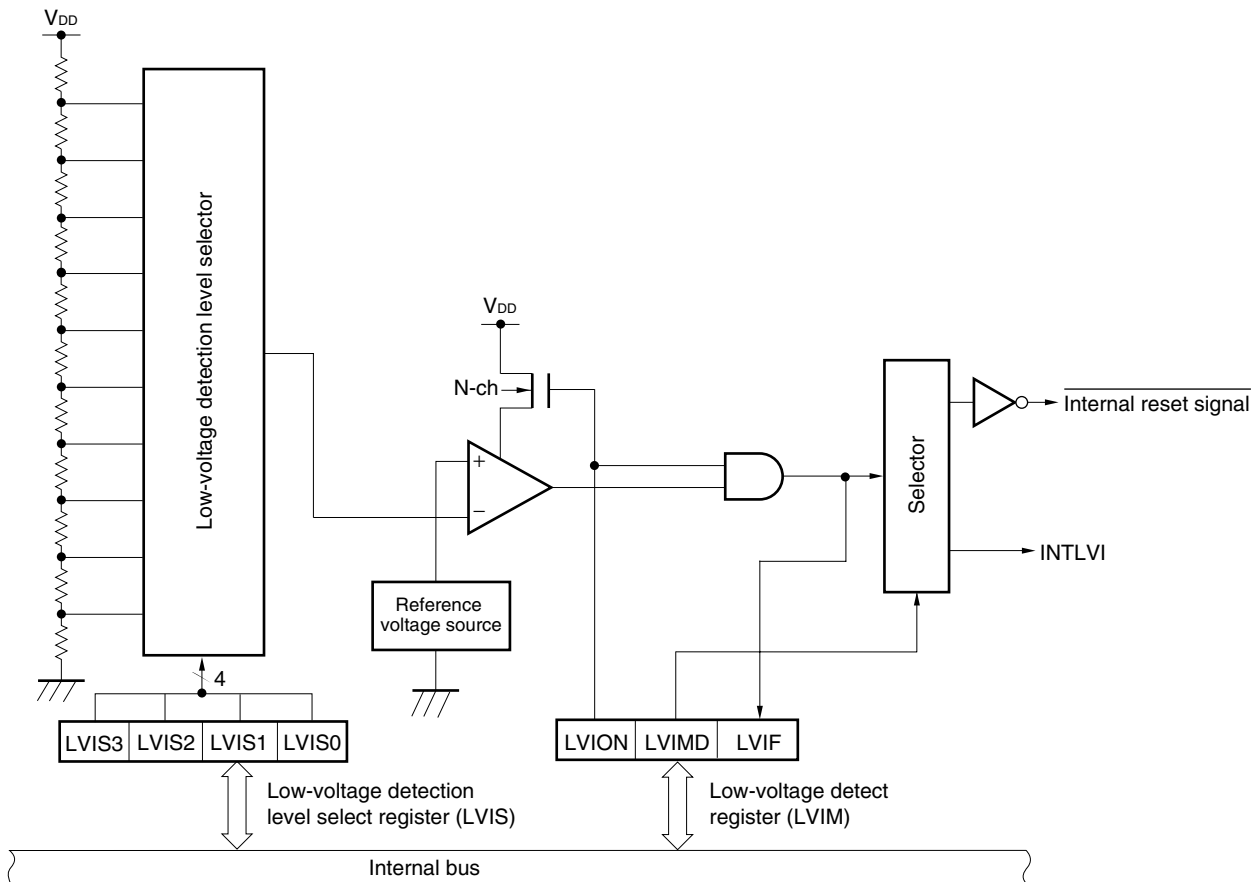
- Compares supply voltage ( $V_{DD}$ ) and detection voltage ( $V_{LVI}$ ), and generates an internal interrupt signal or internal reset signal when  $V_{DD} < V_{LVI}$ .
- Detection levels (ten levels) of supply voltage can be changed by software.
- Interrupt or reset function can be selected by software.
- Operable in STOP mode.

When the low-voltage detector is used to reset, bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of RESF, refer to **CHAPTER 11 RESET FUNCTION**.

### 13.2 Configuration of Low-Voltage Detector

The block diagram of the low-voltage detector is shown in Figure 13-1.

Figure 13-1. Block Diagram of Low-Voltage Detector



### 13.3 Registers Controlling Low-Voltage Detector

The low-voltage detector is controlled by the following registers.

- Low-voltage detect register (LVIM)
- Low-voltage detection level select register (LVIS)

#### (1) Low-voltage detect register (LVIM)

This register sets low-voltage detection and the operation mode.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H<sup>Note 1</sup>.

**Figure 13-2. Format of Low-Voltage Detect Register (LVIM)**

Address: FF50H After reset: 00H<sup>Note 1</sup> R/W<sup>Note 2</sup>

Symbol	<7>	6	5	4	3	2	<1>	<0>
LVIM	LVION	0	0	0	0	0	LVIMD	LVIF

LVION <sup>Note 3</sup>	Enabling low-voltage detection operation
0	Disable operation
1	Enable operation

LVIMD	Low-voltage detection operation mode selection
0	Generate interrupt signal when supply voltage ( $V_{DD}$ ) < detection voltage ( $V_{LVI}$ )
1	Generate internal reset signal when supply voltage ( $V_{DD}$ ) < detection voltage ( $V_{LVI}$ )

LVIF <sup>Note 4</sup>	Low-voltage detection flag
0	Supply voltage ( $V_{DD}$ ) $\geq$ detection voltage ( $V_{LVI}$ ), or when operation is disabled
1	Supply voltage ( $V_{DD}$ ) < detection voltage ( $V_{LVI}$ )

- Notes**
1. For a reset by LVI, the value of LVIM is not initialized.
  2. Bit 0 is a read-only bit.
  3. When LVION is set to 1, operation of the comparator in the LVI circuit is started. Use software to instigate a wait of at least 0.2 ms from when LVION is set to 1 until the voltage is confirmed at LVIF.
  4. The value of LVIF is output as the interrupt request signal INTLVI when LVION = 1 and LVIMD = 0.

- Cautions**
1. To stop LVI, follow either of the procedures below.
    - When using 8-bit manipulation instruction: Write 00H to LVIM.
    - When using 1-bit memory manipulation instruction: Clear LVION to 0.
  2. Be sure to set bits 2 to 6 to 0.

**(2) Low-voltage detection level select register (LVIS)**

This register selects the low-voltage detection level.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H<sup>Note</sup>.

**Figure 13-3. Format of Low-Voltage Detection Level Select Register (LVIS)**

Address: FF51H, After reset: 00H<sup>Note</sup> R/W

Symbol	7	6	5	4	3	2	1	0
LVIS	0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0

LVIS3	LVIS2	LVIS1	LVIS0	Detection level
0	0	0	0	V <sub>LV10</sub> (4.3 V ±0.2 V)
0	0	0	1	V <sub>LV11</sub> (4.1 V ±0.2 V)
0	0	1	0	V <sub>LV12</sub> (3.9 V ±0.2 V)
0	0	1	1	V <sub>LV13</sub> (3.7 V ±0.2 V)
0	1	0	0	V <sub>LV14</sub> (3.5 V ±0.2 V)
0	1	0	1	V <sub>LV15</sub> (3.3 V ±0.15 V)
0	1	1	0	V <sub>LV16</sub> (3.1 V ±0.15 V)
0	1	1	1	V <sub>LV17</sub> (2.85 V ±0.15 V)
1	0	0	0	V <sub>LV18</sub> (2.6 V ±0.1 V)
1	0	0	1	V <sub>LV19</sub> (2.35 V ±0.1 V)
Other than above				Setting prohibited

**Note** For a reset by LVI, the value of LVIS is not initialized.

**Cautions** 1. Bits 4 to 7 must be set to 0.

2. If a value other than the above is written during LVI operation, the value becomes undefined at the very moment it is written, and thus be sure to stop LVI (bit 7 of LVIM register (LVION) = 0) before writing.

### 13.4 Operation of Low-Voltage Detector

The low-voltage detector can be used in the following two modes.

- Used as reset  
Compares the supply voltage ( $V_{DD}$ ) and detection voltage ( $V_{LVI}$ ), and generates an internal reset signal when  $V_{DD} < V_{LVI}$ , and releases internal reset when  $V_{DD} \geq V_{LVI}$ .
- Used as interrupt  
Compares the supply voltage ( $V_{DD}$ ) and detection voltage ( $V_{LVI}$ ), and generates an interrupt signal (INTLVI) when  $V_{DD} < V_{LVI}$ .

The operation is set as follows.

#### (1) When used as reset

- When starting operation
  - <1> Mask the LVI interrupt ( $LVIMK = 1$ ).
  - <2> Set the detection voltage using bits 3 to 0 ( $LVIS3$  to  $LVIS0$ ) of the low-voltage detection level select register ( $LVIS$ ).
  - <3> Set bit 7 ( $LVION$ ) of  $LVIM$  to 1 (enables LVI operation).
  - <4> Use software to instigate a wait of at least 0.2 ms.
  - <5> Wait until “supply voltage ( $V_{DD}$ )  $\geq$  detection voltage ( $V_{LVI}$ )” at bit 0 ( $LVIF$ ) of  $LVIM$  is confirmed.
  - <6> Set bit 1 ( $LVIMD$ ) of  $LVIM$  to 1 (generates internal reset signal when supply voltage ( $V_{DD}$ ) < detection voltage ( $V_{LVI}$ )).

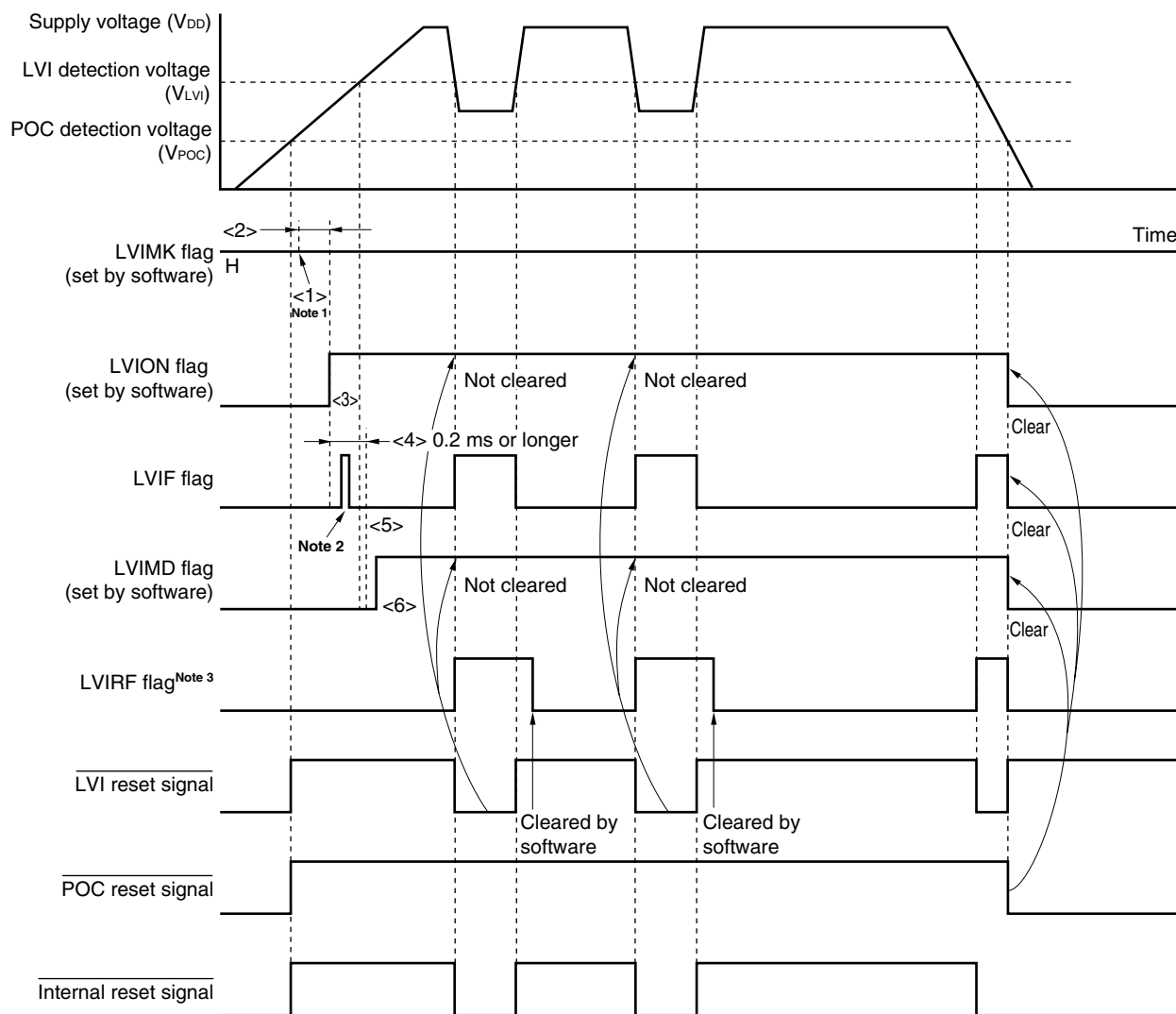
Figure 13-4 shows the timing of generating the internal reset signal of the low-voltage detector. Numbers <1> to <6> in this figure correspond to <1> to <6> above.

**Cautions 1.** <1> must always be executed. When  $LVIMK = 0$ , an interrupt may occur immediately after the processing in <3>.

**2.** If supply voltage ( $V_{DD}$ )  $\geq$  detection voltage ( $V_{LVI}$ ) when  $LVIMD$  is set to 1, an internal reset signal is not generated.

- When stopping operation  
Either of the following procedures must be executed.
  - When using 8-bit memory manipulation instruction: Write 00H to  $LVIM$ .
  - When using 1-bit memory manipulation instruction: Clear  $LVIMD$  to 0 and  $LVION$  to 0 in that order.

Figure 13-4. Timing of Low-Voltage Detector Internal Reset Signal Generation



- Notes**
1. The LVIMK flag is set to "1" by reset signal generation.
  2. The LVIF flag may be set (1).
  3. LVIRF is bit 0 of the reset control flag register (RESF). For details of RESF, refer to **CHAPTER 11 RESET FUNCTION**.

**Remark** <1> to <6> in Figure 13-4 above correspond to <1> to <6> in the description of "when starting operation" in **13.4 (1) When used as reset**.



**(2) When used as interrupt**

- When starting operation

- <1> Mask the LVI interrupt (LVIMK = 1).
- <2> Set the detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level select register (LVIS).
- <3> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).
- <4> Use software to instigate a wait of at least 0.2 ms.
- <5> Wait until “supply voltage ( $V_{DD}$ )  $\geq$  detection voltage ( $V_{LVI}$ )” at bit 0 (LVIF) of LVIM is confirmed.
- <6> Clear the interrupt request flag of LVI (LVIIF) to 0.
- <7> Release the interrupt mask flag of LVI (LVIMK).
- <8> Execute the EI instruction (when vector interrupts are used).

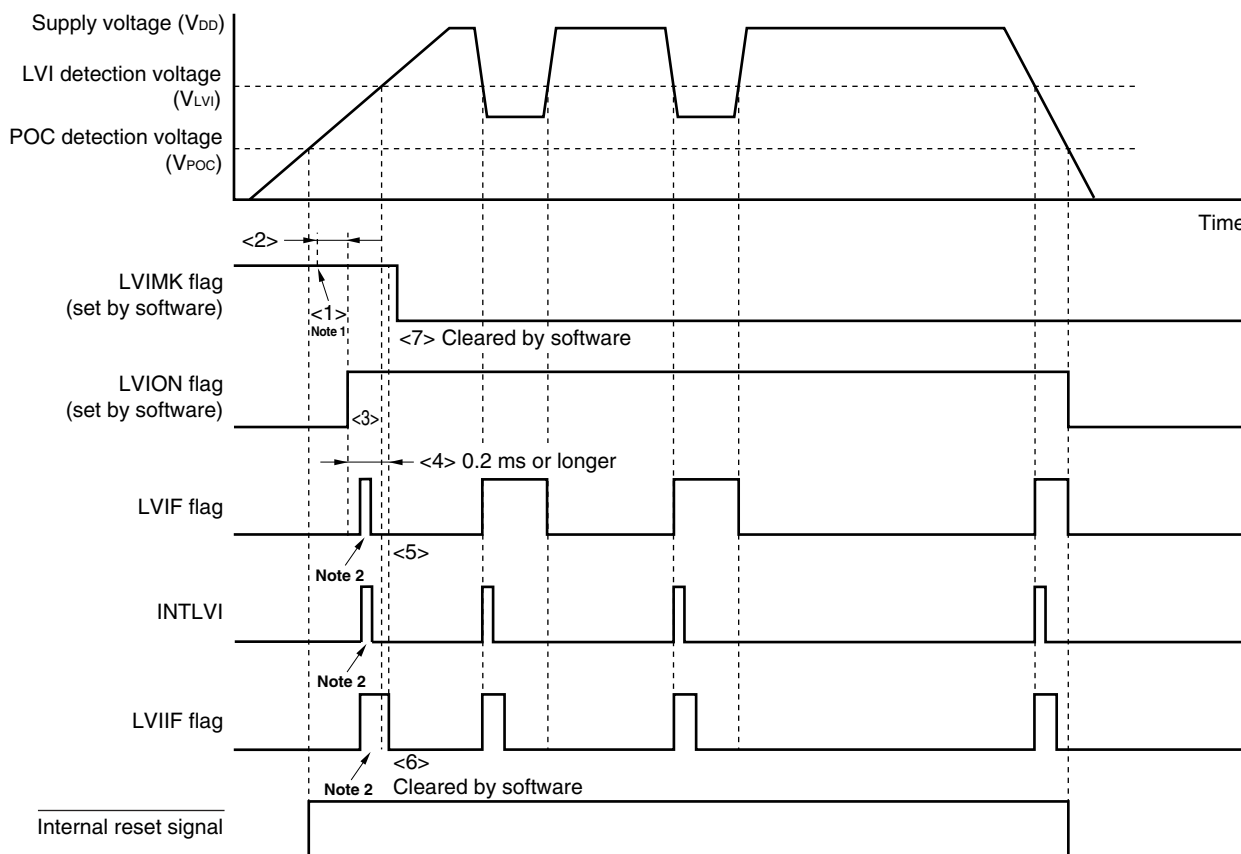
Figure 13-5 shows the timing of generating the interrupt signal of the low-voltage detector. Numbers <1> to <7> in this figure correspond to <1> to <7> above.

- When stopping operation

Either of the following procedures must be executed.

- When using 8-bit memory manipulation instruction: Write 00H to LVIM.
- When using 1-bit memory manipulation instruction: Clear LVION to 0.

Figure 13-5. Timing of Low-Voltage Detector Interrupt Signal Generation



- Notes**
1. The LVIMK flag is set to "1" by reset signal generation.
  2. An interrupt request signal (INTLVI) may be generated, and the LVIF and LVIIF flags may be set to 1.

**Remark**  $<1>$  to  $<7>$  in Figure 13-5 above correspond to  $<1>$  to  $<7>$  in the description of "when starting operation" in 13.4 (2) **When used as interrupt**.

### 13.5 Cautions for Low-Voltage Detector

In a system where the supply voltage ( $V_{DD}$ ) fluctuates for a certain period in the vicinity of the LVI detection voltage ( $V_{LVI}$ ), the operation is as follows depending on how the low-voltage detector is used.

#### <1> When used as reset

The system may be repeatedly reset and released from the reset status.

In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking action (1) below.

#### <2> When used as interrupt

Interrupt requests may be frequently generated. Take (b) of action (2) below.

In this system, take the following actions.

<Action>

#### (1) When used as reset

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports (see **Figure 13-6**).

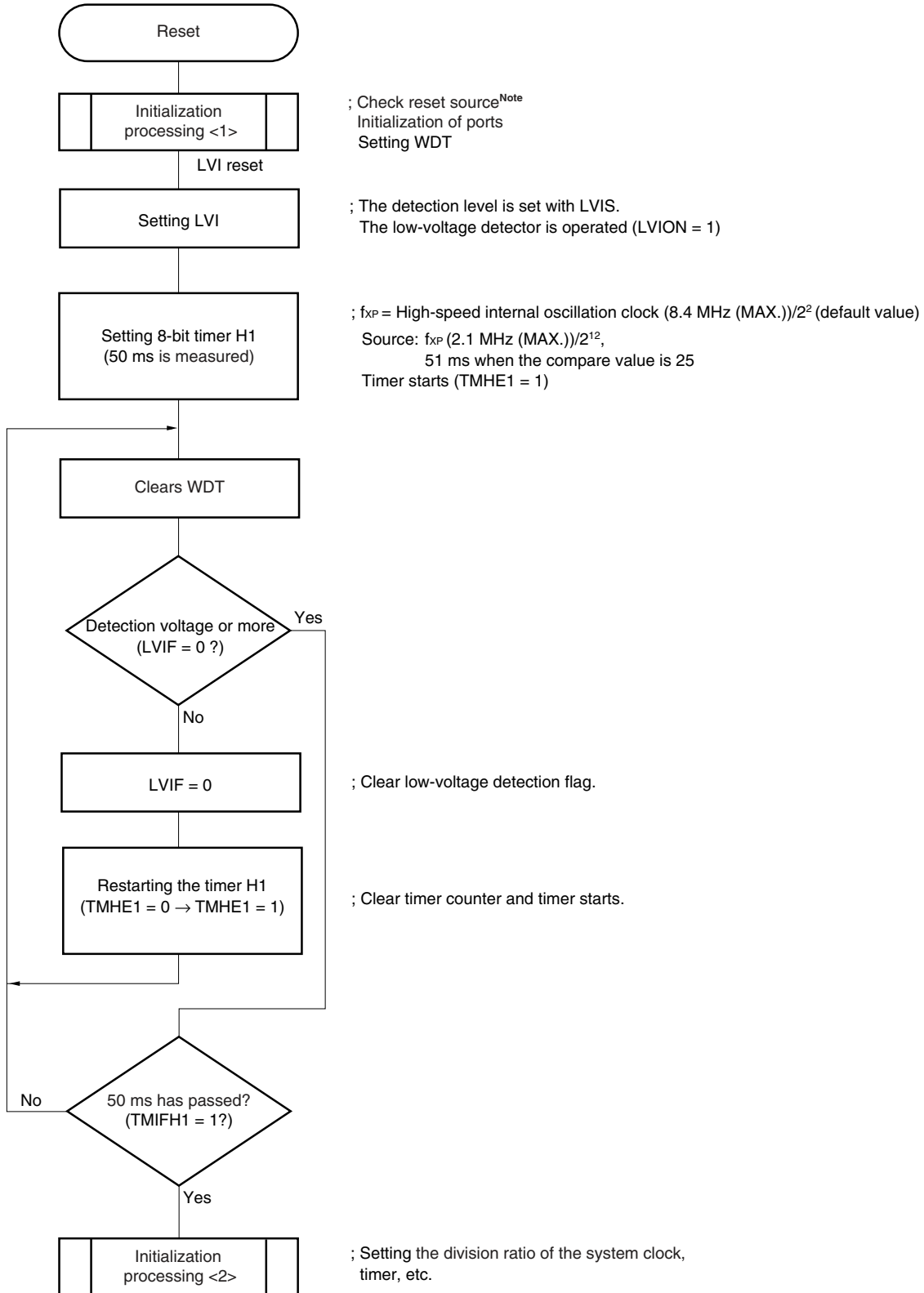
#### (2) When used as interrupt

- (a) Perform the processing<sup>Note</sup> for low voltage detection. Check that “supply voltage ( $V_{DD}$ )  $\geq$  detection voltage ( $V_{LVI}$ )” in the servicing routine of the LVI interrupt by using bit 0 (LVIF) of the low-voltage detection register (LVIM). Clear bit 1 (LVIIF) of interrupt request flag register 0 (IF0) to 0.
- (b) In a system where the supply voltage fluctuation period is long in the vicinity of the LVI detection voltage, wait for the supply voltage fluctuation period, check that “supply voltage ( $V_{DD}$ )  $\geq$  detection voltage ( $V_{LVI}$ )” using the LVIF flag and clear LVIIF flag to 0.

**Note** For low voltage detection processing, the CPU clock speed is switched to slow speed, etc.

Figure 13-6. Example of Software Processing After Release of Reset (1/2)

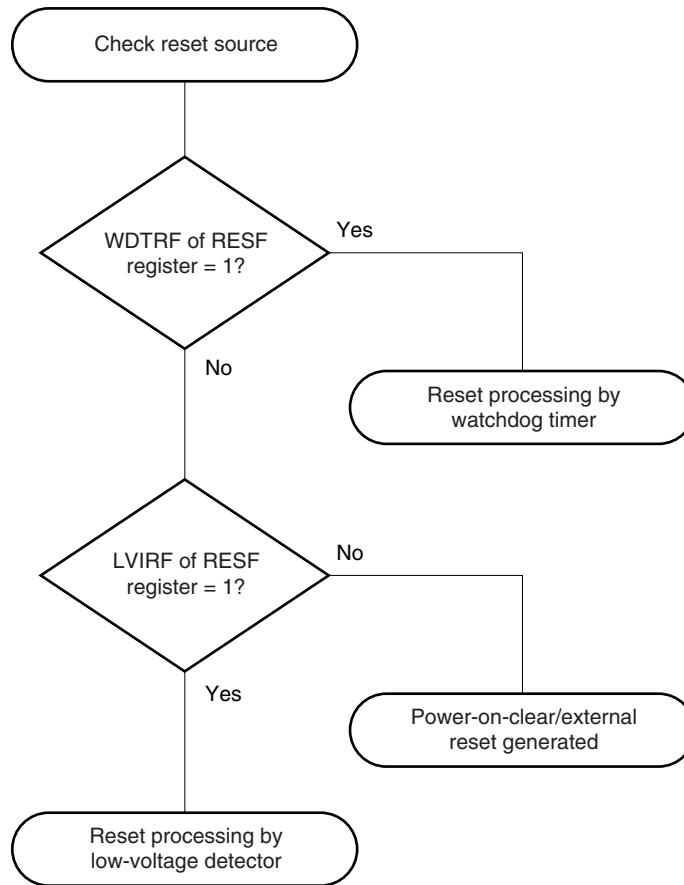
- If supply voltage fluctuation is 50 ms or less in vicinity of LVI detection voltage



**Note** A flowchart is shown on the next page.

Figure 13-6. Example of Software Processing After Release of Reset (2/2)

- Checking reset source



## CHAPTER 14 OPTION BYTE

### 14.1 Functions of Option Byte

The address 0080H of the flash memory of the  $\mu$ PD78F9510, 78F9511, 78F9512 is an option byte area. When power is supplied or when starting after a reset, the option byte is automatically referenced, and settings for the specified functions are performed. When using the product, be sure to set the following functions by using the option byte.

**(1) Selection of system clock source**

- High-speed internal oscillation clock
- Crystal/ceramic oscillation clock
- External clock input

**(2) Low-speed internal oscillation clock oscillation**

- Cannot be stopped.
- Can be stopped by software.

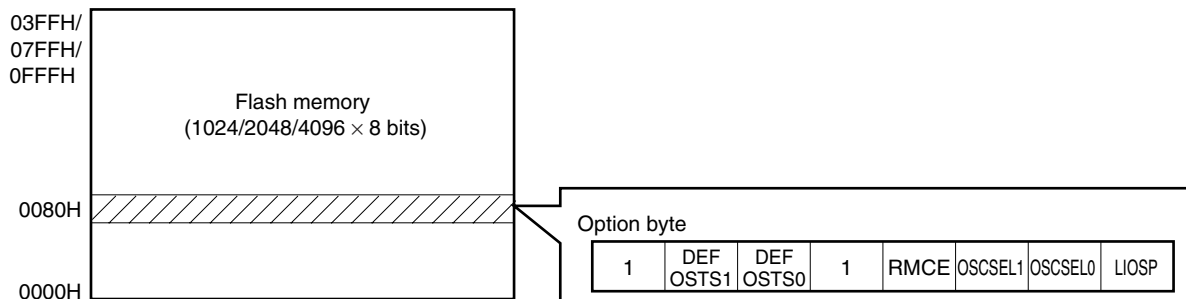
**(3) Control of  $\overline{\text{RESET}}$  pin**

- Used as  $\overline{\text{RESET}}$  pin
- $\overline{\text{RESET}}$  pin is used as an input port pin (P34) (refer to **14.3 Caution When the  $\overline{\text{RESET}}$  Pin Is Used as an Input-Only Port Pin (P34)**).

**(4) Oscillation stabilization time on power application or after reset release**

- $2^{10}/f_x$
- $2^{12}/f_x$
- $2^{15}/f_x$
- $2^{17}/f_x$

**Figure 14-1. Positioning of Option Byte**



## 14.2 Format of Option Byte

Format of option bytes is shown below.

Figure 14-2. Format of Option Byte (1/2)

Address: 0080H

7	6	5	4	3	2	1	0
1	DEFOSTS1	DEFOSTS0	1	RMCE	OSCSEL1	OSCSEL0	LIOCP

DEFOSTS1	DEFOSTS0	Oscillation stabilization time on power application or after reset release
0	0	$2^{10}/f_x$ (102.4 $\mu$ s)
0	1	$2^{12}/f_x$ (409.6 $\mu$ s)
1	0	$2^{15}/f_x$ (3.27 ms)
1	1	$2^{17}/f_x$ (13.1 ms)

**Caution** The setting of this option is valid only when the crystal/ceramic oscillation clock is selected as the system clock source. No wait time elapses if the high-speed internal oscillation clock or external clock input is selected as the system clock source.

RMCE	Control of $\overline{\text{RESET}}$ pin
1	$\overline{\text{RESET}}$ pin is used as is.
0	$\overline{\text{RESET}}$ pin is used as input port pin (P34).

**Caution** Because the option byte is referenced after reset release, if a low level is input to the  $\overline{\text{RESET}}$  pin before the option byte is referenced, then the reset state is not released.

Also, when setting 0 to RMCE, connect the pull-up resistor.

OSCSEL1	OSCSEL0	Selection of system clock source
0	0	Crystal/ceramic oscillation clock
0	1	External clock input
1	×	High-speed internal oscillation clock

**Caution** Because the X1 and X2 pins are also used as the P23 and P22 pins, the conditions under which the X1 and X2 pins can be used differ depending on the selected system clock source.

(1) Crystal/ceramic oscillation clock is selected

The X1 and X2 pins cannot be used as I/O port pins because they are used as clock input pins.

(2) External clock input is selected

Because the X1 pin is used as an external clock input pin, P23 cannot be used as an I/O port pin.

(3) High-speed internal oscillation clock is selected

P23 and P22 pins can be used as I/O port pins.

**Remark** × : don't care

Figure 14-2. Format of Option Byte (2/2)

LIOCP	Low-speed internal oscillates
1	Cannot be stopped (oscillation does not stop even if 1 is written to the LSRSTOP bit)
0	Can be stopped by software (oscillation stops when 1 is written to the LSRSTOP bit)

**Cautions 1.** If it is selected that low-speed internal oscillator cannot be stopped, the count clock to the watchdog timer (WDT) is fixed to low-speed internal oscillation clock.

- 2.** If it is selected that low-speed internal oscillator can be stopped by software, supply of the count clock to WDT is stopped in the HALT/STOP mode, regardless of the setting of bit 0 (LSRSTOP) of the low-speed internal oscillation mode register (LSRCM). Similarly, clock supply is also stopped when a clock other than the low-speed internal oscillation clock is selected as a count clock to WDT.

While the low-speed internal oscillator is operating (LSRSTOP = 0), the clock can be supplied to the 8-bit timer H1 even in the STOP mode.

**Remarks 1.** ( ):  $f_x = 10 \text{ MHz}$

- 2.** For the oscillation stabilization time of the resonator, refer to the characteristics of the resonator to be used.
- 3.** An example of software coding for setting the option bytes is shown below.

```
OPB CSEG AT 0080H
```

```
DB 10010001B ; Set to option byte
```

```
                ; Low-speed internal oscillator cannot be stopped
```

```
                ; The system clock is a crystal or ceramic resonator.
```

```
                ; The  $\overline{\text{RESET}}$  pin is used as an input-only port pin (P34).
```

```
                ; Minimum oscillation stabilization time ( $2^{10}/f_x$ )
```

- 4.** For details on the timing at which the option byte is referenced, see **CHAPTER 11 RESET FUNCTION**.

### 14.3 Caution When the $\overline{\text{RESET}}$ Pin Is Used as an Input-Only Port Pin (P34)

Be aware of the following when re-erasing/-writing (by on-board programming using a dedicated flash memory programmer) an already-written device which has been set as “The  $\overline{\text{RESET}}$  pin is used as an input-only port pin (P34)” by the option byte function.

Before supplying power to the target system, connect a dedicated flash memory programmer and turn its power on.

If the power is supplied to the target system beforehand, the flash memory programming mode cannot be switched to.



## CHAPTER 15 FLASH MEMORY

### 15.1 Features

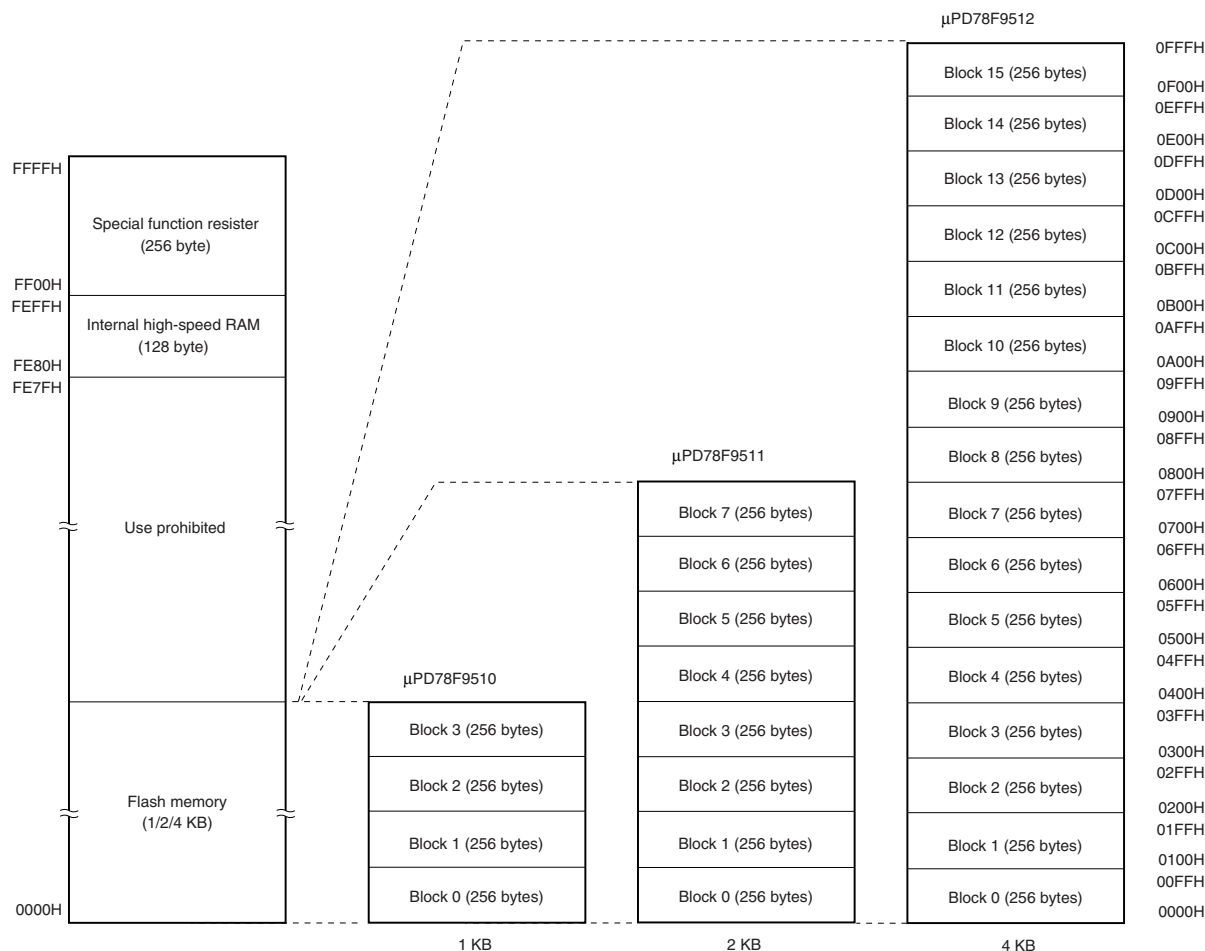
The internal flash memory of the  $\mu$ PD78F9510, 78F9511, 78F9512 has the following features.

- Erase/write even without preparing a separate dedicated power supply
- Capacity: 1/2/4 KB
  - Erase unit: 1 block (256 bytes)
  - Write unit: 1 block (at on-board/off-board programming time), 1 byte (at self programming time)
- Rewriting method
  - Rewriting by communication with dedicated flash memory programmer (on-board/off-board programming)
  - Rewriting flash memory by user program (self programming)
- Supports rewriting of the flash memory at on-board/off-board programming time through security functions
- Supports security functions in block units at self programming time through protect bytes

## 15.2 Memory Configuration

The 1/2/4 KB internal flash memory area is divided into 8/16 blocks and can be programmed/erased in block units. All the blocks can also be erased at once, by using a dedicated flash memory programmer.

Figure 15-1. Flash Memory Mapping



## 15.3 Functional Outline

The internal flash memory of the  $\mu$ PD78F9510, 78F9511, 78F9512 can be rewritten by using the rewrite function of the dedicated flash memory programmer, regardless of whether the  $\mu$ PD78F9510, 78F9511, 78F9512 has already been mounted on the target system or not (on-board/off-board programming).

The function for rewriting a program with the user program (self programming), which is ideal for an application when it is assumed that the program is changed after production/shipment of the target system, is provided.

Refer to Table 15-1 for the flash memory writing control function.

In addition, a security function that prohibits rewriting the user program written to the internal flash memory is also supported, so that the program cannot be changed by an unauthorized person.

Refer to **15.7.3 Security settings** for details on the security function.

Table 15-1. Rewrite Method

Rewrite Method	Functional Outline	Operation Mode
On-board programming	Flash memory can be rewritten after the device is mounted on the target system, by using a dedicated flash memory programmer.	Flash memory programming mode
Off-board programming	Flash memory can be rewritten before the device is mounted on the target system, by using a dedicated flash memory programmer and a dedicated program adapter board (FA series).	
Self programming	Flash memory can be rewritten by executing a user program that has been written to the flash memory in advance by means of on-board/off-board programming.	Self programming mode

- Remarks**
- The FA series is a product of Naito Densai Machida Mfg. Co., Ltd.
  - Refer to the following sections for details on the flash memory writing control function.
    - 15.7 On-Board and Off-Board Flash Memory Programming**
    - 15.8 Flash Memory Programming by Self Writing**

## 15.4 Writing with Flash Memory Programmer

The following two types of dedicated flash memory programmers can be used for writing data to the internal flash memory of the  $\mu$ PD78F9510, 78F9511, 78F9512.

- FlashPro4 (PG-FP4, FL-PR4)
- PG-FPL2

Data can be written to the flash memory on-board or off-board, by using a dedicated flash memory programmer.

### (1) On-board programming

The contents of the flash memory can be rewritten after the  $\mu$ PD78F9510, 78F9511, 78F9512 have been mounted on the target system. The connectors that connect the dedicated flash memory programmer and the test pad must be mounted on the target system. The test pad is required only when writing data with the crystal/ceramic resonator mounted (refer to Figure 15-6 for mounting of the test pad).

### (2) Off-board programming

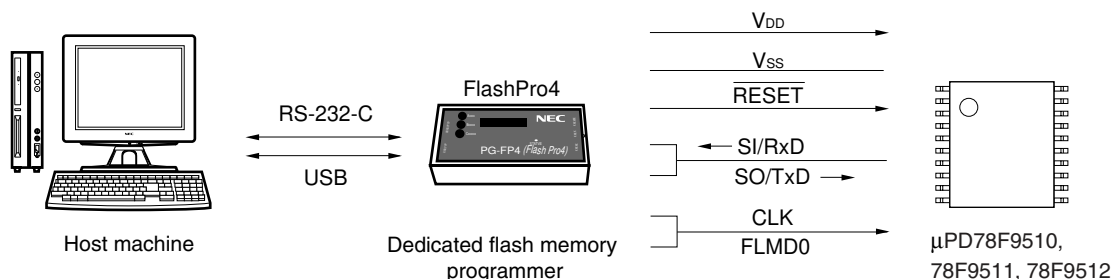
Data can be written to the flash memory with a dedicated program adapter (FA series) before the  $\mu$ PD78F9510, 78F9511, 78F9512 is mounted on the target system.

**Remark** The FL-PR4 and FA series are products of Naito Densai Machida Mfg. Co., Ltd.

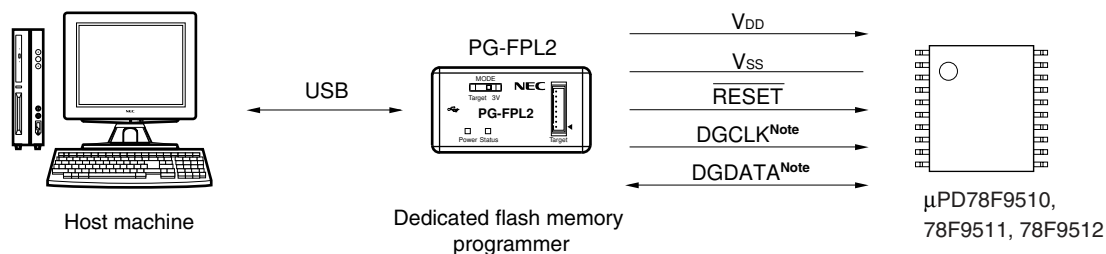
## 15.5 Programming Environment

The environment required for writing a program to the flash memory is illustrated below.

**Figure 15-2. Environment for Writing Program to Flash Memory (FlashPro4)**



**Figure 15-3. Environment for Writing Program to Flash Memory (PG-FPL2)**



**Note** DGCLK is a clock for communication, while DGDATA is a transmit/receive signal for communication data.

A host machine that controls the dedicated flash memory programmer is necessary. When using the PG-FP4 or FL-PR4, data can be written with just the dedicated flash memory programmer after downloading the program from the host machine.

UART is used for manipulation such as writing and erasing when interfacing between the dedicated flash memory programmer and the μPD78F9510, 78F9511, 78F9512. To write the flash memory off-board, a dedicated program adapter (FA series) is necessary.

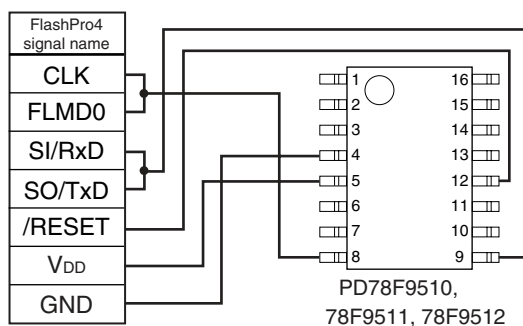
Download the latest programmer firmware, GUI, and parameter file from the download site for development tools (<http://www.necel.com/micro/ods/eng/index.html>).

**Table 15-2. Wiring Between PD78F9510, 78F9511, 78F9512 and FlashPro4**

FlashPro4 Connection Pin			PD78F9510, 78F9511, 78F9512 Connection Pin	
Pin Name	I/O	Pin Function	Pin Name	Pin No.
CLK <sup>Note</sup>	Output	Clock to PD78F9510, 78F9511, 78F9512	X1/P23	8
FLMD0 <sup>Note</sup>	Output	On-board mode signal		
SI/RxD <sup>Note</sup>	Input	Receive signal	X2/P22	9
SO/TxD <sup>Note</sup>	Output	Receive signal/on-board mode signal		
/RESET	Output	Reset signal	$\overline{\text{RESET}}$ /P34	12
V <sub>DD</sub>	–	V <sub>DD</sub> voltage generation/voltage monitor	V <sub>DD</sub>	5
GND	–	Ground	V <sub>SS</sub>	4

**Note** In the PD78F9510, 78F9511, 78F9512, the CLK and FLMD0 signals are connected to the X1 pin and the SI/RxD and SO/TxD signals to the X2 signal; therefore, these signals need to be directly connected.

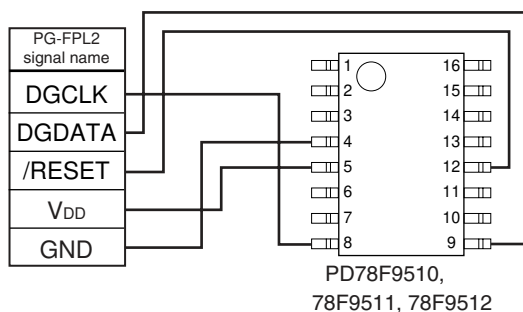
**Figure 15-4. Wiring diagram with FlashPro4**



**Table 15-3. Wiring Between PD78F9510, 78F9511, 78F9512 and PG-FPL2**

PG-FPL2 Connection Pin			PD78F9510, 78F9511, 78F9512 Connection Pin	
Pin Name	I/O	Pin Function	Pin Name	Pin No.
DGCLK	Output	Clock to PD78F9510, 78F9511, 78F9512	X1/P23	8
DGDATA	I/O	Transmit/receive signal, on-board mode signal	X2/P22	9
/RESET	Output	Reset signal	$\overline{\text{RESET}}$ /P34	12
V <sub>DD</sub>	–	V <sub>DD</sub> voltage generation	V <sub>DD</sub>	5
GND	–	Ground	V <sub>SS</sub>	4

**Figure 15-5. Wiring diagram with PG-FPL2**



## 15.6 Processing of Pins on Board

To write the flash memory on-board, connectors that connect the dedicated flash memory programmer must be provided on the target system. First provide a function that selects the normal operation mode or flash memory programming mode on the board.

When the flash memory programming mode is set, all the pins not used for programming the flash memory are in the same status as immediately after reset. Therefore, if the external device does not recognize the state immediately after reset, the pins must be processed as described below.

The state of the pins in the self programming mode is the same as that in the HALT mode.

### 15.6.1 X1 and X2 pins

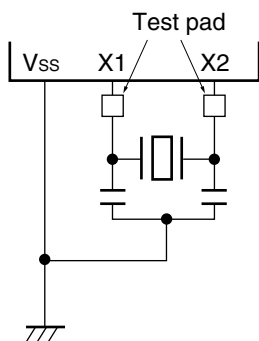
The X1 and X2 pins are used as the serial interface of flash memory programming. Therefore, if the X1 and X2 pins are connected to an external device, a signal conflict occurs. To prevent the conflict of signals, isolate the connection with the external device.

Similarly, when a capacitor is connected to the X1 and X2 pins, the waveform during communication is changed, and thus communication may be disabled depending on the capacitor capacitance. Make sure to isolate the connection with the capacitor during flash programming.

Perform the following processing (1) and (2) when on-board writing is performed with the resonator mounted, when it is difficult to isolate the resonator, while a crystal or ceramic resonator is selected as the system clock.

- (1) Mount the minimum-possible test pads between the device and the resonator, and connect the programmer via the test pad. Keep the wiring as short as possible (refer to **Figure 15-6** and **Table 15-4**).
- (2) Set the oscillation frequency of the communication clock for writing using the GUI software of the dedicated flash memory programmer. Research the series/parallel resonant and antiresonant frequencies of the resonator used, and set the oscillation frequency so that it is outside the range of the resonant frequency  $\pm 10\%$  (refer to **Figure 15-7** and **Table 15-5**).

**Figure 15-6. Example of Mounting Test Pads**



**Table 15-4. Clock to Be Used and Mounting of Test Pads**

Clock to Be Used		Mounting of Test Pads
High-speed internal oscillation clock		Not required
External clock		
Crystal/ceramic oscillation clock	Before resonator is mounted	Required
	After resonator is mounted	

Figure 15-7. PG-FP4 GUI Software Setting Example

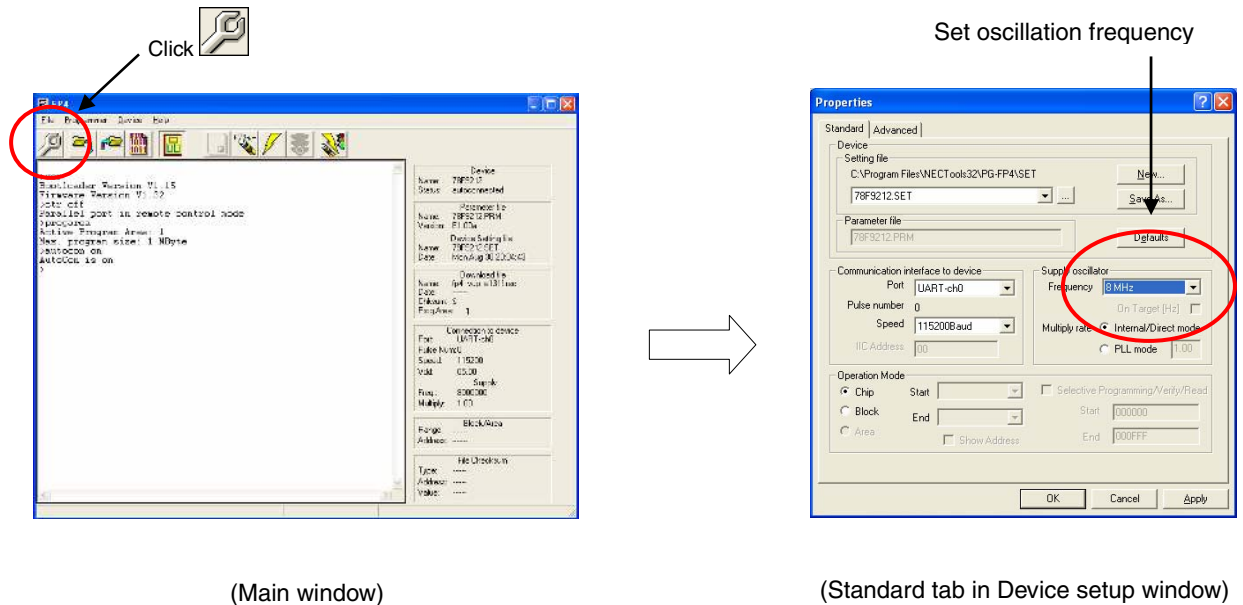


Table 15-5. Oscillation Frequency and PG-FP4 GUI Software Setting Value Example

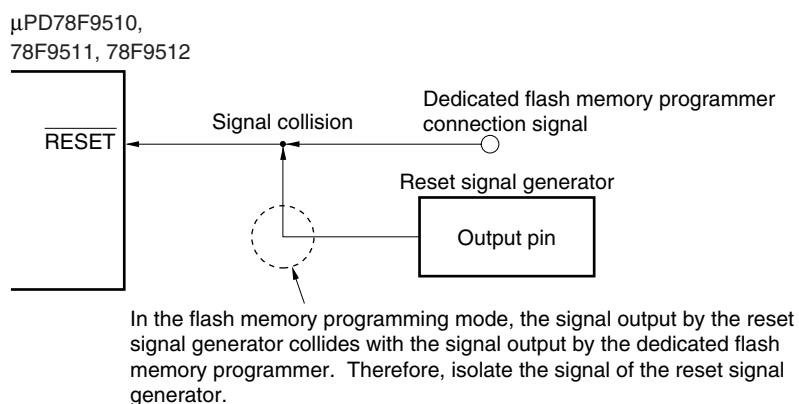
Oscillation Frequency	PG-FP4 GUI Software Setting Value Example (Communication Frequency)
$1 \text{ MHz} \leq f_x < 4 \text{ MHz}$	8 MHz
$4 \text{ MHz} \leq f_x < 8 \text{ MHz}$	9 MHz
$8 \text{ MHz} \leq f_x < 9 \text{ MHz}$	10 MHz
$9 \text{ MHz} \leq f_x \leq 10 \text{ MHz}$	8 MHz

**Caution** The above values are recommended values. Depending on the usage environment these values may change, so set them after having performed sufficient evaluations.

### 15.6.2 RESET pin

If the reset signal of the dedicated flash memory programmer is connected to the RESET pin that is connected to the reset signal generator on the board, signal collision takes place. To prevent this collision, isolate the connection with the reset signal generator.

If the reset signal is input from the user system while the flash memory programming mode is set, the flash memory will not be correctly programmed. Do not input any signal other than the reset signal of the dedicated flash memory programmer.

**Figure 15-8. Signal Collision ( $\overline{\text{RESET}}$  Pin)**

### 15.6.3 Port pins

When the flash memory programming mode is set, all the pins not used for flash memory programming enter the same status as that immediately after reset. If external devices connected to the ports do not recognize the port status immediately after reset, the port pin must be connected to  $V_{DD}$  or  $V_{SS}$  via a resistor.

The state of the pins in the self programming mode is the same as that in the HALT mode.

### 15.6.4 Power supply

Connect the  $V_{DD}$  pin to  $V_{DD}$  of the flash memory programmer, and the  $V_{SS}$  pin to  $V_{SS}$  of the flash memory programmer.



## 15.7 On-Board and Off-Board Flash Memory Programming

### 15.7.1 Flash memory programming mode

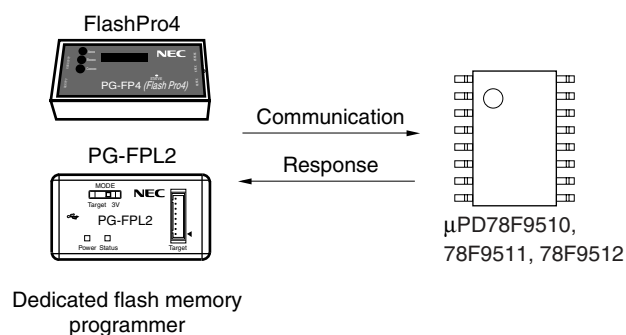
To rewrite the contents of the flash memory by using the dedicated flash memory programmer, set the  $\mu$ PD78F9510, 78F9511, 78F9512 in the flash memory programming mode. When the  $\mu$ PD78F9510, 78F9511, 78F9512 are connected to the flash memory programmer and a communication command is transmitted to the microcontroller, the microcontroller is set in the flash memory programming mode.

Change the mode by using a jumper when writing the flash memory on-board.

### 15.7.2 Communication commands

The dedicated flash memory programmer controls the  $\mu$ PD78F9510, 78F9511, 78F9512 by using commands. The signals sent from the flash memory programmer to the  $\mu$ PD78F9510, 78F9511, 78F9512 are called communication commands, and the commands sent from the  $\mu$ PD78F9510, 78F9511, 78F9512 to the dedicated flash memory programmer are called response.

**Figure 15-9. Communication Commands**



Communication commands are listed in the table below. All these communication commands are issued from the flash memory programmer and the  $\mu$ PD78F9510, 78F9511, 78F9512 perform processing corresponding to the respective communication commands.

**Table 15-6. Communication Commands**

Classification	Communication Command Name	Function
Erase	Batch erase (chip erase) command	Erases the contents of the entire memory
	Block erase command	Erases the contents of the memory of the specified block
Write	Write command	Writes to the specified address range and executes a verify check of the contents.
Checksum	Checksum command	Reads the checksum of the specified address range and compares with the written data.
Blank check	Blank check command	Confirms the erasure status of the entire memory.
Security	Security set command	Prohibits batch erase (chip erase) command, block erase command, and write command to prevent operation by third parties.

The  $\mu$ PD78F9510, 78F9511, 78F9512 returns a response for the communication command issued by the dedicated flash memory programmer. The response name sent from the  $\mu$ PD78F9510, 78F9511, 78F9512 are listed below.

Table 15-7. Response Name

Command Name	Function
ACK	Acknowledges command/data.
NAK	Acknowledges illegal command/data.

### 15.7.3 Security settings

The operations shown below can be prohibited using the security setting command.

- Batch erase (chip erase) is prohibited

Execution of the block erase and batch erase (chip erase) commands for entire blocks in the flash memory is prohibited. Once execution of the batch erase (chip erase) command is prohibited, all the prohibition settings can no longer be cancelled.

**Caution** After the security setting of the batch erase is set, erasure cannot be performed for the device. In addition, even if a write command is executed, data different from that which has already been written to the flash memory cannot be written because the erase command is disabled.

- Block erase is prohibited

Execution of the block erase command in the flash memory is prohibited. This prohibition setting can be cancelled using the batch erase (chip erase) command.

- Write is prohibited

Execution of the write and block erase commands for entire blocks in the flash memory is prohibited. This prohibition setting can be cancelled using the batch erase (chip erase) command.

**Remark** The security setting is valid when the programming mode is set next time.

The batch erase (chip erase), block erase, and write commands are enabled by the default setting when the flash memory is shipped. The above security settings are possible only for on-board/off-board programming. Each security setting can be used in combination.

Table 15-8 shows the relationship between the erase and write commands when the  $\mu$ PD78F9510, 78F9511, 78F9512 security function is enabled.

Table 15-8. Relationship Between Commands When Security Function Is Enabled

Security \ Command	Batch Erase (Chip Erase) Command	Block Erase Command	Write Command
When batch erase (chip erase) security operation is enabled	Disabled	Disabled	Enabled <sup>Note</sup>
When block erase security operation is enabled	Enabled		Enabled
When write security operation is enabled			Disabled

**Note** Since the erase command is disabled, data different from that which has already been written to the flash memory cannot be written.

Table 15-9 shows the relationship between the security setting and the operation in each programming mode.

**Table 15-9. Relationship Between Security Setting and Operation In Each Programming Mode**

Programming Mode \ Security Setting	On-Board/Off-Board Programming		Self Programming	
	Security Setting	Security Operation	Security Setting	Security Operation
Batch erase (chip erase)	Possible	Valid <sup>Note 1</sup>	Impossible	Invalid <sup>Note 2</sup>
Block erase				
Write				

- Notes**
1. Execution of each command is prohibited by the security setting.
  2. Execution of self programming command is possible regardless of the security setting.

### 15.8 Flash Memory Programming by Self Writing

The  $\mu$ PD78F9510, 78F9511, 78F9512 support a self programming function that can be used to rewrite the flash memory via a user program, making it possible to upgrade programs in the field.

**Caution** Self programming processing must be included in the program before performing self writing.

- Remarks**
1. For usage of self programming, refer to the examples from 15.8.4. onward.
  2. To use the internal flash memory of the  $\mu$ PD78F9510, 78F9511, 78F9512 as the external EEPROM for storing data, refer to **78K0S/Kx1+ EEPROM Emulation Application Note (U17379E)**.

#### 15.8.1 Outline of self programming

To execute self programming, shift the mode from the normal operation of the user program (normal mode) to the self programming mode. Write/erase processing for the flash memory, which has been set to the register in advance, is performed by executing the HALT instruction during self programming mode. The HALT state is automatically released when processing is completed.

To shift to the self programming mode, execute a specific sequence for a specific register. Refer to **15.8.4 Example of shifting normal mode to self programming mode** for details.

**Remark** Data written by self programming can be referenced with the MOV instruction.

**Table 15-10. Self Programming Mode**

Mode	User Program Execution	Execution of Write/erase for Flash Memory with HALT Instruction
Normal mode	Enabled	—
Self programming mode	Enabled <sup>Note</sup>	Enabled

**Note** Maskable interrupt servicing is disabled during self programming mode.

Figure 15-10 shows a block diagram for self programming, Figure 15-11 shows the self programming state transition diagram, Table 15-11 lists the commands for controlling self programming.

Figure 15-10. Block Diagram of Self Programming

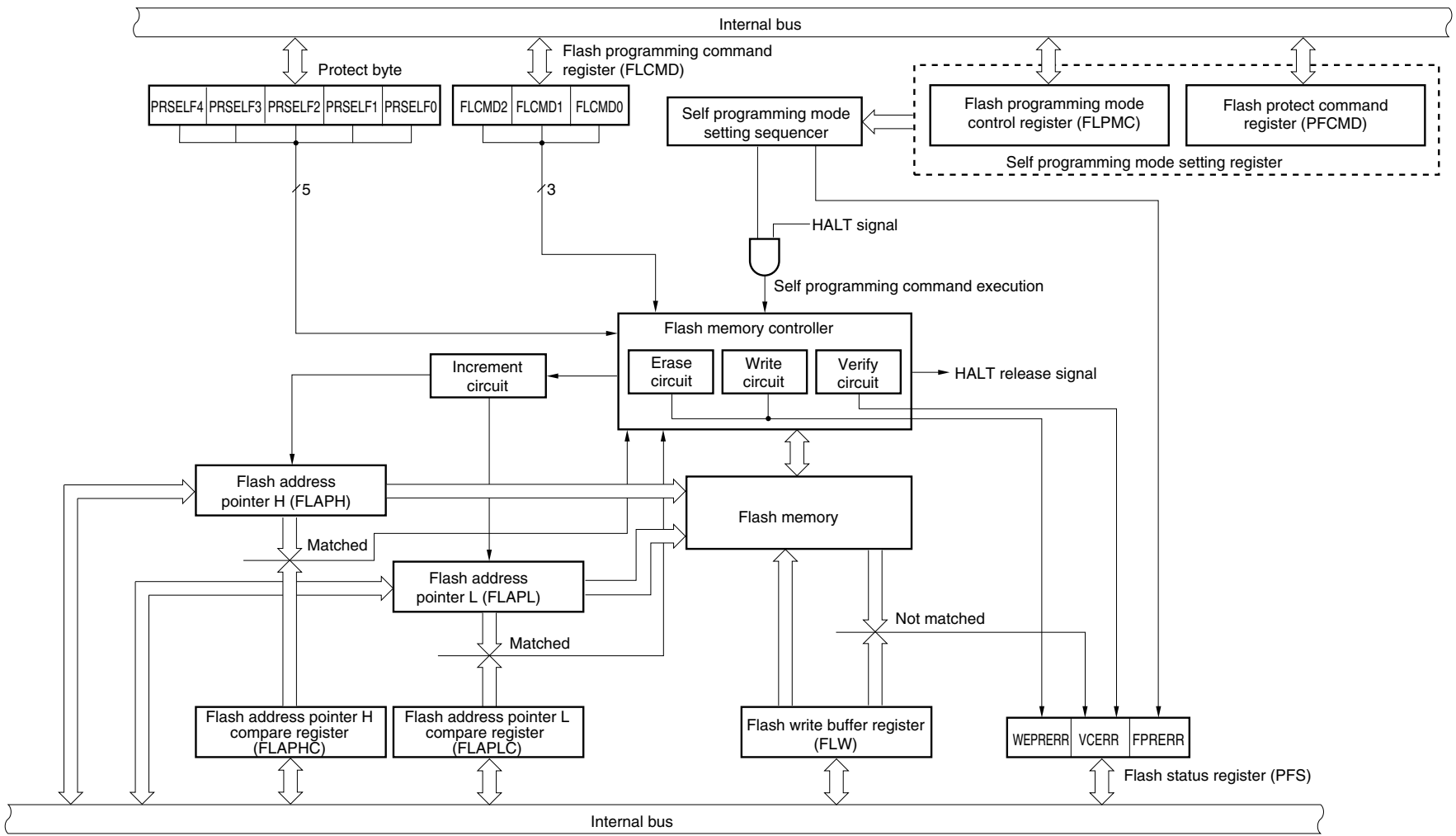


Figure 15-11. Self Programming State Transition Diagram

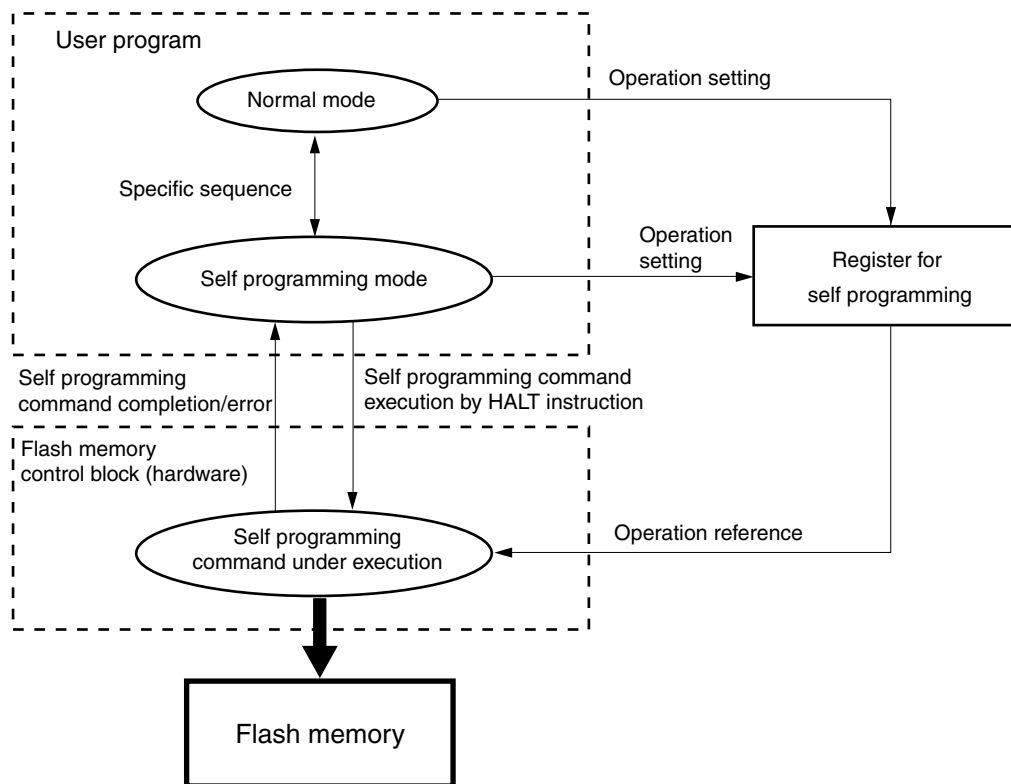


Table 15-11. Self Programming Controlling Commands

Command Name	Function	Time Taken from HALT Instruction Execution to Command Execution End
Internal verify 1	This command is used to check if data has been correctly written to the flash memory. It is used to check whether data has been written to an entire block.	Internal verify for 1 block (internal verify command executed once): 6.8 ms
Internal verify 2	This command is used to check if data has been correctly written to the flash memory. It is used to check whether data has been written to multiple addresses in the same block.	Internal verify of 1 byte: 27 $\mu$ s
Block erasure	This command is used to erase a specified block. Specify the block number before execution.	8.5 ms
Block blank check	This command is used to check if data in a specified block has been erased. Specify the block number, then execute this command.	480 $\mu$ s
Byte write	This command is used to write 1-byte data to the specified address in the flash memory. Specify the write address and write data, then execute this command.	150 $\mu$ s

**Remark** The internal verify 1 command can be executed by specifying an address in the same block, but internal verify 2 is recommended if data is written to multiple addresses in the same block.

### 15.8.2 Cautions on self programming function

- No instructions can be executed while a self programming command is being executed. Therefore, clear and restart the watchdog timer counter in advance so that the watchdog timer does not overflow during self programming. Refer to Table 15-11 for the time taken for the execution of self programming.
- Interrupts that occur during self programming can be acknowledged after self programming mode ends. To avoid this operation, disable interrupt servicing (by setting MK0 to FFH, and executing the DI instruction) when shifting from the normal mode to the self programming mode with a specific sequence.
- RAM is not used while a self programming command is being executed.
- If the supply voltage drops or the reset signal is input while the flash memory is being written or erased, writing/erasing is not guaranteed.
- The value of the blank data set during block erasure is FFH.
- Set the CPU clock beforehand so that it is 1 MHz or higher during self programming.
- Execute self programming after executing the NOP and HALT instructions immediately after executing a specific sequence to set self programming mode. At this time, the HALT instruction is automatically released after  $10 \mu\text{s}$  (MAX.) + 2 CPU clocks ( $f_{\text{CPU}}$ ).
- If the clock of the oscillator or an external clock is selected as the system clock, execute the NOP and HALT instructions immediately after executing a specific sequence to set self programming mode, wait for  $8 \mu\text{s}$  after releasing the HALT status, and then execute self programming.
- Check FPRERR using a 1-bit memory manipulation instruction.
- The state of the pins in self programming mode is the same as that in HALT mode.
- Since the security function set via on-board/off-board programming is disabled in self programming mode, the self programming command can be executed regardless of the security function setting. To disable write or erase processing during self programming, set the protect byte.
- Be sure to clear bits 4 to 7 of flash address pointer H (FLAPH) and flash address pointer H compare register (FLAPHC) to 0 before executing the self programming command. If self programming is executed with these bits set to 1, the device may malfunction.
- Clear the value of the FLCMD register to 00H immediately before setting to self programming mode and normal mode.

### 15.8.3 Registers used for self programming function

The following registers are used for the self programming function.

- Flash programming mode control register (FLPMC)
- Flash protect command register (PFCMD)
- Flash status register (PFS)
- Flash programming command register (FLCMD)
- Flash address pointers H and L (FLAPH and FLAPL)
- Flash address pointer H compare register and flash address pointer L compare register (FLAPHC and FLAPLC)
- Flash write buffer register (FLW)

The  $\mu\text{PD78F9510}$ ,  $78F9511$ ,  $78F9512$  has an area called a protect byte at address 0081H of the flash memory.

**(1) Flash programming mode control register (FLPMC)**

This register is used to set the operation mode when data is written to the flash memory in the self programming mode, and to read the set value of the protect byte.

Data can be written to FLPMC only in a specific sequence (refer to **15.8.3 (2) Flash protect command register (PFCMD)**) so that the application system does not stop by accident because of malfunction due to noise or program hang-up.

This register is set with an 8-bit memory manipulation instruction.

Reset signal generation makes the contents of this register undefined.

**Figure 15-12. Format of Flash Programming Mode Control Register (FLPMC)**

Address: FFA2H    After reset: Undefined<sup>Note 1</sup>    R/W<sup>Note 2</sup>

Symbol	7	6	5	4	3	2	1	0
FLPMC	0	PRSELF4	PRSELF3	PRSELF2	PRSELF1	PRSELF0	0	FLSPM

FLSPM	Selection of operation mode during self programming mode
0	Normal mode This is the normal operation status. Executing the HALT instruction sets standby status.
1	Self programming mode Self programming commands can be executed by executing the specific sequence to change modes while in normal mode. Set a command, an address, and data to be written, then execute the HALT instruction to execute self programming.

PRSELF4	PRSELF3	PRSELF2	PRSELF1	PRSELF0	The set value of the protect byte is read to these bits.
---------	---------	---------	---------	---------	--

- Notes**
1. Bit 0 (FLSPM) is cleared to 0 when reset is released. The set value of the protect byte is read to bits 2 to 6 (PRSELF0 to PRSELF4) after reset is released.
  2. Bits 2 to 6 (PRSELF0 to PRSELF4) are read-only.

- Cautions**
1. **Cautions in the case of setting the self programming mode, refer to 15.8.2 Cautions on self programming function.**
  2. **Set the CPU clock beforehand so that it is 1 MHz or higher during self programming.**
  3. **Execute self programming after executing the NOP and HALT instructions immediately after executing a specific sequence to set self programming mode. At this time, the HALT instruction is automatically released after 10  $\mu$ s (MAX.) + 2 CPU clocks ( $f_{CPU}$ ).**
  4. **If the clock of the oscillator or an external clock is selected as the system clock, execute the NOP and HALT instructions immediately after executing a specific sequence to set self programming mode, wait for 8  $\mu$ s after releasing the HALT status, and then execute self programming.**
  5. **Clear the value of the FLCMD register to 00H immediately before setting to self programming mode and normal mode.**

**(2) Flash protect command register (PFCMD)**

If the application system stops inadvertently due to malfunction caused by noise or program hang-up, an operation to write the flash programming mode control register (FLPMC) may have a serious effect on the system. PFCMD is used to protect FLPMC from being written, so that the application system does not stop inadvertently.

Writing FLPMC is enabled only when a write operation is performed in the following specific sequence.

- <1> Write a specific value to PFCMD (A5H)
- <2> Write the value to be set to bit 0 (FLSPM) of the FLPMC (writing in this step is invalid)
- <3> Write the inverted value of the value to be set to bit 0 (FLSPM) of the FLPMC (writing in this step is invalid)
- <4> Write the value to be set to bit 0 (FLSPM) of the FLPMC (writing in this step is valid)

**Caution** Interrupt servicing cannot be executed in self programming mode. Disable interrupt servicing (by executing the DI instruction while MK0 = FFH) between the points before executing the specific sequence that sets self programming mode and after executing the specific sequence that changes the mode to the normal mode.

This rewrites the value of the register, so that the register cannot be written illegally.

Occurrence of an illegal write operation can be checked by bit 0 (FPRERR) of the flash status register (PFS). Check FPRERR using a 1-bit memory manipulation instruction.

A5H must be written to PFCMD each time the value of FLPMC is changed.

PFCMD can be set by an 8-bit memory manipulation instruction.

Reset signal generation makes PFCMD undefined.

**Figure 15-13. Format of Flash Protect Command Register (PFCMD)**

Address: FFA0H	After reset: Undefined	W						
Symbol	7	6	5	4	3	2	1	0
PFCMD	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0

**(3) Flash status register (PFS)**

If data is not written to the flash programming mode control register (FLPMC), which is protected, in the correct sequence (writing the flash protect command register (PFCMD)), FLPMC is not written and a protection error occurs. If this happens, bit 0 of PFS (FPRERR) is set to 1.

When FPRERR is 1, it can be cleared to 0 by writing 0 to it.

Errors that may occur during self programming are reflected in bit 1 (VCERR) and bit 2 (WEPRERR) of PFS. VCERR or WEPRERR can be cleared by writing 0 to them.

All the flags of the PFS register must be pre-cleared to 0 to check if the operation is performed correctly.

PFS can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears PFS to 00H.

**Caution** Check FPRERR using a 1-bit memory manipulation instruction.



Figure 15-14. Format of Flash Status Register (PFS)

Address: FFA1H	After reset: 00H	R/W						
Symbol	7	6	5	4	3	2	1	0
PFS	0	0	0	0	0	WEPRERR	VCERR	FPRERR

## 1. Operating conditions of FPRERR flag

## &lt;Setting conditions&gt;

- If PFCMD is written when the store instruction operation recently performed on a peripheral register is not to write a specific value (A5H) to FLPMC
- If the first store instruction operation after <1> is on a peripheral register other than FLPMC
- If the first store instruction operation after <2> is on a peripheral register other than FLPMC
- If a value other than the inverted value of the value to be set to FLPMC is written by the first store instruction after <2>
- If the first store instruction operation after <3> is on a peripheral register other than FLPMC
- If a value other than the value to be set to FLPMC (value written in <2>) is written by the first store instruction after <3>

**Remark** The numbers in angle brackets above correspond to the those in (2) **Flash protect command register (PFCMD)**.

## &lt;Reset conditions&gt;

- If 0 is written to the FPRERR flag
- If the reset signal is generation

## 2. Operating conditions of VCERR flag

## &lt;Setting conditions&gt;

- Erasure verification error
- Internal writing verification error

If VCERR is set, it means that the flash memory has not been erased or written correctly. Erase or write the memory again in the specified procedure.

**Remark** The VCERR flag may also be set if an erase or write protect error occurs.

## &lt;Reset conditions&gt;

- When 0 is written to the VCERR flag
- When the reset signal generation

## 3. Operating conditions of WEPRERR flag

## &lt;Setting conditions&gt;

- If the area specified by the protect byte to be protected from erasing or writing is specified by the flash address pointer H (FLAPH) and a command is executed to this area
- If 1 is written to a bit that has not been erased (a bit for which the data is 0).

## &lt;Reset conditions&gt;

- When 0 is written to the WEPRERR flag
- When the reset signal generation

**(4) Flash programming command register (FLCMD)**

This register is used to specify whether the flash memory is erased, written, or verified in the self programming mode.

This register is set by using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 15-15. Format of Flash Programming Command Register (FLCMD)**

Address: FFA3H    After reset: 00H    R/W

Symbol	7	6	5	4	3	2	1	0
FLCMD	0	0	0	0	0	FLCMD2	FLCMD1	FLCMD0

FLCMD2	FLCMD1	FLCMD0	Command Name	Function
0	0	1	Internal verify 1	This command is used to check if data has been correctly written to the flash memory. It is used to check whether data has been written to an entire block. If an error occurs, bit 1 (VCERR) or bit 2 (WEPRERR) of the flash status register (PFS) is set to 1.
0	1	0	Internal verify 2	This command is used to check if data has been correctly written to the flash memory. It is used to check whether data has been written to multiple addresses in the same block. If an error occurs, bit 1 (VCERR) or bit 2 (WEPRERR) of the flash status register (PFS) is set to 1.
0	1	1	Block erase	This command is used to erase specified block. It is used both in the on-board mode and self programming mode.
1	0	0	Block blank check	This command is used to check if the specified block has been erased.
1	0	1	Byte write	This command is used to write 1-byte data to the specified address in the flash memory. Specify the write address and write data, then execute this command.  If 1 is written to a bit that has not been erased (a bit for which the data is 0), then bit 2 (WEPRERR) of the flash status register (PFS) becomes 1.
Other than above <sup>Note</sup>			Setting prohibited	

**Note** If any command other than those above is executed, command execution may immediately be terminated, and bit 1 or 2 (WEPRERR or VCERR) of the flash status register (PFS) may be set to 1.

**(5) Flash address pointers H and L (FLAPH and FLAPL)**

These registers are used to specify the start address of the flash memory when the memory is erased, written, or verified in the self programming mode.

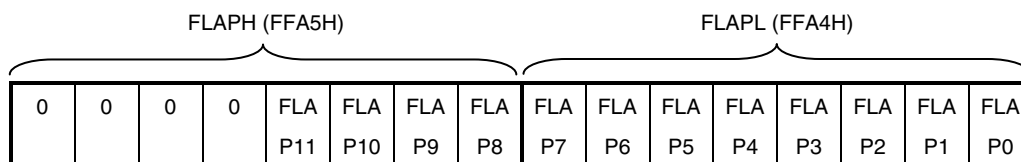
FLAPH and FLAPL consist of counters, and they are incremented until the values match with those of FLAPHC and FLAPLC when the programming command is not executed. When the programming command is executed, therefore, set the value again.

These registers are set with a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation makes these registers undefined.

**Figure 15-16. Format of Flash Address Pointer H/L (FLAPH/FLAPL)**

Address: FFA4H, FFA5H    After reset: 00H    R/W



**Caution** Be sure to clear bits 4 to 7 of flash address pointer H (FLAPH) and flash address pointer H compare register (FLAPHC) to 0 before executing the self programming command. If the value of these bits is 1 when executing the self programming command.

**(6) Flash address pointer H compare register and flash address pointer L compare register (FLAPHC and FLAPLC)**

These registers are used to specify the address range in which the internal sequencer operates when the flash memory is verified in the self programming mode.

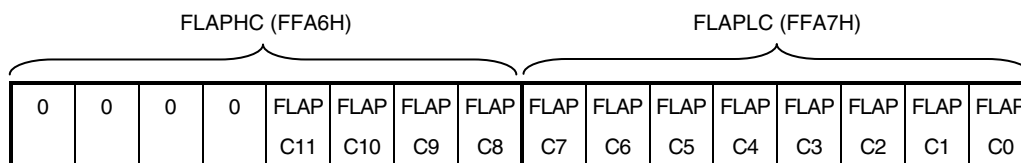
Set FLAPHC to the same value as that of FLAPH. Set the last address of the range in which verification is to be executed to FLAPLC.

These registers are set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

**Figure 15-17. Format of Flash Address Pointer H/L Compare Registers (FLAPHC/FLAPLC)**

Address: FFA6H, FFA7H    After reset: 00H    R/W



- Cautions**
1. Be sure to clear bits 4 to 7 of FLAPH and FLAPHC to 0 before executing the self programming command. If the value of these bits is 1 when executing the self programming command.
  2. Set the number of the block subject to a block erase, verify, or blank check (same value as FLAPH) to FLAPHC.
  3. Clear FLAPLC to 00H when a block erase is performed, and set this register to FFH when a blank check is performed.

**(7) Flash write buffer register (FLW)**

This register is used to store the data to be written to the flash memory.

This register is set with an 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

**Figure 15-18. Format of Flash Write Buffer Register (FLW)**

Address: FFA8H    After reset: 00H    R/W

Symbol	7	6	5	4	3	2	1	0
FLW	FLW7	FLW6	FLW5	FLW4	FLW3	FLW2	FLW1	FLW0

**(8) Protect byte**

This protect byte is used to specify the area that is to be protected from writing or erasing. The specified area is valid only in the self programming mode. Because self programming of the protected area is invalid, the data written to the protected area is guaranteed.

**Figure 15-19. Format of Protect Byte (1/2)**

Address: 0081H

7	6	5	4	3	2	1	0
1	PRSELF4	PRSELF3	PRSELF2	PRSELF1	PRSELF0	1	1

•  $\mu$ PD78F9510

PRSELF4	PRSELF3	PRSELF2	PRSELF1	PRSELF0	Status
0	1	1	1	0	Blocks 3 to 0 are protected.
0	1	1	1	1	Blocks 1 and 0 are protected. Blocks 2 and 3 can be written or erased.
1	1	1	1	1	All blocks can be written or erased.
Other than above					Setting prohibited

•  $\mu$ PD78F9511

PRSELF4	PRSELF3	PRSELF2	PRSELF1	PRSELF0	Status
0	1	1	0	0	Blocks 7 to 0 are protected.
0	1	1	0	1	Blocks 5 to 0 are protected. Blocks 6 and 7 can be written or erased.
0	1	1	1	0	Blocks 3 to 0 are protected. Blocks 4 to 7 can be written or erased.
0	1	1	1	1	Blocks 1 and 0 are protected. Blocks 2 to 7 can be written or erased.
1	1	1	1	1	All blocks can be written or erased.
Other than above					Setting prohibited

Figure 15-19. Format of Protect Byte (2/2)

•  $\mu$  PD78F9512

PRSELF4	PRSELF3	PRSELF2	PRSELF1	PRSELF0	Status
0	1	0	0	0	Blocks 15 to 0 are protected.
0	1	0	0	1	Blocks 13 to 0 are protected. Blocks 14 and 15 can be written or erased.
0	1	0	1	0	Blocks 11 to 0 are protected. Blocks 12 to 15 can be written or erased.
0	1	0	1	1	Blocks 9 to 0 are protected. Blocks 10 to 15 can be written or erased.
0	1	1	0	0	Blocks 7 to 0 are protected. Blocks 8 to 15 can be written or erased.
0	1	1	0	1	Blocks 5 to 0 are protected. Blocks 6 to 15 can be written or erased.
0	1	1	1	0	Blocks 3 to 0 are protected. Blocks 4 to 15 can be written or erased.
0	1	1	1	1	Blocks 1 and 0 are protected. Blocks 2 to 15 can be written or erased.
1	1	1	1	1	All blocks can be written or erased.
Other than above					Setting prohibited

#### 15.8.4 Example of shifting normal mode to self programming mode

The operating mode must be shifted from normal mode to self programming mode before performing self programming.

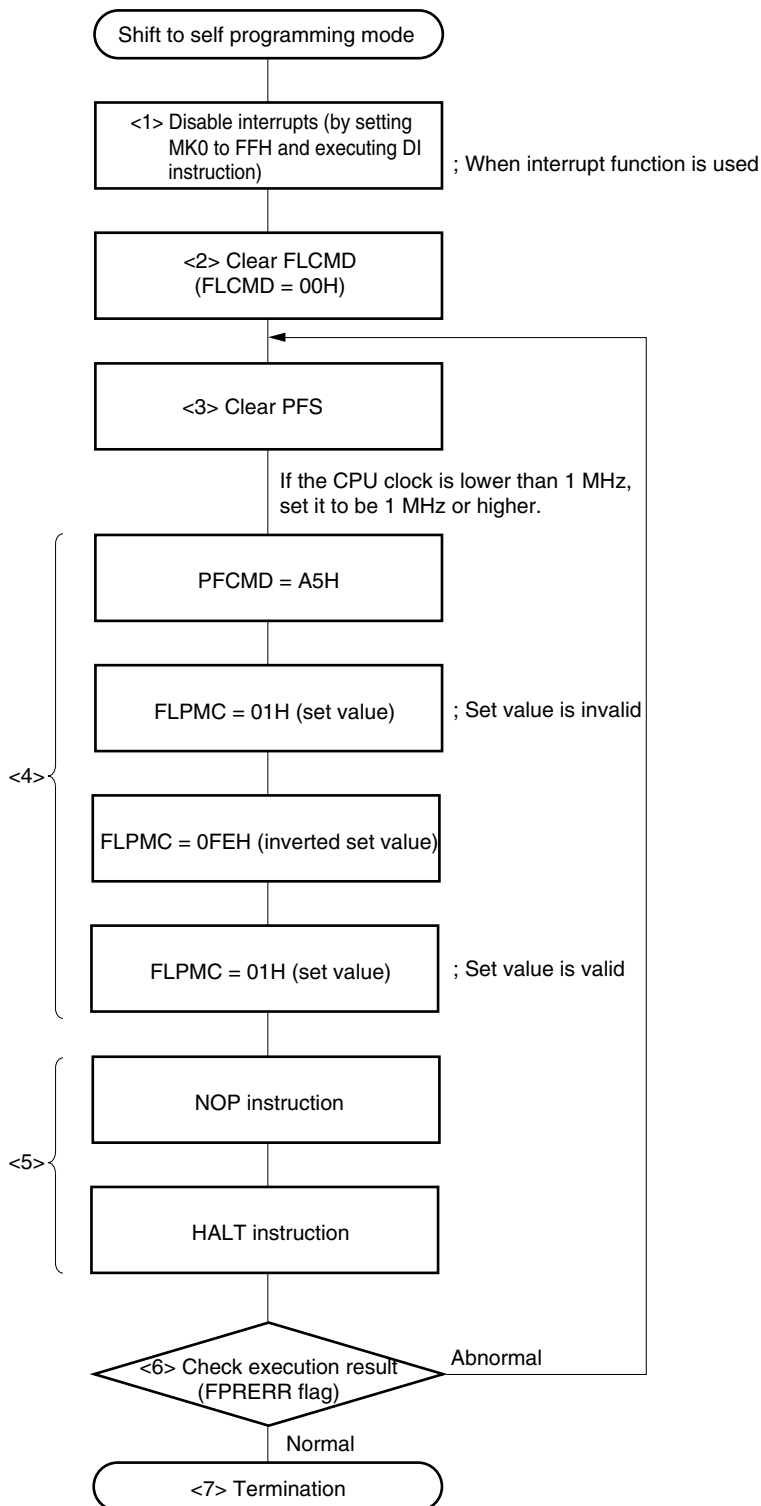
An example of shifting to self programming mode is explained below.

- <1> Disable interrupts if the interrupt function is used (by setting the interrupt mask flag registers (MK0) to FFH and executing the DI instruction).
- <2> Clear FLCMD (FLCMD = 00H).
- <3> Clear the flash status register (PFS).
- <4> Set self programming mode using a specific sequence.
  - Write a specific value (A5H) to PFCMD.
  - Write 01H to FLPMC (writing in this step is invalid).
  - Write 0FEH (inverted value of 01H) to FLPMC (writing in this step is invalid).
  - Write 01H to FLPMC (writing in this step is valid).
- <5> Execute NOP instruction and HALT instruction.
- <6> Check the execution result of the specific sequence using bit 0 (FPRERR) of PFS.  
Abnormal → <3>, normal → <7>
- <7> Mode shift is completed.

**Note** If the CPU clock is lower than 1 MHz, set it to be 1 MHz or higher.

**Caution** Be sure to perform the series of operations described above using the user program at an address where data is not erased nor written.

Figure 15-20. Example of Shifting to Self Programming Mode



**Caution** Be sure to perform the series of operations described above using the user program at an address where data is not erased nor written.

**Remark** <1> to <7> in Figure 15-20 correspond to <1> to <7> in 15.8.4 (previous page).

An example of the program that shifts the mode to self programming mode is shown below.

```
;-----  
;START  
;-----  
    MOV     MK0,#11111111B    ; Masks all interrupts  
    MOV     FLCMD,#00H       ; Clear FLCMD register  
  
    DI  
  
ModeOnLoop:                    ; Configure settings so that the CPU clock  $\geq$  1 MHz  
    MOV     PFS,#00H         ; Clears flash status register  
    MOV     PFCMD,#0A5H      ; PFCMD register control  
    MOV     FLPMC,#01H       ; FLPMC register control (sets value)  
    MOV     FLPMC,#0FEH      ; FLPMC register control (inverts set value)  
    MOV     FLPMC,#01H       ; Sets self programming mode with FLPMC register  
                                ; control (sets value)  
  
    NOP  
    HALT  
    BT     PFS.0,$ModeOLoop  ; Checks completion of write to specific registers  
                                ; Repeats the same processing when an error occurs  
  
;-----  
;END  
;-----
```

### 15.8.5 Example of shifting self programming mode to normal mode

The operating mode must be returned from self programming mode to normal mode after performing self programming.

An example of shifting to normal mode is explained below.

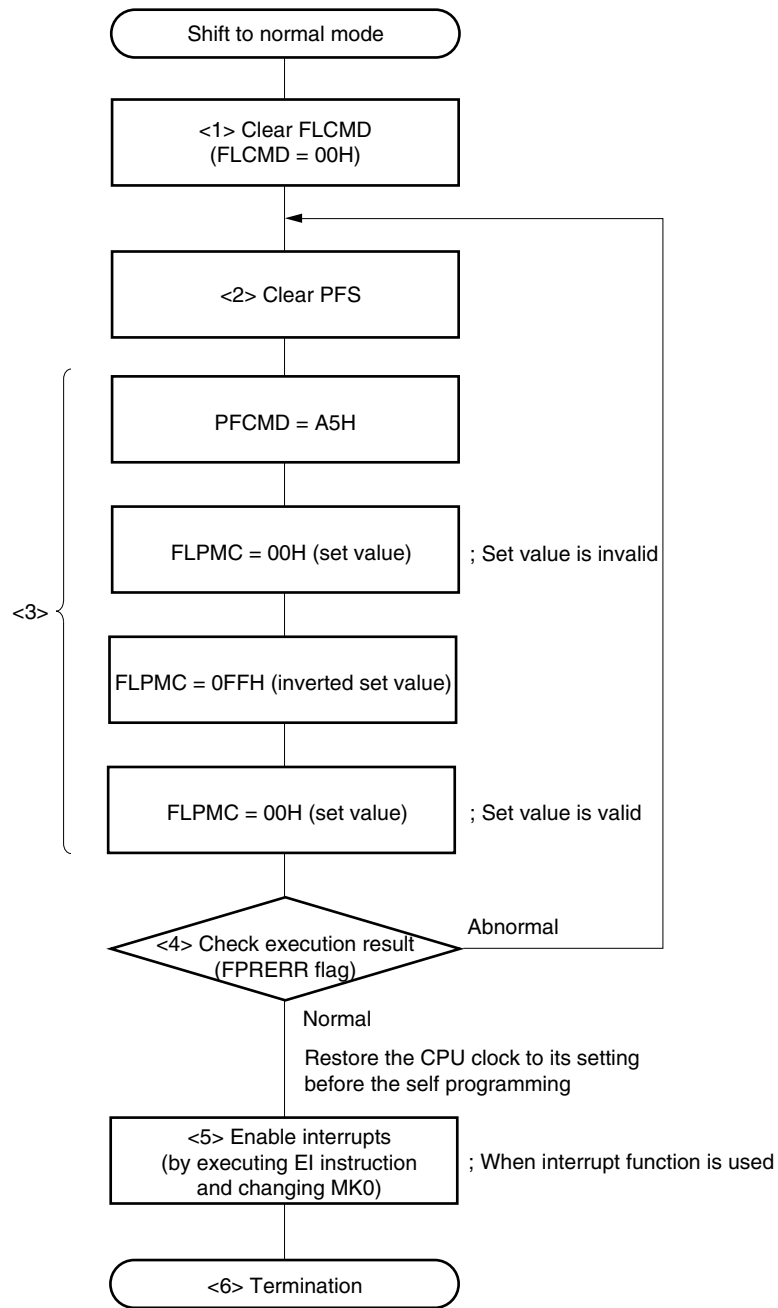
- <1> Clear FLCMD (FLCMD = 00H).
- <2> Clear the flash status register (PFS).
- <3> Set normal mode using a specific sequence.
  - Write the specific value (A5H) to PFCMD.
  - Write 00H to FLPMC (writing in this step is invalid)
  - Write 0FFH (inverted value of 00H) to FLPMC (writing in this step is invalid)
  - Write 00H to FLPMC (writing in this step is valid)
- <4> Check the execution result of the specific sequence using bit 0 (FPRERR) of PFS<sup>Note</sup>.  
Abnormal → <2>, normal → <5>
- <5> Enable interrupt servicing (by executing the EI instruction and changing MK0) to restore the original state.
- <6> Mode shift is completed

**Note** Restore the CPU clock to its setting before self programming, after normal completion of the specific sequence.

**Caution** Be sure to perform the series of operations described above using the user program at an address where data is not erased nor written.



Figure 15-21. Example of Shifting to Normal Mode



**Caution** Be sure to perform the series of operations described above using the user program at an address where data is not erased nor written.

**Remark** <1> to <6> in Figure 15-21 correspond to <1> to <6> in 15.8.5 (previous page).

An example of a program that shifts the mode to normal mode is shown below.

```
;-----  
;START  
;-----  
  
      MOV     FLCMD,#00H      ; Clear FLCMD register  
  
ModeOffLoop:  
      MOV     PFS,#00H       ; Clears flash status register  
      MOV     PFCMD,#0A5H    ; PFCMD register control  
      MOV     FLPMC,#00H     ; FLPMC register control (sets value)  
      MOV     FLPMC,#0FFH    ; FLPMC register control (inverts set value)  
      MOV     FLPMC,#00H     ; Sets normal mode via FLPMC register control (sets value)  
  
      BT     PFS.0,$ModeOffLoop ; Checks completion of write to specific registers  
                                           ; Repeats the same processing when an error occurs  
                                           ; Restore the CPU clock to its setting before the self  
                                           ; programming, after normal completion of the specific  
                                           ; sequence  
  
      MOV     MK0,#INT_MK0   ; Restores interrupt mask flag  
  
      EI  
  
;-----  
;END  
;-----
```

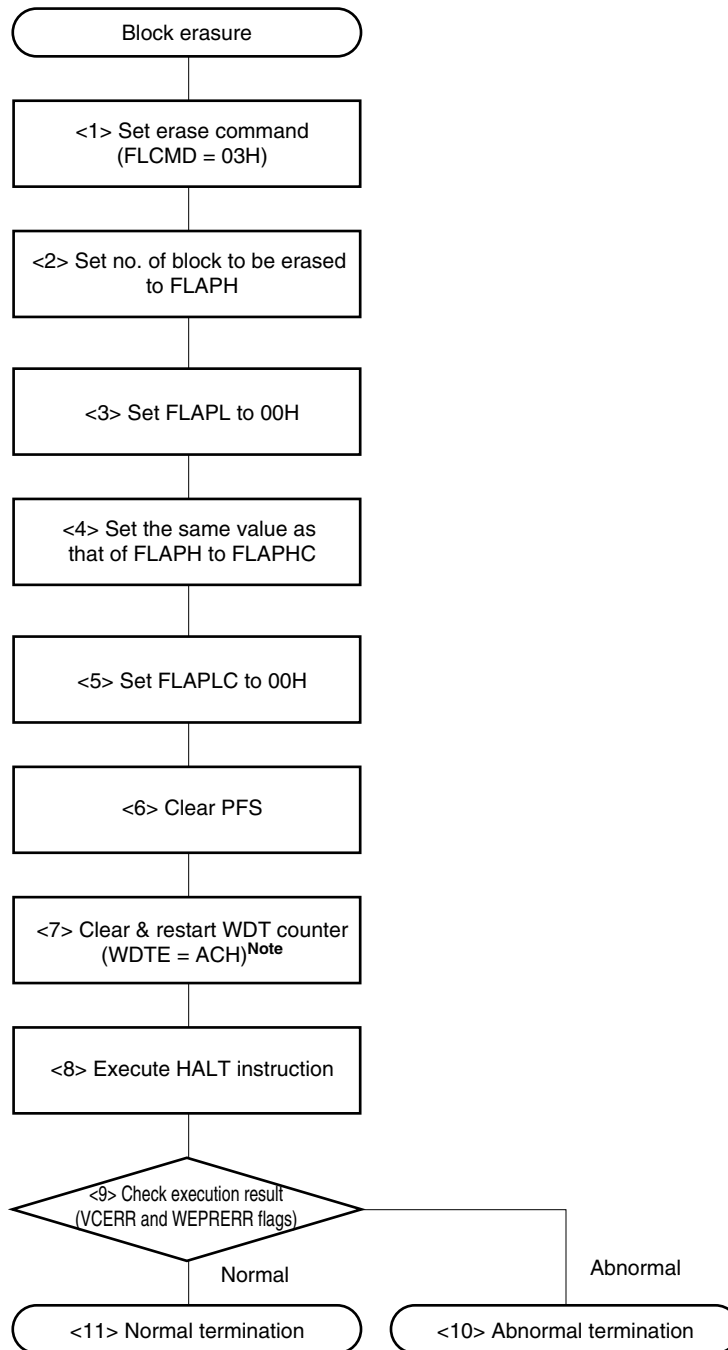
### 15.8.6 Example of block erase operation in self programming mode

An example of the block erase operation in self programming mode is explained below.

- <1> Set 03H (block erase) to the flash program command register (FLCMD).
- <2> Set the block number to be erased, to flash address pointer H (FLAPH).
- <3> Set flash address pointer L (FLAPL) to 00H.
- <4> Write the same value as FLAPH to the flash address pointer H compare register (FLAPHC).
- <5> Set the flash address pointer L compare register (FLAPLC) to 00H.
- <6> Clear the flash status register (PFS).
- <7> Write ACH to the watchdog timer enable register (WDTE) (clear and restart the watchdog timer counter)<sup>Note</sup>.
- <8> Execute the HALT instruction then start self programming. (Execute an instruction immediately after the HALT instruction if self programming has been executed.)
- <9> Check if a self programming error has occurred using bit 1 (VCERR) and bit 2 (WEPRERR) of PFS.
  - Abnormal → <10>
  - Normal → <11>
- <10> Block erase processing is abnormally terminated.
- <11> Block erase processing is normally terminated.

**Note** This setting is not required when the watchdog timer is not used.

Figure 15-22. Example of Block Erase Operation in Self Programming Mode



**Note** This setting is not required when the watchdog timer is not used.

**Remark** <1> to <11> in Figure 15-22 correspond to <1> to <11> in 15.8.6 (previous page).

An example of a program that performs a block erase in self programming mode is shown below.

```
;-----  
;START  
;-----  
  
FlashBlockErase:  
    MOV    FLCMD,#03H    ; Sets flash control command (block erase)  
    MOV    FLAPH,#07H    ; Sets number of block to be erased (block 7 is specified here)  
    MOV    FLAPL,#00H    ; Fixes FLAPL to "00H"  
    MOV    FLAPHC,#07H   ; Sets erase block compare number (same value as that of FLAPH)  
    MOV    FLAPLC,#00H   ; Fixes FLAPLC to "00H"  
  
    MOV    PFS,#00H      ; Clears flash status register  
    MOV    WDTE,#0ACH    ; Clears & restarts WDT  
    HALT                    ; Self programming is started  
    MOV    A,PFS  
    MOV    CmdStatus,A    ; Execution result is stored in variable  
                                ; (CmdStatus = 0: normal termination, other than 0: abnormal  
                                ; termination)  
  
;-----  
;END  
;-----
```

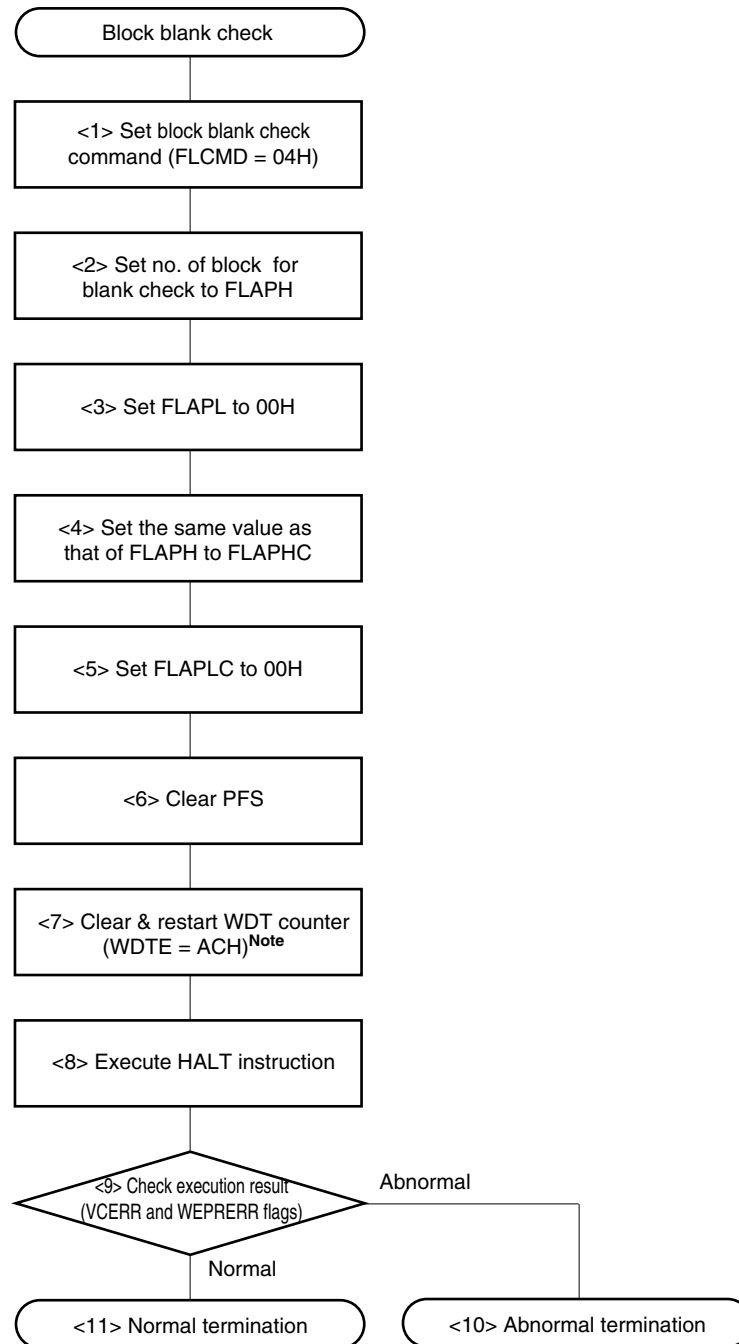
### 15.8.7 Example of block blank check operation in self programming mode

An example of the block blank check operation in self programming mode is explained below.

- <1> Set 04H (block blank check) to the flash program command register (FLCMD).
- <2> Set the number of block for which a blank check is performed, to flash address pointer H (FLAPH).
- <3> Set flash address pointer L (FLAPL) to 00H.
- <4> Write the same value as FLAPH to the flash address pointer H compare register (FLAPHC).
- <5> Set the flash address pointer L compare register (FLAPLC) to FFH.
- <6> Clear the flash status register (PFS).
- <7> Write ACH to the watchdog timer enable register (WDTE) (clear and restart the watchdog timer counter)<sup>Note</sup>.
- <8> Execute the HALT instruction then start self programming. (Execute an instruction immediately after the HALT instruction if self programming has been executed.)
- <9> Check if a self programming error has occurred using bit 1 (VCERR) and bit 2 (WEPRERR) of PFS.  
Abnormal → <10>  
Normal → <11>
- <10> Block blank check is abnormally terminated.
- <11> Block blank check is normally terminated.

**Note** This setting is not required when the watchdog timer is not used.

Figure 15-23. Example of Block Blank Check Operation in Self Programming Mode



**Note** This setting is not required when the watchdog timer is not used.

**Remark** <1> to <11> in Figure 15-23 correspond to <1> to <11> in 15.8.7 (previous page).

An example of a program that performs a block blank check in self programming mode is shown below.

```
-----  
;START  
-----  
  
FlashBlockBlankCheck:  
    MOV     FLCMD,#04H    ; Sets flash control command (block blank check)  
    MOV     FLAPH,#07H    ; Sets number of block for blank check (block 7 is specified  
                          ; here)  
    MOV     FLAPL,#00H    ; Fixes FLAPL to "00H"  
    MOV     FLAPHC,#07H   ; Sets blank check block compare number (same value as that of  
                          ; FLAPH)  
    MOV     FLAPLC,#0FFH  ; Fixes FLAPLC to "FFH"  
  
    MOV     PFS,#00H     ; Clears flash status register  
    MOV     WDTE,#0ACH   ; Clears & restarts WDT  
    HALT                               ; Self programming is started  
    MOV     A,PFS  
    MOV     CmdStatus,A   ; Execution result is stored in variable  
                          ; (CmdStatus = 0: normal termination, other than 0: abnormal  
                          ; termination)  
  
-----  
;END  
-----
```



### 15.8.8 Example of byte write operation in self programming mode

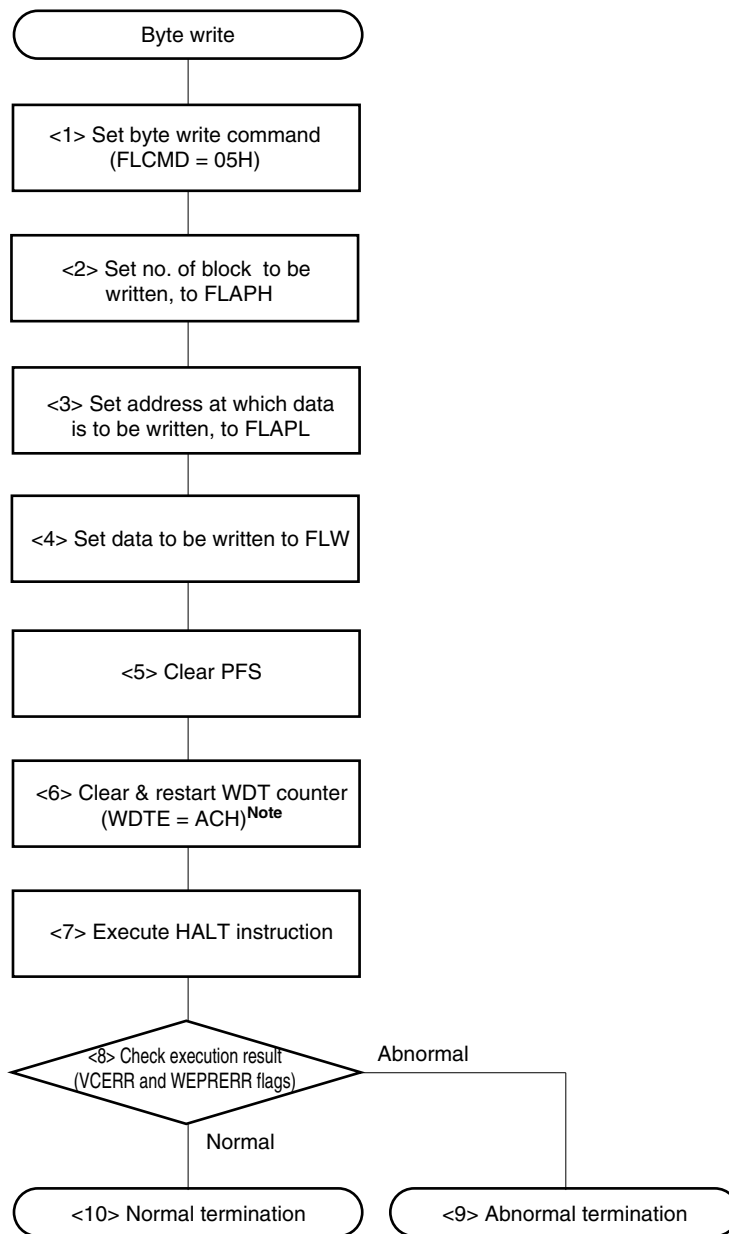
An example of the byte write operation in self programming mode is explained below.

- <1> Set 05H (byte write) to the flash program command register (FLCMD).
- <2> Set the number of block to which data is to be written, to flash address pointer H (FLAPH).
- <3> Set the address at which data is to be written, to flash address pointer L (FLAPL).
- <4> Set the data to be written, to the flash write buffer register (FLW).
- <5> Clear the flash status register (PFS).
- <6> Write ACH to the watchdog timer enable register (WDTE) (clear and restart the watchdog timer counter)<sup>Note</sup>.
- <7> Execute the HALT instruction then start self programming. (Execute an instruction immediately after the HALT instruction if self programming has been executed.)
- <8> Check if a self programming error has occurred using bit 1 (VCERR) and bit 2 (WEPRERR) of PFS.
  - Abnormal → <9>
  - Normal → <10>
- <9> Byte write processing is abnormally terminated.
- <10> Byte write processing is normally terminated.

**Note** This setting is not required when the watchdog timer is not used.

**Caution** If a write results in failure, erase the block once and write to it again.

Figure 15-24. Example of Byte Write Operation in Self Programming Mode



**Note** This setting is not required when the watchdog timer is not used.

**Remark** <1> to <10> in Figure 15-24 correspond to <1> to <10> in 15.8.8 (previous page).

An example of a program that performs a byte write in self programming mode is shown below.

```
;-----  
;START  
;-----  
FlashWrite:  
    MOV     FLCMD,#05H      ; Sets flash control command (byte write)  
    MOV     FLAPH,#07H     ; Sets address to which data is to be written, with  
                          ; FLAPH (block 7 is specified here)  
    MOV     FLAPL,#20H     ; Sets address to which data is to be written, with  
                          ; FLAPL (address 20H is specified here)  
    MOV     FLW,#10H       ; Sets data to be written (10H is specified here)  
  
    MOV     PFS,#00H       ; Clears flash status register  
    MOV     WDTE,#0ACH     ; Clears & restarts WDT  
    HALT                               ; Self programming is started  
    MOV     A,PFS  
    MOV     CmdStatus,A    ; Execution result is stored in variable  
                          ; (CmdStatus = 0: normal termination, other than 0: abnormal  
                          ; termination)  
  
;-----  
;END  
;-----
```

### 15.8.9 Example of internal verify operation in self programming mode

An example of the internal verify operation in self programming mode is explained below.

- Internal verify 1

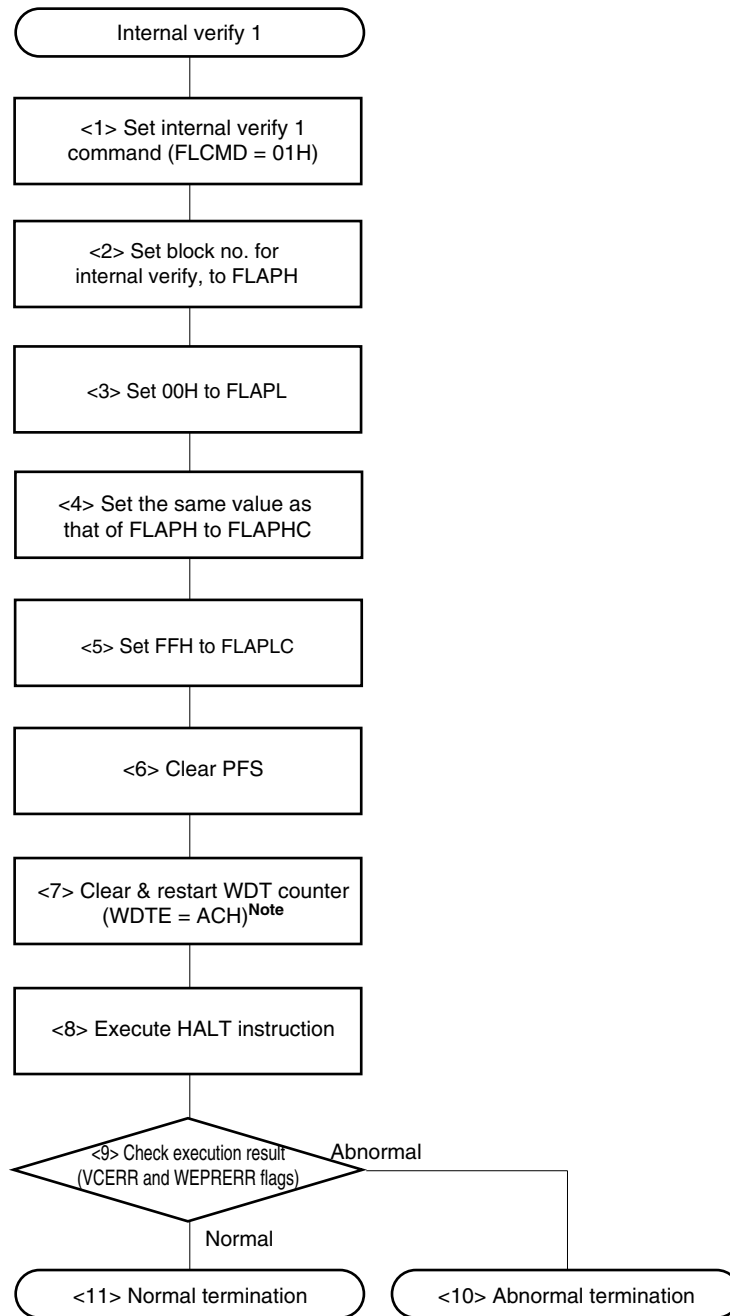
- <1> Set 01H (internal verify 1) to the flash program command register (FLCMD).
- <2> Set the block number for which internal verify is performed, to flash address pointer H (FLAPH).
- <3> Set 00H to the flash address pointer L (FLAPL).
- <4> Write the same value as that of FLAPH to the flash address pointer H compare register (FLAPHC).
- <5> Set FFH to the flash address pointer L compare register (FLAPLC).
- <6> Clear the flash status register (PFS).
- <7> Write ACH to the watchdog timer enable register (WDTE) (clear and restart the watchdog timer counter)<sup>Note</sup>.
- <8> Execute the HALT instruction then start self programming. (Execute an instruction immediately after the HALT instruction if self programming has been executed.)
- <9> Check if a self programming error has occurred using bit 1 (VCERR) and bit 2 (WEPRERR) of PFS.
  - Abnormal → <10>
  - Normal → <11>
- <10> Internal verify processing is terminated abnormally.
- <11> Internal verify processing is terminated normally.

- Internal verify 2

- <1> Set 02H (internal verify 2) to the flash program command register (FLCMD).
- <2> Set the block number for which internal verify is performed, to flash address pointer H (FLAPH).
- <3> Set the verify start address to the flash address pointer L (FLAPL).
- <4> Write the same value as that of FLAPH to the flash address pointer H compare register (FLAPHC).
- <5> Set the verify end address to the flash address pointer L compare register (FLAPLC).
- <6> Clear the flash status register (PFS).
- <7> Write ACH to the watchdog timer enable register (WDTE) (clear and restart the watchdog timer counter)<sup>Note</sup>.
- <8> Execute the HALT instruction then start self programming. (Execute an instruction immediately after the HALT instruction if self programming has been executed.)
- <9> Check if a self programming error has occurred using bit 1 (VCERR) and bit 2 (WEPRERR) of PFS.
  - Abnormal → <10>
  - Normal → <11>
- <10> Internal verify processing is terminated abnormally.
- <11> Internal verify processing is terminated normally.

**Note** This setting is not required when the watchdog timer is not used.

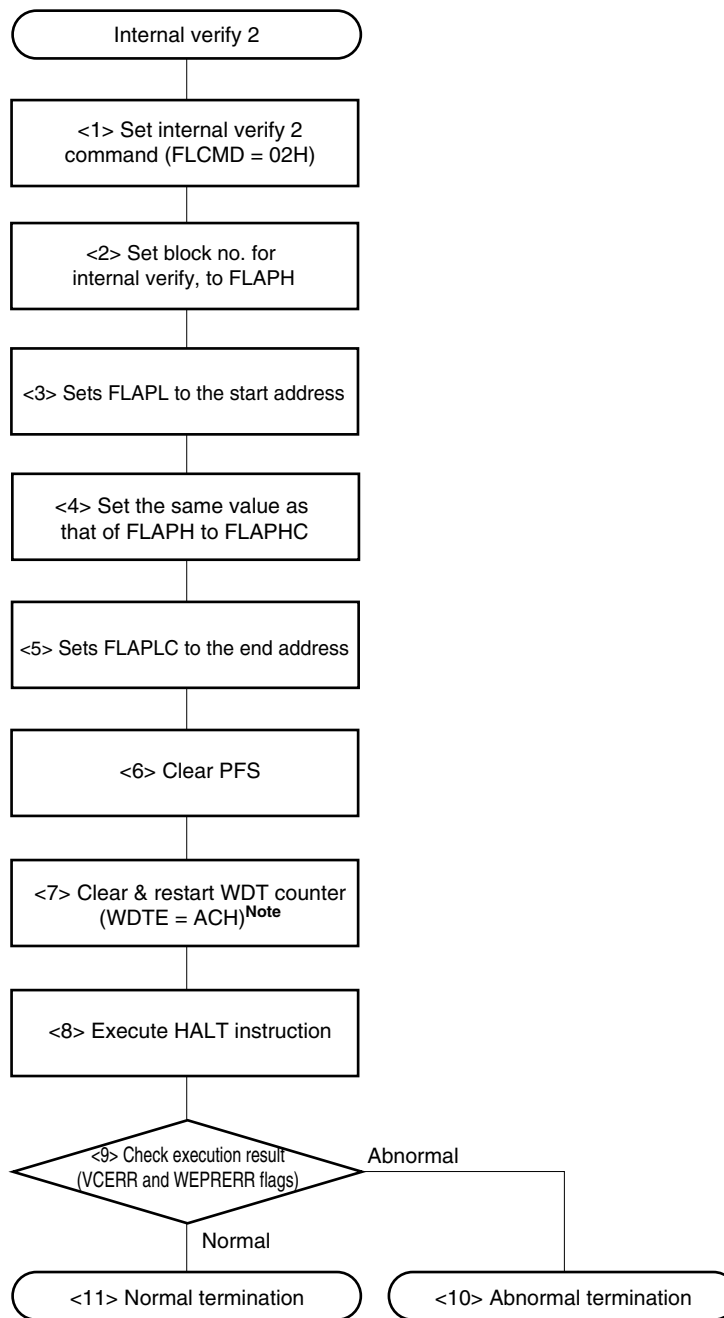
Figure 15-25. Example of Internal Verify 1 Operation in Self Programming Mode



**Note** This setting is not required when the watchdog timer is not used.

**Remark** <1> to <11> in Figure 15-25 correspond to Internal verify 1 <1> to <11> in **15.8.9** (previous page).

Figure 15-26. Example of Internal Verify 2 Operation in Self Programming Mode



**Note** This setting is not required when the watchdog timer is not used.

**Remark** <1> to <11> in Figure 15-26 correspond to Internal verify 2 <1> to <11> in **15.8.9** (the page before last).

Example programs that perform internal verify 1 and 2 in self programming mode are shown below.

- Internal verify 1

```

;-----
;START
;-----
FlashVerify:
    MOV     FLCMD,#01H      ; Sets flash control command (internal verify 1)
    MOV     FLAPH,#07H     ; Sets block number for which internal verify is performed,
                          ; to FLAPH (Example: Block 7 is specified here)

    MOV     FLAPL,#00H     ; Sets 00H
    MOV     FLAPHC,#07H
    MOV     FLAPLC,#FFH   ; Sets FFH

    MOV     PFS,#00H      ; Clears flash status register
    MOV     WDTE,#0ACH    ; Clears & restarts WDT
    HALT                    ; Self programming is started
    MOV     A,PFS
    MOV     CmdStatus,A   ; Execution result is stored in variable
                          ; (CmdStatus = 0: normal termination, other than 0: abnormal
                          ; termination)

;-----
;END
;-----

```

- Internal verify 2

```

;-----
;START
;-----
FlashVerify:
    MOV     FLCMD,#02H     ; Sets flash control command (internal verify 2)
    MOV     FLAPH,#07H     ; Sets block number for which internal verify is
                          ; performed, to FLAPH (Example: Block 7 is specified here)

    MOV     FLAPL,#00H     ; Sets FLAPL to the start address for verify (Example: Address
                          ; 00H is specified here)

    MOV     FLAPHC,#07H
    MOV     FLAPLC,#20H   ; Sets FLAPLC to the end address for verify (Example: Address
                          ; 20H is specified here)

    MOV     PFS,#00H      ; Clears flash status register
    MOV     WDTE,#0ACH    ; Clears & restarts WDT
    HALT                    ; Self programming is started
    MOV     A,PFS
    MOV     CmdStatus,A   ; Execution result is stored in variable
                          ; (CmdStatus = 0: normal termination, other than 0: abnormal
                          ; termination)

;-----
;END
;-----

```

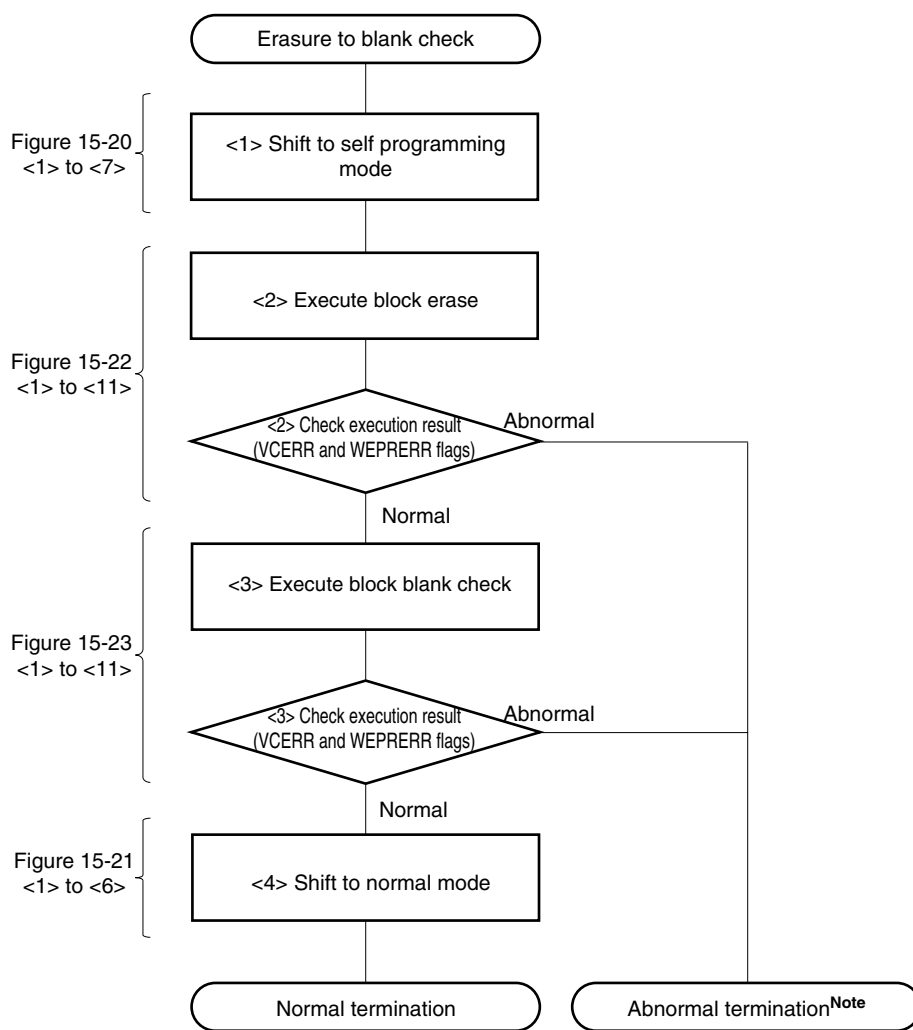
**15.8.10 Examples of operation when command execution time should be minimized in self programming mode**

Examples of operation when the command execution time should be minimized in self programming mode are explained below.

**(1) Erasure to blank check**

- <1> Mode is shifted from normal mode to self programming mode (<1> to <7> in 15.8.4)
- <2> Execution of block erase → Error check (<1> to <11> in 15.8.6)
- <3> Execution of block blank check → Error check (<1> to <11> in 15.8.7)
- <4> Mode is shifted from self programming mode to normal mode (<1> to <6> in 15.8.5)

**Figure 15-27. Example of Operation When Command Execution Time Should Be Minimized (from Erasure to Blank Check)**



**Note** Perform processing to shift to normal mode in order to return to normal processing.

**Remark** <1> to <4> in Figure 15-27 correspond to <1> to <4> in 15.8.10 (1) above.



An example of a program when the command execution time (from erasure to blank check) should be minimized in self programming mode is shown below.

```

;-----
;START
;-----
        MOV     MKO,#11111111B    ; Masks all interrupts
        MOV     FLCMD,#00H        ; Clears FLCMD register

        DI

ModeOnLoop:
        ; Configure settings so that the CPU clock  $\geq$  1 MHz
        MOV     PFS,#00H          ; Clears flash status register
        MOV     PFCMD,#0A5H       ; PFCMD register control
        MOV     FLPMC,#01H        ; FLPMC register control (sets value)
        MOV     FLPMC,#0FEH       ; FLPMC register control (inverts set value)
        MOV     FLPMC,#01H        ; Sets self programming mode with FLPMC register control (sets
                                   ; value)

        NOP
        HALT

        BT     PFS.0,$ModeOnLoop ; Checks completion of write to specific registers
                                   ; Repeats the same processing when an error occurs

FlashBlockErase:
        MOV     FLCMD,#03H        ; Sets flash control command (block erase)
        MOV     FLAPH,#07H        ; Sets number of block to be erased (block 7 is specified
                                   ; here)
        MOV     FLAPL,#00H        ; Fixes FLAPL to "00H"
        MOV     FLAPHC,#07H       ; Sets erase block compare number (same value as that of
                                   ; FLAPH)
        MOV     FLAPLC,#00H       ; Fixes FLAPLC to "00H"

        MOV     WDTE,#0ACH        ; Clears & restarts WDT
        HALT                       ; Self programming is started
        MOV     A,PFS
        CMP     A,#00H
        BNZ     $StatusError      ; Checks erase error
                                   ; Performs abnormal termination processing when an error
                                   ; occurs.

FlashBlockBlankCheck:
        MOV     FLCMD,#04H        ; Sets flash control command (block blank check)
        MOV     FLAPH,#07H        ; Sets number of block for blank check (block 7 is specified
                                   ; here)
        MOV     FLAPL,#00H        ; Fixes FLAPL to "00H"

```

```

MOV     FLAPHC,#07H      ; Sets blank check block compare number (same value as of
                        ; FLAPH)
MOV     FLAPLC,#0FFH    ; Fixes FLAPLC to "FFH"
MOV     WDTE,#0ACH      ; Clears & restarts WDT
HALT                                ; Self programming is started
MOV     A,PFS
CMP     A,#00H
BNZ     $StatusError    ; Checks blank check error
                        ; Performs abnormal termination processing when an error
                        ; occurs.

MOV     FLCMD,#00H      ; Clears FLCMD register
ModeOffLoop:
MOV     PFS,#00H        ; Clears flash status register
MOV     PFCMD,#0A5H     ; PFCMD register control
MOV     FLPMC,#00H      ; FLPMC register control (sets value)
MOV     FLPMC,#0FFH     ; FLPMC register control (inverts set value)
MOV     FLPMC,#00H      ; Sets normal mode via FLPMC register control (sets value)

BT     PFS.0,$ModeOffLoop ; Checks completion of write to specific registers
                        ; Repeats the same processing when an error occurs
                        ; Restore the CPU clock to its setting before the self
                        ; programming, after normal completion of the specific
                        ; sequence

MOV     MK0,#INT_MK0    ; Restores interrupt mask flag

EI

BR     StatusNormal

;-----
;END (abnormal termination processing); Perform processing to shift to
normal mode in order to return to normal processing
;-----
StatusError:

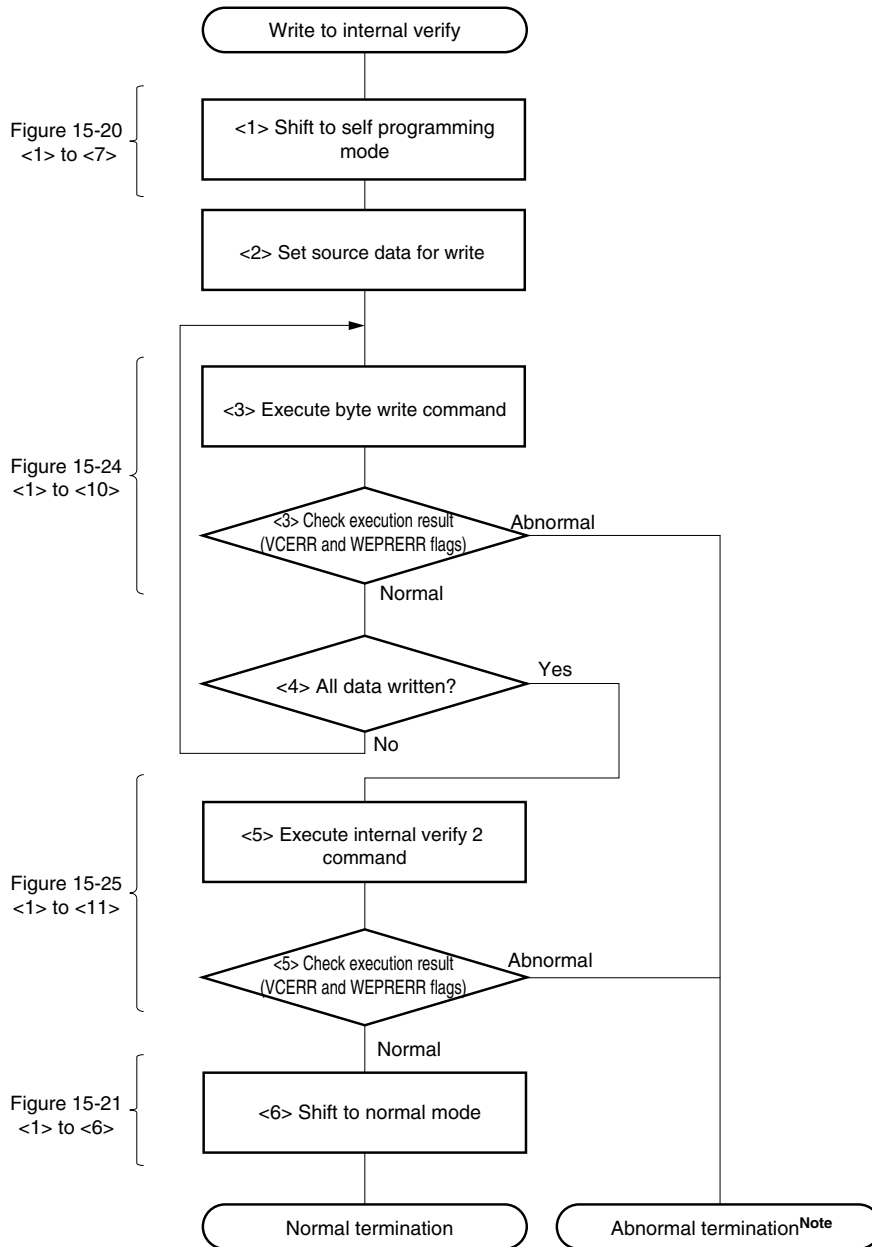
;-----
;END (normal termination processing)
;-----
StatusNormal:

```

**(2) Write to internal verify**

- <1> Mode is shifted from normal mode to self programming mode (<1> to <7> in 15.8.4)
- <2> Specification of source data for write
- <3> Execution of byte write → Error check (<1> to <10> in 15.8.8)
- <4> <3> is repeated until all data are written.
- <5> Execution of internal verify 2 → Error check (<1> to <11> in 15.8.9)
- <6> Mode is shifted from self programming mode to normal mode (<1> to <6> in 15.8.5)

**Figure 15-28. Example of Operation When Command Execution Time Should Be Minimized (from Write to Internal Verify)**



**Note** Perform processing to shift to normal mode in order to return to normal processing.

**Remark** <1> to <6> in Figure 15-28 correspond to <1> to <6> in 15.8.10 (2) above.

An example of a program when the command execution time (from write to internal verify) should be minimized in self programming mode is shown below.

```

;-----
;START
;-----
    MOV     MK0,#11111111B   ; Masks all interrupts
    MOV     FLCMD,#00H      ; Clears FLCMD register
    DI

ModeOnLoop:
    ; Configure settings so that the CPU clock ≥ 1 MHz
    MOV     PFS,#00H       ; Clears flash status register
    MOV     PFCMD,#0A5H    ; PFCMD register control
    MOV     FLPMC,#01H     ; FLPMC register control (sets value)
    MOV     FLPMC,#0FEH    ; FLPMC register control (inverts set value)
    MOV     FLPMC,#01H     ; Sets self programming mode with FLPMC register control
    ; (sets value)

    NOP
    HALT
    BT      PFS.0,$ModeOnLoop ; Checks completion of write to specific registers
    ; Repeats the same processing when an error occurs

FlashWrite:
    MOVW    HL,#DataAdrTop  ; Sets address at which data to be written is located
    MOVW    DE,#WriteAdr   ; Sets address at which data is to be written

FlashWriteLoop:
    MOV     FLCMD,#05H     ; Sets flash control command (byte write)
    MOV     A,D
    MOV     FLAPH,A       ; Sets address at which data is to be written
    MOV     A,E
    MOV     FLAPL,A       ; Sets address at which data is to be written
    MOV     A,[HL]
    MOV     FLW,A         ; Sets data to be written

    MOV     WDTE,#0ACH     ; Clears & restarts WDT
    HALT    ; Self programming is started
    MOV     A,PFS
    CMP     A,#00H
    BNZ     $StatusError   ; Checks write error
    ; Performs abnormal termination processing when an error
    ; occurs.

    INCW    HL             ; address at which data to be written is located + 1
    MOVW    AX,HL
    CMPW    AX,#DataAdrBtm ; Performs internal verify processing
    BNC     $FlashVerify   ; if write of all data is completed

```

```

        INCW    DE                ; Address at which data is to be written + 1
        BR     FlashWriteLoop

FlashVerify:
        MOVW   HL,#WriteAdr      ; Sets verify address

        MOV    FLCMD,#02H        ; Sets flash control command (internal verify 2)
        MOV    A,H
        MOV    FLAPH,A          ; Sets verify start address
        MOV    A,L
        MOV    FLAPL,A          ; Sets verify start address
        MOV    A,D
        MOV    FLAPHC,A         ; Sets verify end address
        MOV    A,E
        MOV    FLAPLC,A         ; Sets verify end address

        MOV    WDTE,#0ACH        ; Clears & restarts WDT
        HALT                    ; Self programming is started

        MOV    A,PFS
        CMP    A,#00H
        BNZ    $StatusError      ; Checks internal verify error
                                        ; Performs abnormal termination processing when an error
                                        ; occurs.

        MOV    FLCMD,#00H        ; Clears FLCMD register

ModeOffLoop:
        MOV    PFS,#00H          ; Clears flash status register
        MOV    PFCMD,#0A5H       ; PFCMD register control
        MOV    FLPMC,#00H        ; FLPMC register control (sets value)
        MOV    FLPMC,#0FFH       ; FLPMC register control (inverts set value)
        MOV    FLPMC,#00H        ; Sets normal mode via FLPMC register control (sets value)

        BT    PFS.0,$ModeOffLoop ; Checks completion of write to specific registers
                                        ; Repeats the same processing when an error occurs
                                        ; Restore the CPU clock to its setting before the self
                                        ; programming, after normal completion of the specific
                                        ; sequence

        MOV    MK0,#INT_MK0      ; Restores interrupt mask flag

        EI

        BR     StatusNormal

;-----
;END (abnormal termination processing); Perform processing to shift to
normal mode in order to return to normal processing
;-----
StatusError:

```

```
;------  
;END (normal termination processing)  
;------  
StatusNormal:  
  
;------  
; Data to be written  
;------  
DataAdrTop:  
    DB    XXH  
    DB    XXH  
    DB    XXH  
    DB    XXH  
  
    :  
    :  
  
    DB    XXH  
DataAdrBtm:  
;------
```

**Remark** Internal verify 2 is used in the above program example. Use internal verify 1 to verify a whole block.

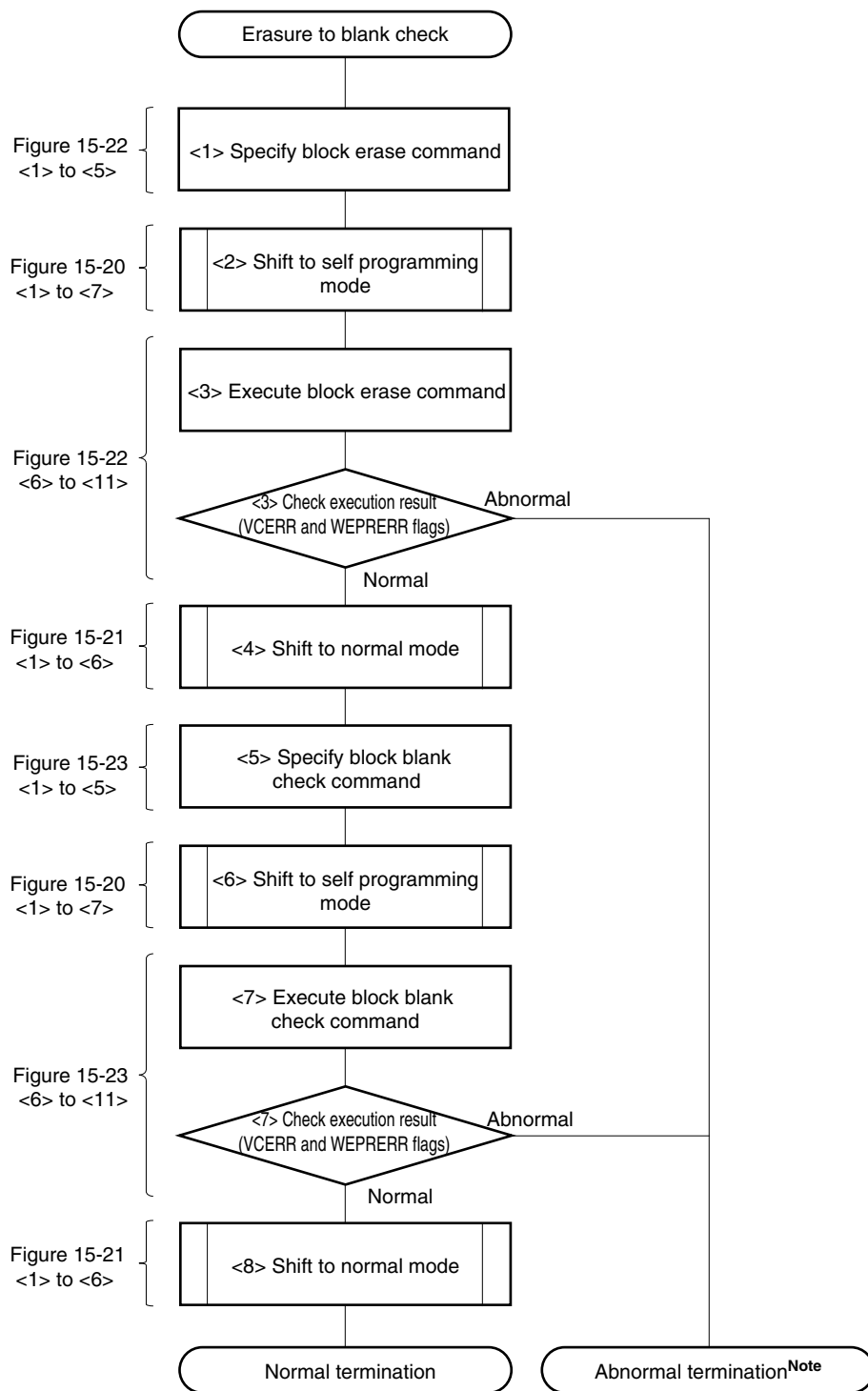
**15.8.11 Examples of operation when interrupt-disabled time should be minimized in self programming mode**

Examples of operation when the interrupt-disabled time should be minimized in self programming mode are explained below.

**(1) Erasure to blank check**

- <1> Specification of block erase command (<1> to <5> in **15.8.6**)
- <2> Mode is shifted from normal mode to self programming mode (<1> to <7> in **15.8.4**)
- <3> Execution of block erase command → Error check (<6> to <11> in **15.8.6**)
- <4> Mode is shifted from self programming mode to normal mode (<1> to <6> in **15.8.5**)
- <5> Specification of block blank check command (<1> to <5> in **15.8.7**)
- <6> Mode is shifted from normal mode to self programming mode (<1> to <7> in **15.8.4**)
- <7> Execution of block blank check command → Error check (<6> to <11> in **15.8.7**)
- <8> Mode is shifted from self programming mode to normal mode (<1> to <6> in **15.8.5**)

**Figure 15-29. Example of Operation When Interrupt-Disabled Time Should Be Minimized (from Erasure to Blank Check)**



**Note** Perform processing to shift to normal mode in order to return to normal processing.

**Remark** <1> to <8> in Figure 15-29 correspond to <1> to <8> in **15.8.11 (1)** (previous page).



An example of a program when the interrupt-disabled time (from erasure to blank check) should be minimized in self programming mode is shown below.

```

;-----
;START
;-----
FlashBlockErase:
    ; Sets erase command
    MOV     FLCMD,#03H      ; Sets flash control command (block erase)
    MOV     FLAPH,#07H     ; Sets number of block to be erased (block 7 is specified here)
    MOV     FLAPL,#00H    ; Fixes FLAPL to "00H"
    MOV     FLAPHC,#07H   ; Sets erase block compare number (same value as that of FLAPH)
    MOV     FLAPLC,#00H   ; Fixes FLAPLC to "00H"

    CALL    !ModeOn       ; Shift to self programming mode

    ; Execution of erase command
    MOV     PFS,#00H      ; Clears flash status register
    MOV     WDTE,#0ACH    ; Clears & restarts WDT
    HALT                    ; Self programming is started
    MOV     A,PFS
    CMP     A,#00H
    BNZ     $StatusError  ; Checks erase error
                                ; Performs abnormal termination processing when an error
                                ; occurs.

    CALL    !ModeOff      ; Shift to normal mode

    ; Sets blank check command
    MOV     FLCMD,#04H    ; Sets flash control command (block blank check)
    MOV     FLAPH,#07H    ; Sets block number for blank check (block 7 is specified here)
    MOV     FLAPL,#00H    ; Fixes FLAPL to "00H"
    MOV     FLAPHC,#07H   ; Sets blank check block compare number (same value as that of
                                ; FLAPH)
    MOV     FLAPLC,#0FFH  ; Fixes FLAPLC to "FFH"

    CALL    !ModeOn       ; Shift to self programming mode

    ; Execution of blank check command
    MOV     PFS,#00H      ; Clears flash status register
    MOV     WDTE,#0ACH    ; Clears & restarts WDT
    HALT                    ; Self programming is started
    MOV     A,PFS
    CMP     A,#00H
    BNZ     $StatusError  ; Checks blank check error
                                ; Performs abnormal termination processing when an error occurs

```

```

CALL    !ModeOff      ; Shift to normal mode

BR      StatusNormal

;-----
;END (abnormal termination processing); Perform processing to shift to
normal mode in order to return to normal processing
;-----
StatusError:

;-----
;END (normal termination processing)
;-----
StatusNormal:

;-----
;Processing to shift to self programming mode
;-----
ModeOn:
MOV     MK0,#11111111B ; Masks all interrupts
MOV     FLCMD,#00H     ; Clears FLCMD register

DI

ModeOnLoop:                ; Configure settings so that the CPU clock ≥ 1 MHz
MOV     PFS,#00H        ; Clears flash status register
MOV     PFCMD,#0A5H     ; PFCMD register control
MOV     FLPMC,#01H     ; FLPMC register control (sets value)
MOV     FLPMC,#0FEH    ; FLPMC register control (inverts set value)
MOV     FLPMC,#01H     ; Sets self programming mode via FLPMC register control (sets
                        ; value)

NOP
HALT
BT      PFS.0,$ModeOnLoop ; Checks completion of write to specific registers
                        ; Repeats the same processing when an error occurs

RET

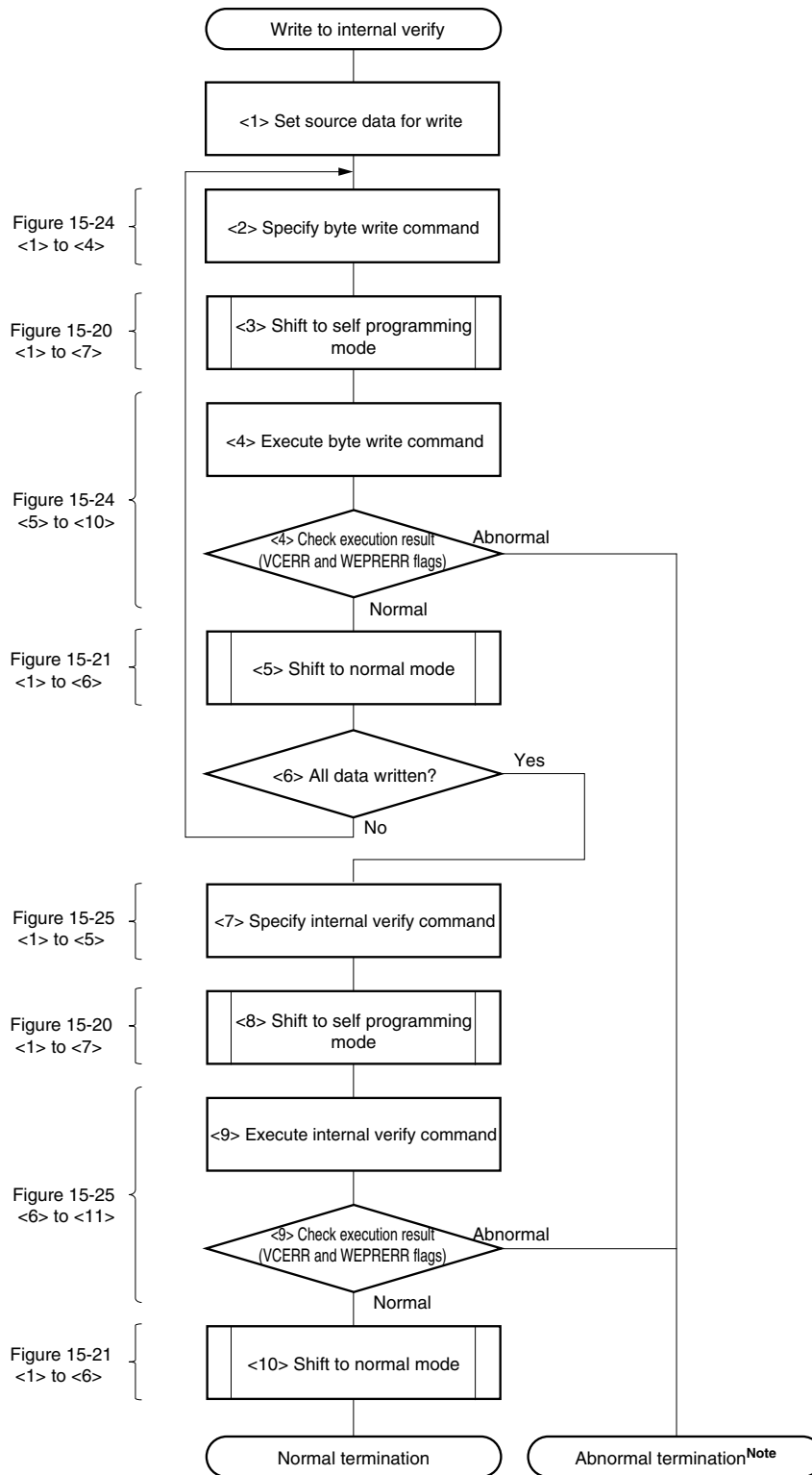
```

```
-----  
; Processing to shift to normal mode  
-----  
ModeOffLoop:  
    MOV     FLCMD,#00H      ; Clears FLCMD register  
    MOV     PFS,#00H       ; Clears flash status register  
    MOV     PFCMD,#0A5H    ; PFCMD register control  
    MOV     FLPMC,#00H     ; FLPMC register control (sets value)  
    MOV     FLPMC,#0FFH    ; FLPMC register control (inverts set value)  
    MOV     FLPMC,#00H     ; Sets normal mode via FLPMC register control (sets value)  
  
    BT     PFS.0,$ModeOffLoop ; Checks completion of write to specific registers  
                                ; Repeats the same processing when an error occurs  
                                ; Restore the CPU clock to its setting before the self  
                                ; programming, after normal completion of the specific  
                                ; sequence  
  
    MOV     MK0,#INT_MK0   ; Restores interrupt mask flag  
  
    EI  
  
    RET
```

**(2) Write to internal verify**

- <1> Specification of source data for write
- <2> Specification of byte write command (<1> to <4> in **15.8.8**)
- <3> Mode is shifted from normal mode to self programming mode (<1> to <7> in **15.8.4**)
- <4> Execution of byte write command → Error check (<5> to <10> in **15.8.8**)
- <5> Mode is shifted from self programming mode to normal mode (<1> to <6> in **15.8.5**)
- <6> <2> to <5> is repeated until all data are written.
- <7> The internal verify command is specified (<1> to <5> in **15.8.9**)
- <8> Mode is shifted from normal mode to self programming mode (<1> to <7> in **15.8.4**)
- <9> Execution of internal verify command → Error check (<6> to <11> in **15.8.9**)
- <10> Mode is shifted from self programming mode to normal mode (<1> to <6> in **15.8.5**)

**Figure 15-30. Example of Operation When Interrupt-Disabled Time Should Be Minimized (from Write to Internal Verify)**



**Note** Perform processing to shift to normal mode in order to return to normal processing.

**Remark** <1> to <10> in Figure 15-30 correspond to <1> to <10> in **15.8.11 (2)** (previous page).

An example of a program when the interrupt-disabled time (from write to internal verify) should be minimized in self programming mode is shown below.

```

;-----
;START
;-----
        ; Sets write command
FlashWrite:
        MOVW    HL,#DataAdrTop ; Sets address at which data to be written is located
        MOVW    DE,#WriteAdr  ; Sets address at which data is to be written

FlashWriteLoop:
        MOV     FLCMD,#05H     ; Sets flash control command (byte write)
        MOV     A,D
        MOV     FLAPH,A       ; Sets address at which data is to be written
        MOV     A,E
        MOV     FLAPL,A       ; Sets address at which data is to be written
        MOV     A,[HL]
        MOV     FLW,A         ; Sets data to be written

        CALL    !ModeOn       ; Shift to self programming mode

        ; Execution of write command
        MOV     PFS,#00H      ; Clears flash status register
        MOV     WDTE,#0ACH    ; Clears & restarts WDT
        HALT                    ; Self programming is started
        MOV     A,PFS
        CMP     A,#00H
        BNZ     $StatusError   ; Checks write error
                                ; Performs abnormal termination processing when an error
                                ; occurs.

        CALL    !ModeOff      ; Shift to normal mode

        MOV     MK0,#INT_MK0  ; Restores interrupt mask flag

        EI

        ; Judgment of writing all data
        INCW    HL             ; Address at which data to be written is located + 1
        MOVW    AX,HL
        CMPW    AX,#DataAdrBtm ; Performs internal verify processing
        BNC     $FlashVerify   ; if write of all data is completed

        INCW    DE             ; Address at which data is to be written + 1
        BR     FlashWriteLoop

        ; Setting internal verify command

```

```

FlashVerify:
    MOVW    HL,#WriteAdr    ; Sets verify address

    MOV     FLCMD,#02H      ; Sets flash control command (internal verify 2)
    MOV     A,H
    MOV     FLAPH,A        ; Sets verify start address
    MOV     A,L
    MOV     FLAPL,A        ; Sets verify start address
    MOV     A,D
    MOV     FLAPHC,A       ; Sets verify end address
    MOV     A,E
    MOV     FLAPLC,A       ; Sets verify end address

    CALL    !ModeOn        ; Shift to self programming mode

    ; Execution of internal verify command
    MOV     PFS,#00H       ; Clears flash status register
    MOV     WDTE,#0ACH     ; Clears & restarts WDT
    HALT                    ; Self programming is started
    MOV     A,PFS
    CMP     A,#00H
    BNZ     $StatusError   ; Checks internal verify error
                                ; Performs abnormal termination processing when an error occurs

    CALL    !ModeOff       ; Shift to normal mode

    BR     StatusNormal

;-----
;END (abnormal termination processing); Perform processing to shift to
normal mode in order to return to normal processing
;-----
StatusError:

;-----
;END (normal termination processing)
;-----
StatusNormal:

```

```

;-----
;Processing to shift to self programming mode
;-----
ModeOn:
    MOV     MK0,#11111111B ; Masks all interrupts
    MOV     FLCMD,#00H     ; Clears FLCMD register

    DI

ModeOnLoop:
    ; Configure settings so that the CPU clock ≥ 1 MHz
    MOV     PFS,#00H      ; Clears flash status register
    MOV     PFCMD,#0A5H   ; PFCMD register control
    MOV     FLPMC,#01H    ; FLPMC register control (sets value)
    MOV     FLPMC,#0FEH   ; FLPMC register control (inverts set value)
    MOV     FLPMC,#01H    ; Sets self programming mode via FLPMC register control (sets
    ; value)

    NOP
    HALT
    BT      PFS.0,$ModeOnLoop ; Checks completion of write to specific registers
    ; Repeats the same processing when an error occurs

    RET

;-----
; Processing to shift to normal mode
;-----
ModeOffLoop:
    MOV     FLCMD,#00H    ; Clears FLCMD register
    MOV     PFS,#00H     ; Clears flash status register
    MOV     PFCMD,#0A5H  ; PFCMD register control
    MOV     FLPMC,#00H   ; FLPMC register control (sets value)
    MOV     FLPMC,#0FFH  ; FLPMC register control (inverts set value)
    MOV     FLPMC,#00H   ; Sets normal mode via FLPMC register control (sets value)

    BT      PFS.0,$ModeOffloop ; Checks completion of write to specific registers
    ; Repeats the same processing when an error occurs
    ; Restore the CPU clock to its setting before the self
    ; programming, after normal completion of the specific
    ; sequence
    MOV     MK0,#INT_MK0 ; Restores interrupt mask flag

    EI

    RET

```



```
;-----  
;Data to be written  
;-----  
DataAdrTop:  
    DB      XXH  
    DB      XXH  
    DB      XXH  
    DB      XXH  
  
    :  
    :  
  
    DB      XXH  
DataAdrBtm:  
;-----
```

**Remark** Internal verify 2 is used in the above program example. Use internal verify 1 to verify a whole block.

## CHAPTER 16 INSTRUCTION SET OVERVIEW

This chapter lists the instruction set of the  $\mu$ PD78F9510, 78F9511, 78F9512. For details of the operation and machine language (instruction code) of each instruction, refer to **78K/0S Series Instructions User's Manual (U11047E)**.

### 16.1 Operation

#### 16.1.1 Operand identifiers and description methods

Operands are described in "Operand" column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more description methods, select one of them. Uppercase letters and the symbols #, !, \$, and [ ] are key words and are described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- \$: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #, !, \$ and [ ] symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

**Table 16-1. Operand Identifiers and Description Methods**

Identifier	Description Method
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH Immediate data or labels FE20H to FF1FH Immediate data or labels (even addresses only)
addr16 addr5	0000H to FFFFH Immediate data or labels (only even addresses for 16-bit data transfer instructions) 0040H to 007FH Immediate data or labels (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

**Remark** For symbols of special function registers, see **Table 3-3 Special Function Registers**.

**16.1.2 Description of “Operation” column**

A:	A register; 8-bit accumulator
X:	X register
B:	B register
C:	C register
D:	D register
E:	E register
H:	H register
L:	L register
AX:	AX register pair; 16-bit accumulator
BC:	BC register pair
DE:	DE register pair
HL:	HL register pair
PC:	Program counter
SP:	Stack pointer
PSW:	Program status word
CY:	Carry flag
AC:	Auxiliary carry flag
Z:	Zero flag
IE:	Interrupt request enable flag
( ):	Memory contents indicated by address or register contents in parentheses
×H, ×L:	Higher 8 bits and lower 8 bits of 16-bit register
∧:	Logical product (AND)
∨:	Logical sum (OR)
⊕:	Exclusive logical sum (exclusive OR)
—:	Inverted data
addr16:	16-bit immediate data or label
jdisp8:	Signed 8-bit data (displacement value)

**16.1.3 Description of “Flag” column**

(Blank):	Unchanged
0:	Cleared to 0
1:	Set to 1
×:	Set/cleared according to the result
R:	Previously saved value is stored

## 16.2 Operation List

Mnemonic	Operand	Bytes	Clocks	Operation	Flag			
					Z	AC	CY	
MOV	r, #byte	3	6	$r \leftarrow \text{byte}$				
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow \text{byte}$				
	sfr, #byte	3	6	$\text{sfr} \leftarrow \text{byte}$				
	A, r	Note 1	2	4	$A \leftarrow r$			
	r, A	Note 1	2	4	$r \leftarrow A$			
	A, saddr		2	4	$A \leftarrow (\text{saddr})$			
	saddr, A		2	4	$(\text{saddr}) \leftarrow A$			
	A, sfr		2	4	$A \leftarrow \text{sfr}$			
	sfr, A		2	4	$\text{sfr} \leftarrow A$			
	A, !addr16		3	8	$A \leftarrow (\text{addr16})$			
	!addr16, A		3	8	$(\text{addr16}) \leftarrow A$			
	PSW, #byte		3	6	$\text{PSW} \leftarrow \text{byte}$	x	x	x
	A, PSW		2	4	$A \leftarrow \text{PSW}$			
	PSW, A		2	4	$\text{PSW} \leftarrow A$	x	x	x
	A, [DE]		1	6	$A \leftarrow (\text{DE})$			
	[DE], A		1	6	$(\text{DE}) \leftarrow A$			
	A, [HL]		1	6	$A \leftarrow (\text{HL})$			
	[HL], A		1	6	$(\text{HL}) \leftarrow A$			
	A, [HL + byte]		2	6	$A \leftarrow (\text{HL} + \text{byte})$			
	[HL + byte], A		2	6	$(\text{HL} + \text{byte}) \leftarrow A$			
XCH	A, X		1	4	$A \leftrightarrow X$			
	A, r	Note 2	2	6	$A \leftrightarrow r$			
	A, saddr		2	6	$A \leftrightarrow (\text{saddr})$			
	A, sfr		2	6	$A \leftrightarrow \text{sfr}$			
	A, [DE]		1	8	$A \leftrightarrow (\text{DE})$			
	A, [HL]		1	8	$A \leftrightarrow (\text{HL})$			
	A, [HL, byte]		2	8	$A \leftrightarrow (\text{HL} + \text{byte})$			

- Notes**
1. Except  $r = A$ .
  2. Except  $r = A, X$ .

**Remark** One instruction clock cycle is one CPU clock cycle ( $f_{\text{CPU}}$ ) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
MOVW	rp, #word	3	6	$rp \leftarrow \text{word}$			
	AX, saddrp	2	6	$AX \leftarrow (\text{saddrp})$			
	saddrp, AX	2	8	$(\text{saddrp}) \leftarrow AX$			
	AX, rp <small>Note</small>	1	4	$AX \leftarrow rp$			
	rp, AX <small>Note</small>	1	4	$rp \leftarrow AX$			
XCHW	AX, rp <small>Note</small>	1	8	$AX \leftrightarrow rp$			
ADD	A, #byte	2	4	$A, CY \leftarrow A + \text{byte}$	x	x	x
	saddr, #byte	3	6	$(\text{saddr}), CY \leftarrow (\text{saddr}) + \text{byte}$	x	x	x
	A, r	2	4	$A, CY \leftarrow A + r$	x	x	x
	A, saddr	2	4	$A, CY \leftarrow A + (\text{saddr})$	x	x	x
	A, !addr16	3	8	$A, CY \leftarrow A + (\text{addr16})$	x	x	x
	A, [HL]	1	6	$A, CY \leftarrow A + (\text{HL})$	x	x	x
	A, [HL + byte]	2	6	$A, CY \leftarrow A + (\text{HL} + \text{byte})$	x	x	x
ADDC	A, #byte	2	4	$A, CY \leftarrow A + \text{byte} + CY$	x	x	x
	saddr, #byte	3	6	$(\text{saddr}), CY \leftarrow (\text{saddr}) + \text{byte} + CY$	x	x	x
	A, r	2	4	$A, CY \leftarrow A + r + CY$	x	x	x
	A, saddr	2	4	$A, CY \leftarrow A + (\text{saddr}) + CY$	x	x	x
	A, !addr16	3	8	$A, CY \leftarrow A + (\text{addr16}) + CY$	x	x	x
	A, [HL]	1	6	$A, CY \leftarrow A + (\text{HL}) + CY$	x	x	x
	A, [HL + byte]	2	6	$A, CY \leftarrow A + (\text{HL} + \text{byte}) + CY$	x	x	x
SUB	A, #byte	2	4	$A, CY \leftarrow A - \text{byte}$	x	x	x
	saddr, #byte	3	6	$(\text{saddr}), CY \leftarrow (\text{saddr}) - \text{byte}$	x	x	x
	A, r	2	4	$A, CY \leftarrow A - r$	x	x	x
	A, saddr	2	4	$A, CY \leftarrow A - (\text{saddr})$	x	x	x
	A, !addr16	3	8	$A, CY \leftarrow A - (\text{addr16})$	x	x	x
	A, [HL]	1	6	$A, CY \leftarrow A - (\text{HL})$	x	x	x
	A, [HL + byte]	2	6	$A, CY \leftarrow A - (\text{HL} + \text{byte})$	x	x	x

**Note** Only when rp = BC, DE, or HL.

**Remark** One instruction clock cycle is one CPU clock cycle ( $f_{CPU}$ ) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
SUBC	A, #byte	2	4	$A, CY \leftarrow A - \text{byte} - CY$	×	×	×
	saddr, #byte	3	6	$(\text{saddr}), CY \leftarrow (\text{saddr}) - \text{byte} - CY$	×	×	×
	A, r	2	4	$A, CY \leftarrow A - r - CY$	×	×	×
	A, saddr	2	4	$A, CY \leftarrow A - (\text{saddr}) - CY$	×	×	×
	A, !addr16	3	8	$A, CY \leftarrow A - (\text{addr16}) - CY$	×	×	×
	A, [HL]	1	6	$A, CY \leftarrow A - (\text{HL}) - CY$	×	×	×
	A, [HL + byte]	2	6	$A, CY \leftarrow A - (\text{HL} + \text{byte}) - CY$	×	×	×
AND	A, #byte	2	4	$A \leftarrow A \wedge \text{byte}$	×		
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow (\text{saddr}) \wedge \text{byte}$	×		
	A, r	2	4	$A \leftarrow A \wedge r$	×		
	A, saddr	2	4	$A \leftarrow A \wedge (\text{saddr})$	×		
	A, !addr16	3	8	$A \leftarrow A \wedge (\text{addr16})$	×		
	A, [HL]	1	6	$A \leftarrow A \wedge (\text{HL})$	×		
	A, [HL + byte]	2	6	$A \leftarrow A \wedge (\text{HL} + \text{byte})$	×		
OR	A, #byte	2	4	$A \leftarrow A \vee \text{byte}$	×		
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow (\text{saddr}) \vee \text{byte}$	×		
	A, r	2	4	$A \leftarrow A \vee r$	×		
	A, saddr	2	4	$A \leftarrow A \vee (\text{saddr})$	×		
	A, !addr16	3	8	$A \leftarrow A \vee (\text{addr16})$	×		
	A, [HL]	1	6	$A \leftarrow A \vee (\text{HL})$	×		
	A, [HL + byte]	2	6	$A \leftarrow A \vee (\text{HL} + \text{byte})$	×		
XOR	A, #byte	2	4	$A \leftarrow A \nabla \text{byte}$	×		
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow (\text{saddr}) \nabla \text{byte}$	×		
	A, r	2	4	$A \leftarrow A \nabla r$	×		
	A, saddr	2	4	$A \leftarrow A \nabla (\text{saddr})$	×		
	A, !addr16	3	8	$A \leftarrow A \nabla (\text{addr16})$	×		
	A, [HL]	1	6	$A \leftarrow A \nabla (\text{HL})$	×		
	A, [HL + byte]	2	6	$A \leftarrow A \nabla (\text{HL} + \text{byte})$	×		

**Remark** One instruction clock cycle is one CPU clock cycle ( $f_{\text{CPU}}$ ) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r – 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, A <sub>7</sub> ← A <sub>0</sub> , A <sub>m-1</sub> ← A <sub>m</sub> ) × 1			×
ROL	A, 1	1	2	(CY, A <sub>0</sub> ← A <sub>7</sub> , A <sub>m+1</sub> ← A <sub>m</sub> ) × 1			×
RORC	A, 1	1	2	(CY ← A <sub>0</sub> , A <sub>7</sub> ← CY, A <sub>m-1</sub> ← A <sub>m</sub> ) × 1			×
ROLC	A, 1	1	2	(CY ← A <sub>7</sub> , A <sub>0</sub> ← CY, A <sub>m+1</sub> ← A <sub>m</sub> ) × 1			×
SET1	saddr.bit	3	6	(saddr.bit) ← 1			
	sfr.bit	3	6	sfr.bit ← 1			
	A.bit	2	4	A.bit ← 1			
	PSW.bit	3	6	PSW.bit ← 1	×	×	×
	[HL].bit	2	10	(HL).bit ← 1			
CLR1	saddr.bit	3	6	(saddr.bit) ← 0			
	sfr.bit	3	6	sfr.bit ← 0			
	A.bit	2	4	A.bit ← 0			
	PSW.bit	3	6	PSW.bit ← 0	×	×	×
	[HL].bit	2	10	(HL).bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×

**Remark** One instruction clock cycle is one CPU clock cycle ( $f_{CPU}$ ) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
CALL	laddr16	3	6	$(SP - 1) \leftarrow (PC + 3)_H, (SP - 2) \leftarrow (PC + 3)_L,$ $PC \leftarrow \text{addr16}, SP \leftarrow SP - 2$			
CALLT	[addr5]	1	8	$(SP - 1) \leftarrow (PC + 1)_H, (SP - 2) \leftarrow (PC + 1)_L,$ $PC_H \leftarrow (00000000, \text{addr5} + 1),$ $PC_L \leftarrow (00000000, \text{addr5}), SP \leftarrow SP - 2$			
RET		1	6	$PC_H \leftarrow (SP + 1), PC_L \leftarrow (SP), SP \leftarrow SP + 2$			
RETI		1	8	$PC_H \leftarrow (SP + 1), PC_L \leftarrow (SP),$ $PSW \leftarrow (SP + 2), SP \leftarrow SP + 3, NMIS \leftarrow 0$	R	R	R
PUSH	PSW	1	2	$(SP - 1) \leftarrow PSW, SP \leftarrow SP - 1$			
	rp	1	4	$(SP - 1) \leftarrow rp_H, (SP - 2) \leftarrow rp_L, SP \leftarrow SP - 2$			
POP	PSW	1	4	$PSW \leftarrow (SP), SP \leftarrow SP + 1$	R	R	R
	rp	1	6	$rp_H \leftarrow (SP + 1), rp_L \leftarrow (SP), SP \leftarrow SP + 2$			
MOVW	SP, AX	2	8	$SP \leftarrow AX$			
	AX, SP	2	6	$AX \leftarrow SP$			
BR	laddr16	3	6	$PC \leftarrow \text{addr16}$			
	\$addr16	2	6	$PC \leftarrow PC + 2 + \text{jdisp8}$			
	AX	1	6	$PC_H \leftarrow A, PC_L \leftarrow X$			
BC	\$saddr16	2	6	$PC \leftarrow PC + 2 + \text{jdisp8}$ if CY = 1			
BNC	\$saddr16	2	6	$PC \leftarrow PC + 2 + \text{jdisp8}$ if CY = 0			
BZ	\$saddr16	2	6	$PC \leftarrow PC + 2 + \text{jdisp8}$ if Z = 1			
BNZ	\$saddr16	2	6	$PC \leftarrow PC + 2 + \text{jdisp8}$ if Z = 0			
BT	saddr.bit, \$addr16	4	10	$PC \leftarrow PC + 4 + \text{jdisp8}$ if (saddr.bit) = 1			
	sfr.bit, \$addr16	4	10	$PC \leftarrow PC + 4 + \text{jdisp8}$ if sfr.bit = 1			
	A.bit, \$addr16	3	8	$PC \leftarrow PC + 3 + \text{jdisp8}$ if A.bit = 1			
	PSW.bit, \$addr16	4	10	$PC \leftarrow PC + 4 + \text{jdisp8}$ if PSW.bit = 1			
BF	saddr.bit, \$addr16	4	10	$PC \leftarrow PC + 4 + \text{jdisp8}$ if (saddr.bit) = 0			
	sfr.bit, \$addr16	4	10	$PC \leftarrow PC + 4 + \text{jdisp8}$ if sfr.bit = 0			
	A.bit, \$addr16	3	8	$PC \leftarrow PC + 3 + \text{jdisp8}$ if A.bit = 0			
	PSW.bit, \$addr16	4	10	$PC \leftarrow PC + 4 + \text{jdisp8}$ if PSW.bit = 0			
DBNZ	B, \$addr16	2	6	$B \leftarrow B - 1,$ then $PC \leftarrow PC + 2 + \text{jdisp8}$ if $B \neq 0$			
	C, \$addr16	2	6	$C \leftarrow C - 1,$ then $PC \leftarrow PC + 2 + \text{jdisp8}$ if $C \neq 0$			
	saddr, \$addr16	3	8	$(\text{saddr}) \leftarrow (\text{saddr}) - 1,$ then $PC \leftarrow PC + 3 + \text{jdisp8}$ if $(\text{saddr}) \neq 0$			
NOP		1	2	No Operation			
EI		3	6	$IE \leftarrow 1$ (Enable Interrupt)			
DI		3	6	$IE \leftarrow 0$ (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

**Remark** One instruction clock cycle is one CPU clock cycle ( $f_{CPU}$ ) selected by the processor clock control register (PCC).



### 16.3 Instructions Listed by Addressing Type

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, INC, DEC, ROR, ROL, RORC, ROLC, PUSH, POP, DBNZ

2nd Operand 1st Operand	#byte	A	r	sfr	saddr	laddr16	PSW	[DE]	[HL]	[HL + byte]	\$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV <sup>Note</sup> XCH <sup>Note</sup> ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV ADD SUB SUBC AND OR XOR CMP	MOV	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP			ROR ROL RORC ROLC	
r	MOV	MOV											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
laddr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											
[HL + byte]		MOV											

**Note** Except r = A.

**(2) 16-bit instructions**

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

1st Operand \ 2nd Operand	#word	AX	rp <sup>Note</sup>	saddrp	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	
rp	MOVW	MOVW <sup>Note</sup>				INCW DECW PUSH POP
saddrp		MOVW				
sp		MOVW				

**Note** Only when rp = BC, DE, or HL.

**(3) Bit manipulation instructions**

SET1, CLR1, NOT1, BT, BF

1st Operand \ 2nd Operand	\$addr16	None
A.bit	BT BF	SET1 CLR1
sfr.bit	BT BF	SET1 CLR1
saddr.bit	BT BF	SET1 CLR1
PSW.bit	BT BF	SET1 CLR1
[HL].bit		SET1 CLR1
CY		SET1 CLR1 NOT1

**(4) Call instructions/branch instructions**

CALL, CALLT, BR, BC, BNC, BZ, BNZ, DBNZ

2nd Operand \ 1st Operand	AX	!addr16	[addr5]	\$addr16
Basic instructions	BR	CALL BR	CALLT	BR BC BNC BZ BNZ
Compound instructions				DBNZ

**(5) Other instructions**

RET, RETI, NOP, EI, DI, HALT, STOP

## CHAPTER 17 ELECTRICAL SPECIFICATIONS (TARGET)

**Caution** These specifications show target values, which may change after device evaluation. The operating voltage range may also change.

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

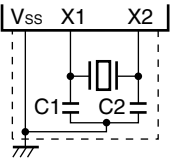
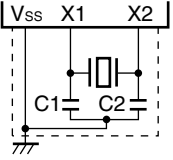
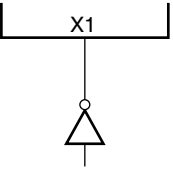
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD}$		-0.3 to +6.5	V
	$V_{SS}$		-0.3 to +0.3	V
Input voltage	$V_I$	P20 to P23, P32, P34, P40 to P47	-0.3 to $V_{DD} + 0.3^{\text{Note}}$	V
Output voltage	$V_O$		-0.3 to $V_{DD} + 0.3^{\text{Note}}$	V
Output current, high	$I_{OH}$	Per pin	-10.0	mA
		Total of P20 to P23, P32, P40 to P47	-44.0	mA
Output current, low	$I_{OL}$	Per pin	20.0	mA
		Total of P20 to P23, P32, P40 to P47	44.0	mA
Operating ambient temperature	$T_A$	In normal operation mode	-40 to +85	$^\circ\text{C}$
		During flash memory programming		$^\circ\text{C}$
Storage temperature	$T_{stg}$	Flash memory blank status	-65 to +150	$^\circ\text{C}$
		Flash memory programming already performed	-40 to +125	$^\circ\text{C}$

**Note** Must be 6.5 V or lower

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

**X1 Oscillator Characteristics ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 2.0$  to  $5.5\text{ V}^{\text{Note 1}}$ ,  $V_{SS} = 0\text{ V}$ )**

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency ( $f_x$ ) <sup>Note 2</sup>		1		10.0	MHz
Crystal resonator		Oscillation frequency ( $f_x$ ) <sup>Note 2</sup>		1		10.0	MHz
External clock		X1 input frequency ( $f_x$ ) <sup>Note 2</sup>	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		10.0	MHz
			$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	1		5.0	
		X1 input high-/low-level width ( $t_{xH}$ , $t_{xL}$ )	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.045		0.5	$\mu\text{s}$
			$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	0.09		0.5	

- Notes 1.** Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage ( $V_{POC}$ ) of the power-on-clear (POC) circuit is  $2.1\text{ V} \pm 0.1\text{ V}$ .
- 2.** Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

**Caution** When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as  $V_{SS}$ .
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

**Remark** For the resonator selection and oscillator constant, users are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

**High-Speed Internal Oscillator Characteristics ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 2.0$  to  $5.5\text{ V}^{\text{Note 1}}$ ,  $V_{SS} = 0\text{ V}$ )**

Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
High-speed internal oscillator	Oscillation frequency ( $f_x = 8\text{ MHz}^{\text{Note 2}}$ ) deviation	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 3$	%
		$T_A = -10$ to $+70^\circ\text{C}$				
		$T_A = -40$ to $+85^\circ\text{C}$			$\pm 5$	%
	Oscillation frequency ( $f_x$ ) <sup>Note 2</sup>	$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	5.5			MHz

**Notes 1.** Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage ( $V_{POC}$ ) of the power-on-clear (POC) circuit is  $2.1\text{ V} \pm 0.1\text{ V}$ .

**2.** Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

**Low-Speed Internal Oscillator Characteristics ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 2.0$  to  $5.5\text{ V}^{\text{Note 1}}$ ,  $V_{SS} = 0\text{ V}$ )**

Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Low-speed internal oscillator	Oscillation frequency ( $f_{RL}$ )		120	240	480	kHz

**Note** Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage ( $V_{POC}$ ) of the power-on-clear (POC) circuit is  $2.1\text{ V} \pm 0.1\text{ V}$ .

**DC Characteristics ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 2.0$  to  $5.5\text{ V}^{\text{Note}}$ ,  $V_{SS} = 0\text{ V}$ ) (1/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	$I_{OH}$	Per pin	$2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			-5	mA
		Total of all pins	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			-25	mA
			$2.0\text{ V} \leq V_{DD} < 4.0\text{ V}$			-15	mA
Output current, low	$I_{OL}$	Per pin	$2.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			10	mA
		Total of all pins	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			30	mA
			$2.0\text{ V} \leq V_{DD} < 4.0\text{ V}$			15	mA
Input voltage, high	$V_{IH1}$	P23 in external clock mode and pins other than P20 and P21		$0.8V_{DD}$		$V_{DD}$	V
	$V_{IH2}$	P23 in other than external clock mode, P20 and P21		$0.7V_{DD}$		$V_{DD}$	V
Input voltage, low	$V_{IL1}$	P23 in external clock mode and pins other than P20 and P21		0		$0.2V_{DD}$	V
	$V_{IL2}$	P23 in other than external clock mode, P20 and P21		0		$0.3V_{DD}$	V
Output voltage, high	$V_{OH}$	Total of output pins $I_{OH} = -15\text{ mA}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ $I_{OH} = -5\text{ mA}$	$V_{DD} - 1.0$			V
		$I_{OH} = -100\ \mu\text{A}$	$2.0\text{ V} \leq V_{DD} < 4.0\text{ V}$	$V_{DD} - 0.5$			V
Output voltage, low	$V_{OL}$	Total of output pins $I_{OL} = 30\text{ mA}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ $I_{OL} = 10\text{ mA}$			1.3	V
		$2.0\text{ V} \leq V_{DD} < 4.0\text{ V}$ $I_{OL} = 400\ \mu\text{A}$				0.4	V
Input leakage current, high	$I_{LIH}$	$V_i = V_{DD}$	Pins other than X1			1	$\mu\text{A}$
Input leakage current, low	$I_{LIL}$	$V_i = 0\text{ V}$	Pins other than X1			-1	$\mu\text{A}$
Output leakage current, high	$I_{LOH}$	$V_o = V_{DD}$	Pins other than X2			1	$\mu\text{A}$
Output leakage current, low	$I_{LOL}$	$V_o = 0\text{ V}$	Pins other than X2			-1	$\mu\text{A}$
Pull-up resistance value	$R_{PU}$	$V_i = 0\text{ V}$		10	30	100	$\text{k}\Omega$
Pull-down resistance value	$R_{PD}$	P22, P23, reset status		10	30	100	$\text{k}\Omega$

**Note** Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage ( $V_{POC}$ ) of the power-on-clear (POC) circuit is  $2.1\text{ V} \pm 0.1\text{ V}$ .

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

**DC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 2.0 to 5.5 V<sup>Note 1</sup>, V<sub>SS</sub> = 0 V) (2/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current <sup>Note 2</sup>	I <sub>DD1</sub> <sup>Note 3</sup>	Crystal/ceramic oscillation, external clock input oscillation operating mode <sup>Note 6</sup>	f <sub>X</sub> = 10 MHz V <sub>DD</sub> = 5.0 V ±10% <sup>Note 4</sup>		6.1	12.2	mA	
			f <sub>X</sub> = 6 MHz V <sub>DD</sub> = 5.0 V ±10% <sup>Note 4</sup>		5.5	11.0	mA	
			f <sub>X</sub> = 5 MHz V <sub>DD</sub> = 3.0 V ±10% <sup>Note 5</sup>		3.0	6.0	mA	
	I <sub>DD2</sub>	Crystal/ceramic oscillation, external clock input HALT mode <sup>Note 6</sup>	f <sub>X</sub> = 10 MHz V <sub>DD</sub> = 5.0 V ±10% <sup>Note 4</sup>	When peripheral functions are stopped		1.7	3.8	mA
				When peripheral functions are operating			6.7	
			f <sub>X</sub> = 6 MHz V <sub>DD</sub> = 5.0 V ±10% <sup>Note 4</sup>	When peripheral functions are stopped		1.3	3.0	mA
				When peripheral functions are operating			6.0	
			f <sub>X</sub> = 5 MHz V <sub>DD</sub> = 3.0 V ±10% <sup>Note 5</sup>	When peripheral functions are stopped		0.48	1	mA
				When peripheral functions are operating			2.1	
	I <sub>DD3</sub> <sup>Note 3</sup>	High-speed internal oscillation operating mode <sup>Note 7</sup>	f <sub>X</sub> = 8 MHz V <sub>DD</sub> = 5.0 V ±10% <sup>Note 4</sup>		5.0	10.0	mA	
	I <sub>DD4</sub>	High-speed internal oscillation HALT mode <sup>Note 7</sup>	f <sub>X</sub> = 8 MHz V <sub>DD</sub> = 5.0 V ±10% <sup>Note 4</sup>	When peripheral functions are stopped		1.4	3.2	mA
				When peripheral functions are operating			5.9	
I <sub>DD5</sub>	STOP mode	V <sub>DD</sub> = 5.0 V ±10%	When low-speed internal oscillation is stopped		3.5	20.0	μA	
			When low-speed internal oscillation is operating		17.5	32.0		
		V <sub>DD</sub> = 3.0 V ±10%	When low-speed internal oscillation is stopped		3.5	15.5	μA	
			When low-speed internal oscillation is operating		11.0	26.0		

- Notes**
1. Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage (V<sub>POC</sub>) of the power-on-clear (POC) circuit is 2.1 V ±0.1 V.
  2. Total current flowing through the internal power supply (V<sub>DD</sub>). Peripheral operation current is included (however, the current that flows through the pull-up resistors of ports is not included).
  3. These currents include peripheral operation currents.
  4. When the processor clock control register (PCC) is set to 00H.
  5. When the processor clock control register (PCC) is set to 02H.
  6. When crystal/ceramic oscillation clock, external clock input is selected as the system clock source using the option byte.
  7. When high-speed internal oscillation clock is selected as the system clock source using the option byte.



## AC Characteristics

**Basic operation ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 2.0$  to  $5.5\text{ V}^{\text{Note 1}}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Cycle time (minimum instruction execution time)	$T_{CY}$	Crystal/ceramic oscillation clock, external clock input	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.2		16	$\mu\text{s}$
			$3.0\text{ V} \leq V_{DD} < 4.0\text{ V}$	0.33		16	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} < 3.0\text{ V}$	0.4		16	$\mu\text{s}$
			$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	1		16	$\mu\text{s}$
		High-speed internal oscillation clock	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.23		4.22	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	0.47		4.22	$\mu\text{s}$
$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	0.95			4.22	$\mu\text{s}$		
TI000 input high-level width, low-level width	$t_{TIH}$ , $t_{TIL}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$2/f_{sam+}$ 0.1 <sup>Note 2</sup>			$\mu\text{s}$	
		$2.0\text{ V} \leq V_{DD} < 4.0\text{ V}$	$2/f_{sam+}$ 0.2 <sup>Note 2</sup>			$\mu\text{s}$	
Interrupt input high-level width, low-level width	$t_{INTH}$ , $t_{INTL}$		1			$\mu\text{s}$	
RESET input low-level width	$t_{RSL}$		2			$\mu\text{s}$	

**Notes 1.** Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage ( $V_{POC}$ ) of the power-on-clear (POC) circuit is  $2.1\text{ V} \pm 0.1\text{ V}$ .

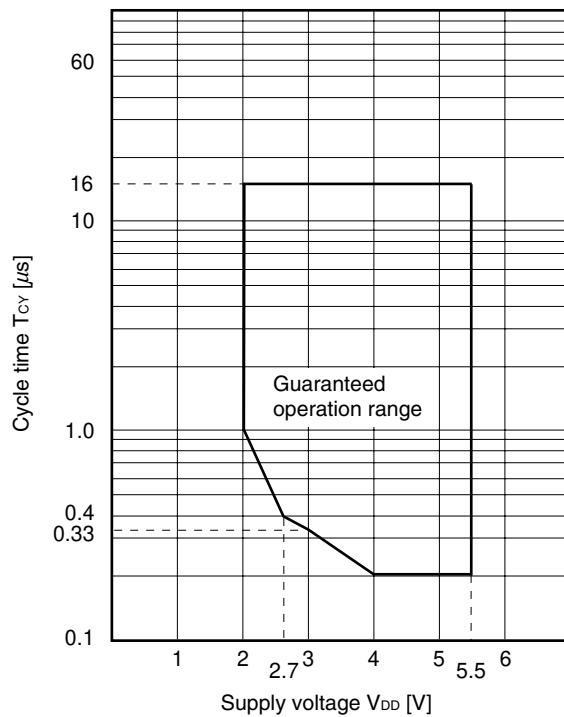
**2.** Selection of  $f_{sam} = f_{XP}$ ,  $f_{XP}/4$ , or  $f_{XP}/256$  is possible using bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00). Note that when selecting the TI000 valid edge as the count clock,  $f_{sam} = f_{XP}$ .

**CPU Clock Frequency, Peripheral Clock Frequency**

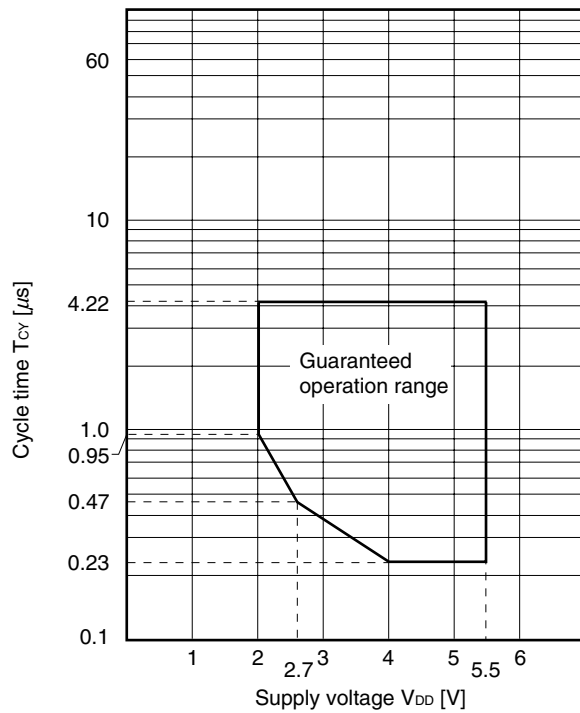
Parameter	Conditions	CPU Clock ( $f_{CPU}$ )	Peripheral Clock ( $f_{XP}$ )
Ceramic resonator, crystal resonator, external clock	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$125\text{ kHz} \leq f_{CPU} \leq 10\text{ MHz}$	$125\text{ kHz} \leq f_{XP} \leq 10\text{ MHz}$
	$3.0\text{ V} \leq V_{DD} < 4.0\text{ V}$	$125\text{ kHz} \leq f_{CPU} \leq 6\text{ MHz}$	
	$2.7\text{ V} \leq V_{DD} < 3.0\text{ V}$	$125\text{ kHz} \leq f_{CPU} \leq 5\text{ MHz}$	
	$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}^{\text{Note}}$	$125\text{ kHz} \leq f_{CPU} \leq 2\text{ MHz}$	$125\text{ kHz} \leq f_{XP} \leq 5\text{ MHz}$
High-speed internal oscillator	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$500\text{ kHz (Typ.)} \leq f_{CPU} \leq 8\text{ MHz (Typ.)}$	$500\text{ kHz (Typ.)} \leq f_{XP} \leq 8\text{ MHz (Typ.)}$
	$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	$500\text{ kHz (Typ.)} \leq f_{CPU} \leq 4\text{ MHz (Typ.)}$	
	$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}^{\text{Note}}$	$500\text{ kHz (Typ.)} \leq f_{CPU} \leq 2\text{ MHz (Typ.)}$	

**Note** Use this product in a voltage range of 2.2 to 5.5 V because the detection voltage ( $V_{POC}$ ) of the power-on-clear (POC) circuit is  $2.1\text{ V} \pm 0.1\text{ V}$ .

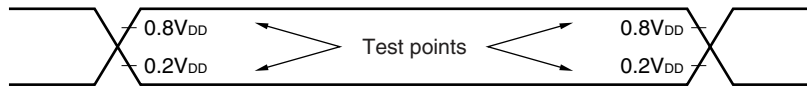
**T<sub>CY</sub> vs. V<sub>DD</sub> (Crystal/Ceramic Oscillation Clock, External Clock Input)**



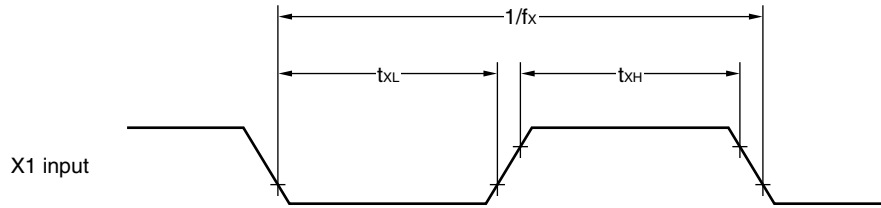
**T<sub>CY</sub> vs. V<sub>DD</sub> (High-speed internal oscillator Clock)**



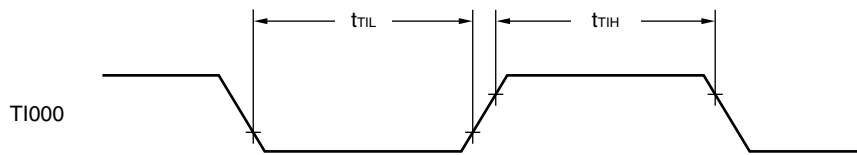
**AC Timing Test Points (Excluding X1 Input)**



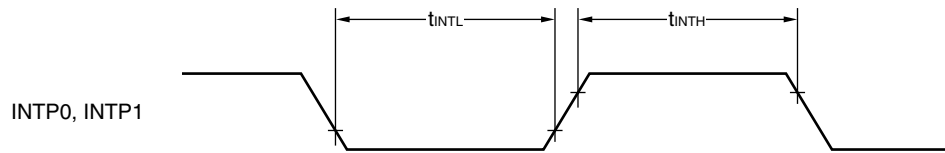
**Clock Timing**



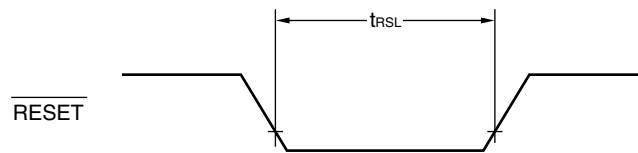
**TI000 Timing**



**Interrupt Input Timing**



**RESET Input Timing**



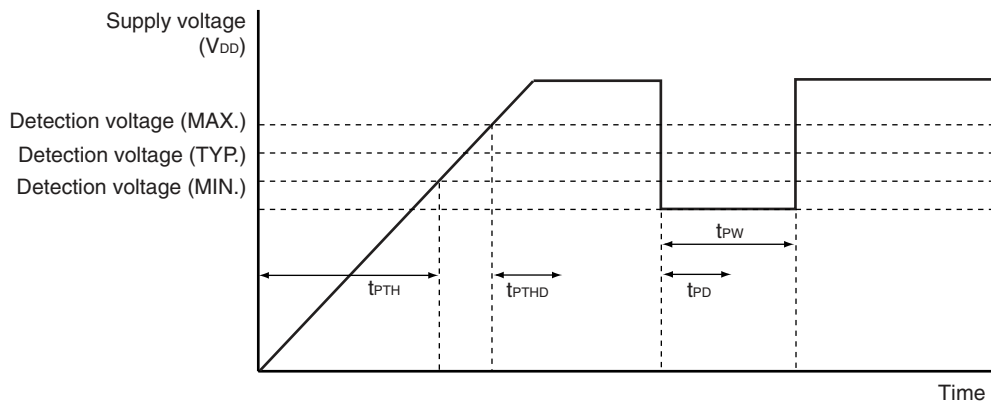
**POC Circuit Characteristics (T<sub>A</sub> = -40 to +85°C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V <sub>POC</sub>		2.0	2.1	2.2	V
Power supply rise time	t <sub>PTH</sub>	V <sub>DD</sub> : 0 V → 2.1 V	1.5			μs
Response delay time 1 <sup>Note 1</sup>	t <sub>PTHD</sub>	When power supply rises, after reaching detection voltage (MAX.)			3.0	ms
Response delay time 2 <sup>Note 2</sup>	t <sub>PD</sub>	When power supply falls			1.0	ms
Minimum pulse width	t <sub>PW</sub>		0.2			ms

**Notes 1.** Time required from voltage detection to internal reset release.

**2.** Time required from voltage detection to internal reset signal generation.

**POC Circuit Timing**

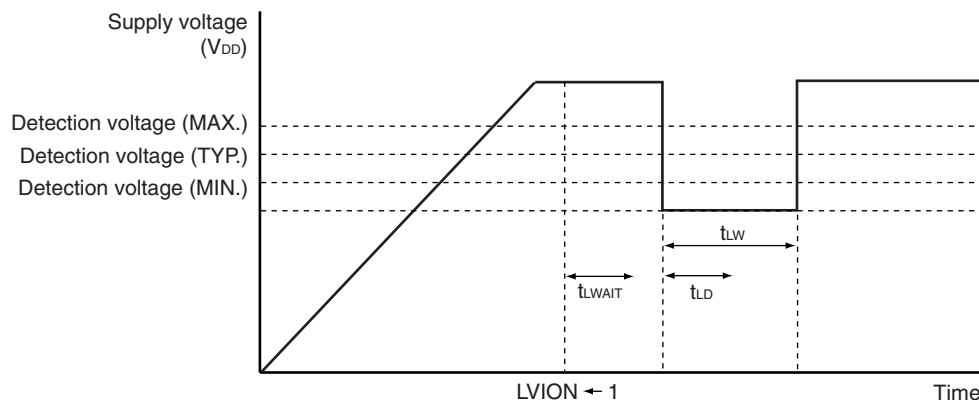


**LVI Circuit Characteristics ( $T_A = -40$  to  $+85^\circ\text{C}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	$V_{LV10}$		4.1	4.3	4.5	V
	$V_{LV11}$		3.9	4.1	4.3	V
	$V_{LV12}$		3.7	3.9	4.1	V
	$V_{LV13}$		3.5	3.7	3.9	V
	$V_{LV14}$		3.3	3.5	3.7	V
	$V_{LV15}$		3.15	3.3	3.45	V
	$V_{LV16}$		2.95	3.1	3.25	V
	$V_{LV17}$		2.7	2.85	3.0	V
	$V_{LV18}$		2.5	2.6	2.7	V
	$V_{LV19}$		2.25	2.35	2.45	V
Response time <sup>Note 1</sup>	$t_{LD}$			0.2	2.0	ms
Minimum pulse width	$t_{LW}$		0.2			ms
Operation stabilization wait time <sup>Note 2</sup>	$t_{LWAIT}$			0.1	0.2	ms

- Notes**
1. Time required from voltage detection to interrupt output or internal reset signal generation.
  2. Time required from setting LVION to 1 to operation stabilization.

- Remarks**
1.  $V_{LV10} > V_{LV11} > V_{LV12} > V_{LV13} > V_{LV14} > V_{LV15} > V_{LV16} > V_{LV17} > V_{LV18} > V_{LV19}$
  2.  $V_{POC} < V_{LV1m}$  ( $m = 0$  to  $9$ )

**LVI Circuit Timing**

**Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics ( $T_A = -40$  to  $+85^\circ\text{C}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	$V_{DDDR}$		2.0		5.5	V
Release signal set time	$t_{SREL}$		0			$\mu\text{s}$

**Flash Memory Programming Characteristics ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	$I_{DD}$	$V_{DD} = 5.5\text{ V}$			7.0	mA
Erasure count <sup>Note</sup> (per 1 block)	$N_{ERASE}$	$T_A = -40$ to $+85^\circ\text{C}$	1000			Times
Chip erase time	$T_{CERASE}$	$T_A = -10$ to $+85^\circ\text{C}$ , $N_{ERASE} \leq 100$	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		0.8	s
			$3.5\text{ V} \leq V_{DD} < 4.5\text{ V}$		1.0	s
			$2.7\text{ V} \leq V_{DD} < 3.5\text{ V}$		1.2	s
		$T_A = -10$ to $+85^\circ\text{C}$ , $N_{ERASE} \leq 1000$	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		4.8	s
			$3.5\text{ V} \leq V_{DD} < 4.5\text{ V}$		5.2	s
			$2.7\text{ V} \leq V_{DD} < 3.5\text{ V}$		6.1	s
		$T_A = -40$ to $+85^\circ\text{C}$ , $N_{ERASE} \leq 100$	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.6	s
			$3.5\text{ V} \leq V_{DD} < 4.5\text{ V}$		1.8	s
			$2.7\text{ V} \leq V_{DD} < 3.5\text{ V}$		2.0	s
		$T_A = -40$ to $+85^\circ\text{C}$ , $N_{ERASE} \leq 1000$	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		9.1	s
			$3.5\text{ V} \leq V_{DD} < 4.5\text{ V}$		10.1	s
			$2.7\text{ V} \leq V_{DD} < 3.5\text{ V}$		12.3	s
Block erase time	$T_{BERASE}$	$T_A = -10$ to $+85^\circ\text{C}$ , $N_{ERASE} \leq 100$	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		0.4	s
			$3.5\text{ V} \leq V_{DD} < 4.5\text{ V}$		0.5	s
			$2.7\text{ V} \leq V_{DD} < 3.5\text{ V}$		0.6	s
		$T_A = -10$ to $+85^\circ\text{C}$ , $N_{ERASE} \leq 1000$	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		2.6	s
			$3.5\text{ V} \leq V_{DD} < 4.5\text{ V}$		2.8	s
			$2.7\text{ V} \leq V_{DD} < 3.5\text{ V}$		3.3	s
		$T_A = -40$ to $+85^\circ\text{C}$ , $N_{ERASE} \leq 100$	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		0.9	s
			$3.5\text{ V} \leq V_{DD} < 4.5\text{ V}$		1.0	s
			$2.7\text{ V} \leq V_{DD} < 3.5\text{ V}$		1.1	s
		$T_A = -40$ to $+85^\circ\text{C}$ , $N_{ERASE} \leq 1000$	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		4.9	s
			$3.5\text{ V} \leq V_{DD} < 4.5\text{ V}$		5.4	s
			$2.7\text{ V} \leq V_{DD} < 3.5\text{ V}$		6.6	s
Byte write time	$T_{WRITE}$	$T_A = -40$ to $+85^\circ\text{C}$ , $N_{ERASE} \leq 1000$			150	$\mu\text{s}$
Internal verify	$T_{VERIFY}$	Per 1 block			6.8	ms
		Per 1 byte			27	$\mu\text{s}$
Blank check	$T_{BLKCHK}$	Per 1 block			480	$\mu\text{s}$
Retention years		$T_A = 85^\circ\text{C}$ <sup>Note 2</sup> , $N_{ERASE} \leq 1000$	10			Years

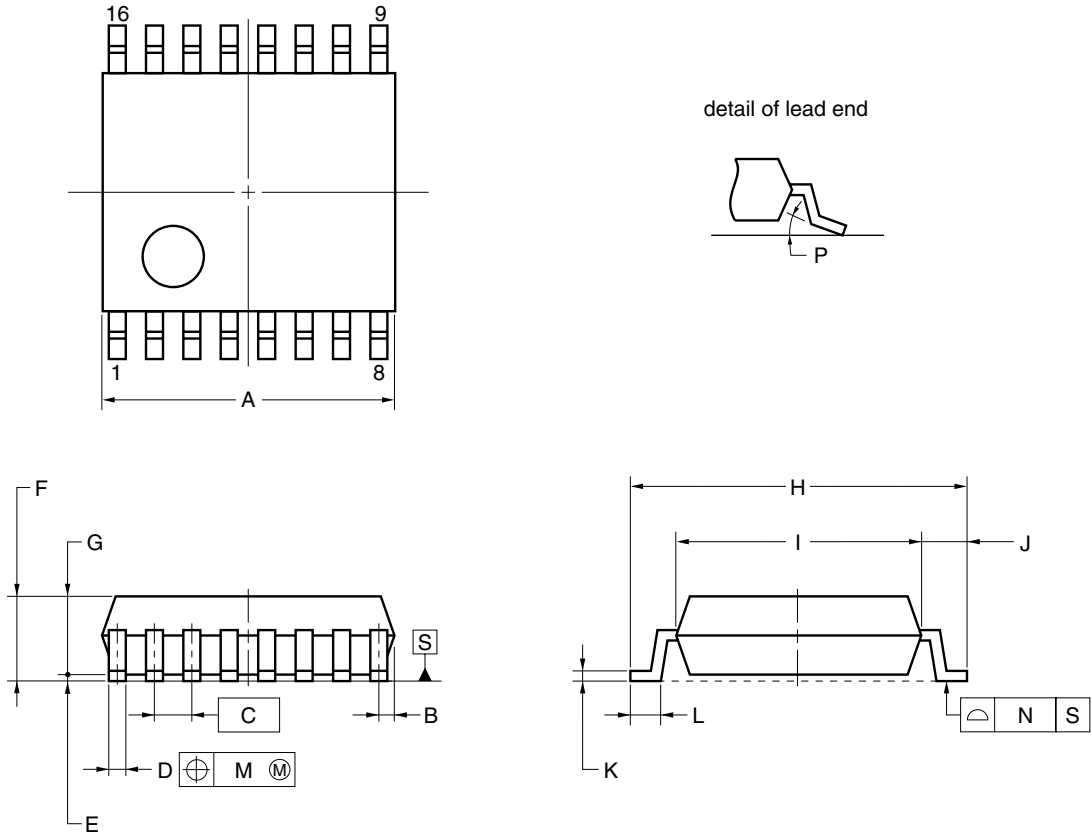
**Notes 1.** Depending on the erasure count ( $N_{ERASE}$ ), the erase time varies. Refer to the chip erase time and block erase time parameters.

**2.** When the average temperature when operating and not operating is  $85^\circ\text{C}$ .

**Remark** When a product is first written after shipment, “erase → write” and “write only” are both taken as one rewrite.

## CHAPTER 18 PACKAGE DRAWING

### 16-PIN PLASTIC SSOP (5.72 mm (225))



**NOTE**

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.2±0.3
B	0.475 MAX.
C	0.65 (T.P.)
D	0.22±0.08
E	0.125±0.075
F	1.565±0.235
G	1.44
H	6.2±0.3
I	4.4±0.2
J	0.9±0.2
K	0.17 <sup>+0.08</sup> <sub>-0.07</sub>
L	0.5±0.2
M	0.10
N	0.10
P	5°±5°

**P16GM-65-225B-5**

## CHAPTER 19 RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.  
For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

- Cautions 1. Products with -A at the end of the part number are lead-free products.**  
**2. For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.**

**Table 19-1. Surface Mounting Type Soldering Conditions**

**16-pin plastic SSOP (lead-free products)**

μPD78F9510GR-JJG-A<sup>Note 1</sup>, 78F9511GR-JJG-A<sup>Note 1</sup>, 78F9512GR-JJG-A<sup>Note 1</sup>

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: 3 times or less, Exposure limit: 7 days <sup>Note 2</sup> (after that, prebake at 125°C for 20 to 72 hours)	IR60-207-3
Wave soldering	For details, contact an NEC Electronics sales representative.	–
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

- Notes 1.** Under development  
**2.** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

**Caution Do not use different soldering methods together (except for partial heating).**



## APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for development of systems using the  $\mu$ PD78F9510, 78F9511, 78F9512. Figure A-1 shows development tools.

- Compatibility with PC98-NX series

Unless stated otherwise, products which are supported by IBM PC/AT™ and compatibles can also be used with the PC98-NX series. When using the PC98-NX series, therefore, refer to the explanations for IBM PC/AT and compatibles.

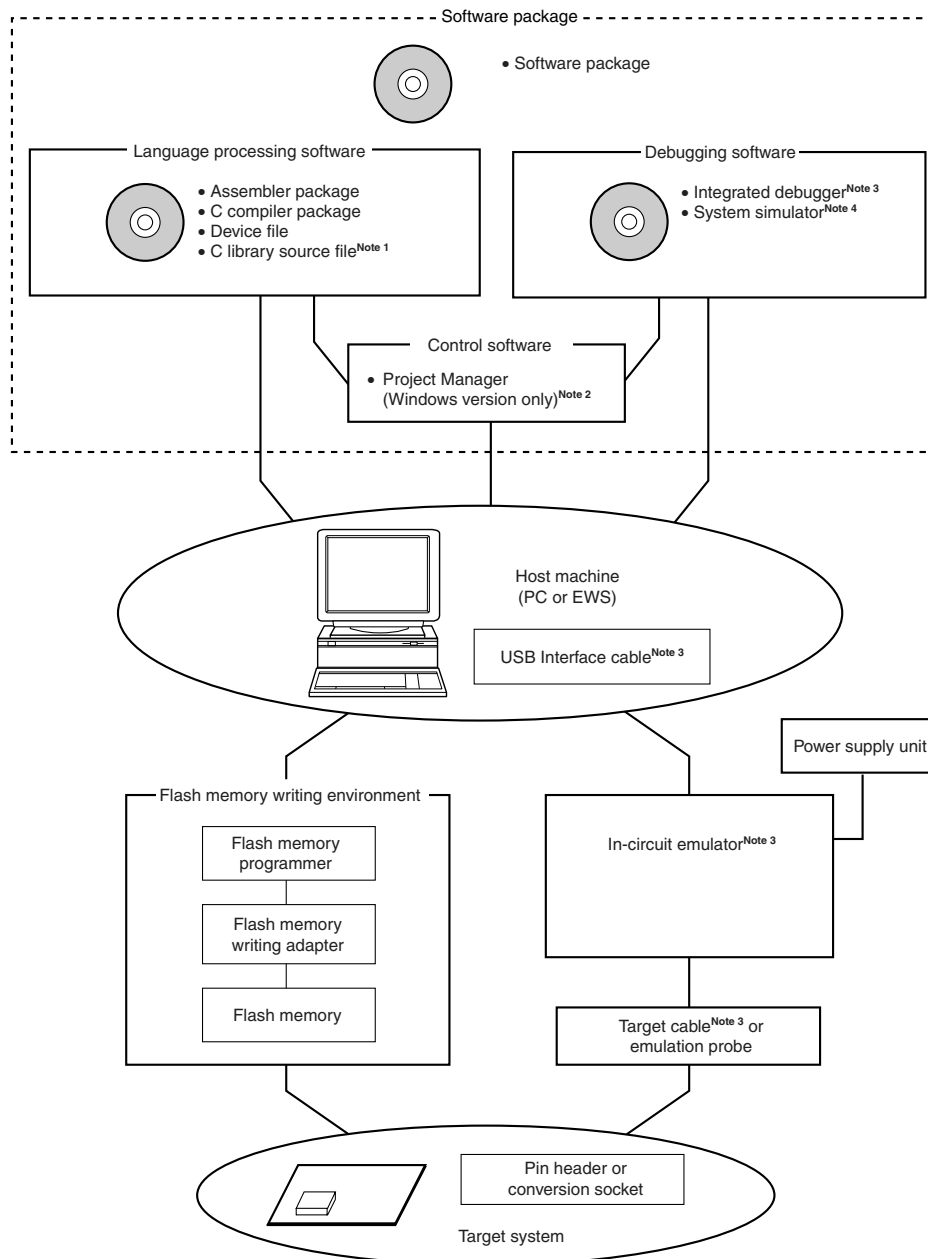
- Windows™

Unless stated otherwise, "Windows" refers to the following operating systems.

- Windows 98
- Windows NT™ Ver. 4.0
- Windows 2000
- Windows XP™

Figure A-1. Development Tools (1/4)

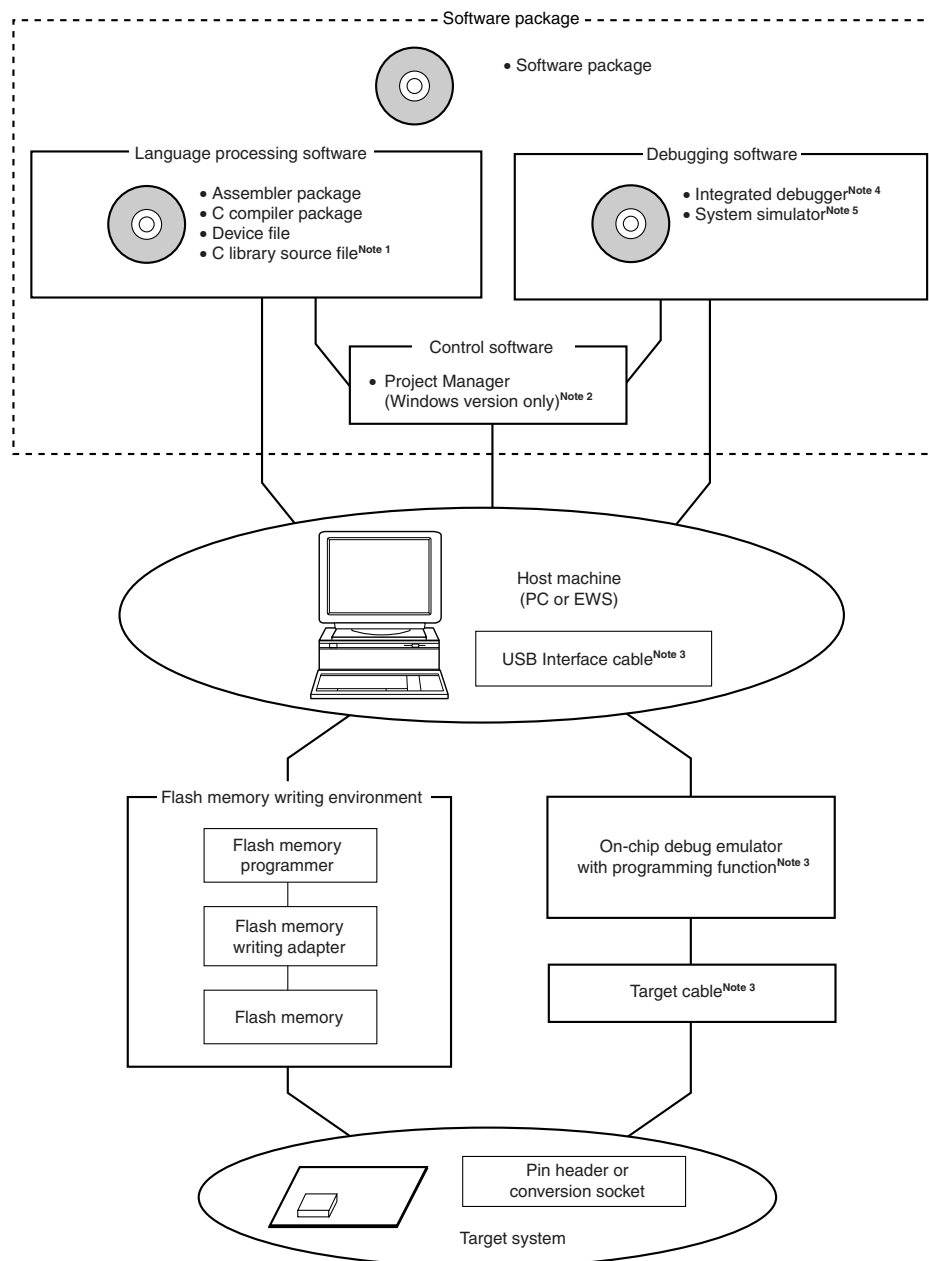
## (1) When using the in-circuit emulator QB-78K0SKX1



- Notes**
1. The C library source file is not included in the software package.
  2. The Project Manager PM+ is included in the assembler package. PM+ is used only in the Windows environment.
  3. The in-circuit emulator QB-78K0SKX1 is provided with the integrated debugger ID78K0S-QB, the on-chip debug emulator with programming function QB-MINI2, a USB interface cable, a power supply unit, and a target cable. Other products are optional.
  4. It is planned to use SM+ for 78K0S/Kx1+ as a system simulator.

Figure A-1. Development Tools (2/4)

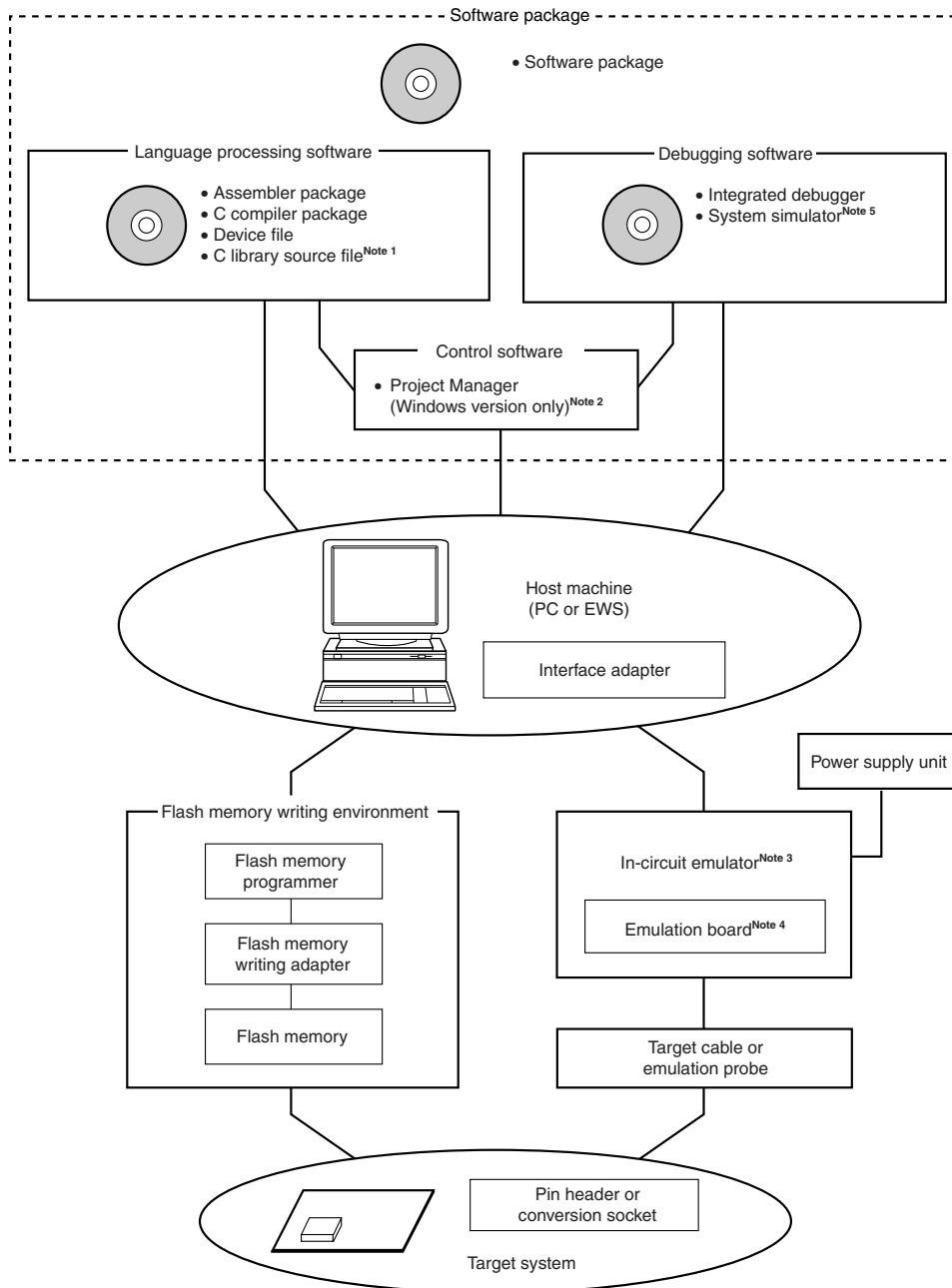
## (2) When using the on-chip debug emulator with programming function QB-MINI2



- Notes**
1. The C library source file is not included in the software package.
  2. The Project Manager PM+ is included in the assembler package. PM+ is used only in the Windows environment.
  3. The on-chip debug emulator with programming function QB-MINI2 is provided with a USB interface cable, and a target cable.
  4. The integrated debugger ID78K0S-QB is not included with the QB-MINI2. The integrated debugger ID78K0S-QB is available on the following website.  
<http://www.necel.com/micro/ods/eng/>
  5. It is planned to use SM+ for 78K0S/Kx1+ as a system simulator.

Figure A-1. Development Tools (3/4)

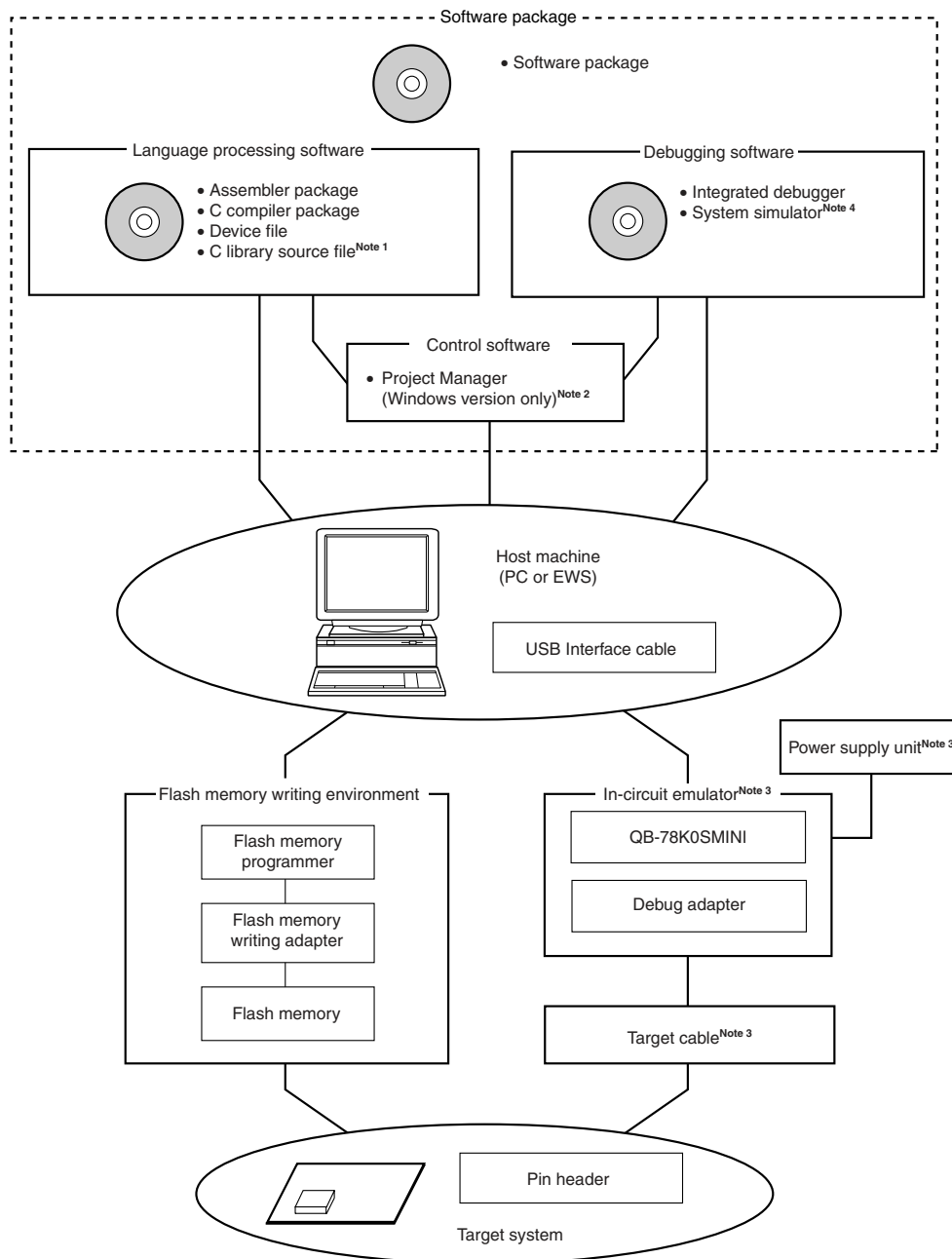
(3) When using the in-circuit emulator IE-78K0S-NS or IE-78K0S-NS-A



- Notes**
1. The C library source file is not included in the software package.
  2. The Project Manager PM+ is included in the assembler package. PM+ is used only in the Windows environment.
  3. All products other than the in-circuit emulators IE-78K0S-NS and IE-78K0S-NS-A are optional.
  4. The in-circuit emulator IE-789234-NS-EM1 is provided with the target cable.
  5. It is planned to use SM+ for 78K0S/Kx1+ as a system simulator.

Figure A-1. Development Tools (4/4)

(4) When using the in-circuit emulator QB-78K0SKX1MINI



- Notes**
1. The C library source file is not included in the software package.
  2. The Project Manager PM+ is included in the assembler package. PM+ is used only in the Windows environment.
  3. The in-circuit emulator QB-78K0SKX1MINI is provided with the integrated debugger ID78K0S-QB, the flash memory programmer PG-FPL2, a power supply unit, and a target cable. Other products are optional.
  4. It is planned to use SM+ for 78K0S/Kx1+ as a system simulator.

## A.1 Software Package

SP78K0S Software package	This is a package that bundles the software tools required for development of the 78K0S Series. The following tools are included. RA78K0S, CC78K0S, ID78K0S-NS, SM+ for 78K0S <sup>Note 1</sup> , SM78K0S <sup>Notes 2</sup> , and device files
	Part number: $\mu$ SxxxxSP78K0S

- Notes**
1. SM+ for 78K0S is not included in SP78K0S Ver. 2.00 or earlier.
  2. The SM78K0S does not support the 78K0S/Kx1+.
  3. The DF789234 is not included in SP78K0S Ver. 2.00 or earlier. The DF789234 is available on the following website.  
<http://www.necel.com/micro/ods/eng/>

**Remark** xxxx in the part number differs depending on the operating system to be used.

$\mu$ SxxxxSP78K0S

xxxx	Host Machine	OS	Supply Medium
AB17	PC-9800 series, IBM PC/AT and compatibles	Japanese Windows	CD-ROM
BB17		English Windows	

## A.2 Language Processing Software

RA78K0S Assembler package	Program that converts program written in mnemonic into object code that can be executed by microcontroller. In addition, automatic functions to generate symbol table and optimize branch instructions are also provided. Used in combination with device file (DF789234) (sold separately). <b>&lt;Caution when used in PC environment&gt;</b> The assembler package is a DOS-based application but may be used under the Windows environment by using PM+ of Windows (included in the assembler package).
	Part number: $\mu$ SxxxxRA78K0S
CC78K0S C library package	Program that converts program written in C language into object codes that can be executed by microcontroller. Used in combination with assembler package (RA78K0S) and device file (DF789234) (both sold separately). <b>&lt;Caution when used in PC environment&gt;</b> The C compiler package is a DOS-based application but may be used under the Windows environment by using PM+ of Windows (included in the assembler package).
	Part number: $\mu$ SxxxxCC78K0S
DF789234 <sup>Note 1</sup> Device file	File containing the information inherent to the device. Used in combination with other tools (RA78K0S, CC78K0S, ID78K0S-NS, ID78K0S-QB, or SM+ for 78K0S) (all sold separately).
	Part number: $\mu$ SxxxxDF789234
CC78K0S-L <sup>Note 2</sup> C library source file	Source file of functions constituting object library included in C compiler package. Necessary for changing object library included in C compiler package according to customer's specifications. Since this is the source file, its working environment does not depend on any particular operating system.
	Part number: $\mu$ SxxxxCC78K0S-L

- Notes**
- DF789234 is a common file that can be used with RA78K0S, CC78K0S, ID78K0S-NS, ID78K0S-QB and SM+ for 78K0S.
  - CC78K0S-L is not included in the software package (SP78K0S).

**Remark** xxxx in the part number differs depending on the host machine and operating system to be used.

μSxxxxRA78K0S  
 μSxxxxCC78K0S  
 μSxxxxCC78K0S-L

xxxx	Host Machine	OS	Supply Media
AB17	PC-9800 series, IBM PC/AT and compatibles	Japanese Windows	CD-ROM
BB17		English Windows	
3P17	HP9000 series 700™	HP-UX™ (Rel.10.10)	
3K17	SPARCstation™	SunOS™ (Rel.4.1.4), Solaris™ (Rel.2.5.1)	

μSxxxxDF789234

xxxx	Host Machine	OS	Supply Media
AB13	PC-9800 series, IBM PC/AT and compatibles	Japanese Windows	3.5" 2HD FD
BB13		English Windows	

### A.3 Control Software

PM+ Project manager	This is control software designed so that the user program can be efficiently developed in the Windows environment. With this software, a series of user program development operations, including starting the editor, build, and starting the debugger, can be executed on the PM+. <b>&lt;Caution&gt;</b> The PM+ is included in the assembler package (RA78K0S). It can be used only in the Windows environment.
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### A.4 Flash Memory Writing Tools

FlashPro4 (FL-PR4, PG-FP4) Flash memory programmer	Flash memory programmer dedicated to the microcontrollers incorporating a flash memory
PG-FPL2 Flash memory programmer	Flash memory programmer dedicated to the microcontrollers incorporating a flash memory
QB-MINI2 On-chip debug emulator with programming function	This is a flash memory programmer dedicated to microcontrollers incorporating a flash memory. It is available also as an on-chip debug emulator which serves to debug hardware and software when developing application systems using all flash microcontrollers (including the 78K0S/Kx1+).
FA-78F9212GR-JJG-MX Flash memory writing adapter	Flash memory writing adapter. Used in connection with the flash memory programmer.

**Remark** FL-PR4 and FA-78F9212GR-JJG-MX are products of Naito Densai Machida Mfg. Co., Ltd.  
 For further information, contact: Naito Densai Machida Mfg. Co., Ltd. (TEL +81-42-750-4172)

## A.5 Debugging Tools (Hardware)

### A.5.1 When using in-circuit emulator QB-78K0SKX1

QB-78K0SKX1 In-circuit emulator	This in-circuit emulator serves to debug hardware and software when developing application systems using the 78K0S/Kx1+. It supports the integrated debugger (ID78K0S-QB). It is connected to the included AC adapter, target cable, and host machine via a USB interface cable.
QB-50-EP-01T Emulation probe	This emulation probe is a flexible type and is used to connect the in-circuit emulator and target system.
QB-16GR-EA-01T Exchange adapter	This exchange adapter is used to perform pin conversion from the in-circuit emulator to target connector.
QB-16GR-NQ-01T Target connector	This target connector is used to mount on the target system.
Specifications of pin header on target system	0.635 mm × 0.635 mm (height: 6 mm)

**Remark** The QB-78K0SKX1 is provided with a AC adapter, a USB interface cable, a target cable, the integrated debugger ID78K0S-QB, and the on-chip debug emulator with programming function QB-MINI2. The QB-78K0SKX1 is also provided with an emulation probe, an exchange adapter, and a target connector depending on the ordering code.

### A.5.2 When using in-circuit emulator QB-MINI2

QB-MINI2 On-chip debug emulator with programming function	This is an on-chip debug emulator which serves to debug hardware and software when developing application systems using all flash microcontrollers (including the 78K0S/Kx1+). It is available also as a flash memory programmer dedicated to microcontrollers incorporating a flash memory.
Specifications of pin header on target system	16-pin general-purpose connector (2.54 mm pitch)

**Remark** The QB-MINI2 is provided with a USB interface cable, and a target cable. In addition, the integrated debugger (including ID78K0S-QB) is used as control software. The integrated debugger is available on the following website.  
<http://www.necel.com/micro/ods/eng/>



**A.5.3 When using in-circuit emulator IE-78K0S-NS or IE-78K0S-NS-A**

IE-78K0S-NS In-circuit emulator	In-circuit emulator for debugging hardware and software of application system using 78K/0S Series. Supports integrated debugger (ID78K0S-NS). Used in combination with AC adapter, emulation probe, and interface adapter for connecting the host machine.
IE-78K0S-NS-A In-circuit emulator	This in-circuit emulator has a coverage function in addition to the functions of the IE-78K0S-NS, and enhanced debugging functions such as an enhanced tracer function and timer function.
IE-70000-MC-PS-B AC adapter	Adapter for supplying power from 100 to 240 VAC outlet.
IE-70000-CD-IF-A PC card interface	PC card and interface cable required when using a notebook type PC as the host machine (PCMCIA socket supported).
IE-70000-PCI-IF-A Interface adapter	Adapter required when using a personal computer incorporating the PCI bus is used as the host machine.
IE-789234-NS-EM1 Emulation board	Emulation board for emulating the peripheral hardware inherent to the device. Used in combination with in-circuit emulator. A target cable is provided.
Specifications of pin header on target system	0.635 mm × 0.635 mm (height: 6 mm)

**A.5.4 When using in-circuit emulator QB-78K0SKX1MINI**

QB-78K0SKX1MINI In-circuit emulator	In-circuit emulator for debugging hardware and software of application system using 78K0S/Kx1+ Series. Supports integrated debugger (ID78K0S-QB). Used in combination with AC adapter, target cable, and USB interface cable for connecting the host machine.
Specifications of pin header on target system	0.635 mm × 0.635 mm (height: 6 mm)

## A.6 Debugging Tools (Software)

<p>ID78K0S-NS (supporting in-circuit emulator IE-78K0S-NS/IE-78K0S-NS-A) Integrated debugger</p>	<p>This debugger supports the in-circuit emulators for the 78K/0S Series. ID78K0S-NS is Windows-based software. This debugger has enhanced debugging functions supporting C language. By using its window integration function that associates the source program, disassemble display, and memory display with trace results, the trace results can be displayed corresponding to the source program. It is used with a device file (DF789234) (sold separately). Part number: <math>\mu</math>SxxxxID78K0S-NS</p>
<p>ID78K0S-QB (supporting in-circuit emulator QB-78K0SKX1MINI) Integrated debugger</p>	<p>This debugger supports the in-circuit emulators for the 78K0S/Kx1+ Series. ID78K0S-QB is Windows-based software. Provided with the debug function supporting C language, source programming, disassemble display, and memory display are possible. This is used with the device file (DF789234) (sold separately). It is provided with the in-circuit emulator QB-78K0SKX1MINI. Ordering number: <math>\mu</math>SxxxxID78K0S-QB (not for sale)</p>
<p>SM+ for 78K0S System simulator</p>	<p>This is a system simulator for the 78K/0S series. SM+ for 78K0S is Windows-based software. This simulator can execute C-source-level or assembler-level debugging while simulating the operations of the target system on the host machine. By using SM+ for 78K0S, the logic and performance of the application can be verified independently of hardware development. Therefore, the development efficiency can be enhanced and the software quality can be improved. This simulator is used with a device file (DF789234) (sold separately). Part number: <math>\mu</math>SxxxxSM789234-B</p>
<p>DF789234<sup>Note</sup> Device file</p>	<p>This is a file that has device-specific information. It is used with the RA78K0S, CC78K0S, ID78K0S-NS, ID78K0S-QB, and SM+ for 78K0S (all sold separately). Part number: <math>\mu</math>SxxxxDF789234</p>

**Note** DF789234 is a common file that can be used with the RA78K0S, CC78K0S, ID78K0S-NS, ID78K0S-QB, and SM+ for 78K0S.

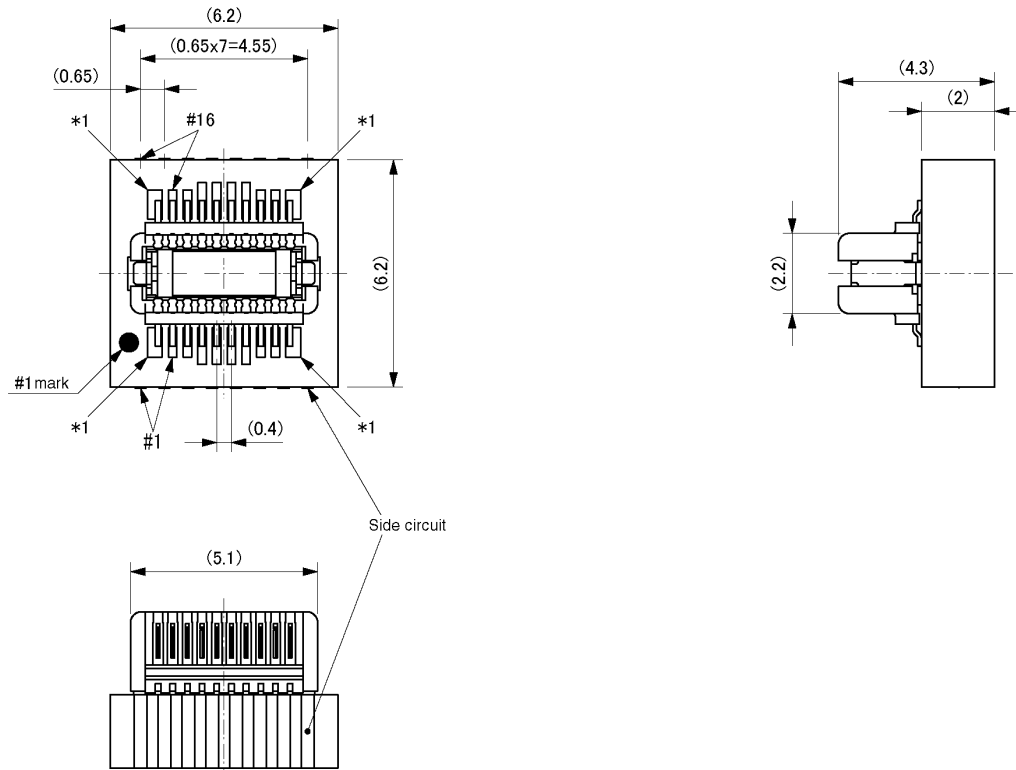
## APPENDIX B NOTES ON TARGET SYSTEM DESIGN

The package drawings of development tools are shown below.

Consider areas on the target system where component mounting is prohibited and areas where there are component mounting height restrictions when the QB-78K0SKX1 is used.

**Figure B-1. Target Connector (QB-16GR-NQ-01T)**

**(a) Package drawing**



**(b) Foot pattern**

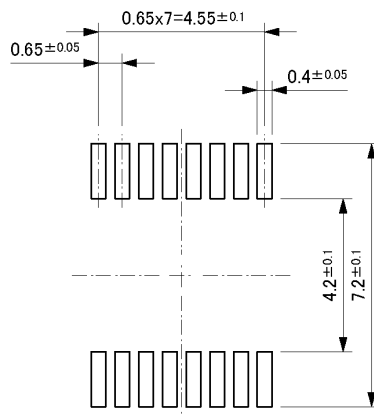


Figure B-2. Exchange Adapter (QB-16GR-EA-01T)

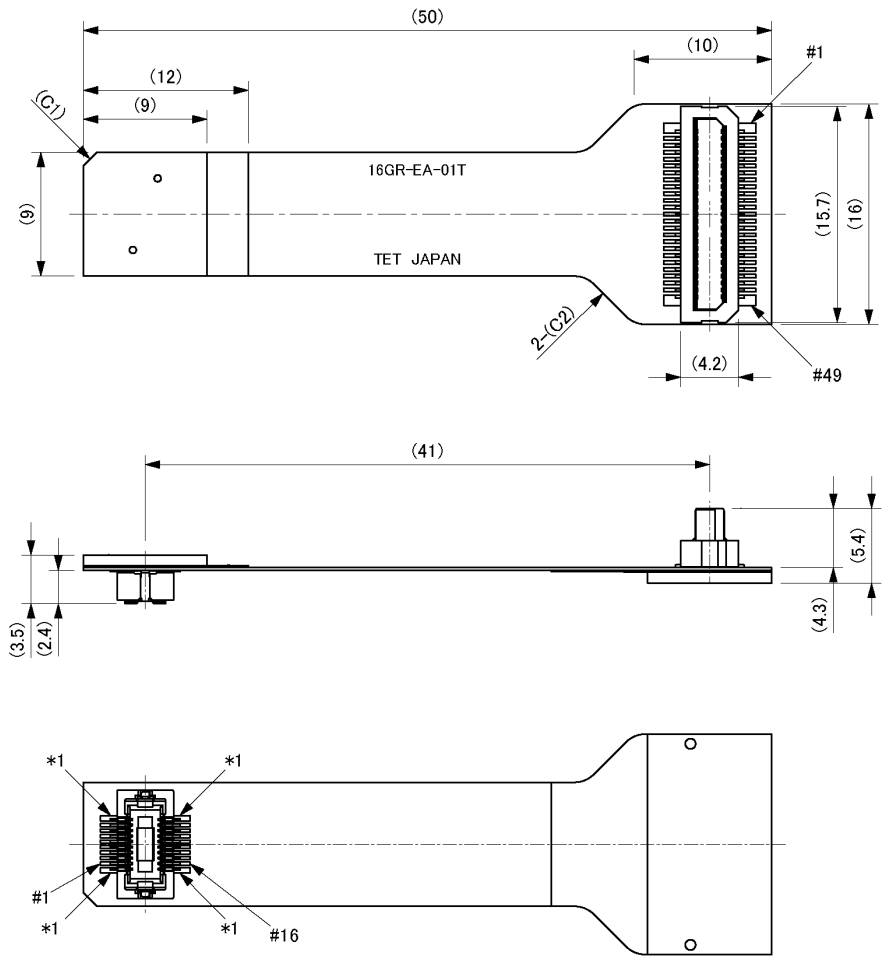
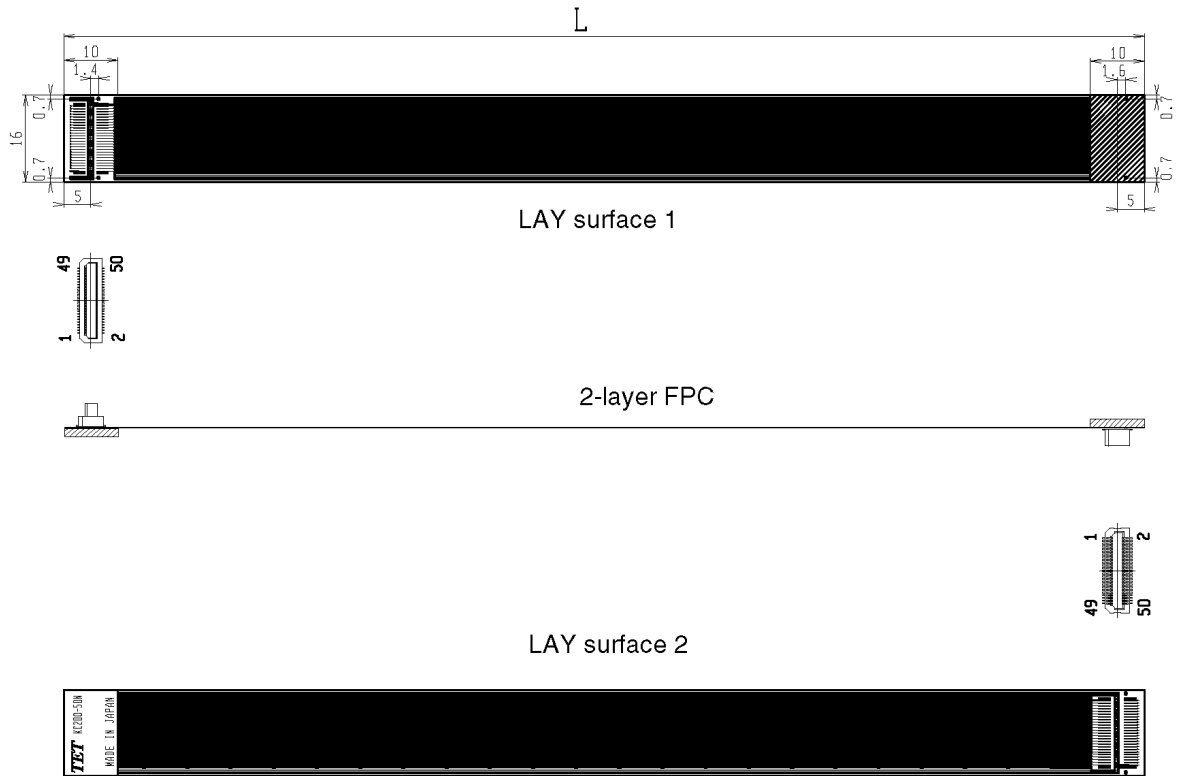


Figure B-3. Emulation Probe (QB-50-EP-01T)



## APPENDIX C REGISTER INDEX

### C.1 Register Index (Register Name)

8-bit timer H compare register 01 (CMP01) ... 123  
8-bit timer H compare register 11 (CMP11) ... 123  
8-bit timer H mode register 1 (TMHMD1) ... 124  
16-bit timer capture/compare register 000 (CR000) ... 82  
16-bit timer capture/compare register 010 (CR010) ... 84  
16-bit timer counter 00 (TM00) ... 82  
16-bit timer mode control register 00 (TMC00) ... 85  
16-bit timer output control register 00 (TOC00) ... 88

#### [C]

Capture/compare control register 00 (CRC00) ... 87

#### [E]

External interrupt mode register 0 (INTM0) ... 150

#### [F]

Flash address pointer H (FLAPH) ... 209  
Flash address pointer L (FLAPL) ... 209  
Flash address pointer H compare register (FLAPHC)... 209  
Flash address pointer L compare register (FLAPLC) ... 209  
Flash programming command register (FLCMD) ... 208  
Flash programming mode control register (FLPMC) ... 205  
Flash protect command register (PFCMD) ... 206  
Flash status register (PFS) ... 206  
Flash write buffer register (FLW) ... 210

#### [I]

Interrupt mask flag register 0 (MK0) ... 150  
Interrupt request flag register 0 (IF0) ... 149

#### [L]

Low-speed internal oscillation mode register (LSRCM) ... 67  
Low-voltage detect register (LVIM) ... 179  
Low-voltage detection level select register (LVIS) ... 180

#### [O]

Oscillation stabilization time select register (OSTS) ... 68, 158

**[P]**

Port mode register 2 (PM2) ... 59, 90  
Port mode register 3 (PM3) ... 59  
Port mode register 4 (PM4) ... 59  
Port register 2 (P2) ... 60  
Port register 3 (P3) ... 60  
Port register 4 (P4) ... 60  
Preprocessor clock control register (PPCC) ... 66  
Prescaler mode register 00 (PRM00) ... 89  
Processor clock control register (PCC) ... 66  
Pull-up resistor option register 2 (PU2) ... 61  
Pull-up resistor option register 3 (PU3) ... 61  
Pull-up resistor option register 4 (PU4) ... 61

**[R]**

Reset control flag register (RESF) ... 173

**[W]**

Watchdog timer enable register (WDTE) ... 139  
Watchdog timer mode register (WDTM) ... 138

**C.2 Register Index (Symbol)****[C]**

CMP01: 8-bit timer H compare register 01 ... 123  
CMP11: 8-bit timer H compare register 11 ... 123  
CR000: 16-bit timer capture/compare register 000 ... 82  
CR010: 16-bit timer capture/compare register 010 ... 84  
CRC00: Capture/compare control register 00 ... 87

**[F]**

FLAPH: Flash address pointer H ... 209  
FLAPHC: Flash address pointer H compare register ... 209  
FLAPL: Flash address pointer L ... 209  
FLAPLC: Flash address pointer L compare register ... 209  
FLCMD: Flash programming command register ... 208  
FLPMC: Flash programming mode control register ... 205  
FLW: Flash write buffer register ... 210

**[I]**

IF0: Interrupt request flag register 0 ... 149  
INTM0: External interrupt mode register 0 ... 150

**[L]**

LSRCM: Low-speed internal oscillation mode register ... 67  
LVIM: Low-voltage detect register ... 179  
LVIS: Low-voltage detection level select register ... 180

**[M]**

MK0: Interrupt mask flag register 0 ... 150

**[O]**

OSTS: Oscillation stabilization time select register ... 68, 158



**[P]**

P2:	Port register 2 ... 60
P3:	Port register 3 ... 60
P4:	Port register 4 ... 60
PCC:	Processor clock control register ... 66
PFCMD:	Flash protect command register ... 206
PFS:	Flash status register ... 206
PM2:	Port mode register 2 ... 59, 90
PM3:	Port mode register 3 ... 59
PM4:	Port mode register 4 ... 59
PPCC:	Preprocessor clock control register ... 66
PRM00:	Prescaler mode register 00 ... 89
PU2:	Pull-up resistor option register 2 ... 61
PU3:	Pull-up resistor option register 3 ... 61
PU4:	Pull-up resistor option register 4 ... 61

**[R]**

RESF:	Reset control flag register ... 173
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**[T]**

TM00:	16-bit timer counter 00 ... 82
TMC00:	16-bit timer mode control register 00 ... 85
TMHMD1:	8-bit timer H mode register 1 ... 124
TOC00:	16-bit timer output control register 00 ... 88

**[W]**

WDTE:	Watchdog timer enable register ... 139
WDTM:	Watchdog timer mode register ... 138

## APPENDIX D LIST OF CAUTIONS

This appendix lists cautions described in this document.

“Classification (hard/soft)” in table is as follows.

Hard: Cautions for microcontroller internal/external hardware

Soft: Cautions for software such as register settings or programs

(1/12)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 2	Hard	Pin functions	P22/X2, P23/X1	The P22/X2 and P23/X1 pins are pulled down during reset.	pp. 20, <input type="checkbox"/> 21, 22, 23
Chapter 3	Soft	Memory space	SP: stack pointer	Since reset signal generation makes the SP contents undefined, be sure to initialize the SP before using the stack memory.	p. 34 <input type="checkbox"/>
				Stack pointers can be set only to the high-speed RAM area, and only the lower 10 bits can be actually set. Thus, if the stack pointer is specified to 0FF00H, it is converted to 0FB00H in the high-speed RAM area, since 0FF00H is in the SFR area and not in the high-speed RAM area. When the value is actually pushed onto the stack, 1 is subtracted from 0FB00H to become 0FAFFH, but since that value is not in the high-speed RAM area, it is converted to 0FEFFH, which is the same value as when 0FF00H is set to the stack pointer.	p. 34 <input type="checkbox"/>
Chapter 4	Hard	Port functions	P22/X2, P23/X1	The P22/X2 and P23/X1 pins are pulled down during reset.	p. 51 <input type="checkbox"/>
			P34	Because the P34 pin functions alternately as the RESET pin, if it is used as an input port pin, the function to input an external reset signal to the RESET pin cannot be used. The function of the port is selected by the option byte. For details, refer to CHAPTER 14 OPTION BYTE. Also, since the option byte is referenced after the reset release, if low level is input to the RESET pin before the referencing, then the reset state is not released. When it is used as an input port pin, connect the pull-up resistor.	p. 57 <input type="checkbox"/>
			P21, P32	Because P21 and P32 are also used as external interrupt pins, the corresponding interrupt request flag is set if each of these pins is set to the output mode and its output level is changed. To use the port pin in the output mode, therefore, set the corresponding interrupt mask flag to 1 in advance.	p. 59 <input type="checkbox"/>
			–	Although a 1-bit memory manipulation instruction manipulates 1 bit, it accesses a port in 8-bit units. Therefore, the contents of the output latch of a pin in the input mode, even if it is not subject to manipulation by the instruction, are undefined in a port with a mixture of inputs and outputs.	p. 62 <input type="checkbox"/>
Chapter 5	Soft	Main clock	OSTS: Oscillation stabilization time select register	To set and then release the STOP mode, set the oscillation stabilization time as follows. Expected oscillation stabilization time of resonator ≤ Oscillation stabilization time set by OSTS	p. 68 <input type="checkbox"/>

Chapter	Classification	Function	Details of Function	Cautions	Page	
Chapter 5	Soft	Main clock	OSTS: Oscillation stabilization time select register	The wait time after the STOP mode is released does not include the time from the release of the STOP mode to the start of clock oscillation (“a” in the figure below), regardless of whether STOP mode was released by reset input or interrupt generation.	p. 68 <input type="checkbox"/>	
				The oscillation stabilization time that elapses on power application or after release of reset is selected by the option byte. For details, refer to CHAPTER 14 OPTION BYTE.	p. 68 <input type="checkbox"/>	
	Hard	Crystal/ceramic oscillator	–	When using the crystal/ceramic oscillator, wire as follows in the area enclosed by the broken lines in Figure 5-6 to avoid an adverse effect from wiring capacitance. <ul style="list-style-type: none"> <li>• Keep the wiring length as short as possible.</li> <li>• Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.</li> <li>• Always make the ground point of the oscillator capacitor the same potential as V<sub>SS</sub>. Do not ground the capacitor to a ground pattern through which a high current flows.</li> <li>• Do not fetch signals from the oscillator.</li> </ul>	p. 69 <input type="checkbox"/>	
Chapter 6	Hard	16-bit timer/event counter 00	TM00: 16-bit timer counter 00	Even if TM00 is read, the value is not captured by CR010.	pp. 82, 114 <input type="checkbox"/>	
				If TM00 is referred to during a timer count, a timer count will be stopped during reference processing, and a timer count is resumed after reference processing is finished. Therefore, if processing which refers to TM00 is performed, an error will arise at a timer count.	pp. 82, 114 <input type="checkbox"/>	
	Soft			CR000: 16-bit timer capture/compare register 000	Set CR000 to other than 0000H in the clear & start mode entered on match between TM00 and CR000. This means a 1-pulse count operation cannot be performed when this register is used as an external event counter.	pp. 83, 114 <input type="checkbox"/>
					In the free-running mode and in the clear & start mode using the valid edge of the TI000 pin, if CR000 is set to 0000H, an interrupt request (INTTM000) is generated when CR000 changes from 0000H to 0001H after an overflow (FFFFH).	pp.83, 114 <input type="checkbox"/>
					If the new value of CR000 is less than the value of 16-bit timer counter 0 (TM00), TM00 continues counting, overflows, and then starts counting from 0 again. If the new value of CR000 is less than the old value, therefore, the timer must be reset to be restarted after the value of CR000 is changed.	pp. 83, 114 <input type="checkbox"/>
					The value of CR000 after 16-bit timer/event counter 00 has stopped is not guaranteed.	pp. 83, 115 <input type="checkbox"/>
					The capture operation may not be performed for CR000 set in compare mode even if a capture trigger is input.	pp. 83, 117 <input type="checkbox"/>
	Hard				When using P21 as the input pin (TI010) of the valid edge, it cannot be used as a timer output pin (TO00). When using P21 as the timer output pin (TO00), it cannot be used as the input pin (TI010) of the valid edge.	pp. 83, 90, 119 <input type="checkbox"/>
					If the register read period and the input of the capture trigger conflict when CR000 is used as a capture register, the capture trigger input takes precedence and the read data is undefined. Also, if the count stop of the timer and the input of the capture trigger conflict, the capture trigger is undefined.	pp. 83, 116 <input type="checkbox"/>
Soft				Changing the CR000 setting may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-bit Timer/Event Counter 00 (17) Changing compare register during timer operation.	p. 83 <input type="checkbox"/>	

Chapter	Classification	Function	Details of Function	Cautions	Page		
Chapter 6	Soft	16-bit timer/event counter 00	CR010: 16-bit timer capture/compare register 010	In the free-running mode and in the clear & start mode using the valid edge of the TI000 pin, if CR010 is set to 0000H, an interrupt request (INTTM01) is generated when CR010 changes from 0000H to 0001H after an overflow (FFFFH).	pp. 84, 114 <input type="checkbox"/>		
				If the new value of CR010 is less than the value of 16-bit timer counter 00 (TM00), TM00 continues counting, overflows, and then starts counting from 0 again. If the new value of CR010 is less than the old value, therefore, the timer must be reset to be restarted after the value of CR010 is changed.	pp. 84, 114 <input type="checkbox"/>		
				The value of CR010 after 16-bit timer/event counter 00 has stopped is not guaranteed.	pp. 84, 115 <input type="checkbox"/>		
	Hard			The capture operation may not be performed for CR010 set in compare mode even if a capture trigger is input.	pp. 84, 117 <input type="checkbox"/>		
				If the register read period and the input of the capture trigger conflict when CR010 is used as a capture register, the capture trigger input takes precedence and the read data is undefined. Also, if the timer count stop and the input of the capture trigger conflict, the capture data is undefined.	pp. 84, 116 <input type="checkbox"/>		
				Changing the CR010 setting during TM00 operation may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-bit Timer/Event Counter 00 (17) Changing compare register during timer operation.	p. 85 <input type="checkbox"/>		
	Soft			TMC00: 16-bit timer mode control register 00	16-bit timer counter 00 (TM00) starts operating as soon as values other than 0 and 0 (operation stop mode) are set to TMC002 and TMC003, respectively. Set TMC002 and TMC003 to 0 and 0 to stop operation.	16-bit timer counter 00 (TM00) starts operating as soon as values other than 0 and 0 (operation stop mode) are set to TMC002 and TMC003, respectively. Set TMC002 and TMC003 to 0 and 0 to stop operation.	pp. 85, 114 <input type="checkbox"/>
						The timer operation must be stopped before writing to bits other than the OVF00 flag.	pp. 86, 115 <input type="checkbox"/>
						If the timer is stopped, timer counts and timer interrupts do not occur, even if a signal is input to the TI000/TI010 pins.	pp. 86, 114 <input type="checkbox"/>
		Except when the valid edge of the TI000 pin is selected as the count clock, stop the timer operation before setting STOP mode or system clock stop mode; otherwise the timer may malfunction when the system clock starts.	pp. 86, 119 <input type="checkbox"/>				
		Set the valid edge of the TI000 pin with bits 4 and 5 of prescaler mode register 00 (PRM00) after stopping the timer operation.	pp. 86, 115 <input type="checkbox"/>				
		If the clear & start mode entered on a match between TM00 and CR000, clear & start mode at the valid edge of the TI000 pin, or free-running mode is selected, when the set value of CR000 is FFFFH and the TM00 value changes from FFFFH to 0000H, the OVF00 flag is set to 1.	p. 86 <input type="checkbox"/>				
		Even if the OVF00 flag is cleared before the next count clock is counted (before TM00 becomes 0001H) after the occurrence of a TM00 overflow, the OVF00 flag is re-set and clearance becomes invalid.	pp. 86, 116 <input type="checkbox"/>				
		The capture operation is performed at the fall of the count clock. An interrupt request input (INTTM0n0), however, occurs at the rise of the next count clock.	pp. 86, 117 <input type="checkbox"/>				
	Hard	CRC00: Capture/compare control register 00	The timer operation must be stopped before setting CRC00.	The timer operation must be stopped before setting CRC00.	pp. 87, 115 <input type="checkbox"/>		
When the clear & start mode entered on a match between TM00 and CR000 is selected by 16-bit timer mode control register 00 (TMC00), CR000 should not be specified as a capture register.				pp. 87, 114 <input type="checkbox"/>			
To ensure the reliability of the capture operation, the capture trigger requires a pulse longer than two cycles of the count clock selected by prescaler mode register 00 (PRM00) (refer to Figure 6-17).				pp. 87, 117 <input type="checkbox"/>			

Chapter	Classification	Function	Details of Function	Caution	Page	
Chapter 6	Soft	16-bit timer/ event counter 00	TOC00: 16-bit timer output control register 00	Timer operation must be stopped before setting other than OSPT00.	pp. 88, 115 <input type="checkbox"/>	
				If LVS00 and LVR00 are read, 0 is read.	pp. 88, 115 <input type="checkbox"/>	
				OSPT00 is automatically cleared after data is set, so 0 is read.	pp. 88, 115 <input type="checkbox"/>	
				Do not set OSPT00 to 1 other than in one-shot pulse output mode.	pp. 88, 115 <input type="checkbox"/>	
	Hard		Soft	PRM00: Prescaler mode register 00	A write interval of two cycles or more of the count clock selected by prescaler mode register 00 (PRM00) is required, when OSPT00 is set to 1 successively.	pp. 88, 115 <input type="checkbox"/>
					When TOE00 is 0, set TOE00, LVS00, and LVR00 at the same time with the 8-bit memory manipulation instruction. When TOE00 is 1, LVS00 and LVR00 can be set with the 1-bit memory manipulation instruction.	p. 89 <input type="checkbox"/>
	Hard		Soft	Interval timer	Always set data to PRM00 after stopping the timer operation.	pp. 89, 115 <input type="checkbox"/>
					If the valid edge of the TI000 pin is to be set as the count clock, do not set the clear/start mode and the capture trigger at the valid edge of the TI000 pin.	pp. 89, 117 <input type="checkbox"/>
					In the following cases, note with caution that the valid edge of the TI0n0 pin is detected. <1> Immediately after a system reset, if a high level is input to the TI0n0 pin, the operation of 16-bit timer counter 00 (TM00) is enabled →If the rising edge or both rising and falling edges are specified as the valid edge of the TI0n0 pin, a rising edge is detected immediately after the TM00 operation is enabled. <2> If the TM00 operation is stopped while the TI0n0 pin is at high level, TM00 operation is then enabled after a low level is input to the TI0n0 pin →If the falling edge or both rising and falling edges are specified as the valid edge of the TI0n0 pin, a falling edge is detected immediately after the TM00 operation is enabled. <3> If the TM00 operation is stopped while the TI0n0 pin is at low level, TM00 operation is then enabled after a high level is input to the TI0n0 pin →If the rising edge or both rising and falling edges are specified as the valid edge of the TI0n0 pin, a rising edge is detected immediately after the TM00 operation is enabled.	pp. 90, 119 <input type="checkbox"/>
					The sampling clock used to eliminate noise differs when the valid edge of TI000 is used as the count clock and when it is used as a capture trigger. In the former case, the count clock is $f_{XP}$ , and in the latter case the count clock is selected by prescaler mode register 00 (PRM00). The capture operation is not performed until the valid edge is sampled and the valid level is detected twice, thus eliminating noise with a short pulse width.	pp. 90, 119 <input type="checkbox"/>
					When using P21 as the input pin (TI010) of the valid edge, it cannot be used as a timer output pin (TO00). When using P21 as the timer output pin (TO00), it cannot be used as the input pin (TI010) of the valid edge.	pp. 90, 119 <input type="checkbox"/>
					Changing the CR000 setting during TM00 operation may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-bit Timer/Event Counter 00 (17) Changing compare register during timer operation.	p. 91 <input type="checkbox"/>
					When reading the external event counter count value, TM00 should be read.	pp. 95, 119 <input type="checkbox"/>

Chapter	Classification	Function	Details of Function	Cautions	Page	
Chapter 6	Soft	16-bit timer/event counter 00	Pulse width measurement	To use two capture registers, set the TI000 and TI010 pins.	pp. 96, 117 <input type="checkbox"/>	
				The measurable pulse width in this operation example is up to 1 cycle of the timer counter.	pp.96, 98, 100, 102 <input type="checkbox"/>	
			Square-wave output	Changing the CR000 setting during TM00 operation may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-bit Timer/Event Counter 00 (17) Changing compare register during timer operation.	p. 104 <input type="checkbox"/>	
			PPG output	Changing the CRC0n0 setting during TM00 operation may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-bit Timer/Event Counter 00 (17) Changing compare register during timer operation.	p. 106 <input type="checkbox"/>	
				Values in the following range should be set to CR000 and CR010. 0000H < CR010 < CR000 ≤ FFFFH	pp.107, 119 <input type="checkbox"/>	
			PPG output	The cycle of the pulse generated through PPG output (CR000 setting value + 1) has a duty of (CR010 setting value + 1)/(CR000 setting value + 1).	pp.107, 119 <input type="checkbox"/>	
			One-shot pulse output: software trigger	Do not set the OSPT00 bit to 1 again while the one-shot pulse is being output. To output the one-shot pulse again, wait until the current one-shot pulse output is completed.	pp.109, 115 <input type="checkbox"/>	
				When using the one-shot pulse output of 16-bit timer/event counter 00 with a software trigger, do not change the level of the TI000 pin or its alternate-function port pin. Because the external trigger is valid even in this case, the timer is cleared and started even at the level of the TI000 pin or its alternate-function port pin, resulting in the output of a pulse at an undesired timing.	pp.109, 115 <input type="checkbox"/>	
				Do not set 0000H to the CR000 and CR010 registers.	pp.110, 116 <input type="checkbox"/>	
			One-shot pulse output: external trigger	16-bit timer counter 00 starts operating as soon as a value other than 00 (operation stop mode) is set to the TMC003 and TMC002 bits.	pp.111, 114 <input type="checkbox"/>	
				Do not input the external trigger again while the one-shot pulse is output. To output the one-shot pulse again, wait until the current one-shot pulse output is completed.	pp.111, 116 <input type="checkbox"/>	
				Do not set the CR000 and CR010 registers to 0000H.	pp.112, 116 <input type="checkbox"/>	
			Timer start errors	16-bit timer counter 00 starts operating as soon as a value other than 00 (operation stop mode) is set to the TMC002 and TMC003 bits.	pp.113, 114 <input type="checkbox"/>	
				An error of up to one clock may occur in the time required for a match signal to be generated after timer start. This is because 16-bit timer counter 00 (TM00) is started asynchronously to the count clock.	p. 114 <input type="checkbox"/>	
			Soft	One-shot pulse output	One-shot pulse output normally operates only in the free-running mode or in the clear & start mode at the valid edge of the TI000 pin. Because an overflow does not occur in the clear & start mode on a match between TM00 and CR000, one-shot pulse output is not possible.	p. 115 <input type="checkbox"/>
				Capture operation	When the CRC001 bit value is 1, capture is not performed in the CR000 register if both the rising and falling edges have been selected as the valid edges of the TI000 pin.	p. 117 <input type="checkbox"/>
When the CRC001 bit value is 1, the TM00 count value is not captured in the CR000 register when a valid edge of the TI010 pin is detected, but the input from the TI010 pin can be used as an external interrupt source because INTTM000 is generated at that timing.	p. 117 <input type="checkbox"/>					

Chapter	Chapter Classification	Function	Details of Function	Cautions	Page
Chapter 6	Soft	16-bit timer/event counter 00	Changing compare register during timer operation	With the 16-bit timer capture/compare register 0n0 (CR0n0) used as a compare register, when changing CR0n0 around the timing of a match between 16-bit timer counter 00 (TM00) and 16-bit timer capture/compare register 0n0 (CR0n0) during timer counting, the change timing may conflict with the timing of the match, so the operation is not guaranteed in such cases. To change CR0n0 during timer counting, INTTM000 interrupt servicing performs the following operation.	p. 118 <input type="checkbox"/>
				If CR010 is changed during timer counting without performing processing <1> above, the value in CR010 may be rewritten twice or more, causing an inversion of the output level of the TO00 pin at each rewrite.	p. 118 <input type="checkbox"/>
			External event counter	The timing of the count start is after two valid edge detections.	p. 119 <input type="checkbox"/>
Chapter 7	Soft	8-bit timer H1	CMP01: 8-bit timer H compare register 01	CMP01 cannot be rewritten during timer count operation.	p. 123 <input type="checkbox"/>
				CMP11: 8-bit timer H compare register 11	In the PWM output mode, be sure to set CMP11 when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to CMP11).
			TMHMD1: 8-bit timer H mode register 1	When TMHE1 = 1, setting the other bits of the TMHMD1 register is prohibited.	p. 125 <input type="checkbox"/>
				In the PWM output mode, be sure to set 8-bit timer H compare register 11 (CMP11) when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to the CMP11 register).	p. 125 <input type="checkbox"/>
	Hard	Soft	PWM output	In PWM output mode, the setting value for the CMP11 register can be changed during timer count operation. However, three operation clocks (signal selected using the CKS12 to CKS10 bits of the TMHMD1 register) or more are required to transfer the register value after rewriting the CMP11 register value.	p. 130 <input type="checkbox"/>
				Be sure to set the CMP11 register when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to the CMP11 register).	p. 130 <input type="checkbox"/>
Chapter 8	Soft	Watchdog timer	WDTM: Watchdog timer mode register	Set bits 7, 6, and 5 to 0, 1, and 1, respectively. Do not set the other values.	p. 138 <input type="checkbox"/>
				After reset is released, WDTM can be written only once by an 8-bit memory manipulation instruction. If writing is attempted a second time, an internal reset signal is generated. However, at the first write, if "1" and "x" are set for WDSC4 and WDSC3 respectively and the watchdog timer is stopped, then the internal reset signal does not occur even if the following are executed. <ul style="list-style-type: none"> <li>• Second write to WDTM</li> <li>• 1-bit memory manipulation instruction to WDTE</li> <li>• Writing of a value other than "ACH" to WDTE</li> </ul>	p. 139 <input type="checkbox"/>
				WDTM cannot be set by a 1-bit memory manipulation instruction.	p. 139 <input type="checkbox"/>
				When using the flash memory self programming by self writing, set the overflow time for the watchdog timer so that enough overflow time is secured (Example 1-byte writing: 200 μs MIN., 1-block deletion: 10 ms MIN.).	p. 139 <input type="checkbox"/>

Chapter	Classification	Function	Details of Function	Cautions	Page	
Chapter 8	Soft	Watchdog timer	WDTE: Watchdog timer enable register	If a value other than ACH is written to WDTE, an internal reset signal is generated.	p. 139 <input type="checkbox"/>	
				If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated.	p. 139 <input type="checkbox"/>	
				The value read from WDTE is 9AH (this differs from the written value (ACH)).	p. 139 <input type="checkbox"/>	
	Hard		When “low-speed internal oscillator cannot be stopped” is selected by option byte	In this mode, operation of the watchdog timer cannot be stopped even during STOP instruction execution. For 8-bit timer H1 (TMH1), a division of the low-speed internal oscillation clock can be selected as the count source, so clear the watchdog timer using the interrupt request of TMH1 before the watchdog timer overflows after STOP instruction execution. If this processing is not performed, an internal reset signal is generated when the watchdog timer overflows after STOP instruction execution.	p. 140 <input type="checkbox"/>	
				when “low-speed internal oscillator can be stopped by software” is selected by option byte	In this mode, watchdog timer operation is stopped during HALT/STOP instruction execution. After HALT/STOP mode is released, counting is started again using the operation clock of the watchdog timer set before HALT/STOP instruction execution by WDTM. At this time, the counter is not cleared to 0 but holds its value.	p. 142 <input type="checkbox"/>
Chapter 9	Soft	Interrupt functions	IF0: Interrupt request flag registers, MK0: Interrupt mask flag registers	Because P21 and P32 have an alternate function as external interrupt inputs, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, the interrupt mask flag should be set to 1 before using the output mode.	pp. 149, 150 <input type="checkbox"/>	
				INTM0: External interrupt mode register 0	Be sure to clear bits 0, 1, 6, and 7 to 0.	p. 150 <input type="checkbox"/>
					Before setting the INTM0 register, be sure to set the corresponding interrupt mask flag (××MK× = 1) to disable interrupts. After setting the INTM0 register, clear the interrupt request flag (××IF× = 0), then clear the interrupt mask flag (××MK× = 0), which will enable interrupts.	p. 151 <input type="checkbox"/>
				Interrupt requests are held pending	Interrupt requests will be held pending while the interrupt request flag registers (IF0) or interrupt mask flag registers (MK0) are being accessed.	p. 153 <input type="checkbox"/>
Interrupt request pending	Multiple interrupts can be acknowledged even for low-priority interrupts.	p. 154 <input type="checkbox"/>				



Chapter	Chapter Classification	Function	Details of Function	Cautions	Page	
Chapter 10	Soft	Standby function	–	The LSRSTOP setting is valid only when “Can be stopped by software” is set for the low-speed internal oscillator by the option byte.	p. 156 <input type="checkbox"/>	
			STOP mode	When shifting to the STOP mode, be sure to stop the peripheral hardware operation before executing STOP instruction (except the peripheral hardware that operates on the low-speed internal oscillation clock).	p. 157 <input type="checkbox"/>	
				If the low-speed internal oscillator is operating before the STOP mode is set, oscillation of the low-speed internal oscillation clock cannot be stopped in the STOP mode (refer to Table 10-1).	p. 157 <input type="checkbox"/>	
			Hard	OSTS: Oscillation stabilization time select register	To set and then release the STOP mode, set the oscillation stabilization time as follows. Expected oscillation stabilization time of resonator ≤ Oscillation stabilization time set by OSTS	p. 158 <input type="checkbox"/>
					The wait time after the STOP mode is released does not include the time from the release of the STOP mode to the start of clock oscillation (“a” in the figure below), regardless of whether STOP mode was released by reset signal generation or interrupt generation.	p. 158 <input type="checkbox"/>
			Soft	HALT mode setting and operating statuses	The oscillation stabilization time that elapses on power application or after release of reset is selected by the option byte. For details, refer to CHAPTER 14 OPTION BYTE.	p. 158 <input type="checkbox"/>
					Because an interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag clear, the standby mode is immediately cleared if set.	p. 159 <input type="checkbox"/>
Hard	STOP mode setting and operating statuses	Because an interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set. Thus, in the STOP mode, the normal operation mode is restored after the STOP instruction is executed and then the operation is stopped for 34 μs (TYP.) (after an additional wait time for stabilizing the oscillation set by the oscillation stabilization time select register (OSTS) has elapsed when crystal/ceramic oscillation is used).	p. 162 <input type="checkbox"/>			
		–	For an external reset, input a low level for 2 μs or more to the RESET pin.	p. 166 <input type="checkbox"/>		
Chapter 11	Hard	Reset function	–	During reset signal generation, the system clock and low-speed internal oscillation clock stop oscillating.	p. 166 <input type="checkbox"/>	
			When the RESET pin is used as an input-only port pin (P34), the μPD78F9510, 78F9511, 78F9512 is reset if a low level is input to the RESET pin after reset is released by the POC circuit and before the option byte is referenced again. The reset status is retained until a high level is input to the RESET pin.	p. 166 <input type="checkbox"/>		
			The LVI circuit is not reset by the internal reset signal of the LVI circuit.	p. 167 <input type="checkbox"/>		
			Timing of reset by overflow of watchdog timer	The watchdog timer is also reset in the case of an internal reset of the watchdog timer.	p. 169 <input type="checkbox"/>	
	Soft	RESF: Reset control flag register	Do not read data by a 1-bit memory manipulation instruction.	p. 173 <input type="checkbox"/>		

Chapter	Chapter Classification	Function	Details of Function	Cautions	Page
Chapter 12	Soft	Power-on-clear circuit	Functions of power-on-clear circuit	If an internal reset signal is generated in the POC circuit, the reset control flag register (RESF) is cleared to 00H.	p. 174 <input type="checkbox"/>
	Because the detection voltage ( $V_{POC}$ ) of the POC circuit is in a range of $2.1\text{ V} \pm 0.1\text{ V}$ , use a voltage in the range of 2.2 to 5.5 V.			p. 174 <input type="checkbox"/>	
	Soft		Cautions for power-on-clear circuit	In a system where the supply voltage ( $V_{DD}$ ) fluctuates for a certain period in the vicinity of the POC detection voltage ( $V_{POC}$ ), the system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking the following action.	p. 176 <input type="checkbox"/>
Chapter 13	Soft	Low-voltage detector	LVIM: Low-voltage detect register	To stop LVI, follow either of the procedures below.	p. 179 <input type="checkbox"/>
				<ul style="list-style-type: none"> <li>When using 8-bit manipulation instruction: Write 00H to LVIM.</li> <li>When using 1-bit memory manipulation instruction: Clear LVION to 0.</li> </ul>	
				Be sure to set bits 2 to 6 to 0.	p. 179 <input type="checkbox"/>
			LVIS: Low-voltage detection level select register	Bits 4 to 7 must be set to 0.	p. 180 <input type="checkbox"/>
				If a value other than the above is written during LVI operation, the value becomes undefined at the very moment it is written, and thus be sure to stop LVI (bit 7 of LVIM register (LVION) = 0) before writing.	p. 180 <input type="checkbox"/>
When used as reset	<1> must always be executed. When LVIMK = 0, an interrupt may occur immediately after the processing in <3>.	p. 181 <input type="checkbox"/>			
	If supply voltage ( $V_{DD}$ ) $\geq$ detection voltage ( $V_{LVI}$ ) when LVIM is set to 1, an internal reset signal is not generated.	p. 181 <input type="checkbox"/>			
Cautions for low-voltage detector	In a system where the supply voltage ( $V_{DD}$ ) fluctuates for a certain period in the vicinity of the LVI detection voltage ( $V_{LVI}$ ), the operation is as follows depending on how the low-voltage detector is used.	p. 185 <input type="checkbox"/>			
Chapter 15	Hard	Option byte	Oscillation stabilization time on power application or after reset release	The setting of this option is valid only when the crystal/ceramic oscillation clock is selected as the system clock source. No wait time elapses if the high-speed internal oscillation clock or external clock input is selected as the system clock source.	p. 189 <input type="checkbox"/>
			Control of RESET pin	Because the option byte is referenced after reset release, if a low level is input to the RESET pin before the option byte is referenced, then the reset state is not released. Also, when setting 0 to RMCE, connect the pull-up resistor.	p. 189 <input type="checkbox"/>

Chapter	Chapter Classification	Function	Details of Function	Cautions	Page
Chapter 14	Hard	Option byte	Selection of system clock source	<p>Because the X1 and X2 pins are also used as the P23 and P22 pins, the conditions under which the X1 and X2 pins can be used differ depending on the selected system clock source.</p> <p>(1) Crystal/ceramic oscillation clock is selected The X1 and X2 pins cannot be used as I/O port pins because they are used as clock input pins.</p> <p>(2) External clock input is selected Because the X1 pin is used as an external clock input pin, P121 cannot be used as an I/O port pin.</p> <p>(3) High-speed internal oscillation clock is selected P23 and P22 can be used as I/O port pins.</p>	p. 189 <input type="checkbox"/>
			Low-speed internal oscillates	<p>If it is selected that low-speed internal oscillator cannot be stopped, the count clock to the watchdog timer (WDT) is fixed to low-speed internal oscillation clock.</p> <p>If it is selected that low-speed internal oscillator can be stopped by software, supply of the count clock to WDT is stopped in the HALT/STOP mode, regardless of the setting of bit 0 (LSRSTOP) of the low-speed internal oscillation mode register (LSRCM). Similarly, clock supply is also stopped when a clock other than the low-speed internal oscillation clock is selected as a count clock to WDT. While the low-speed internal oscillator is operating (LSRSTOP = 0), the clock can be supplied to the 8-bit timer H1 even in the STOP mode.</p>	p. 190 <input type="checkbox"/>
			Caution when the RESET pin is used as an input-only port pin (P34)	Be aware of the following when re-erasing/-writing (by on-board programming using a dedicated flash memory programmer) an already-written device which has been set as "The RESET pin is used as an input-only port pin (P34)" by the option byte function. Before supplying power to the target system, connect a dedicated flash memory programmer and turn its power on. If the power is supplied to the target system beforehand, the flash memory programming mode cannot be switched to.	p. 190 <input type="checkbox"/>
			Flash memory	PG-FP4 GUI software setting value example	The above values are recommended values. Depending on the usage environment these values may change, so set them after having performed sufficient evaluations.
Chapter 15	Soft	Flash memory	Security settings	After the security setting of the batch erase is set, erasure cannot be performed for the device. In addition, even if a write command is executed, data different from that which has already been written to the flash memory cannot be written because the erase command is disabled.	p. 200 <input type="checkbox"/>
			Self programming function	Self programming processing must be included in the program before performing self writing.	p. 201 <input type="checkbox"/>
				No instructions can be executed while a self programming command is being executed. Therefore, clear and restart the watchdog timer counter in advance so that the watchdog timer does not overflow during self programming. Refer to Table 15-11 for the time taken for the execution of self programming.	p. 204 <input type="checkbox"/>
				Interrupts that occur during self programming can be acknowledged after self programming mode ends. To avoid this operation, disable interrupt servicing (by setting MK0 to FFH, and executing the DI instruction) when shifting from the normal mode to the self programming mode with a specific sequence.	p. 204 <input type="checkbox"/>
				RAM is not used while a self programming command is being executed.	p. 204 <input type="checkbox"/>
				If the supply voltage drops or the reset signal is input while the flash memory is being written or erased, writing/erasing is not guaranteed.	p. 204 <input type="checkbox"/>

Chapter	Chapter Classification	Function	Details of Function	Cautions	Page
Chapter 15	Soft	Flash memory	Self programming function	The value of the blank data set during block erasure is FFH.	p. 204 <input type="checkbox"/>
				Set the CPU clock beforehand so that it is 1 MHz or higher during self programming.	p. 204 <input type="checkbox"/>
				Execute self programming after executing the NOP and HALT instructions immediately after executing a specific sequence to set self programming mode. At this time, the HALT instruction is automatically released after 10 $\mu$ s (MAX.) + 2 CPU clocks ( $f_{CPU}$ ).	p. 204 <input type="checkbox"/>
				If the clock of the oscillator or an external clock is selected as the system clock, execute the NOP and HALT instructions immediately after executing a specific sequence to set self programming mode, wait for 8 $\mu$ s after releasing the HALT status, and then execute self programming.	p. 204 <input type="checkbox"/>
				Check FPRERR using a 1-bit memory manipulation instruction.	p. 204 <input type="checkbox"/>
				The state of the pins in self programming mode is the same as that in HALT mode.	p. 204 <input type="checkbox"/>
				Since the security function set via on-board/off-board programming is disabled in self programming mode, the self programming command can be executed regardless of the security function setting. To disable write or erase processing during self programming, set the protect byte.	p. 204 <input type="checkbox"/>
				Be sure to clear bits 5 to 7 of flash address pointer H (FLAPH) and flash address pointer H compare register (FLAPHC) to 0 before executing the self programming command. If self programming is executed with these bits set to 1, the device may malfunction.	p. 204 <input type="checkbox"/>
				Clear the value of the FLCMD register to 00H immediately before setting to self programming mode and normal mode.	p. 204 <input type="checkbox"/>
			FLPMC: Flash programming mode control register	Caution in the case of setting the self programming mode, refer to 15.8.2 Caution on self programming function.	p. 205 <input type="checkbox"/>
				Set the CPU clock beforehand so that it is 1 MHz or higher during self programming.	p. 205 <input type="checkbox"/>
				Execute self programming after executing the NOP and HALT instructions immediately after executing a specific sequence to set self programming mode. At this time, the HALT instruction is automatically released after 10 $\mu$ s (MAX.) + 2 CPU clocks ( $f_{CPU}$ ).	p. 205 <input type="checkbox"/>
				If the clock of the oscillator or an external clock is selected as the system clock, execute the NOP and HALT instructions immediately after executing a specific sequence to set self programming mode, wait for 8 $\mu$ s after releasing the HALT status, and then execute self programming.	p. 205 <input type="checkbox"/>
			PFCMD: Flash protect command register	Interrupt servicing cannot be executed in self programming mode. Disable interrupt servicing (by executing the DI instruction while MK0 = FFH) between the points before executing the specific sequence that sets self programming mode and after executing the specific sequence that changes the mode to the normal mode.	p. 206 <input type="checkbox"/>
			PFS: Flash status register	Check FPRERR using a 1-bit memory manipulation instruction.	p. 206 <input type="checkbox"/>
			FLAPH, FLAPL: Flash address pointers H and L	Be sure to clear bits 4 to 7 of FLAPH and FLAPHC to 0 before executing the self programming command. If the value of these bits is 1 when executing the self programming command.	p. 209 <input type="checkbox"/>

**APPENDIX D LIST OF CAUTIONS**

(12/12)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 15	Soft	Flash memory	FLAPHC, FLAPLC: Flash address pointer H/L compare registers	Be sure to clear bits 4 to 7 of FLAPH and FLAPHC to 0 before executing the self programming command. If the value of these bits is 1 when executing the self programming command.	p. 209 <input type="checkbox"/>
				Set the number of the block subject to a block erase, verify, or blank check (same value as FLAPH) to FLAPHC.	p. 209 <input type="checkbox"/>
				Clear FLAPLC to 00H when a block erase is performed, and FFH when a blank check is performed.	p. 209 <input type="checkbox"/>
			Shifting to self programming mode	Be sure to perform the series of operations described above using the user program at an address where data is not erased nor written.	pp.211, 212, 214, 215 <input type="checkbox"/>
			Shifting to normal mode		
Byte write	If a write results in failure, erase the block once and write to it again.	p. 223 <input type="checkbox"/>			
Chapter 17	Hard	Recommended soldering conditions	–	These specifications show target values, which may change after device evaluation. The operating voltage range may also change.	p. 258 <input type="checkbox"/>
			Absolute maximum ratings	Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.	p. 258 <input type="checkbox"/>
			X1 oscillator characteristics	When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance. <ul style="list-style-type: none"> <li>• Keep the wiring length as short as possible.</li> <li>• Do not cross the wiring with the other signal lines.</li> <li>• Do not route the wiring near a signal line through which a high fluctuating current flows.</li> <li>• Always make the ground point of the oscillator capacitor the same potential as V<sub>SS</sub>.</li> <li>• Do not ground the capacitor to a ground pattern through which a high current flows.</li> <li>• Do not fetch signals from the oscillator.</li> </ul>	p. 259 <input type="checkbox"/>
Chapter 19	Hard	Recommended soldering conditions	Lead-free products	Products with -A at the end of the part number are lead-free products.	p. 270 <input type="checkbox"/>
			–	For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.	p. 270 <input type="checkbox"/>
			–	Do not use different soldering methods together (except for partial heating).	p. 270 <input type="checkbox"/>

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