
ML610Q174

The low power micro controller corresponding to 5v for household appliances

GENERAL DESCRIPTION

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as 10-bit A/D converter, timer, PWM, synchronous serial port, UART, I2C bus interface (master), Battery level detect circuit, LCD driver, are incorporated around 8-bit CPU nX-U8/100.

The CPU nX-U8/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel processing.

The on-chip debug function that is installed enables program debugging and programming.

FEATURES

- CPU
 - 8-bit RISC CPU (CPU name: nX-U8/100)
 - Instruction system: 16-bit instructions
 - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
 - On-Chip debug function
 - Minimum instruction execution time
 - Approx 30.5 μ s (at 32.768kHz system clock)
 - Approx 0.122 μ s (at 8.192MHz system clock) @ $V_{DD} = 2.2$ to 5.5V
- Internal memory
 - Internal 128-Kbyte flash ROM (64K \times 16-bit) (including unusable 1KByte TEST area)
 - Internal 2-Kbyte Data Flash (1-Kbyte \times 2)
 - Internal 4-Kbyte RAM (4096 \times 8-bit)
- Interrupt controller
 - 1 non-maskable interrupt sources (Internal source: 1, External source: 1)
 - 26 maskable interrupt sources (Internal source: 22, External source: 4)
- Time base counter
 - Low-speed time base counter \times 1 channel
 - High-speed time base counter \times 1 channel
- Watchdog timer
 - Generates a non-maskable interrupt upon the first overflow and a system reset occurs upon the second
 - Free running
 - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)
- Timers
 - 8 bits \times 6ch (16-bit configuration available)

- PWM
 - Resolution 16 bits × 3 channel(IGBT control)
- Synchronous serial port
 - 2ch
 - Master/slave selectable
 - LSB first/MSB first selectable
 - 8-bit length/16-bit length selectable
- UART
 - Half-duplex
 - TXD/RXD × 2 channels
 - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
 - Positive logic/negative logic selectable
 - Built-in baud rate generator
- I²C bus interface
 - Master function only
 - Fast mode (400kbit/s@8MHz), Standard mode (100kbit/s@8MHz)
- Successive approximation type A/D converter
 - 10-bit A/D converter
 - Input: 12ch (Maximum)
 - Conversion time: 12.75μs per channel
- Analog Comparator
 - 2ch
 - Interrupt allow edge selection and sampling selection
- General-purpose ports ×61 (Maximum)
 - Input-only port × 6ch
 - Output-only port × 6ch (including secondary functions)
 - Input/output × 19ch (including secondary functions)
 - Input/output × 30ch (including LCD driver functions)
- LCD driver
 - 128 dots max. (32 seg × 4 com), 1/1 to 1/4 duty
 - Frame frequency selectable (approx. 64Hz, 73Hz, 85Hz, 102Hz, 32Hz, 128Hz, 171Hz, and 256Hz)
 - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
 - LCD drive voltage generation: external or internal selectable
- Power supply voltage detect function
 - Judgment voltages: One of 4 levels
 - Judgment accuracy: ±2% (Typ.)

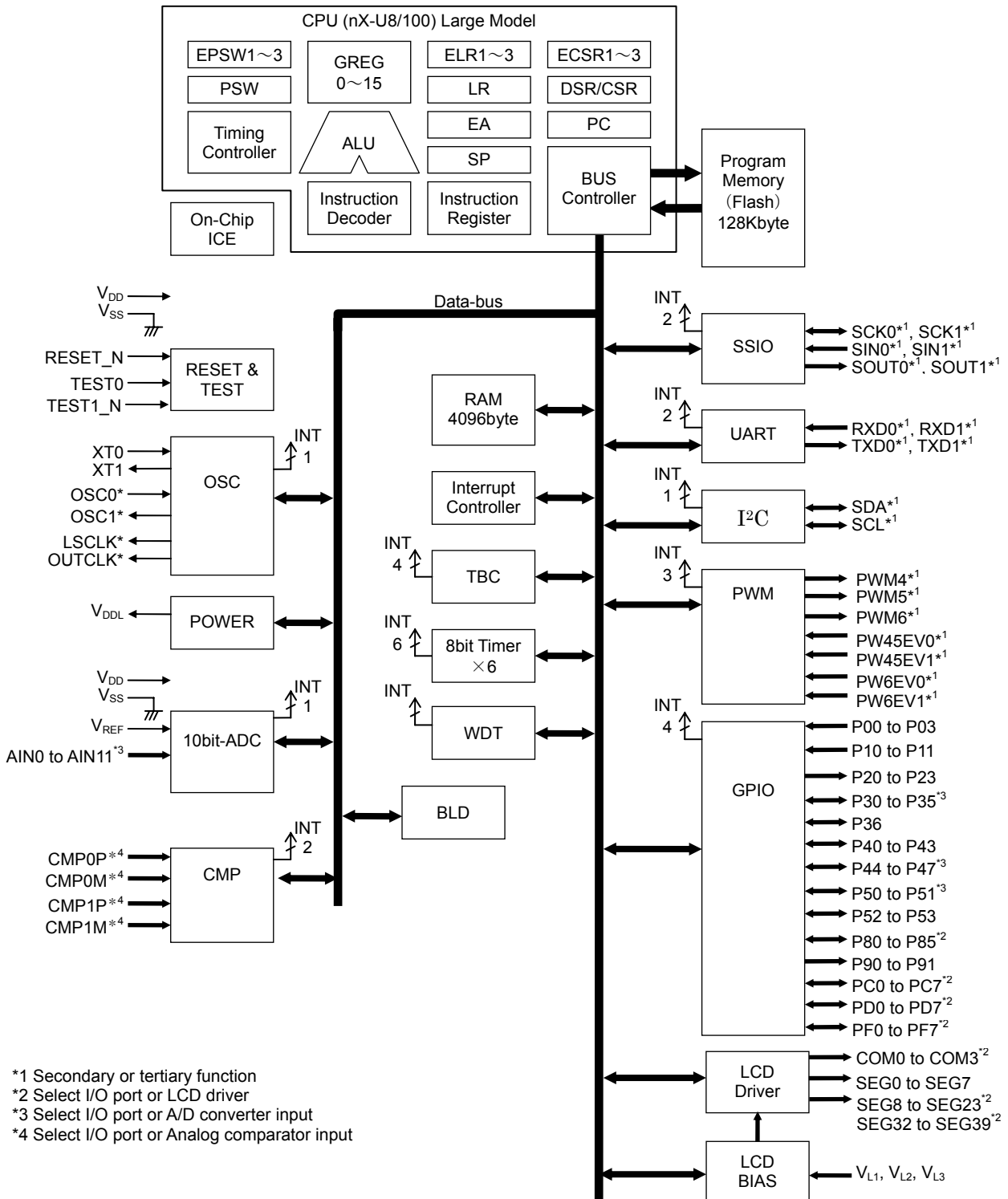
- Reset
 - Reset through the RESET_N pin
 - Reset by the watchdog timer (WDT) overflow
- Clock
 - Low-speed clock (This LSI can not guarantee the operation without low-speed clock)
Crystal oscillation (32.768 kHz) or Built-in RC oscillation (32.7kHz)
 - High-speed clock
Built-in oscillation (8.192MHz/8MHz), Crystal/Ceramic oscillation (8MHz), external clock
- Power management
 - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
 - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
 - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
 - Block control function: Operation of an intact functional block circuit is powered down. (register reset and clock stop)
- Shipment
 - 80-pin QFP (QFP80-P-1420-0.80)
 - ML610Q174-xxxGA (blank product: ML610Q174-NNNGA)

xxx: ROM code number
- Guaranteed operating range
 - Operating temperature: -40°C to 85°C
 - Operating voltage: $V_{\text{DD}} = 2.2\text{V}$ to 5.5V , $V_{\text{REF}} = 4.5\text{V}$ to 5.5V

BLOCK DIAGRAM

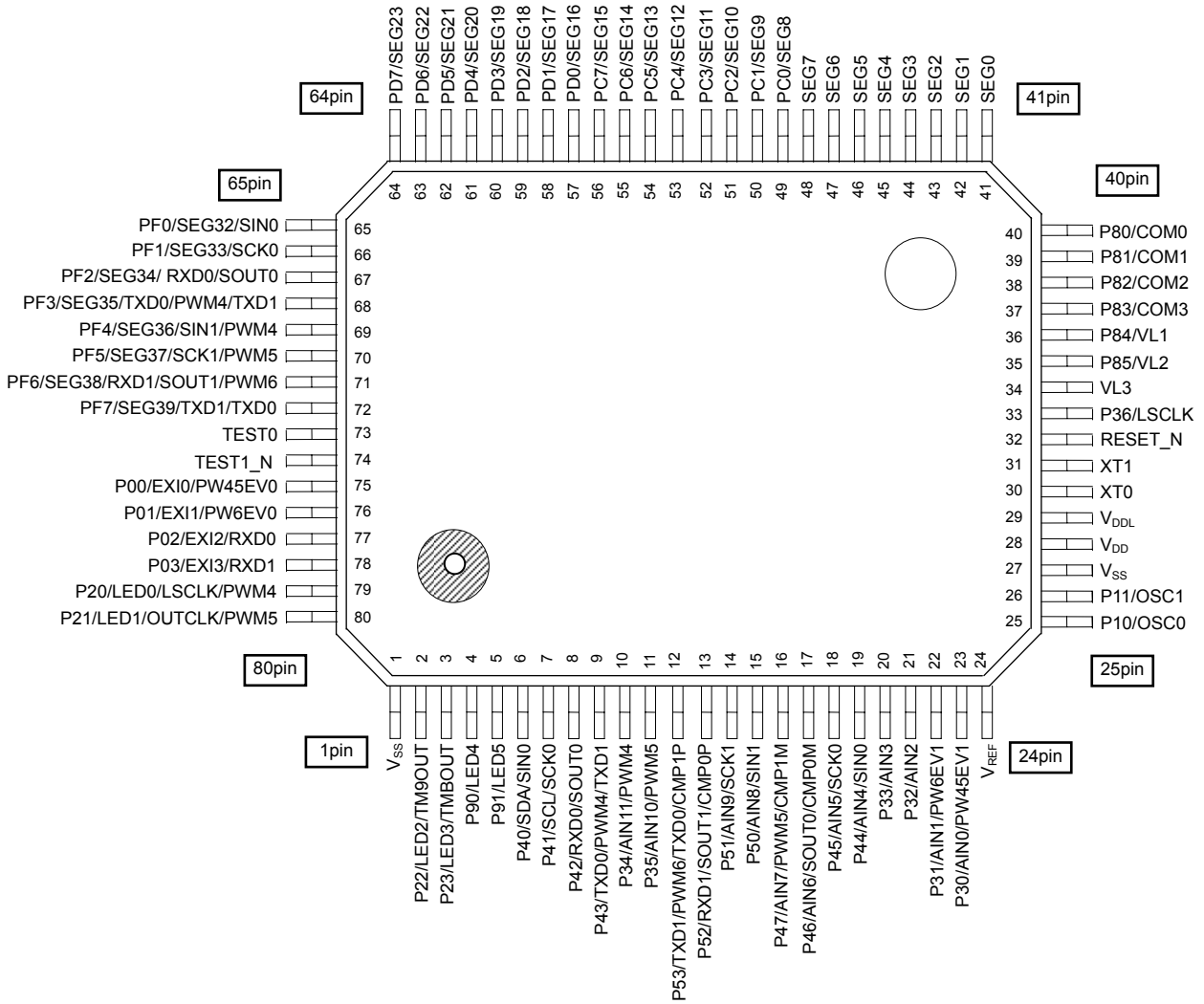
Figure 1-1 is a block diagram of the ML610Q174.

Symbols with an asterisk “*” indicate that each of them is the secondary or tertiary function of the corresponding port.



PIN CONFIGURATION

ML610Q174 QFP package product



LIST OF PINS

Pin No.	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
1,27	V _{SS}	—	Negative power supply pin	—	—	—	—	—	—
28	V _{DD}	—	Positive power supply pin	—	—	—	—	—	—
29	V _{DDL}	—	Power supply for internal logic (internally generated)	—	—	—	—	—	—
34	V _{L3}	—	Power supply pin for LCD bias	—	—	—	—	—	—
73	TEST0	I/O	Input/output pin for testing	—	—	—	—	—	—
74	TEST1_N	I/O	Input/output pin for testing	—	—	—	—	—	—
32	RESET_N	I	Reset input pin	—	—	—	—	—	—
30	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
31	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
24	V _{REF}	I	Reference power supply pin of Successive-approximation type ADC	—	—	—	—	—	—
75	P00/EXI0/ PW45EV0	I	Input port / External interrupt / PW45EV0 input	—	—	—	—	—	—
76	P01/EXI1/ PW6EV0	I	Input port / External interrupt/ PW6EV0 input	—	—	—	—	—	—
77	P02/EXI2/ RXD0	I	Input port / External interrupt UART0 data input	—	—	—	—	—	—
78	P03/EXI3/ RXD1	I	Input port / External interrupt / UART1 data input	—	—	—	—	—	—
25	P10	I	Input port	OSC0	I	High-speed clock oscillation pin	—	—	—
26	P11	I	Input port	OSC1	O	High-speed clock oscillation pin	—	—	—
79	P20/ LED0	O	Output port / LED drive	LSCLK	O	Low-speed clock output	PWM4	O	PWM4 output
80	P21/ LED1	O	Output port / LED drive	OUTCLK	O	Low-speed clock output	PWM5	O	PWM5 output
2	P22/ LED2	O	Output port / LED drive	—	—	—	TM9OUT	O	Timer9 output
3	P23/ LED3	O	Output port / LED drive	—	—	—	TMBOUT	O	TimerB output
23	P30/ PW45EV1 /AIN0	I/O	Input/output port / PW45EV1 input / Successive approximation type ADC input	—	—	—	—	—	—
22	P31/ PW6EV1 AIN1	I/O	Input/output port / PW6EV1 input / Successive approximation type ADC input	—	—	—	—	—	—
21	P32/ AIN2	I/O	Input/output port / Successive approximation type ADC input	—	—	—	—	—	—
20	P33/ AIN3	I/O	Input/output port / Successive approximation type ADC input	—	—	—	—	—	—
10	P34/ AIN11	I/O	Input/output port / Successive approximation type ADC input	—	—	—	PWM4	O	PWM4 output
11	P35/ AIN10	I/O	Input/output port / Successive approximation type ADC input	—	—	—	PWM5	O	PWM5 output
33	P36	I/O	Input/output port	LSCLK	O	Low-speed clock output	—	—	—

Pin No.	Primary function			Secondary function			Tertiary function			Fourthly function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
6	P40	I/O	Input/output port	SDA	I/O	I ² C data input/output	SIN0	I	SSIO0 data input	—	—	—
7	P41	I/O	Input/output port	SCL	I/O	I ² C clock input/output	SCK0	I/O	SSIO0 synchronous clock input/output	—	—	—
8	P42	I/O	Input/output port	RXD0	I	UART0 data input	SOUT0	O	SSIO0 data output	—	—	—
9	P43	I/O	Input/output port	TXD0	O	UART0 data output	PWM4	O	PWM4 output	TXD1	O	UAR1 data output
19	P44/ TOP4CK/ AIN4	I/O	Input/output port / Timer0 / PWM4 external clock input / Successive approximation type ADC input	—	—	—	SIN0	I	SSIO0 data input	—	—	—
18	P45/ T1P5CK/ AIN5	I/O	Input/output port / Timer1 / PWM5 external clock input / Successive approximation type ADC input	—	—	—	SCK0	I/O	SSIO0 synchronous clock input/output	—	—	—
17	P46/ T8AP6CK / AIN6/ CMP0M	I	Input/output port / Timer8,A / PWM6 external clock input / Successive approximation type ADC input / Comparator0 inverting input	—	—	—	SOUT0	O	SSIO0 data output	—	—	—
16	P47/ T9BCK/ AIN7/ CMP1M	I	Input/output port / Timer9,B external clock input / Successive approximation type ADC input / Comparator1 inverting input	—	—	—	PWM5	O	PWM5 output	—	—	—
15	P50/ AIN8	I/O	Input/output port / Successive approximation type ADC input	—	—	—	SIN1	I	SSIO1 data input	—	—	—
14	P51/ AIN9	I/O	Input/output port / Successive approximation type ADC input	—	—	—	SCK1	I/O	SSIO1 synchronous clock input/output	—	—	—
13	P52/ CMP0P	I/O	Input/output port / Comparator0 non-inverting input	RXD1	I	UART1 data input	SOUT1	O	SSIO1 data output	—	—	—
12	P53/ CMP1P	I/O	Input/output port / Comparator1 non-inverting input	TXD1	O	UART1 data input	PWM6	O	PWM6 output	TXD0	O	UAR0 data output
40	P80/ COM0	I/O	Input/output port / LCD common pin	—	—	—	—	—	—	—	—	—
39	P81/ COM1	I/O	Input/output port / LCD common pin	—	—	—	—	—	—	—	—	—
38	P82/ COM2	I/O	Input/output port / LCD common pin	—	—	—	—	—	—	—	—	—
37	P83/ COM3	I/O	Input/output port / LCD common pin	—	—	—	—	—	—	—	—	—
36	P84/ V _{L1}	I/O	Input/output port / Power supply pin for LCD bias	—	—	—	—	—	—	—	—	—

Pin No.	Primary function			Secondary function			Tertiary function			Fourthly function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
35	P85/ V _{L2}	I/O	Input/output port/ Power supply pin for LCD bias	—	—	—	—	—	—	—	—	—
4	P90/ LED4	O	Output port / LED drive	—	—	—	—	—	—	—	—	—
5	P91/ LED5	O	Output port / LED drive	—	—	—	—	—	—	—	—	—
41	SEG0	O	LCD segment pin	—	—	—	—	—	—	—	—	—
42	SEG1	O	LCD segment pin	—	—	—	—	—	—	—	—	—
43	SEG2	O	LCD segment pin	—	—	—	—	—	—	—	—	—
44	SEG3	O	LCD segment pin	—	—	—	—	—	—	—	—	—
45	SEG4	O	LCD segment pin	—	—	—	—	—	—	—	—	—
46	SEG5	O	LCD segment pin	—	—	—	—	—	—	—	—	—
47	SEG6	O	LCD segment pin	—	—	—	—	—	—	—	—	—
48	SEG7	O	LCD segment pin	—	—	—	—	—	—	—	—	—
49	PC0 / SEG8	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
50	PC1 / SEG9	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
51	PC2 / SEG10	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
52	PC3 / SEG11	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
53	PC4 / SEG12	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
54	PC5 / SEG13	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
55	PC6 / SEG14	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
56	PC7 / SEG15	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
57	PD0 / SEG16	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
58	PD1 / SEG17	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
59	PD2 / SEG18	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
60	PD3 / SEG19	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
61	PD4 / SEG20	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
62	PD5 / SEG21	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
63	PD6 / SEG22	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
64	PD7 / SEG23	I/O	Input/output port / LCD segment pin	—	—	—	—	—	—	—	—	—
65	PF0 / SEG32	I/O	Input/output port / LCD segment pin	—	—	—	SIN0	I	SSIO0 data input	—	—	—
66	PF1 / SEG33	I/O	Input/output port / LCD segment pin	—	—	—	SCK0	I/O	SSIO0 synchronou s clock input/output	—	—	—
67	PF2 / SEG34	I/O	Input/output port / LCD segment pin	RXD0	I	UART0 data input	SOUT0	O	SSIO0 data output	—	—	—
68	PF3 / SEG35	I/O	Input/output port / LCD segment pin	TXD0	O	UART0 data output	PWM4	O	PWM4 output	TXD1	O	UAR1 data output
69	PF4 / SEG36	I/O	Input/output port / LCD segment pin	—	—	—	SIN1	I	SSIO1 data input	PWM4	O	PWM4 output
70	PF5 / SEG37	I/O	Input/output port / LCD segment pin	—	—	—	SCK1	I/O	SSIO1 synchronou s clock input/output	PWM5	O	PWM5 output
71	PF6 / SEG38	I/O	Input/output port / LCD segment pin	RXD1	I	UART1 data input	SOUT1	O	SSIO1 data output	PWM6	O	PWM6 output
72	PF7 / SEG39	I/O	Input/output port / LCD segment pin	TXD1	O	UART1 data input	—	—	—	TXD0	O	UAR0 data output

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary	Logic
Power supply				
V _{SS}	—	Negative power supply pin	—	—
V _{DD}	—	Positive power supply pin	—	—
V _{DDL}	—	Positive power supply pin for internal logic (internally generated). Connect capacitors (C _L) (see Measuring Circuit 1) between this pin and V _{SS} .	—	—
V _{L1}	—	Power supply pins for LCD bias (external input). This function is allocated to the primary function of the P84 pin.	—	—
V _{L2}	—	Power supply pins for LCD bias (external input). This function is allocated to the primary function of the P85 pin.	—	—
V _{L3}	—	Power supply pins for LCD bias (external input)	—	—
Test				
TEST0	I/O	Input/output pin for testing. This pin has a pull-down resistor built in.	—	Positive
TEST1_N	I/O	Input/output pin for testing. This pin has a pull-up resistor built in.	—	Negative
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, the device is placed in system reset mode and the internal circuit is initialized. If after that this pin is set to a “H” level, program execution starts. This pin has a pull-up resistor built in.	—	Negative
XT0	I	Crystal connection pin for low-speed clock. A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors C _{DL} and C _{GL} are connected across this pin and V _{SS} as required.	—	—
XT1	O		—	—
OSC0	I	Crystal/ceramic connection pin for high-speed clock. A 8MHz crystal or ceramic is connected to this pin. Capacitors C _{DH} and C _{GH} (see measuring circuit 1) are connected across this pin and V _{SS} .	—	—
OSC1	O		—	—
LSCLK	O	Low-speed clock output. This function is allocated to the secondary function of the P20/P36 pin.	Secondary	—
OUTCLK	O	High-speed clock output. This function is allocated to the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00 to P03	I	General-purpose input ports. Provided with a secondary function for each port. Cannot be used as ports if their secondary functions are used.	Primary	Positive
P10 to P11	I			
General-output input port				
P20 to P23	O	General-purpose output ports. Provided with a secondary function for each port. Cannot be used as ports if their secondary functions are used.	Primary	Positive
P90 to P91	O	General-purpose output ports. Provided with a secondary function for each port. Cannot be used as ports if their secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30 to P36	I/O	General-purpose input/output ports. Provided with a secondary function for each port. Cannot be used as ports if their secondary functions are used.	Primary	Positive
P40 to P47				
P50 to P53				
P80 to P85				
PC0 to PC7		General-purpose input/output ports. Provided with a LCD segment for each port. Cannot be used as ports if LCD segment are used.		
PD0 to PD7				
PF0 to PF7				

Pin name	I/O	Description	Primary/ Secondary	Logic
UART				
TXD0	O	UART0 data output pin. Allocated to the secondary function of the P43 and PF3 pins and the fourthly function of the P53 and PF7 pins.	Secondary Fourthly	Positive
RXD0	I	UART0 data input pin. Allocated to the primary function of the P02 pin and the secondary function of the P42 and PF2 pins.	Secondary	Positive
TXD1	O	UART1 data output pin. Allocated to the secondary function of the P53 and PF7 pins and the fourthly function of the P43 and PF3 pins.	Secondary Fourthly	Positive
RXD1	I	UART1 data input pin. Allocated to the primary function of the P03 pin and the secondary function of the P52 and PF6 pins.	Secondary	Positive
I²C bus interface				
SDA	I/O	I ² C data input/output pin. This pin is used as the secondary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor.	Secondary	Positive
SCL	I/O	I ² C clock output pin. This pin is used as the secondary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SIN0	I	Synchronous serial data input pin. Allocated to the tertiary function of the P40 and P44 and PF0 pins.	Tertiary	Positive
SCK0	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P41 and P45 and PF1 pins.	Tertiary	—
SOUT0	O	Synchronous serial data output pin. Allocated to the tertiary function of the P42 and P46 and PF2 pins.	Tertiary	Positive
SIN1	I	Synchronous serial data input pin. Allocated to the tertiary function of the P50 and PF4 pins.	Tertiary	Positive
SCK1	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P51 and PF5 pins.	Tertiary	—
SOUT1	O	Synchronous serial data output pin. Allocated to the tertiary function of the P52 and PF6 pins.	Tertiary	Positive
PWM				
PWM4	O	PWM4 output pin. Allocated to the tertiary function of the P34 and P43 and P20 and PF3 and PF4 pins.	Tertiary	Positive
PWM5	O	PWM5 output pin. Allocated to the tertiary function of the P35 and P47 and P21 and PF5 pins.	Tertiary	Positive
PWM6	O	PWM6 output pin. Allocated to the tertiary function of the P53 and PF6 pins.	Tertiary	Positive
T0P4CK	I	External clock input pin for timer 0 and PWM4. Allocated to the primary function of the P44 pin.	Primary	—
T1P5CK	I	External clock input pin for timer 1 and PWM5. Allocated to the primary function of the P45 pin.	Primary	—
T8AP6CK	I	External clock input pin for timer 8 and timer A and PWM6. Allocated to the primary function of the P46 pin.	Primary	—
PW45EV0 PW45EV1	I	Control start /stop pin for PWM4 and PWM5. Allocated to the primary function of the P00 and P30 pins.	Primary	—
PW6EV0 PW6EV1	I	Control start /stop pin for PWM6. Allocated to the primary function of the P01 and P31 pins.	Primary	—
External interrupt				
EXI0–EXI3	I	External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software. Allocated to the primary function of the P00–P03 pins.	Primary	Positive/ Negative

Pin name	I/O	Description	Primary/ Secondary	Logic
Timer				
T0P4CK	I	External clock input pin for timer 0 and PWM4. Allocated to the primary function of the P44 pin.	Primary	—
T1P5CK	I	External clock input pin for timer 1 and PWM5. Allocated to the primary function of the P45 pin.	Primary	—
T8AP6CK	I	External clock input pin for timer 8 and timer A and PWM6. Allocated to the primary function of the P46 pin.	Primary	—
T9BCK	I	External clock input pin for timer 9 and timer B. Allocated to the primary function of the P47 pin.	Primary	—
TM9OUT	O	Timer9 overflow output pin. Allocated to the secondary function of the P22 pin.	Tertiary	Positive
TMBOUT	O	TimerB overflow output pin. Allocated to the secondary function of the P23 pin.	Tertiary	Positive
LED drive				
LED0-LED5	O	Pins for LED driving. Allocated to the primary function of the P20–P23 pins and P90–P91 pins.	Primary	Positive/ Negative
Successive-approximation type A/D converter				
V _{REF}	I	Reference power supply pin for successive approximation type A/D converter.	—	—
AIN0–AIN11	I	Analog inputs to Ch0–Ch11 of the successive-approximation type A/D converter. Allocated to the secondary function of the P30 to P35 and P44 to P47 and P50 to P51 pins.	—	—
Analog Comparator				
CMP0P	I	Non-inverting input for comparator0. This pin is used as the primary function of the P52 pin.	—	—
CMP0M	I	Inverting input for comparator0. This pin is used as the primary function of the P46 pin.	—	—
CMP1P	I	Non-inverting input for comparator1. This pin is used as the primary function of the P53 pin.	—	—
CMP1M	I	Inverting input for comparator1. This pin is used as the primary function of the P47 pin.	—	—
LCD driver				
COM0 to COM3	O	LCD common output pins.	—	—
SEG0 to SEG7	O	LCD segment output pins.	—	—
SEG8 to SEG23 SEG32 to SEG39	O	LCD segment output pins. Allocated to the secondary function of the PC0 to PC7 and PD0 to PD7 and PF0 to PF7 pins.	—	—

TERMINATION OF UNUSED PINS

How to Terminate Unused Pins

Pin	Recommended pin termination
RESET_N	open
TEST0	open
TEST1_N	open
V _{REF}	Connect to V _{DD}
V _{L1}	open
P00 to P03	Connect V _{DD} or V _{SS}
P10 to P11	Connect V _{DD} or V _{SS}
P20 to P23	open
P30 to P33 (AIN0 to AIN3)	open
P34 to P35 (AIN11, AIN10)	open
P36	open
P40 to P43	open
P44 to P47 (AIN4 to AIN7)	open
P50 to P51 (AIN8 to AIN9)	open
P52 to P53	open
P80 to P85	open
P90 to P91	open
SEG0 to SEG7	open
PC0 to PC7 (SEG8 to 15)	open
PD0 to PD7 (SEG16 to 23)	open
PF0 to PF7 (SEG32 to 39)	open

Note:

For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V _{DD}	Ta = 25°C	-0.3 to +7.0	V
Power supply voltage 2	V _{DDL}	Ta = 25°C	-0.3 to +3.6	V
Power supply voltage 3	V _{L1}	Ta = 25°C	-0.3 to +2.33	V
Power supply voltage 4	V _{L2}	Ta = 25°C	-0.3 to +4.66	V
Power supply voltage 5	V _{L3}	Ta = 25°C	-0.3 to +7.0	V
Reference voltage	V _{REF}	Ta = 25°C	-0.3 to V _{DD} +0.3	V
Analog input voltage	V _{AI}	Ta = 25°C	-0.3 to V _{DD} +0.3	V
Input voltage	V _{IN}	Ta = 25°C	-0.3 to V _{DD} +0.3	V
Output voltage	V _{OUT}	Ta = 25°C	-0.3 to V _{DD} +0.3	V
Output current 1	I _{OUT1}	Port3,4,5,8,C,D,F Ta = 25°C	-12 to +11	mA
Output current 2	I _{OUT2}	Port2,9 Ta = 25°C	-12 to +20	mA
Power dissipation	PD	Ta = 25°C	1	W
Storage temperature	T _{STG}	—	-55 to +150	°C

Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T _{OP}	—	-40 to +85	°C
Operating voltage	V _{DD}	—	2.2 to 5.5	V
Reference voltage	V _{REF}	—	4.5 to V _{DD}	V
Analog input voltage	V _{AI}	—	V _{SS} to V _{REF}	V
Operating frequency (CPU)	f _{OP}	—	30k to 8.4M	Hz
Low-speed crystal oscillation frequency	f _{XTL}	—	32.768k	Hz
Capacitor externally connected to V _{DD} pin	C _V	—	10±30%	μF
Capacitor externally connected to V _{ref} pin	C _{AV}	—	1±30%	μF
Low-speed crystal oscillation external capacitor	C _{DL}	Use 32.768KHz Crystal Oscillator DT-26 (DAISHINKU CORP.)	12 to 25	pF
	C _{GL}		12 to 25	
High-speed crystal/ceramic oscillation frequency	f _{XTH}	—	8M / 8.192M	Hz
High-speed crystal oscillation external capacitor*	C _{DH}	—	47±30%	pF
	C _{GH}	—	47±30%	
Capacitor externally connected to V _{DDL} pin	C _L	—	10±30%	μF

* C_{GH} and C_{DH} are built into, external capacity is unnecessary for CSTLS8M00G56 (made by Murata Mfg.).

Flash Memory Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T _{OP}	Data flash memory, At write/erase	-40 to +85	°C
		Flash ROM, At write/erase	0 to +40	
Operating voltage	V _{DD}	At write/erase	2.2 to 5.5	V
Maximum rewrite count	C _{EPD}	Data flash memory	6000	times
	C _{EPP}	Flash ROM	100	
Data retention period	Y _{DR}	—	10	years

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Block erase time	T _{BERASE}	—	—	—	100	ms
Sector erase time	T _{SERASE}	—	—	—	100	
1 word write time	T _{WRITE}	—	—	—	40	µs

*1: At the writing of a flash ROM, it is necessary to supply voltage to V_{DDL} pin within the limits of the above-mentioned regulation. Pulldown resistance is built in the V_{PP} pin.

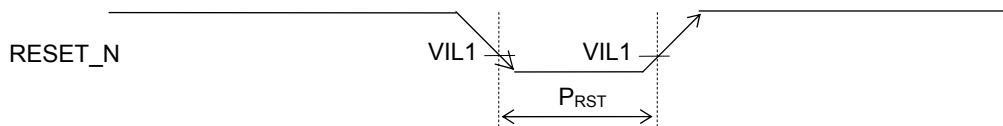
DC Characteristics (1 of 7)

(V_{DD}=2.2 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
High-speed crystal oscillation start time	T _{XTH}	—	—	2	20	ms	1
Low-speed crystal oscillation start time*1	T _{XTL}	—	—	0.6	2	s	
Low-speed RC oscillator frequency	f _{LCR}	Ta= -10 to 60°C	Typ -5%	32.7k	Typ +5%	Hz	
PLL oscillation frequency	f _{PLL}	LSCLK=32.768kHz 1000 clock average	Typ -1%	8.192	Typ +1%	MHz	
Reset pulse width	P _{RST}	—	100	—	—	µs	
Reset noise rejection pulse width	P _{NRST}	—	—	—	0.4		

*1: Use 32.768KHz Crystal Oscillator DT-26 (Daishinku) with capacitance C_{GL}/C_{DL}=12pF.

Reset



Reset by RESET_N pin

DC Characteristics (2 of 7)

($V_{DD}=2.2$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+85^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
BLD threshold voltage	V_{BLD}	$T_a = 25^{\circ}C$	LD3 to 0 = 0H	Typ. -2%	2.35	Typ. +2%	V	1
			LD3 to 0 = 3H		2.80			
			LD3 to 0 = 9H		3.70			
			LD3 to 0 = FH		4.60			

DC Characteristics (3 of 7)

($V_{DD}=2.2$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+85^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Common mode Input voltage	$CMPnM$ V_{IN}	—	0	—	V_{DD} -1.4	V	1
	$CMPnP$ V_{IN}	—	0	—	V_{DD}		
Input offset voltage	V_{CMPOF}	—	—	5	100	mV	
Response time	T_{CMP}	$CMPnP = CMPnM \pm 100mV$	—	—	1	μS	
Supply current (Operating)	I_{CMP}	CMP0,CMP1 operating	—	30	—	μA	

DC Characteristics (4 of 7)

($V_{DD}=2.2$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+85^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
LCD built-in division resistance	R_{LH}	$T_a = -10$ to $+70^{\circ}C$	Typ. -5%	200	Typ. +5%	k Ω	1
	R_{LL}	$T_a = -10$ to $+70^{\circ}C$	Typ. -20%	20	Typ. +20%		

DC Characteristics (5 of 7)

($V_{DD}=2.2$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+85^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU: In STOP state	-40 to +35 $^{\circ}C$	—	0.7	6	μA	1
		Low-speed/high-speed oscillation: Stopped	-40 to +85 $^{\circ}C$	—	0.7	22		
Supply current 2	IDD2	CPU: In HALT state (LTBC,WBC: Operating ^{*2})	-40 to +35 $^{\circ}C$	—	2.0	7		
		High-speed oscillation: Stopped	-40 to +85 $^{\circ}C$	—	2.0	24		
Supply current 3	IDD3	CPU: Running at 32kHz ^{*1}	-40 to +35 $^{\circ}C$	—	13	20		
		High-speed oscillation: Stopped	-40 to +85 $^{\circ}C$	—	13	42		
Supply current 4	IDD4	CPU: Running at 8MHz Crystal/ceramic oscillating mode ^{*2}		—	5	8	mA	

*1: Case when the CPU operating rate is 100% (with no HALT state)

*2: Significant bits of BLKCON0 to BLKCON7 registers are all "1".

DC Characteristics (6 of 7)

($V_{DD}=2.2$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+85^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Output voltage 1 (P20 to P23) (P30 to P36) (P40 to P47) (P50 to P53) (P80 to P85) (P90 to P91) (PC0 to PC7) (PD0 to PD7) (PF0 to PF7)	VOH1	IOH1 = -0.5mA		V_{DD} -0.5	—	—	V	2
	VOL1	IOL1 = +0.5mA		—	—	0.5		
Output voltage 2 (P20-P23) (P90-P91)	VOL2	When LED drive mode is selected	IOL2 = +10mA $V_{DD} \geq 4.5V$	—	—	0.5		
Output voltage 3 (P40-P41)	VOL3	When I ² C mode is selected	IOL3 = +3mA	—	—	0.4		
Output leakage current (P20 to P23) (P30 to P36) (P40 to P47) (P50 to P53) (P80 to P85) (P90 to P91) (PC0 to PC7) (PD0 to PD7) (PF0 to PF7)	IOOH	VOH = V_{DD} (in high-impedance state)		—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)		-1	—	—		
Output current 1 COM0 to COM3	IOL1	VL3=3V、VOL=0.3V		15	40	—	μA	3
		VL3=5V、VOL=0.5V		100	200	—		
	IOH1	VL3=3V、VOH=2.7V		—	-30	-15		
		VL3=5V、VOH=4.5V		—	-90	-45		
Output current 2 SEG0 to SEG23 SEG32 to SEG39	IOL2	VL3=3V、VOL=0.3V		15	30	—		
		VL3=5V、VOL=0.5V		70	150	—		
	IOH2	VL3=3V、VOH=2.7V		—	-13	-6		
		VL3=5V、VOH=4.5V		—	-40	-20		
Input current 1 (RESET_N) (TEST1_N)	IIH1	VIH1 = V_{DD}		0	—	1		
	IIL1	VIL1 = V_{SS}		-1500	-300	-20		
Input current 2 (P00 to P03) (P10 to P11) (P30 to P36) (P40 to P47) (P50 to P53) (P80 to P85) (PC0 to PC7) (PD0 to PD7) (PF0 to PF7)	IIH2	VIH2 = V_{DD} (when pulled down)		2	30	250	μA	4
	IIL2	VIL2 = V_{SS} (when pulled up)		-250	-30	-2		
	IIH2Z	VIH2 = V_{DD} (in high-impedance state)		—	—	1		
	IIL2Z	VIL2 = V_{SS} (in high-impedance state)		-1	—	—		
Input current 3 (TEST0)	IIH3	VIH3 = V_{DD}		20	300	1500		
	IIL3	VIL3 = V_{SS}		-1	—	—		

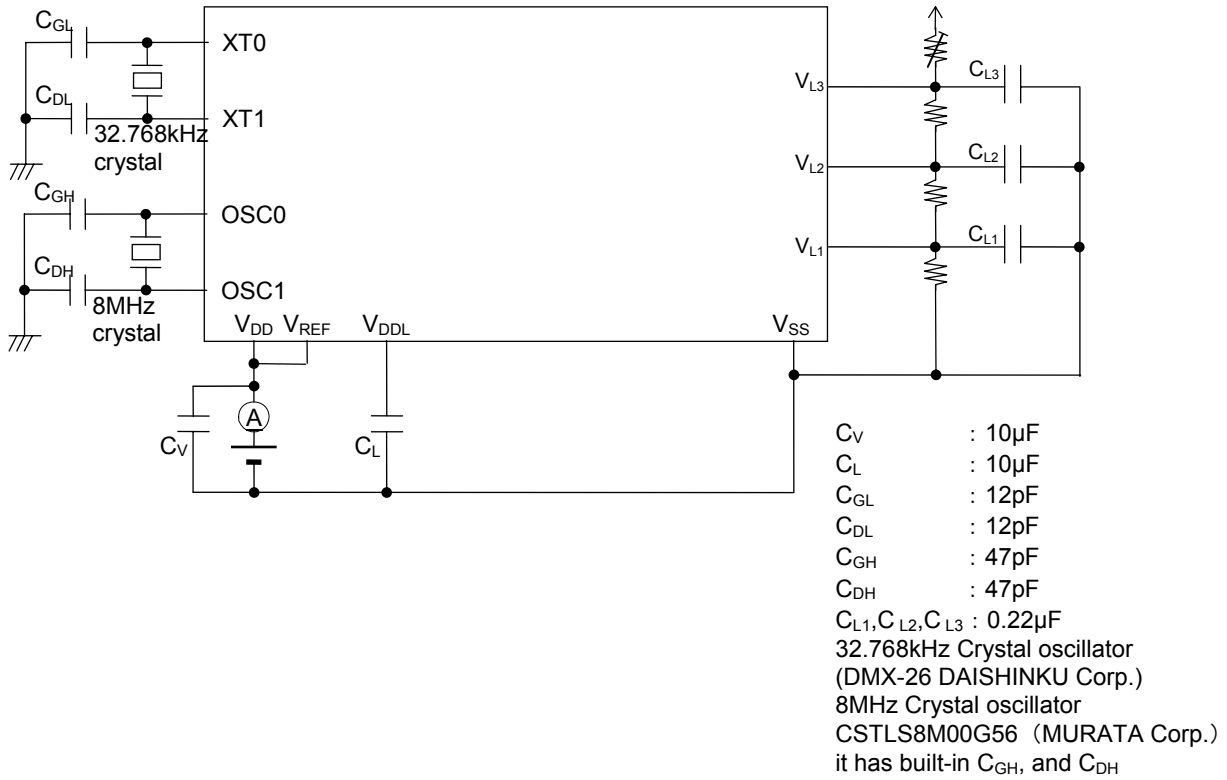
DC Characteristics (7 of 7)

($V_{DD}=2.2$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+85^{\circ}C$, unless otherwise specified)

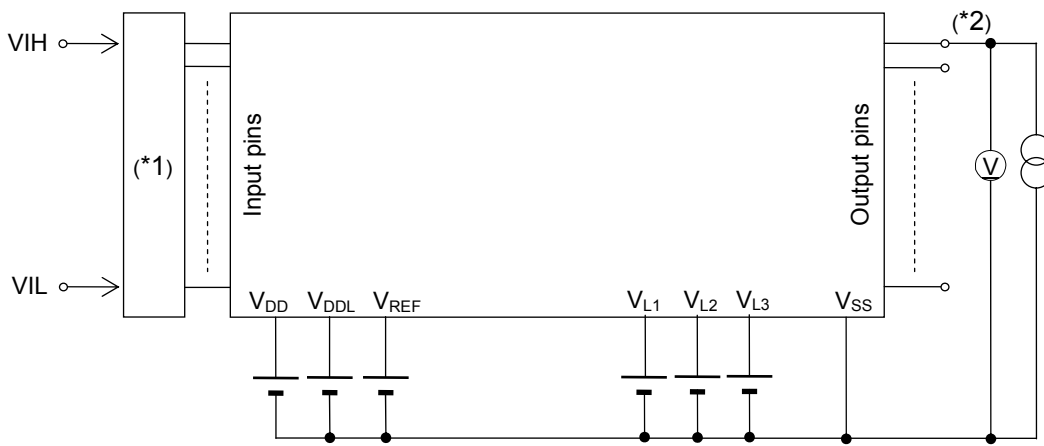
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input voltage 1 (RESET_N) (TEST0) (TEST1_N) (P00 to P03) (P10 to P11) (P30 to P36) (P40 to P47) (P50 to P53) (P80 to P85) (PC0 to PC7) (PD0 to PD7) (PF0 to PF7)	VIH1	—	$0.7 \times V_{DD}$	—	V_{DD}	V	5
	VIL1	—	0	—	$0.3 \times V_{DD}$		
Input pin capacitance (RESET_N) (TEST0) (TEST1_N) (P00 to P03) (P10 to P11) (P30 to P36) (P40 to P47) (P50 to P53) (P80 to P85) (PC0 to PC7) (PD0 to PD7) (PF0 to PF7)	CIN	$f = 10kHz$ $V_{rms} = 50mV$ $T_a = 25^{\circ}C$	—	—	10	pF	—

Measuring Circuits

Measuring circuit 1



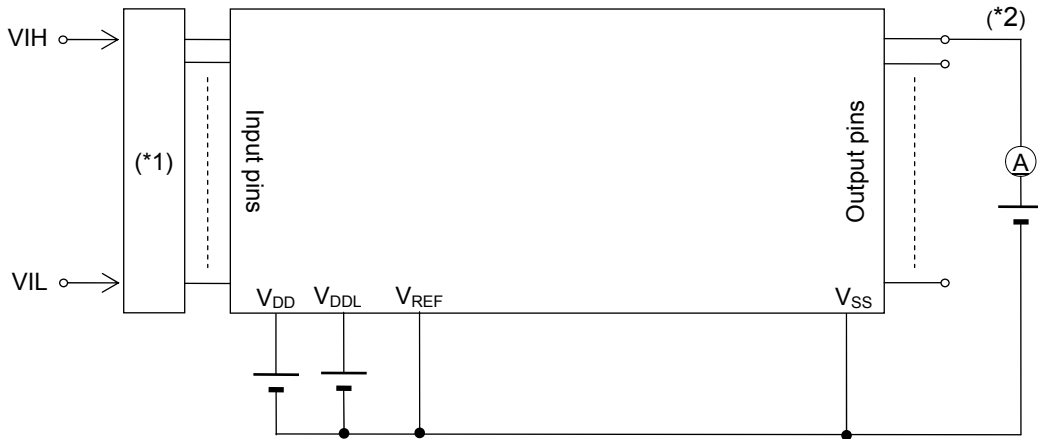
Measuring circuit 2



(*1) Input logic circuit to determine the specified measuring conditions.

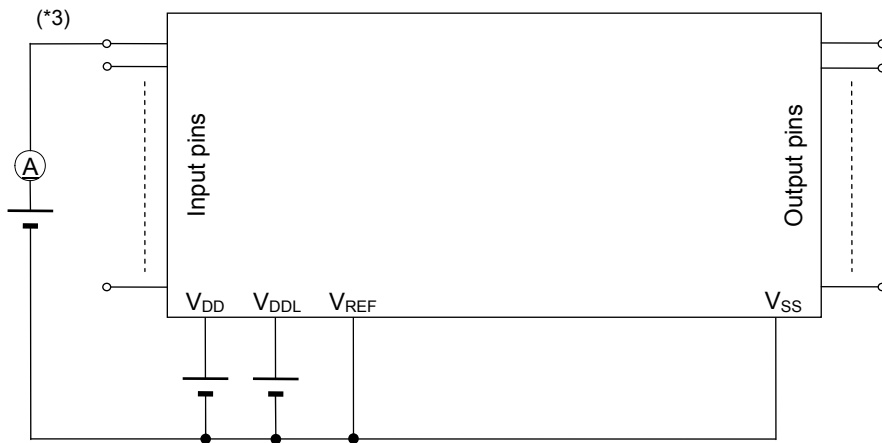
(*2) Measured at the specified output pins.

Measuring circuit 3



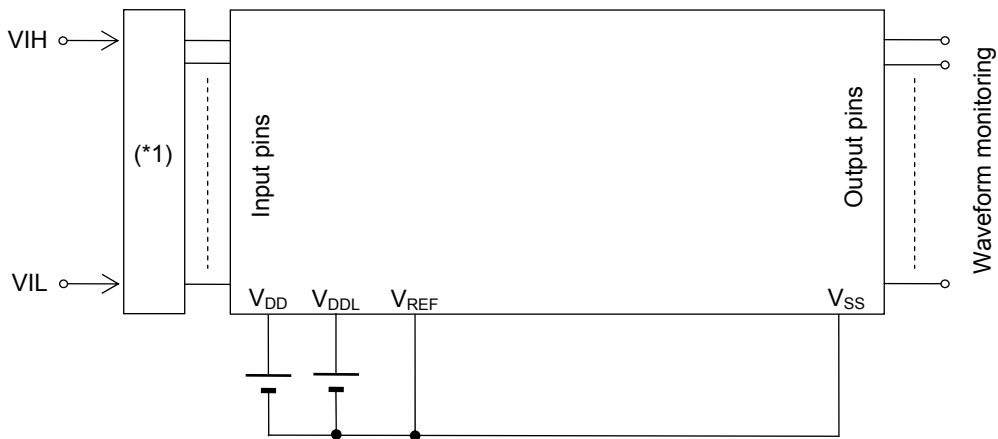
- (*1) Input logic circuit to determine the specified measuring conditions.
- (*2) Measured at the specified output pins.

Measuring circuit 4



- *3: Measured at the specified input pins.

Measuring circuit 5

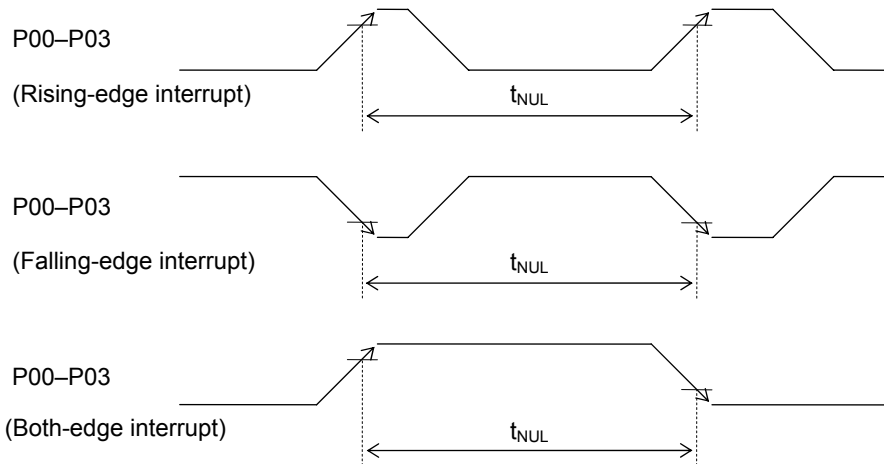


- *1: Input logic circuit to determine the specified measuring conditions.

AC Characteristics (External Interrupt)

($V_{DD}=2.2$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+85^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation	$2.5 \times$ sysclk	—	$3.5 \times$ sysclk	μs

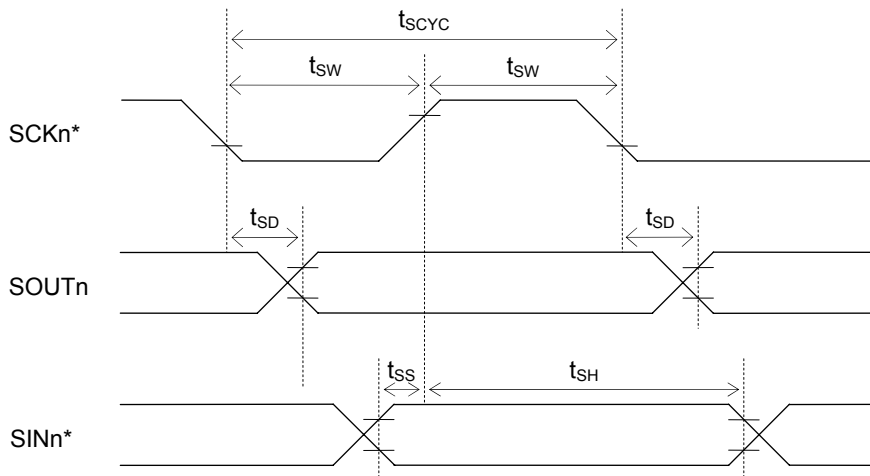


AC Characteristics (Synchronous Serial Port)

($V_{DD}=2.2$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+85^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle (slave mode)	t_{SCYC}	High-speed oscillation stopped	10	—	—	μs
		During high-speed oscillation	500	—	—	ns
SCK output cycle (master mode)	t_{SCYC}	—	—	$SCK^{(*)}$	—	sec
SCK input pulse width (slave mode)	t_{SW}	High-speed oscillation stopped	4	—	—	μs
		During high-speed oscillation	200	—	—	ns
SCK output pulse width (master mode)	t_{SW}	—	$SCK^{(*)} \times 0.4$	$SCK^{(*)} \times 0.5$	$SCK^{(*)} \times 0.6$	sec
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	50	—	—	ns
SIN input hold time	t_{SH}	—	50	—	—	ns

*1: Clock period selected by SnCK3–0 of the serial port n mode register (SIO nMOD1)



*: Indicates the secondary function of the corresponding port.

AC Characteristics (I²C Bus Interface: Standard Mode 100kHz)

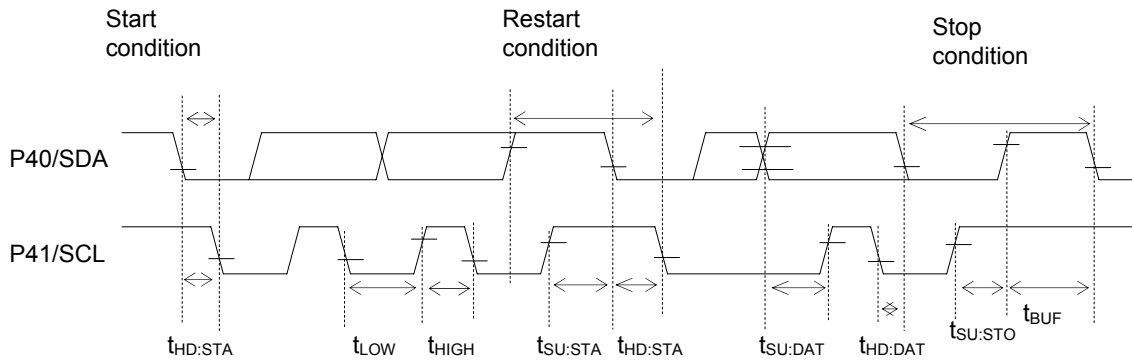
(V_{DD}=2.2 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f _{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	t _{HD:STA}	—	4.0	—	—	μs
SCL "L" level time	t _{LOW}	—	4.7	—	—	μs
SCL "H" level time	t _{HIGH}	—	4.0	—	—	μs
SCL setup time (restart condition)	t _{SU:STA}	—	4.7	—	—	μs
SDA hold time	t _{HD:DAT}	—	0	—	—	μs
SDA setup time	t _{SU:DAT}	—	0.25	—	—	μs
SDA setup time (stop condition)	t _{SU:STO}	—	4.0	—	—	μs
Bus-free time	t _{BUF}	—	4.7	—	—	μs

AC Characteristics (I²C Bus Interface: Fast Mode 400kHz)

(V_{DD}=2.2 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f _{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	t _{HD:STA}	—	0.6	—	—	μs
SCL "L" level time	t _{LOW}	—	1.3	—	—	μs
SCL "H" level time	t _{HIGH}	—	0.6	—	—	μs
SCL setup time (restart condition)	t _{SU:STA}	—	0.6	—	—	μs
SDA hold time	t _{HD:DAT}	—	0	—	—	μs
SDA setup time	t _{SU:DAT}	—	0.1	—	—	μs
SDA setup time (stop condition)	t _{SU:STO}	—	0.6	—	—	μs
Bus-free time	t _{BUF}	—	1.3	—	—	μs

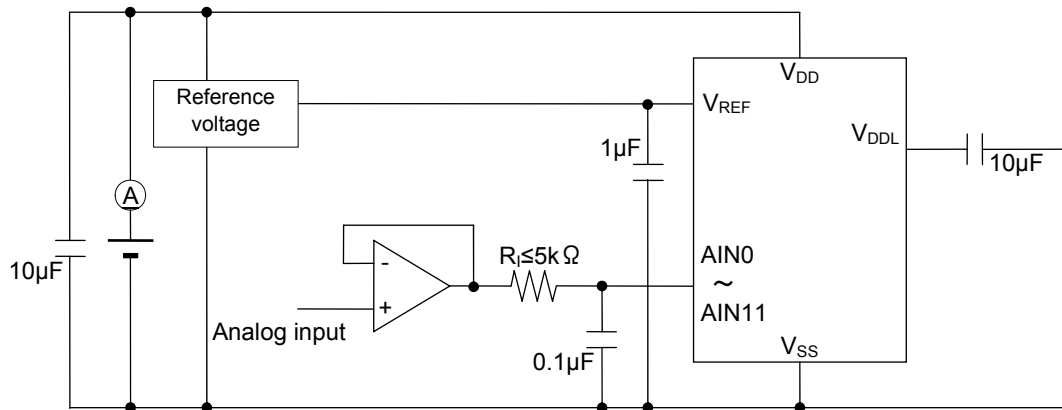


Electrical Characteristics of Successive Approximation Type A/D Converter

($V_{DD}=4.5$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $+85^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	—	—	—	10	bits
Integral non-linearity error	IDL	$2.7V \leq V_{REF} \leq 5.5V$	-4	—	+4	LSB
Differential non-linearity error	DNL	$2.7V \leq V_{REF} \leq 5.5V$	-3	—	+3	
Zero-scale error	V_{OFF}	—	-4	—	+4	
Full-scale error	FSE	—	-4	—	+4	
Input impedance	R_I	—	—	—	5k	Ω
Reference voltage	V_{REF}	—	4.5	—	V_{DD}	V
Conversion time	t_{CONV}	HSCLK=3.0M to 8.4MHz	—	102	—	ϕ/CH

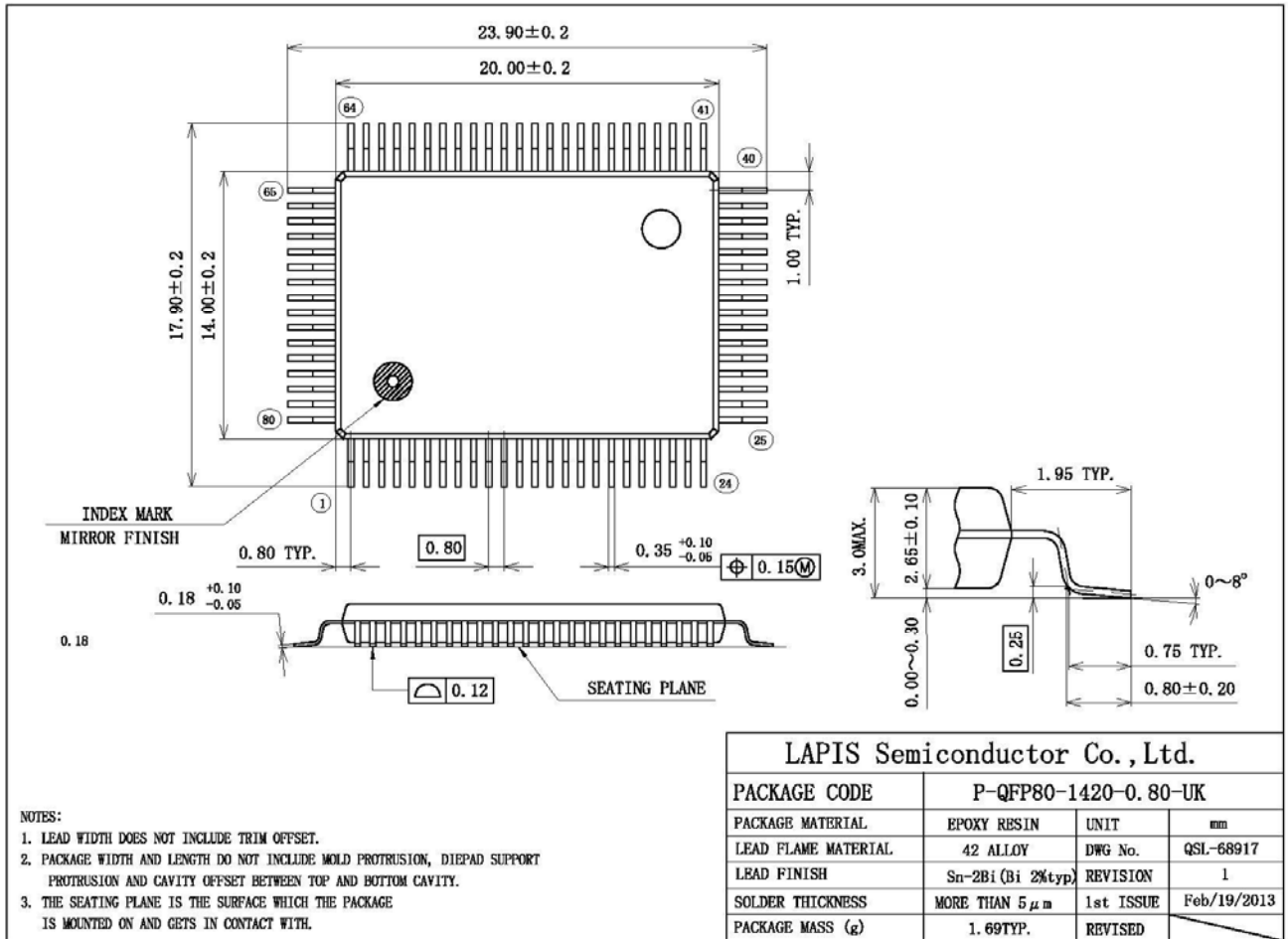
ϕ : Period of high-speed clock (HSCLK)



PACKAGE DIMENSIONS

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact LAPIS SEMICONDUCTOR's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).



REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q174-01	Oct 25, 2013	-	-	Final edition 1

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