Dual Channel 2.5MHz, 2.0A Synchronous Buck with Automatic Power Save

POWER MANAGEMENT

Features

- V_{IN} Range — 2.75 – 5.5V
- V_{OUT} Selectable — 1.0 - 3.3V
- Up to 2A Output Current for Each Channel
- Package with Ultra-Small Footprint : 3 x 3 x 0.6(mm)
- Switching Frequency — 2.5MHz
- Efficiency Up to 94%
- High Light-load Efficiency via Automatic PSAVE Mode
- Low Output Noise in CCM
- Excellent Transient Response
- Start Up into Pre-Biased Output
- 100% Duty-Cycle Low Dropout Operation
- Shutdown Current — <1µA
- Internal Soft-Start
- Input Under-Voltage Lockout
- Output Over-Voltage, Current Limit Protection
- Over-Temperature Protection
- V_{OUT} Further Adjustable Using External Resistors
- PGOOD Feature
- Lead-free, Halogen-free, and RoHS/WEEE Compliant

Applications

- Wireless Access Point/Router/Modem
- Femtocell
- Set-Top Box
- Point-Of-Sale
- Projector

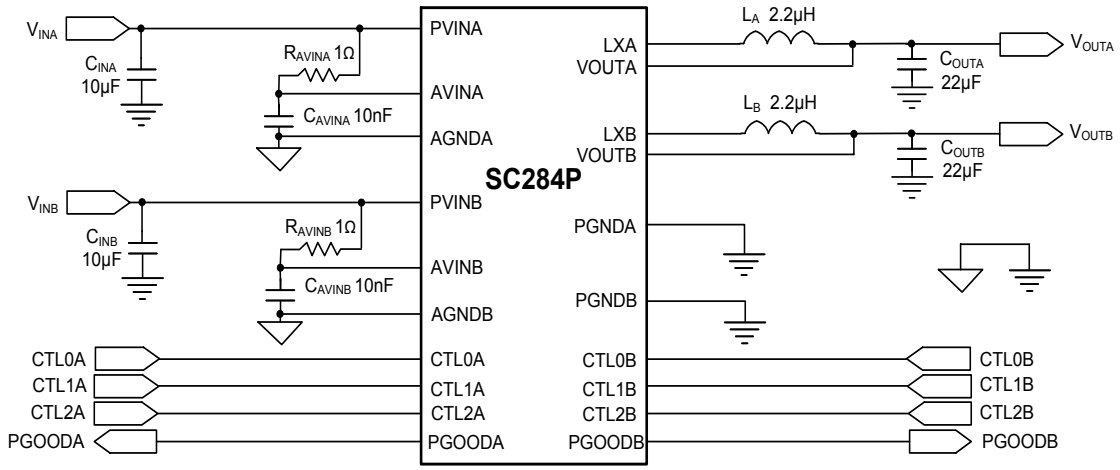
Description

The SC284P is a dual channel 2A synchronous step-down regulator designed to operate with an input voltage range of 2.75 to 5.5 Volts. Each channel offers seven pre-determined output voltages via three control pins programmable from 1.0 to 3.3 Volts. The control pins allow for on-the-fly voltage changes, enabling system designers to implement dynamic power savings. The SC284P is also capable of adjusting the output voltage via an external resistor divider.

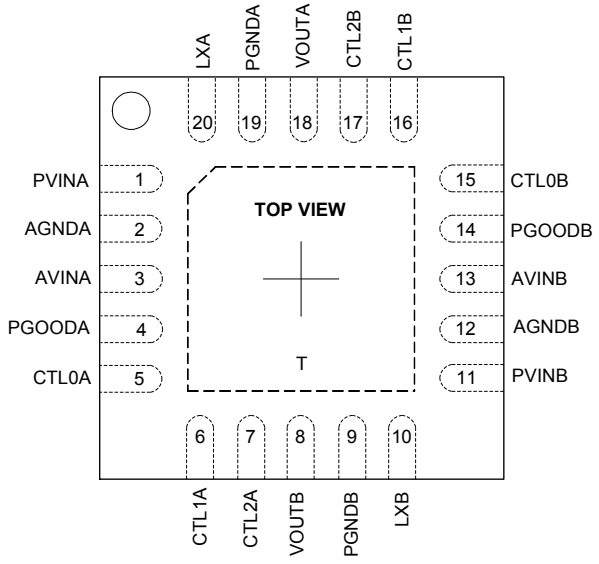
The SC284P is optimized for maximum efficiency over a wide range of load currents. During full load operation, the device operates in PWM mode with fixed 2.5MHz oscillator frequency, allowing the use of small surface mount external components. As the load decreases, the regulator will transition into Power Save mode maintaining high efficiency.

Connecting CTL0 — CTL2 to logic low forces the device into shutdown mode reducing the supply current to less than 1µA. Connecting any of the control pins to logic high enables the converter and sets the output voltage according to Table 1. Other features include under-voltage lockout, soft-start to limit inrush current, and over-temperature protection.

Typical Application Circuit



Pin Configuration



3 x 3 x 0.6(mm) MLPQ-UT20

θ_{JA}= 40°C/W

Ordering Information

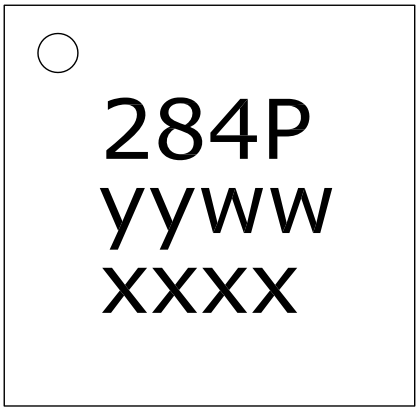
Device	Package
SC284PULTRC[(1)(2)]	3 x 3 x 0.6(mm) MLPQ-UT20
SC284PEVB	Evaluation Board

Notes:

(1) Available in tape and reel only. A reel contains 3,000 devices.

(2) Available in lead-free package only. Device is fully WEEE and RoHS compliant and halogen-free.

Marking Information



284P = Part Number Code

yyww = Date Code

xxxx = Semtech Lot Number

Table 1 – Output Voltage Settings

CTL2[A/B]	CTL1[A/B]	CTL0[A/B]	Output Voltage
0	0	0	Disabled
0	0	1	1.0V
0	1	0	1.1V
0	1	1	1.2V
1	0	0	1.5V
1	0	1	1.8V
1	1	0	2.5V
1	1	1	3.3V

SEMTECH

Absolute Maximum Ratings

AVINA, AVINB, PVINA, PVINB Supply (V) ..... -0.3 to +6.0
LXA and LXB (V) ..... -1 to V_{IN}+1, -3 (20ns Max), 6 Max
VOUTA and VOUTB (V) ..... -0.3 to (V_{IN}+0.3)
CTLXA/B pins (V) ..... -0.3 to (V_{IN} + 0.3)
Peak IR Reflow Temperature (°C) 260
ESD Protection Level[2] (kV) 3kV
Output Short Circuit to GND. ..... Continuous

Recommended Operating Conditions

V_{INA} and V_{INB} Supply (V) ..... 2.75 to 5.5
Maximum Output Current Each Channel (A) 2.0

Thermal Information

Thermal Resistance, Junction to Ambient [1] (°C/W) 40
Maximum Junction Temperature (°C) ..... +150
Storage Temperature Range (°C) ..... -65 to +150

Exceeding the absolute maximum ratings may result in permanent damage to the device and/or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

Notes:
(1) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.
(2) Tested according to JEDEC standard JESD22-A114-B.

Electrical Characteristics

Unless specified: V_{INA}= V_{INB}= 5.0V, V_{OUTA}= V_{OUTB}= 1.5V, C_{INA}= C_{INB}=10µF, C_{OUTA}=C_{OUTB}= 22µF, L= 2.2µH, -40°C ≤ (T_A = T_J)≤ +125 °C. Unless otherwise noted typical values are T_A= +25 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range	$V_{INA/B}$		2.75		5.5	V
Under-Voltage Lockout	UVLO	Rising V_{INA}, V_{INB}	2.55	2.65	2.75	V
		Hysteresis		200		mV
Quiescent Current	I_Q	Channel A & B, PWM mode excluding I_{OUT}, per channel		6		mA
		I_{OUT} = 0mA, CTL_X = V_{IN}		60		µA
Shutdown Current	I_{SHDN}	CTL_{0-2}= GND, Per channel		1	10	µA
Soft-Start Time	t_{SS}	Channel A & B; I_{OUT}= 2A, V_{OUT} =90% of final value		1700		µs
Output Voltage Range	V_{OUT}		1.0		3.3	V
Output Voltage Tolerance[1]	ΔV_{OUT}	Channel A & B; I_{OUT}=400mA, PWM Mode	-2.0		+2.0	%
		PSAVE Mode		1.75		
CTL Settings Regulation	$\Delta V_{CTL-REG}$	Channel A & B; Relative to V_{OUT} at CTL=100, I_{OUTA}=400mA; I_{OUTB}=400mA; PWM Mode		±1		%
Line Regulation	$\Delta V_{LINE-REG}$	Channel A & B; V_{IN}= 2.75 – 5.5V; PWM Mode		±0.2		%/V
Load Regulation	$\Delta V_{LOAD-REG}$	Channel A & B; V_{IN} = 5.0V; I_{OUT}=1mA – 2A		±0.3		%/A

Electrical Characteristics (continued)

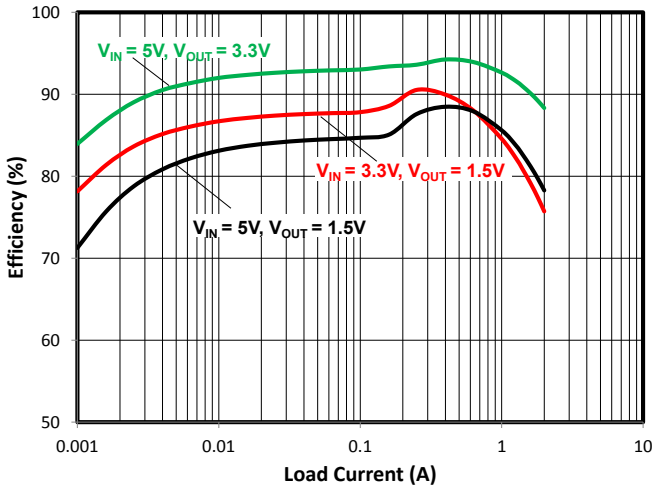
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Current Limit Threshold	I_{LIMIT}	Channel A & B; Peak LX current	2.25	3.0	3.75	A
Oscillator Frequency	f_{OSC}	Channel A & B	2.0	2.5	3.0	MHz
LX Leakage Current(2)	$I_{LK(LX)}$	Channel A & B; V_{IN} = 5.5V; LX = 0V; CTL_{0-2}= GND	-10	-1		µA
		Channel A & B; V_{IN} = 5.5V; LX = 5.0V; CTL_{0-2}= GND		1	10	
Foldback Holding Current	I_{CL_HOLD}	Average LX Current, V_{OUT}=1.5V		600		mA
High Side Switch Resistance(3)	R_{DSON_P}	Channel A & B; I_{LX}= 100mA, T_J= 25 °C		95		mΩ
Low Side Switch Resistance	R_{DSON_N}	Channel A & B; I_{LX}= -100mA, T_J= 25 °C		65		
CTLx Input Current(2)	$I_{CTL\_}$	Channel A & B; CTL_{0-2}=VIN or GND	-2.0		2.0	µA
CTLx Input High Threshold	V_{CTLx_HI}	Channel A & B	1.6			V
CTLx Input Low Threshold	V_{CTLx_LO}	Channel A & B			0.4	V
Impedence of PGOOD Low	R_{PGOOD_LO}			8		Ω
PGOOD Threshold	V_{PG_TH}	VOUT rising		90		%
PGOOD Delay	V_{PG_DLY}	Asserted		2		ms
		PGOOD= Low		20		µs
V_{OUT} Over Voltage Protection	V_{OVP}	Channel A & B		115		%
Thermal Shutdown Temperature(4)	T_{SD}	Channel A & B		160		°C
Thermal Shutdown Hysteresis(4)	T_{SD_HYS}	Channel A & B		10		°C

Notes:
(1) The "Output Voltage Tolerance" includes output voltage accuracy, voltage drift over temperature.
(2) A negative current means the current flows from the pin and a positive current means the current flows into the pin.
(3) Measured from $VIN_{A/B}$ to $LX_{A/B}$.
(4) Thermal shutdown protection is independent for each channel.

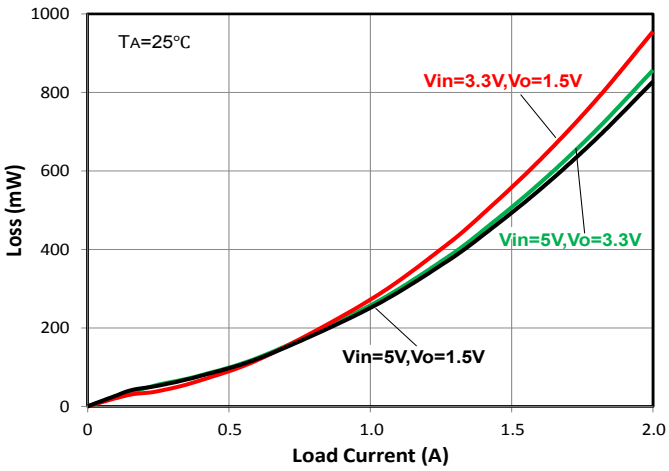
Typical Characteristics

Circuit Conditions: C_{IN}= 10uF/6.3V; C_{OUT}= 22uF/6.3V, Unless otherwise noted, L= 2.2uH (TOKO: 1127AS-2R2M).

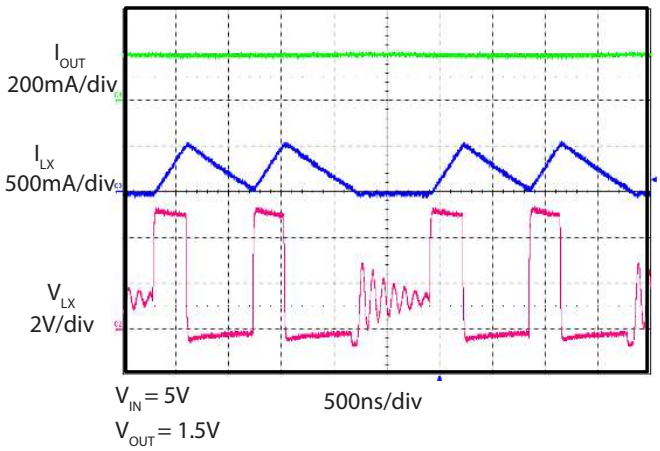
Efficiency vs. Load Current



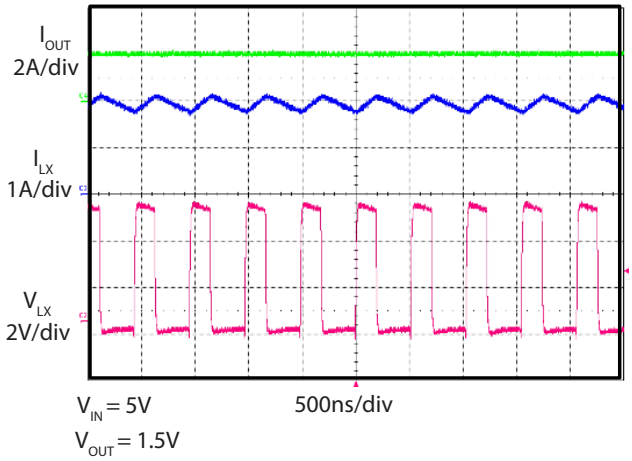
Total Loss (Per Channel) vs. Load Current



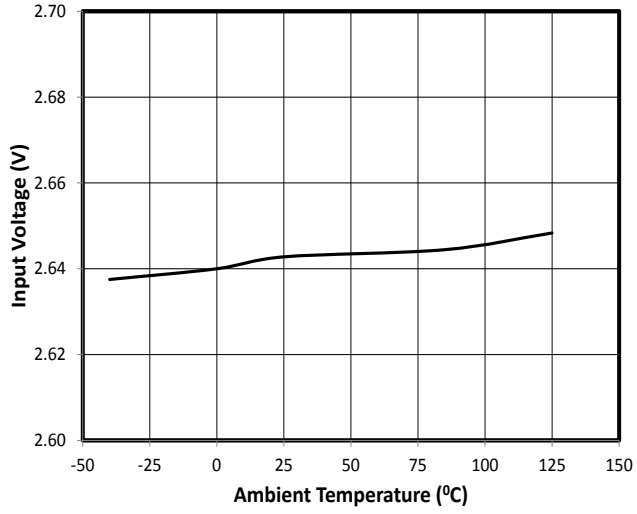
Steady State (PSAVE) Operation (I_{OUT}=200mA)



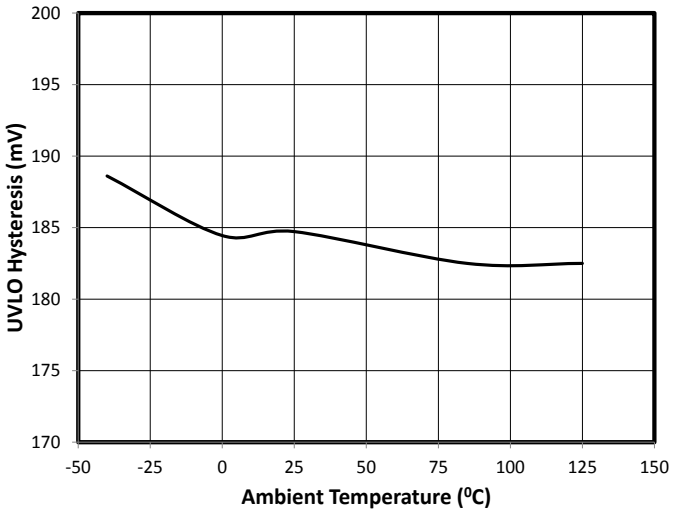
Steady State (PWM) Operation (I_{OUT}=2A)



UVLO Rising Threshold



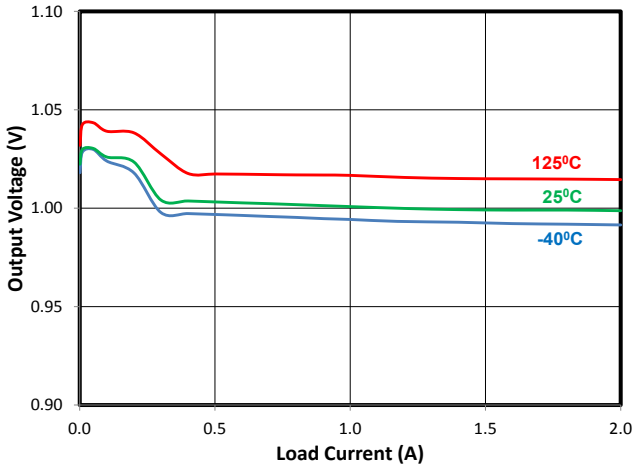
UVLO Hysteresis



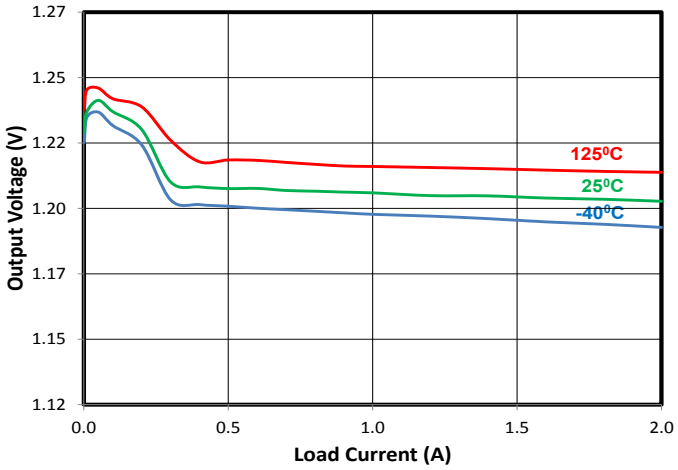
Typical Characteristics

Circuit Conditions: C_{IN}= 10uF/6.3V; C_{OUT}= 22uF/6.3V, Unless otherwise noted, L= 2.2uH (TOKO: 1127AS-2R2M).

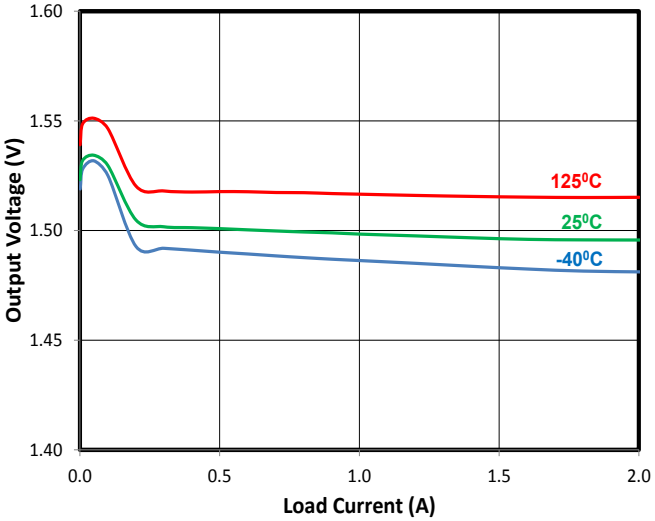
Load Regulation, Vout=1.0V



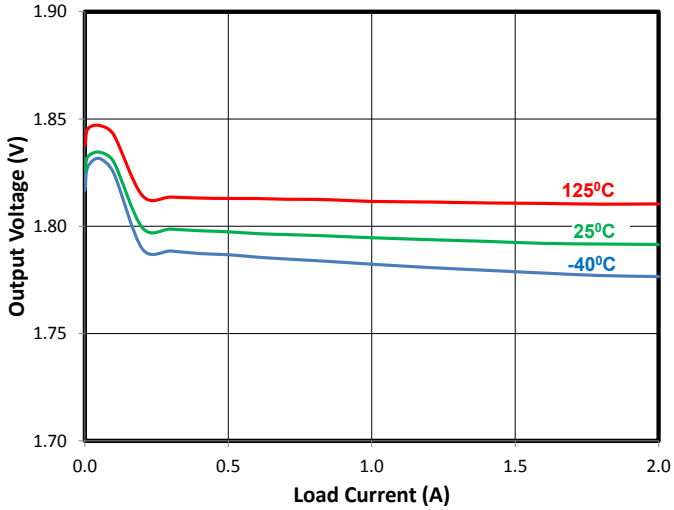
Load Regulation, Vout=1.2V



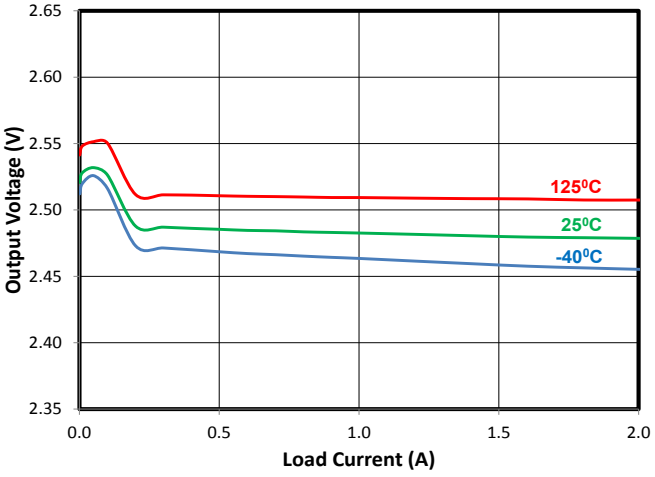
Load Regulation, Vout=1.5V



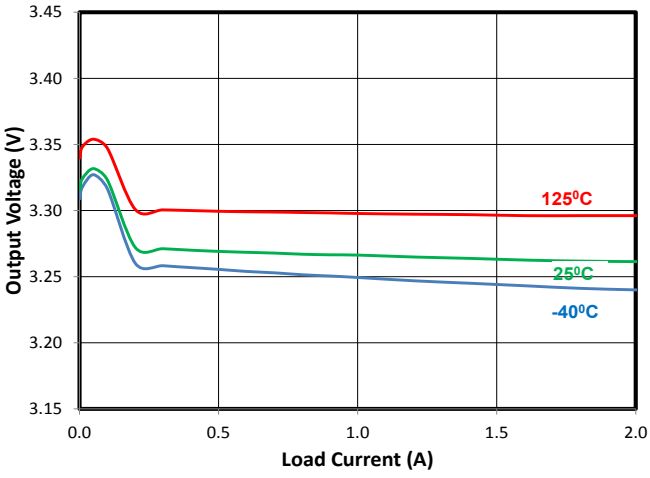
Load Regulation, Vout=1.8V



Load Regulation, Vout=2.5V



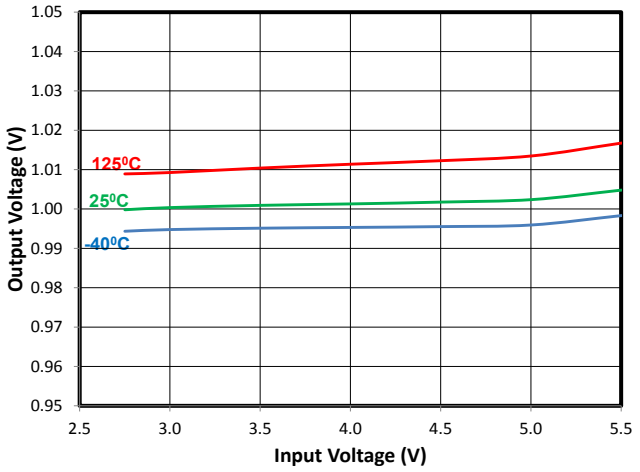
Load Regulation, Vout=3.3V



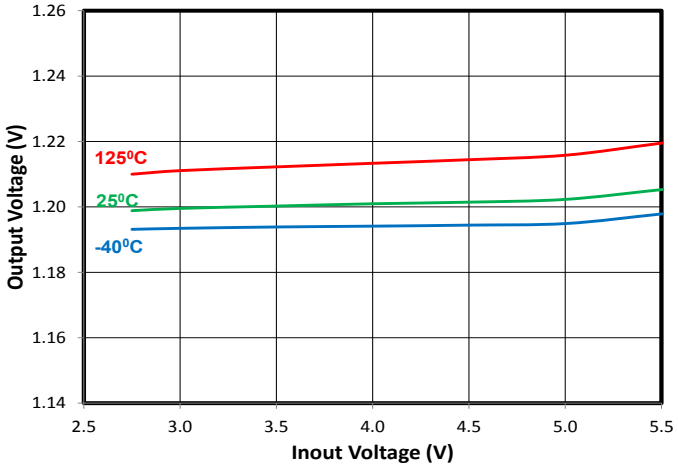
Typical Characteristics

Circuit Conditions: C_{IN}= 10uF/6.3V; C_{OUT}= 22uF/6.3V, Unless otherwise noted, L= 2.2uH (TOKO: 1127AS-2R2M).

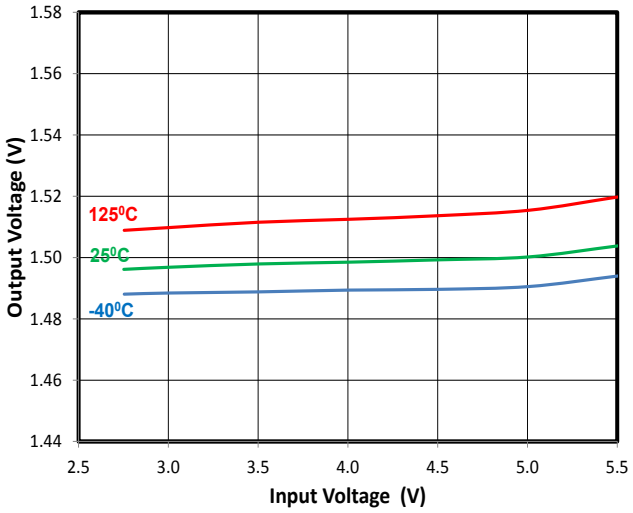
Line Regulation, Vout=1.0V, Iout=500mA



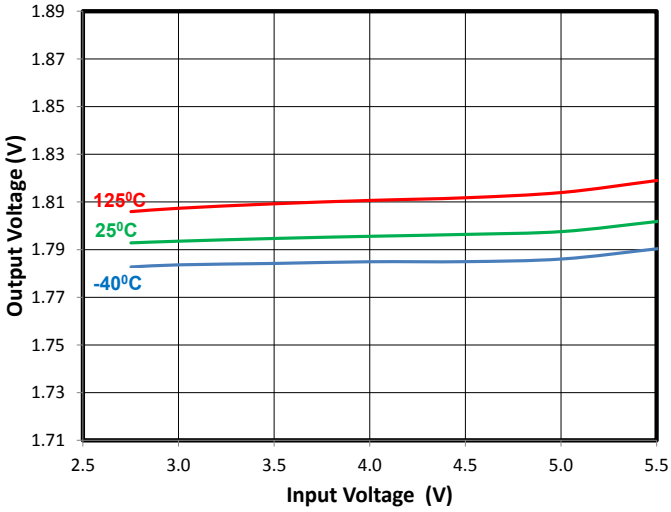
Line Regulation, Vout=1.2V, Iout=500mA



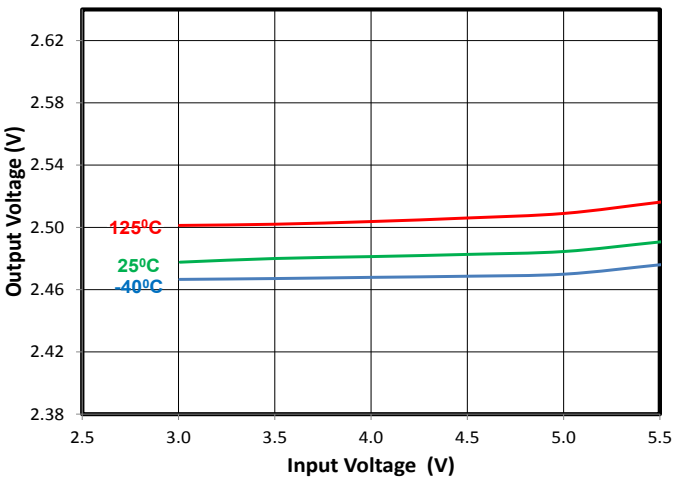
Line Regulation, Vout=1.5V, Iout=500mA



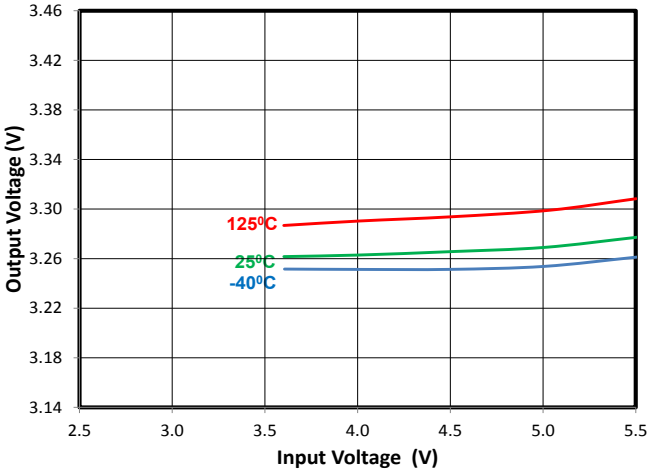
Line Regulation, Vout=1.8V, Iout=500mA



Line Regulation, Vout=2.5V, Iout=500mA



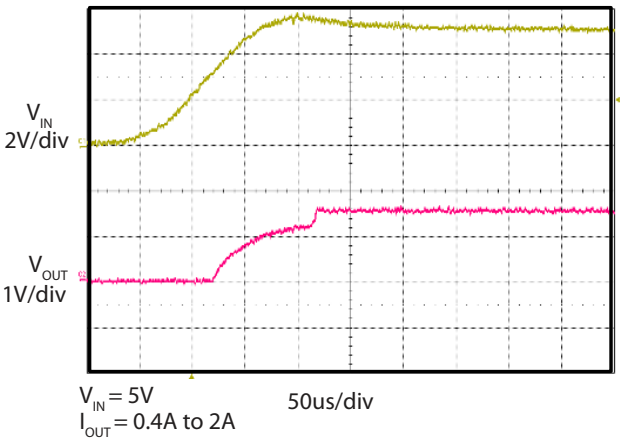
Line Regulation, Vout=3.3V, Iout = 500mA



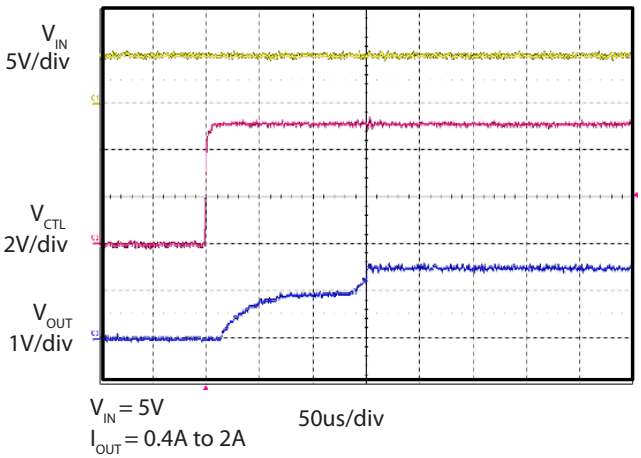
Typical Waveforms

Circuit Conditions: C_{IN}= 10uF/6.3V; C_{OUT}= 22uF/6.3V, L= 2.2uH (TOKO: 1127AS-2R2M).

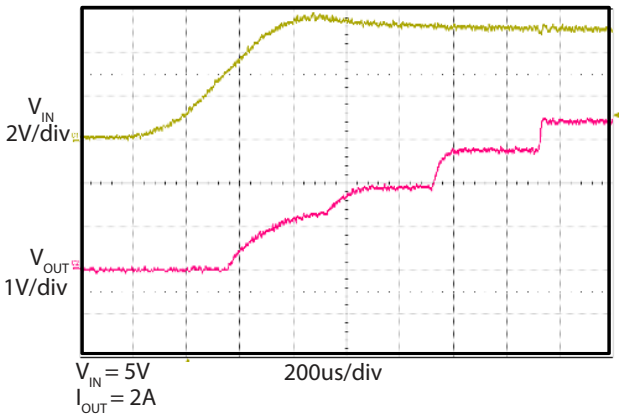
Start Up (Power up V_{IN}=V_{CTLx}) (V_{OUT}=1.5V)



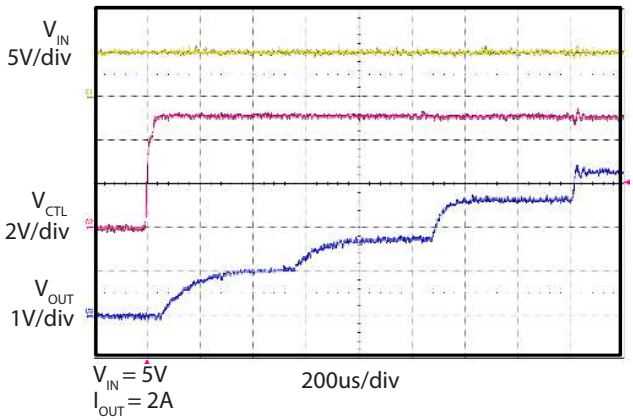
Start Up (Enable) (V_{OUT}=1.5V)



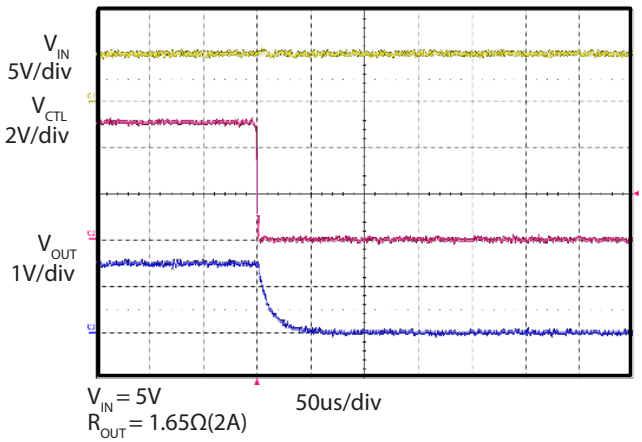
Start Up (Power up V_{IN}=V_{CTLx}) (V_{OUT}=3.3V)



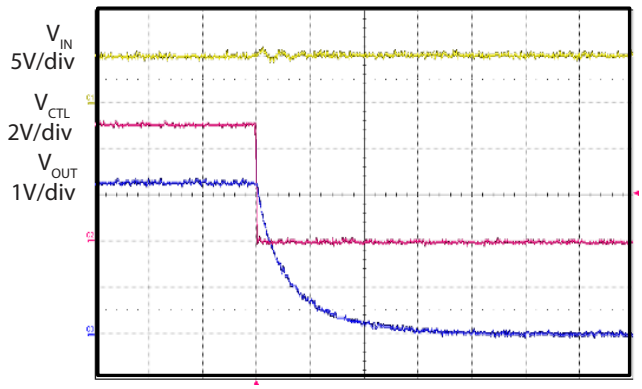
Start Up (Enable) (V_{OUT}=3.3V)



Shutdown (Disable)(V_{OUT}=1.5V)



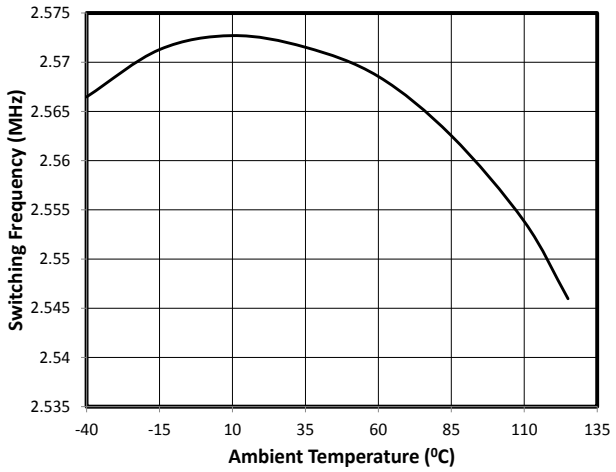
Shutdown (Disable)(V_{OUT}=3.3V)



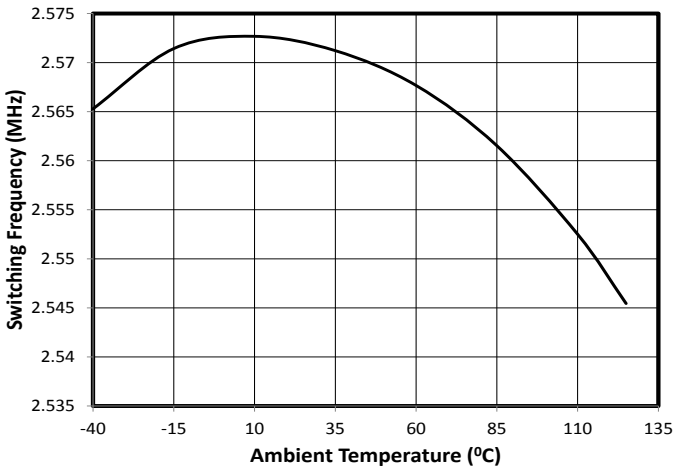
Typical Characteristics

Circuit Conditions: C_{IN}= 10uF/6.3V; C_{OUT}= 22uF/6.3V, Unless otherwise noted, L= 2.2uH (TOKO: 1127AS-2R2M).

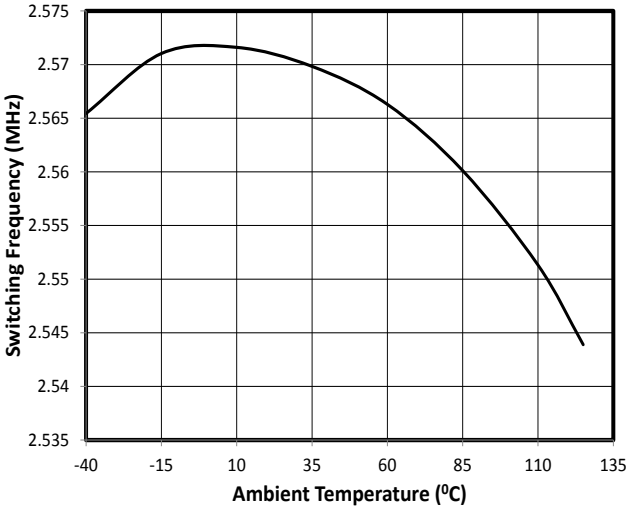
Switching Frequency Vs Temperature, Vout=1.0V



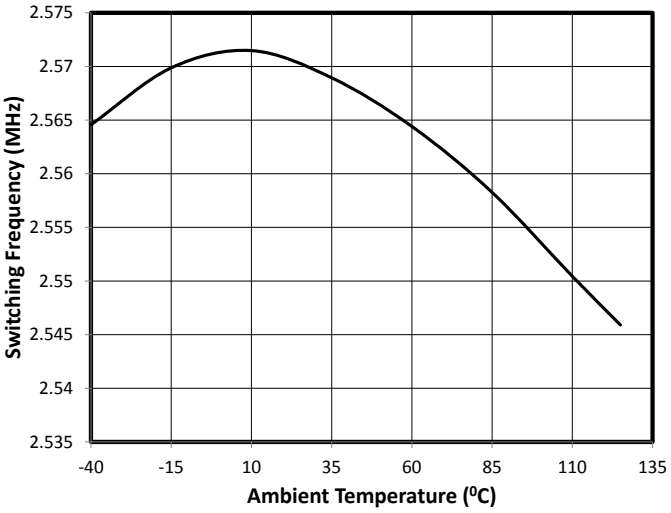
Switching Frequency Vs Temperature, Vout=1.2V



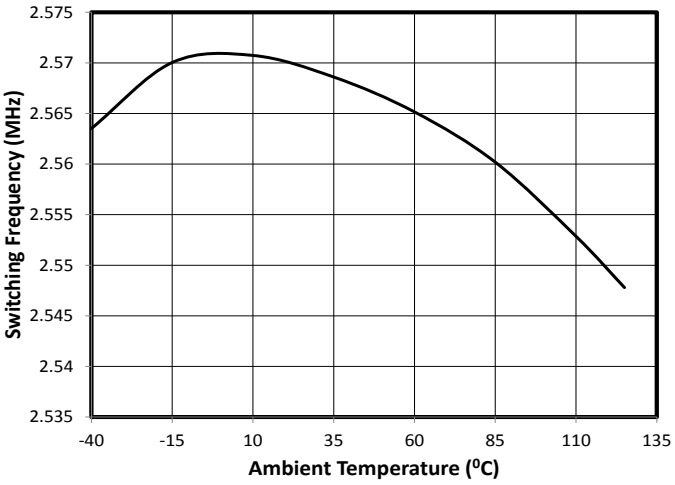
Switching Frequency Vs Temperature, Vout=1.5V



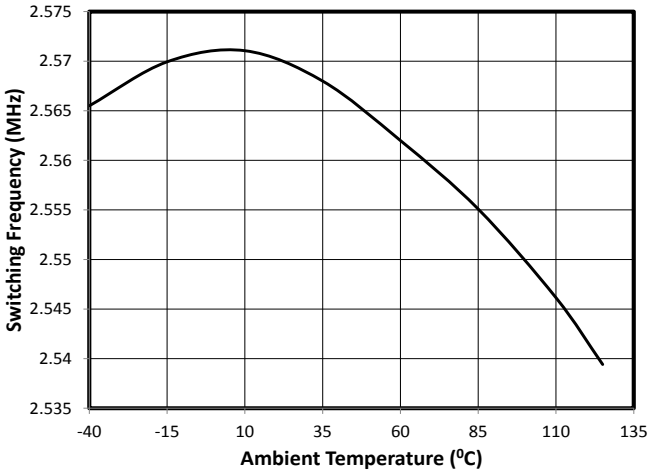
Switching Frequency Vs Temperature, Vout=1.8V



Switching Frequency Vs Temperature, Vout=2.5V



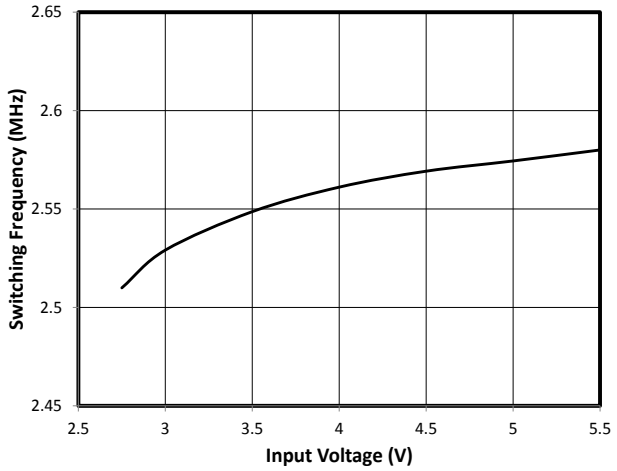
Switching Frequency vs Temperature, Vout=3.3V



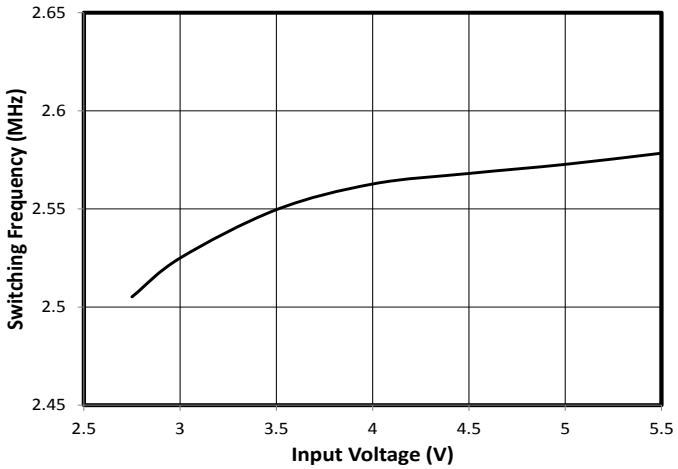
Typical Characteristics

Circuit Conditions: C_{IN}= 10uF/6.3V; C_{OUT}= 22uF/6.3V, Unless otherwise noted, L= 2.2uH (TOKO: 1127AS-2R2M).

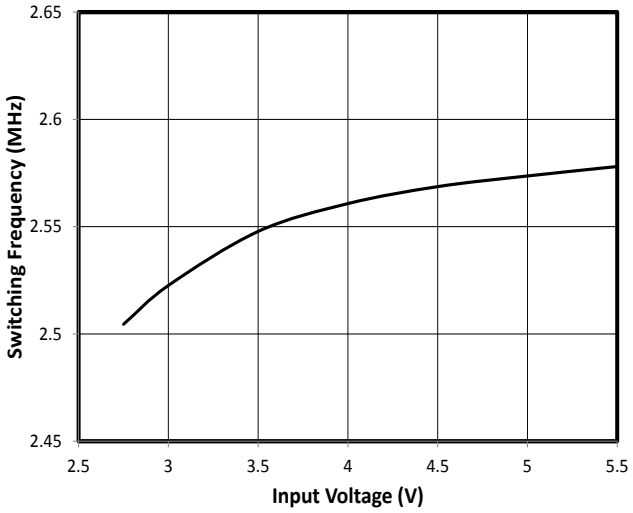
Switching Frequency Vs Input Voltage, Vout=1.0V



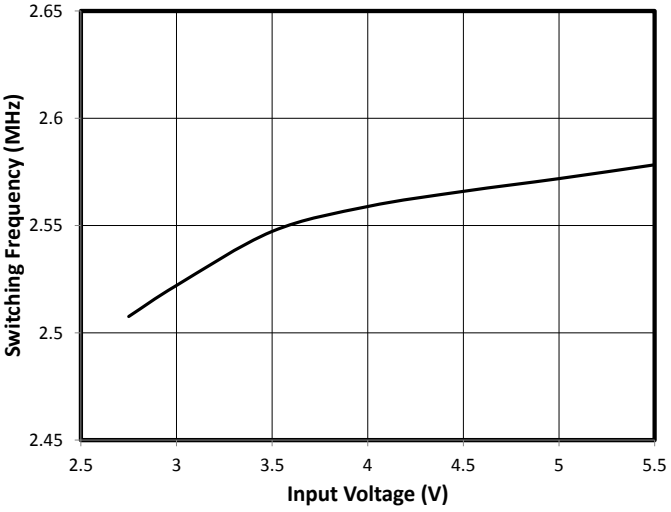
Switching Frequency Vs Input Voltage, Vout=1.2V



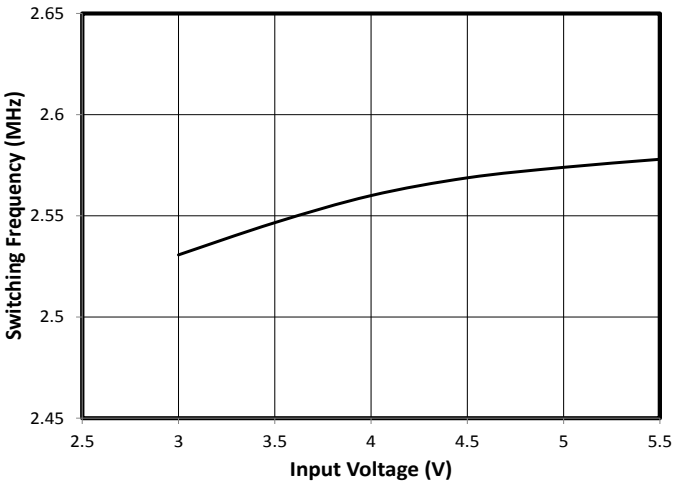
Switching Frequency Vs Input Voltage, Vout=1.5V



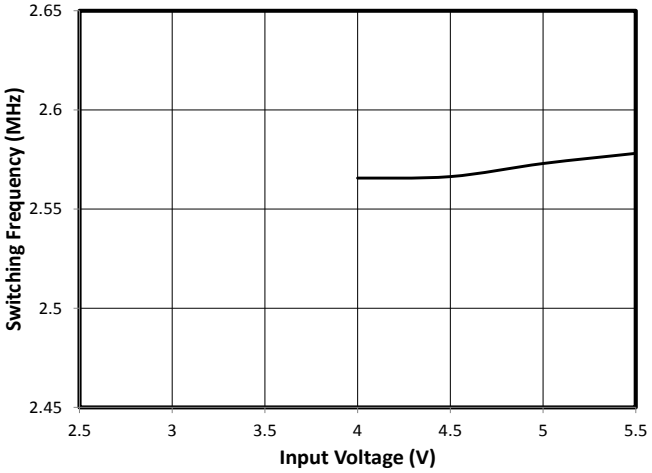
Switching Frequency Vs Input Voltage, Vout=1.8V



Switching Frequency Vs Input Voltage, Vout=2.5V



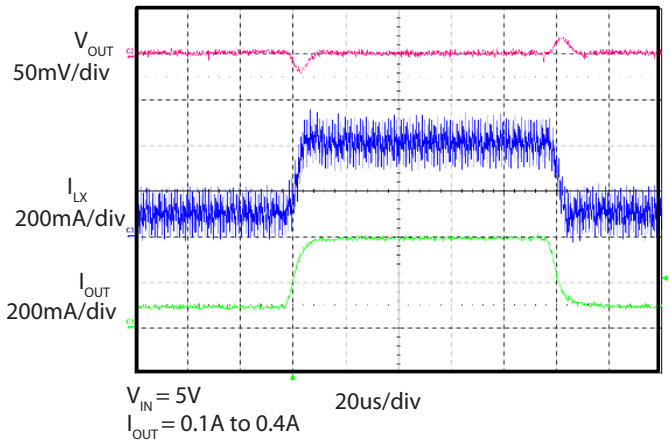
Switching Frequency vs Input Voltage, Vout=3.3V



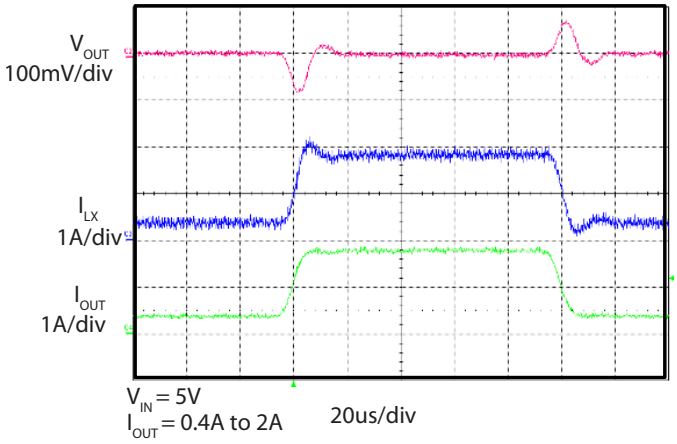
Typical Waveforms

Circuit Conditions: C_{IN}= 10uF/6.3V; C_{OUT}= 22uF/6.3V, L= 2.2uH (TOKO: 1127AS-2R2M).

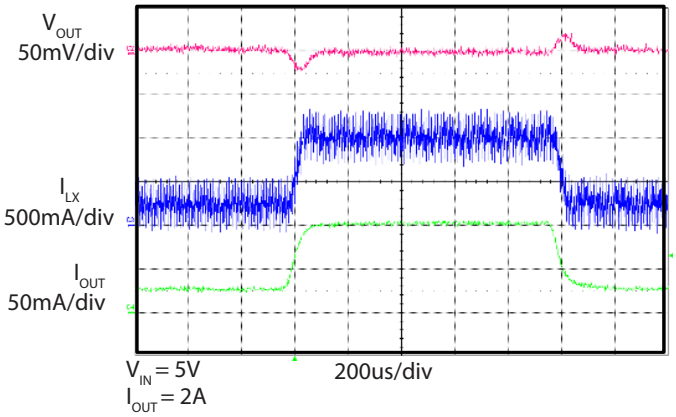
Transient Response (Vout=1.5V, Iout=0.1A to 0.4A)



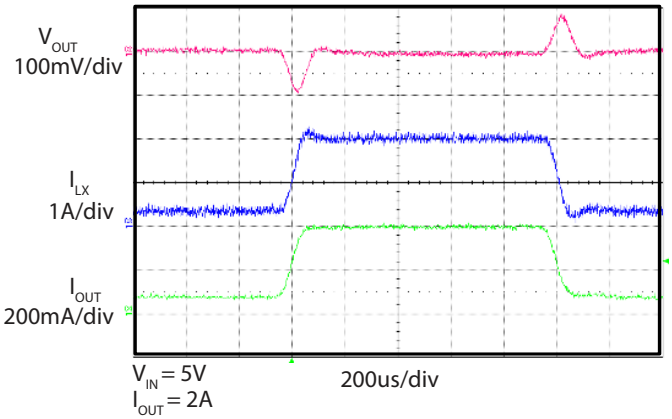
Transient Response (Vout=1.5V, Iout=0.4A to 2A)



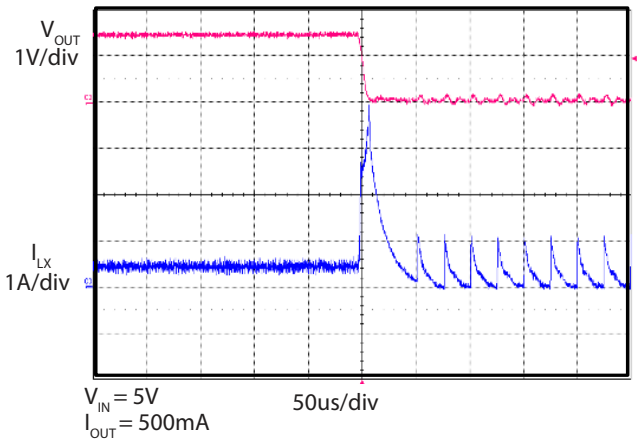
Transient Response (Vout=1.5V, Iout=0.01A to 0.1A)



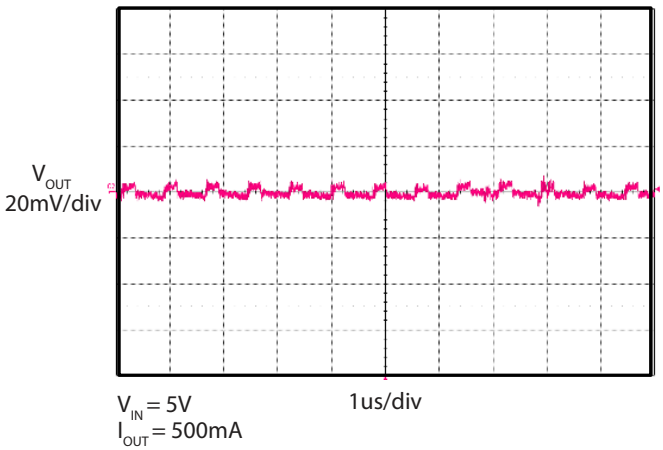
Transient Response (Vout=3.3V, Iout=0.4A to 2A)



Output Hard Short (V_{OUT}=1.5V)



Output Voltage Ripple (V_{OUT}=1.5V)

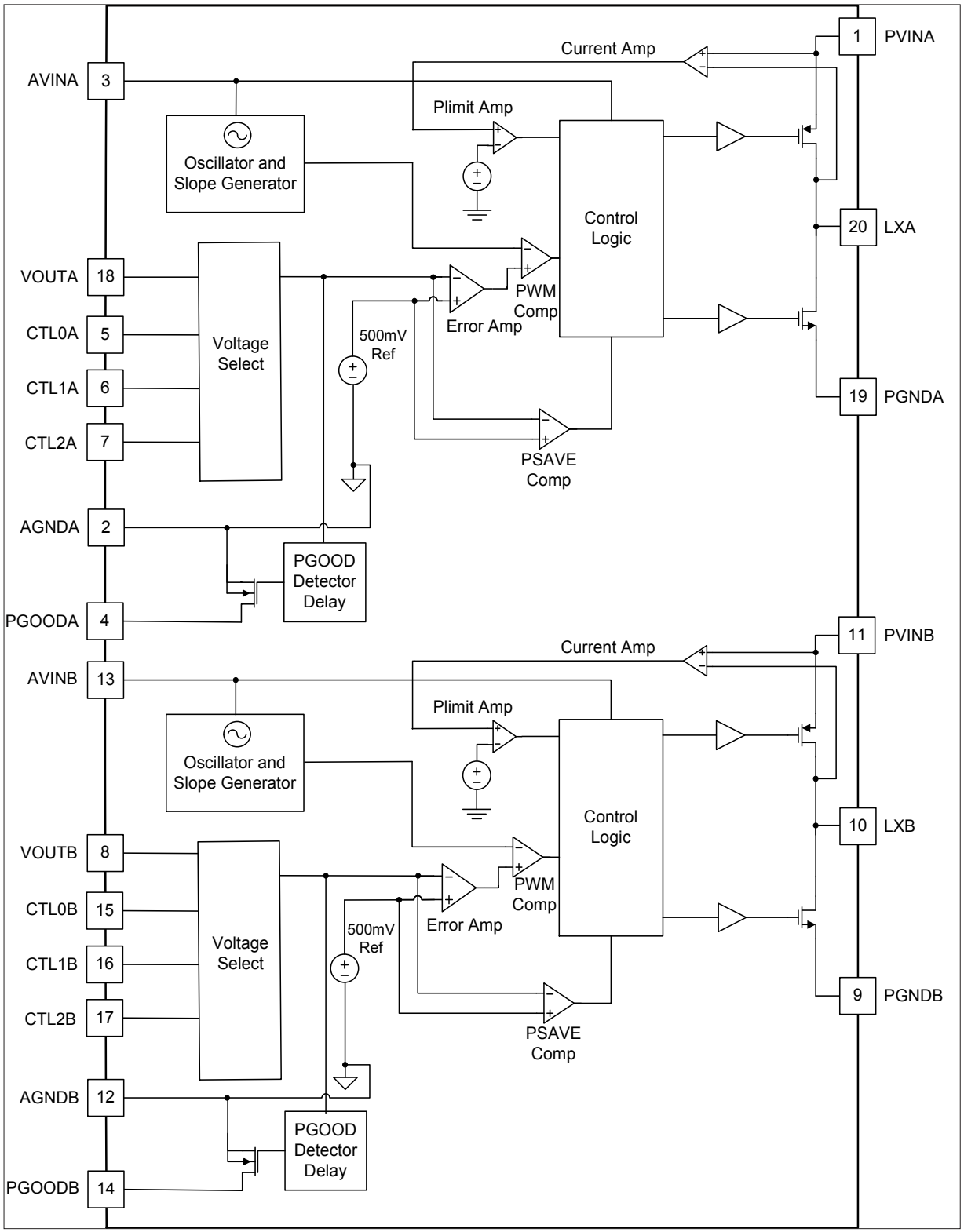


SEMTECH

Pin Descriptions

Pin #	Pin Name	Pin Function
1	PVINA	Channel A — Input supply voltage for the converter power stage and internal circuitry.
2	AGNDA	Ground connection for internal circuitry — connect directly to PGNDA.
3	AVINA	Power supply for internal circuitry — must be connected to PVINA using an R-C filter of 1Ω and 10nF.
4	PGOODA	Power Good indicator for channel A. When the output voltage reaches the PGOODA threshold, this pin will be open drain (after the PGOOD delay), otherwise it is pulled low internally.
5	CTL0A	Channel A — Control bit 0, see Table 1 for decoding. This pin has a 1 MΩ internal pull-down resistor. This resistor is switched in circuit whenever the pin voltage is below the input high threshold, or when the part is in under-voltage lockout.
6	CTL1A	Channel A — Control bit 1, see Table 1 for decoding. This pin has a 1 MΩ internal pull-down resistor. This resistor is switched in circuit whenever the pin voltage is below the input high threshold, or when the part is in under-voltage lockout.
7	CTL2A	Channel A — Control bit 2, see Table 1 for decoding. This pin has a 1 MΩ internal pull-down resistor. This resistor is switched in circuit whenever the pin voltage is below the input high threshold, or when the part is in under-voltage lockout.
8	VOUTB	Output voltage sense pin of Channel B
9	PGNDB	Channel B — Ground connection for converter power stage and internal circuitry.
10	LXB	Switching node of Channel B — connect an inductor between this pin and the output capacitor.
11	PVINB	Channel B — Input supply voltage for the converter power stage and internal circuitry.
12	AGNDB	Ground connection for internal circuitry — connect directly to PGNDB.
13	AVINB	Power supply for internal circuitry — must be connected to PVINB using an R-C filter of 1Ω and 10nF.
14	PGOODB	Power Good indicator for channel B. When the output voltage reaches the PGOODB threshold, this pin will be open drain (after the PGOOD delay), otherwise it is pulled low internally.
15	CTL0B	Channel B — Control bit 0, see Table 1 for decoding. This pin has a 1 MΩ internal pulld-own resistor. This resistor is switched in circuit whenever the pin voltage is below the input high threshold, or when the part is in under-voltage lockout.
16	CTL1B	Channel B — Control bit 1 - see Table 1 for decoding. This pin has a 1 MΩ internal pull-down resistor. This resistor is switched in circuit whenever the pin voltage is below the input high threshold, or when the part is in under-voltage lockout.
17	CTL2B	Channel B — Control bit 2, see Table 1 for decoding. This pin has a 1 MΩ internal pull-down resistor. This resistor is switched in circuit whenever the pin voltage is below the input high threshold, or when the part is in under-voltage lockout.
18	VOUTA	Output voltage sense pin of Channel A
19	PGNDA	Channel A — Ground connection for converter power stage and internal circuitry.
20	LXA	Switching node of Channel A — connect an inductor between this pin and the output capacitor.
	PAD	Thermal pad for heatsinking purposes.

Block Diagram



Applications Information

Detailed Description

The SC284P is a two channel synchronous step-down converter. Both channels of this device are designed to operate at a fixed-frequency of 2.5MHz in CCM and provide the same current capacity of up to 2A. The switching frequency is chosen to minimize the size of the external inductor and capacitors while maintaining high efficiency. Both channels of SC284P are independent.

Operation

During normal operation, the PMOS FET is activated on each rising edge of the internal oscillator. The voltage feedback loop uses an internal feedback resistor divider. The period is set by the internal oscillator. The device has an internal synchronous NMOS rectifier and does not require a Schottky diode on the LX pin.

Programmable Output Voltage

Both channels on SC284P have seven pre-determined output voltage values which can be individually selected by programming the CTL input pins (see Table 1 — Output Voltage Settings). Each CTL pin has an active 1 MΩ internal pull-down resistor. The 1MΩ resistor is switched in circuit whenever the CTL input voltage is below the input threshold, or when the part is in under-voltage lockout. It is recommended to tie all high CTL pins together and use an external pull-up resistor to V_{IN} if there is no enable signal, or if the enable input is an open drain/collector signal. The CTL pins may be driven by a microprocessor to allow dynamic voltage adjustment for systems that reduce the supply voltage when entering sleep states. Avoid all zeros being present on the CTL pins when changing programmable output voltages as this would momentarily disable the device.

SC284P is also capable of regulating a different (higher) output voltage, which is not shown in the Table 1, via an external resistor divider. There will be a typical 2µA current flowing into the V_{OUT} pin. The typical schematic for an adjustable output voltage option from the standard 1.0V with CTL_X=[001], is shown in Figure 1. $R_{FB1A/B}$ and $R_{FB2A/B}$ are used to adjust the desired output voltage. If the $R_{FB2A/B}$ current is such that the 2µA V_{OUT} pin current can be ignored, then $R_{FB1A/B}$ can be found by the next equation. $R_{FB2A/B}$ need to be low enough in value for the current through the resistor chain to be at least 20µA in order to ignore the V_{OUT} pin current.

$$R_{FB1} = \frac{V_{OUT} - V_{OSTD}}{V_{OSTD}} \times R_{FB2}$$

where V_{OSTD} is the pre-determined output voltage via the CTL pins.

C_{FF} is needed to maintain good transient response performance. The correct value of C_{FF} can be found using the following equation.

$$C_{FF}[nF] = 2.5 \times \frac{(V_{OUT} - 0.5)^2}{R_{FB1}[k\Omega] \times (V_{OUT} - V_{OSTD})} \times \left(\frac{V_{OSTD}}{V_{OSTD} - 0.5}\right)$$

To simplify the design, it is recommended to program the desired output voltage from a standard 1.0V as shown in Figure 1 with the correct C_{FF} calculated from Equation 2. For programming the output voltage from other standard voltages, R_{FB1}, R_{FB2} and C_{FF} need to be adjusted to meet Equations 1 and 2.

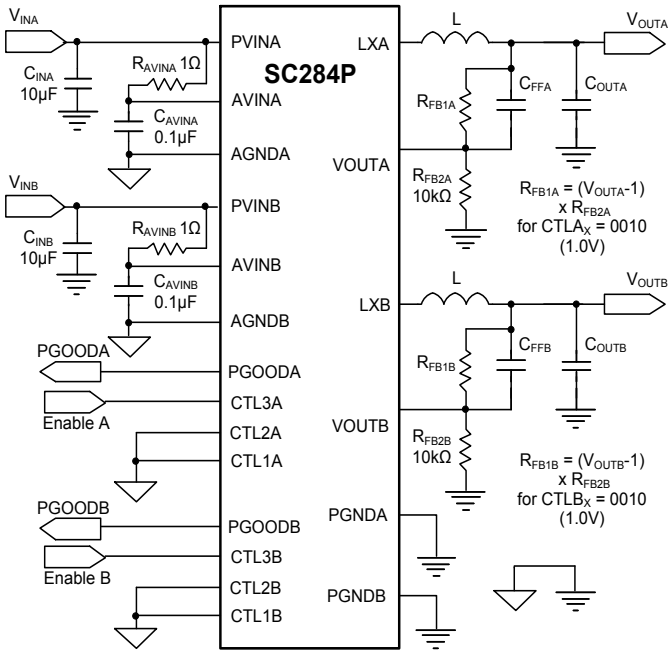


Figure 1 — Output Voltage Programming

Applications Information (continued)

Power Save Mode Operation

When the load current decreases below the PSAVE threshold, PWM switching stops and the device automatically enters PSAVE mode. This threshold varies depending upon the input voltage and the output voltage setting, optimizing efficiency for all possible load currents in PWM or PSAVE mode.

While in PSAVE mode, output voltage regulation is controlled by a series of switching bursts. During a burst, the inductor current is limited to a peak value which controls the on-time of the PMOS switch. After reaching this peak, the PMOS switch is disabled and the inductor current decreases to near 0mA. Switching bursts continue until the output voltage climbs to VOUT +2.5% or until the PSAVE current limit is reached. Switching is then stopped to eliminate switching losses, enhancing overall efficiency. Switching resumes when the output voltage reaches the lower threshold of VOUT and continues until the upper threshold again is reached.

Note that the output voltage is regulated hysteretically while in PSAVE mode between VOUT and VOUT + 2.5%. The period and duty cycle while in PSAVE mode are solely determined by VIN and VOUT until PWM mode resumes. This can result in the switching frequency being much lower than the PWM mode frequency. If the output load current increases enough to cause VOUT to decrease below the PSAVE exit threshold (VOUT-4%), the device automatically exits PSAVE and operates in continuous PWM mode. Note that the PSAVE high and low threshold levels are both set at or above VOUT to minimize undershoot when the SC284P exits PSAVE mode and returns to PWM mode.

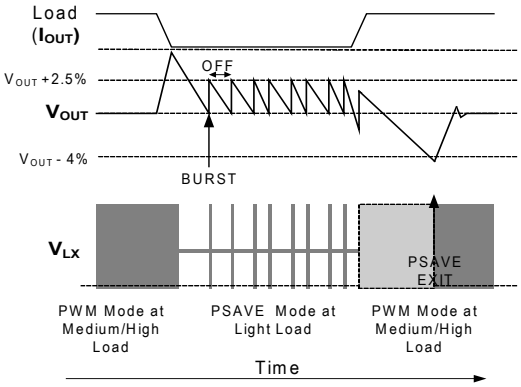


Figure 2 - Transitions Between PWM and PSAVE Modes

Power Good

PGOOD is an open-drain output. When the output voltage drops below nominal voltage, the PGOOD pin is pulled low after a 20µs delay. During start-up, PGOOD will be asserted 1.7ms (typ.) after the output voltage reaches 90% of the final regulation voltage. Over voltage, fold-back current limit and thermal shutdown will force PGOOD low after a 20µs delay. When recovering from a fault, PGOOD will be asserted 1.7ms (typ.) after Vout reaches 90% of the final regulation voltage.

Maximum Power Dissipation

Each channel of SC284P has its own Θ_{JA} of 40°C/W when only one channel is in operation. Since both channels are within the same package, please make sure to use both channels for power calculations. To guarantee an operating junction temperature of less than 125°C, Figure 3 shows the maximum allowable power loss for each channel. The curve is based upon the junction temperature of either channel reaching a maximum of 125°C. Each channel of SC284P can support up to 2A load current.

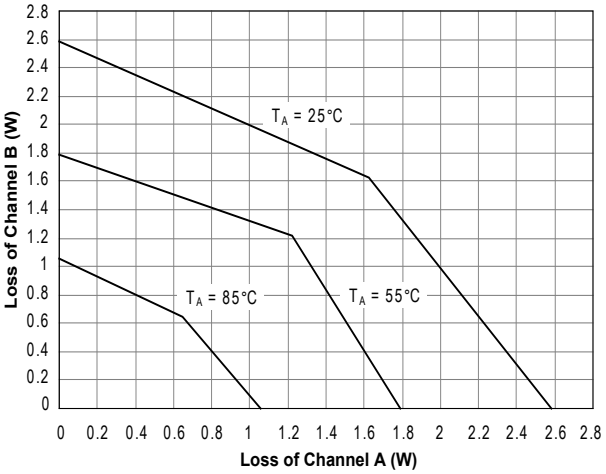


Figure 3 — Maximum allowable loss for each channel for a maximum junction temperature of 125°C

Applications Information (continued)

Protection Features

The SC284P provides the following protection features:

- Current Limit
- Over-Voltage Protection
- Soft-Start
- Thermal Shutdown

Current Limit

The internal PMOS power device in the switching stage is protected by a current limit feature. If the inductor current is above the PMOS current limit for 16 consecutive cycles, the part enters foldback current limit mode and the output current is limited to the current limit holding current (I_{CL_HOLD}) of a few hundred milliampere. Under this condition, the output voltage will be the product of I_{CL_HOLD} and the load resistance. The current limit holding current will decrease when the output voltage increases. The load presented must fall below the current limit holding current for the part to exit foldback current limit mode. Figure 4 shows how the typical current limit holding current varies with output voltage. The SC284P is capable of sustaining an indefinite short circuit without damage and will resume normal operation when the fault is removed. The foldback current limit mode is disabled during soft-start.

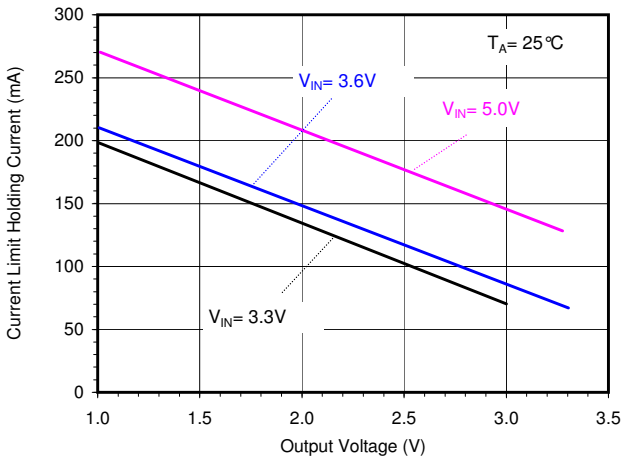


Figure 4— Typical Current Limit Holding Current vs. Output Voltage

Over-Voltage Protection

In the event of a 15% over-voltage on the output, the PWM drive is disabled leaving the LX pin floating.

Soft-Start

Soft-start is activated once VIN reaches the UVLO and one or more CTL pins are set high to enable the part. A thermal shutdown event will also activate the soft-start sequence. Soft-start controls the maximum current during startup thus limiting inrush current. The PMOS current limit is stepped through four soft-start levels of approximately 20%, 25%, 40%, & 100%. Each step is maintained for 400µs following an internal reference start up duration of 100µs giving a total nominal startup period of 1700µs. During startup, the chip operates by controlling the inductor current swings between 0A and current limit. If at any time V_{OUT} reaches 86% of the target or at the end of the soft-start period, the SC284P will switch to PWM mode operation.

The SC284P is capable of starting up into a pre-biased output.

Shut Down

When all CTL pins of a channel are low, the corresponding channel will be disabled, drawing less than 1µA from that input power supply. The internal switches and bandgap voltage will be immediately turned off.

Thermal Shutdown

The device has a thermal shutdown feature to protect the SC284P if the junction temperature exceeds 160°C. During thermal shutdown, the on-chip power devices are disabled, tri-stating the LX output. When the temperature drops by 10°C, it will initiate a soft-start cycle to resume normal operation.

Inductor Selection

The SC284P converter has internal loop compensation. The compensation is designed to work with an output filter corner frequency of less than 40kHz for a V_{IN} of 5V and 50KHz for a V_{IN} of 3.3V over any operating condition. The corner frequency of the output filter is shown in the following equation.

$$f_C = \frac{1}{2\pi \sqrt{L \times C_{OUT}}}$$

Values outside this range may lead to instability, malfunction, or out-of-specification performance.

Applications Information (continued)

In general, the inductance is chosen by making the inductor ripple current to be less than 30% of maximum load current. When choosing an inductor, it is important to consider the change in inductance with DC bias current. The inductor saturation current is specified as the current at which the inductance drops a specific percentage from the nominal value. This is approximately 30%. Except for short-circuit or other fault conditions, the peak current must always be less than the saturation current specified by the manufacturer. The peak current is the maximum load current plus one half of the inductor ripple current at the maximum input voltage. Load and/or line transients can cause the peak current to exceed this level for short durations. Maintaining the peak current below the inductor saturation specification keeps the inductor ripple current and the output voltage ripple at acceptable levels. Manufacturers often provide graphs of actual inductance and saturation characteristics versus applied inductor current. The saturation characteristics of the inductor can vary significantly with core temperature. Core and ambient temperatures should be considered when examining the core saturation characteristics.

When the inductance has been determined, the DC resistance (DCR) must be examined. The efficiency that can be achieved is dependent upon the DCR of the inductor. Lower values give higher efficiency. The RMS DC current rating of the inductor is associated with losses in the copper windings and the resulting temperature rise of the inductor. This is usually specified as the current which produces a 40˚C temperature rise. Most copper windings are rated to accommodate this temperature rise above maximum ambient.

Magnetic fields associated with the output inductor can interfere with nearby circuitry. This can be minimized by the use of low noise shielded inductors which use the minimum gap possible to limit the distance that magnetic fields can radiate from the inductor. However shielded inductors typically have a higher DCR and are thus less efficient than a similarly sized non-shielded inductor.
Final inductor selection depends upon various design considerations such as efficiency, EMI, size, and cost. Table 2 lists the manufacturers of recommended inductor options. The saturation characteristics and DC current ratings are also shown.

Manufacturer Part Number	L (µH)	DCR Max (Ω)	Rated Current (A)	L at Rated Current (µH)	Dimensions LxWxH (mm)
TOKO 1071AS-1R0N	1.00±30%	0.040	2.70	0.70	2.8x3.0x1.5
TOKO 1127AS-2R2M	2.20±20%	0.048	2.50	1.54	3.5x3.7x1.8
Panasonic ELLVGG1R0N	1.00±23%	0.062	2.20	0.70	3.2x3.2x1.5

Table 2 – Recommended Inductors

C_{OUT} Selection

The internal voltage loop compensation in the SC284P limits the minimum output capacitor value to 22µF if using a 2.2µH inductor or 44µF if using a 1µH inductor. This is due to its influence on the the loop crossover frequency, phase margin, and gain margin. The total output capacitance should not exceed 50µF to avoid any start-up problems. For most typical applications it is recommended to use an output capacitance of 22µF to 44µF. When choosing the output capacitor's capacitance, verify the voltage derating effect from the capacitor vendor's data sheet.

Capacitors with X7R or X5R ceramic dielectric are recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

The output voltage droop due to a load transient is determined by the capacitance of the ceramic output capacitor. The ceramic capacitor supplies the load current initially until the loop responds. Within a few switching cycles the loop will respond and the inductor current will increase to match the required load. The output voltage droop during the period prior to the loop responding can be related to the choice of output capacitor by the relationship from the following equation.

$$C_{OUT} = \frac{3 \times \Delta I_{LOAD}}{V_{DROOP} \times f_{OSC}}$$

The output capacitor RMS ripple current may be calculated

Applications Information (continued)

from the following equation.

$$I_{COUT(RMS)} = \frac{1}{2\sqrt{3}} \left(\frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{L \times f_{OSC} \times V_{IN}} \right)$$

Table 3 lists the manufac turers of recommended capacitor options.

Manufacturer Part Nunber	Value (µF)	Type	Rated Voltage (VDC)	Value at 3.3V (µF)	Dimensions LxWxH (mm)
Murata GRM21BR60J106K	10±10%	X5R	6.3	4.74	2.0x1.25x1.25 (EIA:0805)
Murata GRM219R60J106K	10±10%	X5R	6.3	4.05	2.0x1.25x0.85 (EIA:0805)
Murata GRM21BR60J226M	22±20%	X5R	6.3	6.57	2.0x1.25x1.25 (EIA:0805)
Murata GRM31CR60J476M	47±20%	X5R	6.3	20.3	3.2x1.6x1.6 (EIA:1206)

Table 3 – Recommended Capacitors

C_{IN} Selection

The SC284P source input current is a DC supply current with a triangular ripple imposed on it. To prevent large input voltage ripple, a low ESR ceramic capacitor is required. A minimum value of 10µF should be used. It is important to consider the DC voltage coefficient characteristics when determining the actual required value. It should be noted a 10µF, 6.3V, X5R ceramic capacitor with 5V DC applied may exhibit a capacitance as low as 4.05µF. To estimate the required input capacitor, determine the acceptable input ripple voltage and calculate the minimum value required for C_{IN} as shown by the following equation.

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}{\left(\frac{\Delta V}{I_{OUT}} - ESR \right) \times f_{OSC}}$$

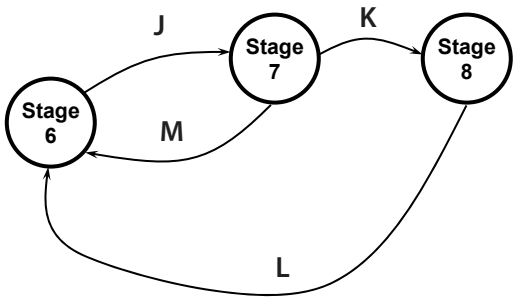
The input capacitor RMS ripple current varies with the input and output voltage. The maximum input capacitor RMS current is found from the next equation .

$$I_{CIN(RMS)} = \sqrt{\frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

The input voltage ripple and RMS current ripple are at a maximum when the input voltage is twice the output voltage or 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the PMOS switch. Low ESR/ESL X5R ceramic capacitors are recommended for this function. To minimize stray inductance, the capacitor should be placed as close as possible to the VIN and GND pins of the SC284P.

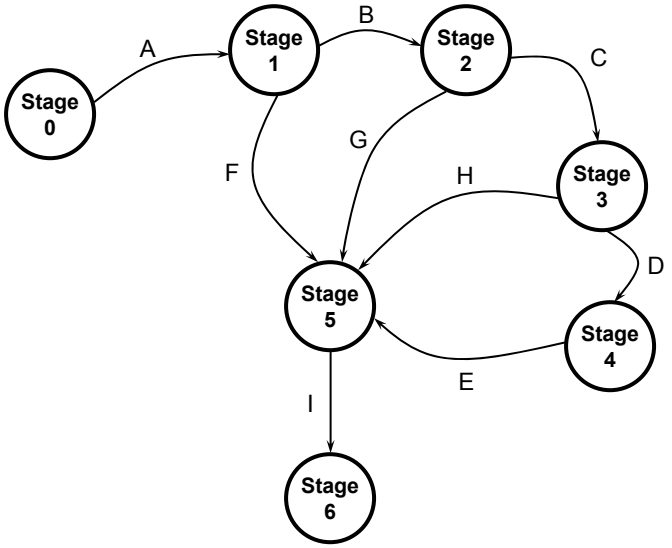
Applications Information (continued)



Stages	Operation description
6	Normal PWM operation Overload protection is enabled and peak current limit at 100% level
7	Cycle by cycle peak current limit
8	OCP protection is activated. Foldback peak current limit. PWM "ON" when inductor current of 0A PWM "OFF" when inductor current hits peak current limit of foldback mode.

Conditions	Operation description
J	Inductor current hits peak current limit
K	Peak current limit for 16 consecutive cycles
L	Vout ≥ 100% target
M	Inductor current doesn't hit peak current limit

Figure 5 — Current Limit Protection



Stages	Operation description
0	Chip is OFF.
1	Peak current limit at 20% level PWM "ON" when inductor current of 0A PWM "OFF" when inductor current hits peak current limit Stage duration of 400µs
2	Peak current limit at 25% level PWM "ON" when inductor current of 0A PWM "OFF" when inductor current hits peak current limit Stage duration of 400µs
3	Peak current limit at 40% level PWM "ON" when inductor current of 500mA PWM "OFF" when inductor current hits peak current limit Stage duration of 400µs
4	Peak current limit at 100% level PWM "ON" when inductor current of 500mA PWM "OFF" when inductor current hits peak current limit Stage duration of 400µs
5	Peak current limit at 100% level Switch to closed-loop PWM operation.
6	Soft Start ends. Normal PWM operation Overload protection is enabled

Conditions	Operation description
A	VIN > UVLO Threshold AND One or more CTL pin is high. AND Internal reference is ready.
B	End of stage 1 AND Vout<86% of target
C	End of stage 2 AND Vout<86% of target
D	End of stage 3 AND Vout<86% of target
E	End of stage 4 AND Vout<86% of target
F	Vout>86% of target
G	Vout>86% of target
H	Vout>86% of target
I	End of soft start time of 1700µs

Figure 6 — Soft Start Operation

Applications Information (continued)

PCB Layout Considerations

The layout diagram in Figure 7 shows a recommended PCB top layer for the SC284P and supporting components. Figure 8 shows the bottom layer for this PCB. Fundamental layout rules must be followed since the layout is critical for achieving the performance specified in the Electrical Characteristics table. Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce, and resistive voltage losses. Poor regulation and instability can result.

The following guidelines are recommended when developing a PCB layout:

1. The input capacitor, C_{IN}, should be placed as close to the VIN and PGND pins as possible. This capacitor provides a low impedance loop for the pulsed currents present at the buck converter's input. Use short wide traces to connect as closely to the IC as possible. This will minimize EMI and input voltage ripple by localizing the high frequency current pulses.
2. Keep the LX pin traces as short as possible to minimize pickup of high frequency switching edges to other parts of the circuit. C_{OUT} and L should be connected as close as possible between the LX and PGND pins, with a direct return to the PGND pin from C_{OUT}.
3. Route the output voltage feedback/sense path away from the inductor and LX node to minimize noise and magnetic interference.
4. Use a ground plane referenced to the SC284P PGND pin. Use several vias to connect to the component side ground to further reduce noise and interference on sensitive circuit nodes.
5. If possible, minimize the resistance from the output and PGND pin to the load. This will reduce the voltage drop on the ground plane and improve the load regulation. It will also improve the overall efficiency by reducing the copper losses on the output and ground planes.
6. Connect the AGND pins to the thermal pad.

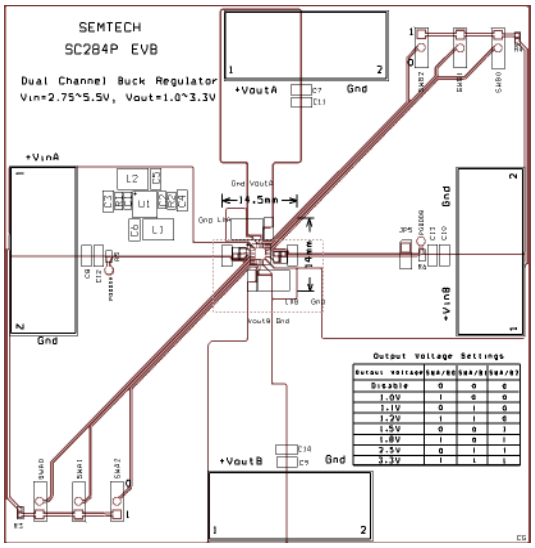


Figure 7 — Recommended PCB Layout (Top Layer)

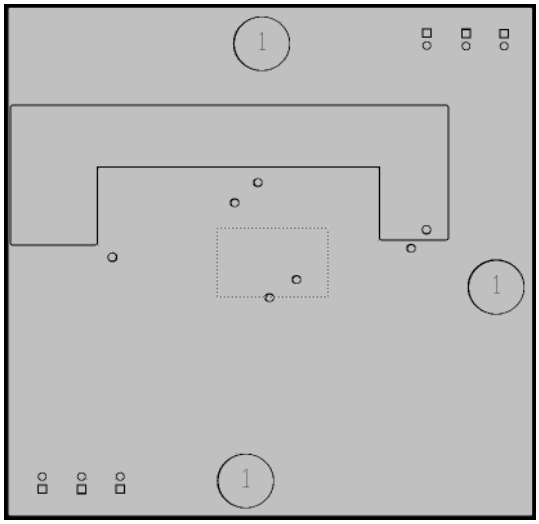


Figure 8 — PCB Bottom Layer

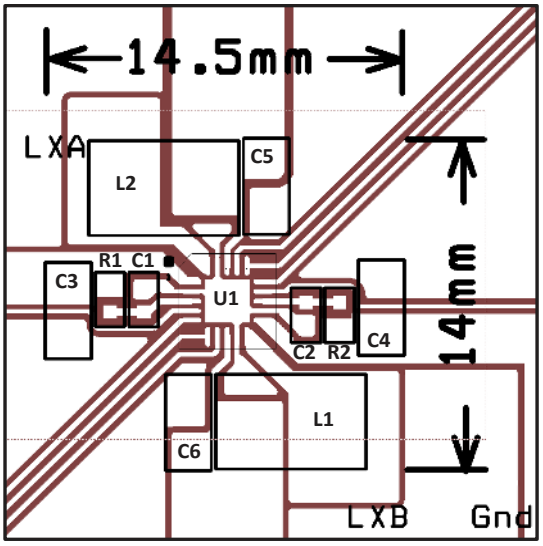
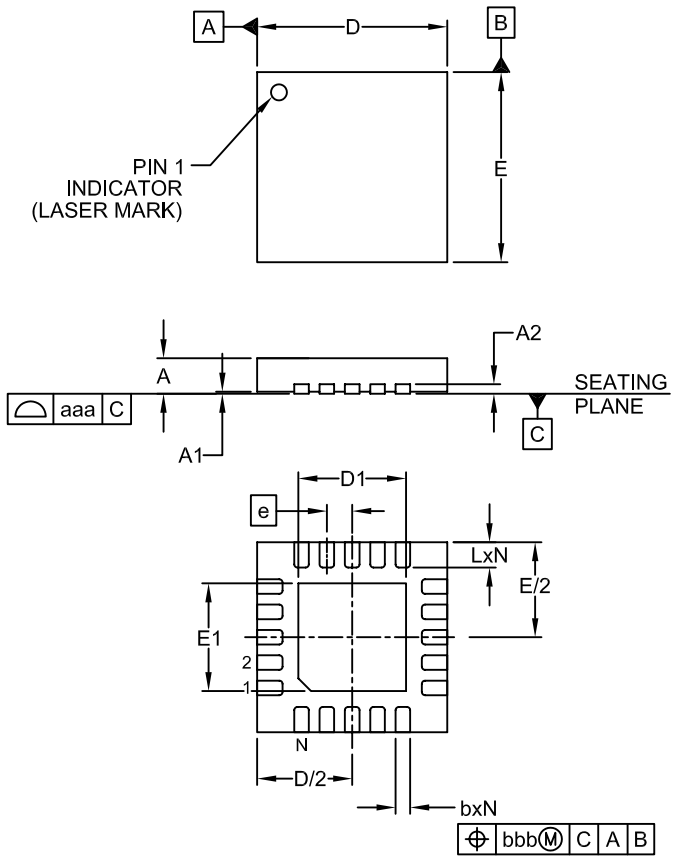


Figure 9 — Recommended PCB Layout (Top Layer Details)

Outline Drawing – 3x3 MLPQ-UT20

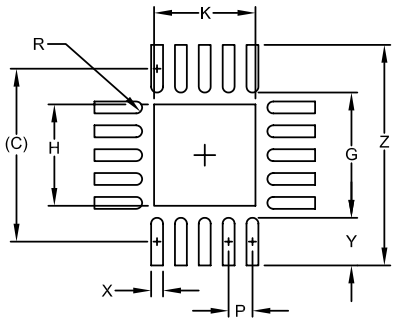


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.152)	
b	.006	.008	.010	0.15	0.20	0.25
D	.114	.118	.122	2.90	3.00	3.10
D1	.061	.067	.071	1.55	1.70	1.80
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e		.016 BSC			0.40 BSC	
L	.012	.016	.020	0.30	0.40	0.50
N		20			20	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.

Land Pattern – 3x3 MLPQ-UT20



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.031	0.80
Z	.146	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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