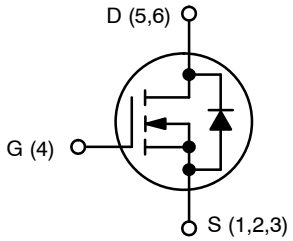
MOSFET – Power, Single N-Channel

100 V, 3.9 mΩ, 138 A

NVMFWS004N10MC

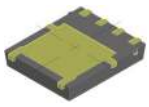
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
100 V	3.9 mΩ @ 10 V	138 A



N−CHANNEL MOSFET

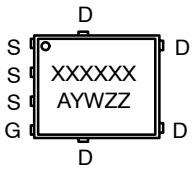
Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free, Beryllium Free and are RoHS Compliant



DFN5
(SO8FL WF)
CASE 507BA

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	100	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	I_D	138	A
		T_C = 100°C		98	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	164	W
		T_C = 100°C		82	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	21	A
		T_A = 100°C		15	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	3.8	W
		T_A = 100°C		1.9	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	900	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	126	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 9.2 A)			E_{AS}	536	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 1)	$R_{\theta JC}$	0.91	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using 1 in^2 pad size, 2 oz. Cu pad.

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		100			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			56		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 100 V	T_J = 25°C			1	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 270 μA		2		4	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 250 μA, ref to 25°C			−9.1		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 48 A			3.3	3.9	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 48 A			120		S
CHARGES & CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 50 V			3600		pF
Output Capacitance	C_{OSS}				1700		
Reverse Transfer Capacitance	C_{RSS}				30		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 48 A			48		nC
Threshold Gate Charge	$Q_{G(TH)}$				11		
Gate−to−Source Charge	Q_{GS}				18		
Gate−to−Drain Charge	Q_{GD}				8		
Plateau Voltage	V_{GP}				5.2		V
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 48 A, R_G = 6 Ω			25		ns
Rise Time	t_r				18		
Turn−Off Delay Time	$t_{d(OFF)}$				39		
Fall Time	t_f				13		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 48 A	T_J = 25°C		0.84	1.3	V
			T_J = 125°C		0.73		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, di/dt = 100 A/μs, I_S = 24 A			65		ns
Reverse Recovery Charge	Q_{RR}				73		nC
Charge Time	t_S				30		ns
Discharge Time	t_D				35		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

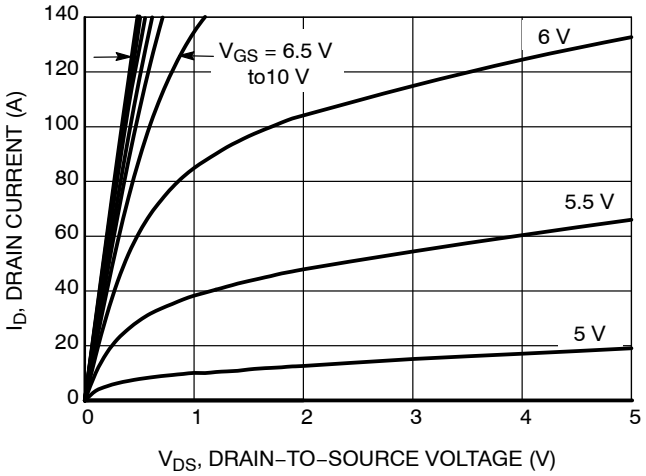


Figure 1. On−Region Characteristics

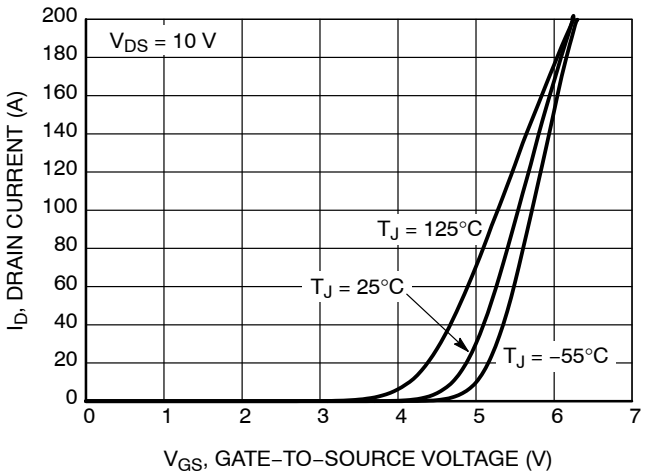


Figure 2. Transfer Characteristics

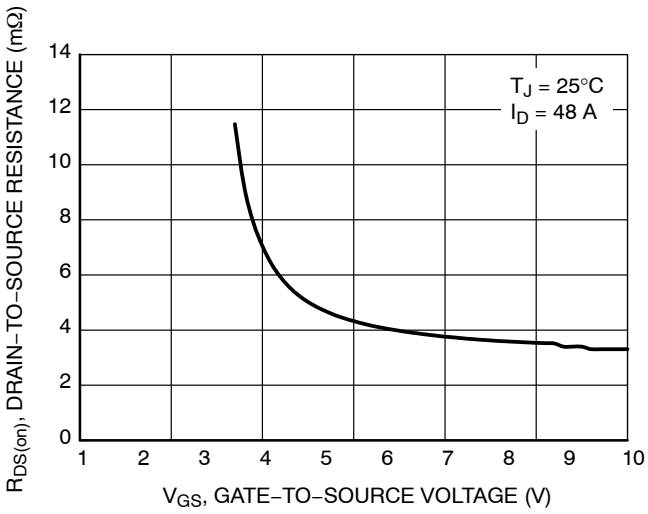


Figure 3. On−Resistance vs. Gate−to−Source Voltage

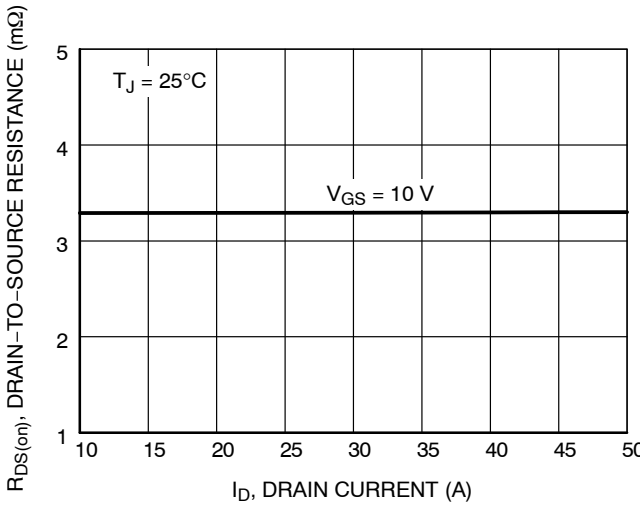


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

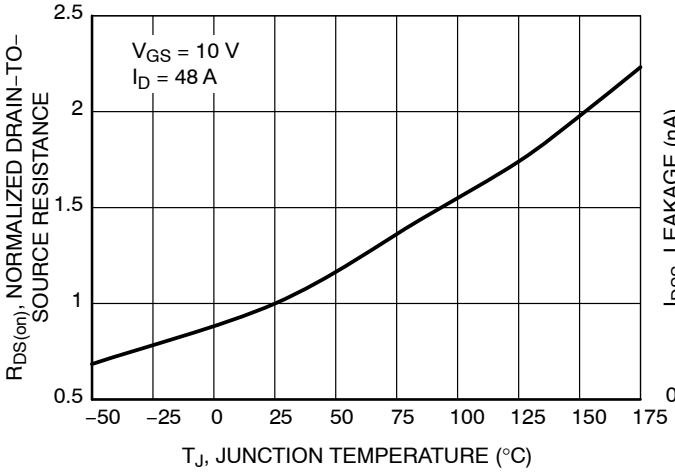


Figure 5. On−Resistance Variation with Temperature

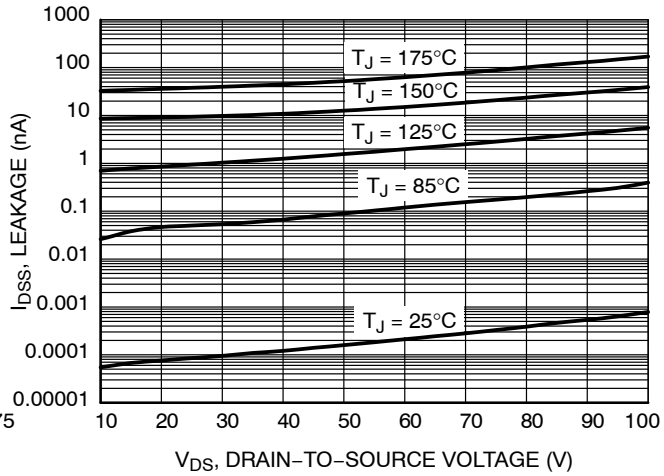


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

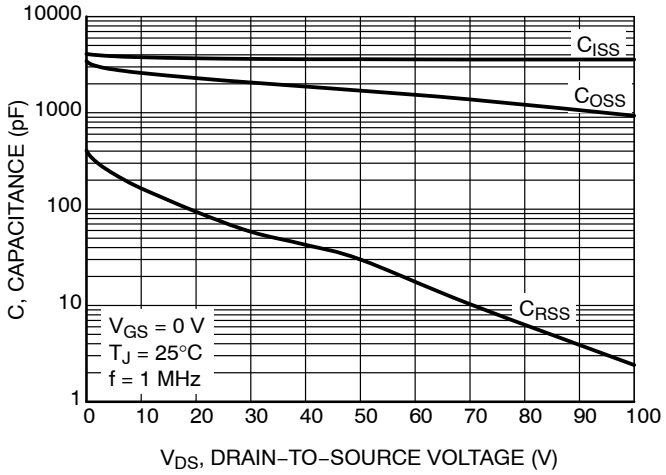


Figure 7. Capacitance Variation

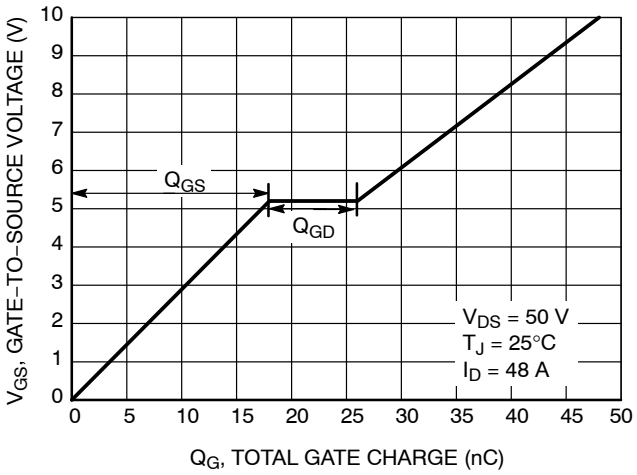


Figure 8. Gate−to−Source Voltage vs. Total Charge

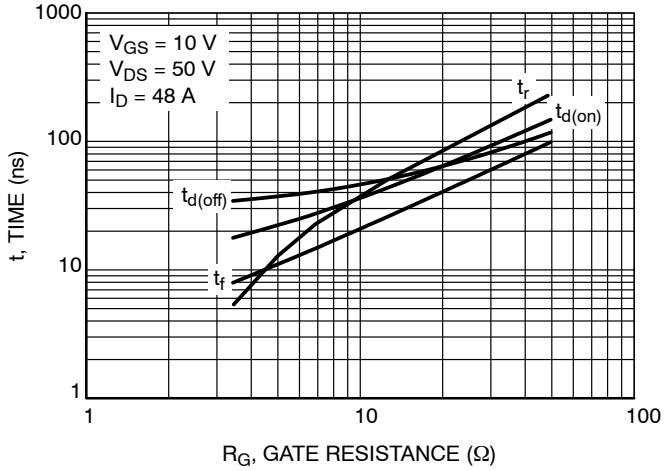


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

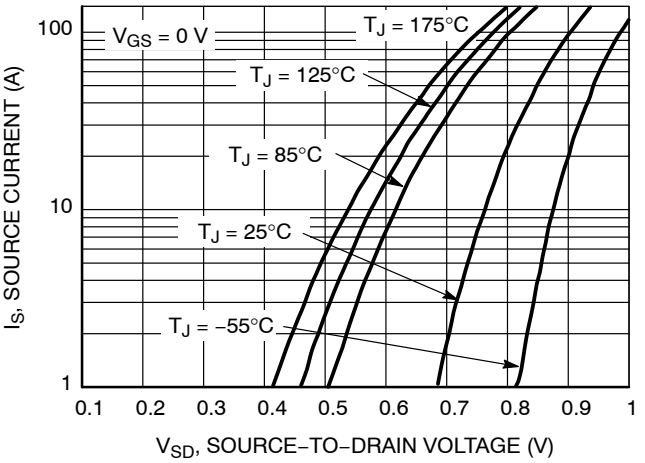


Figure 10. Diode Forward Voltage vs. Current

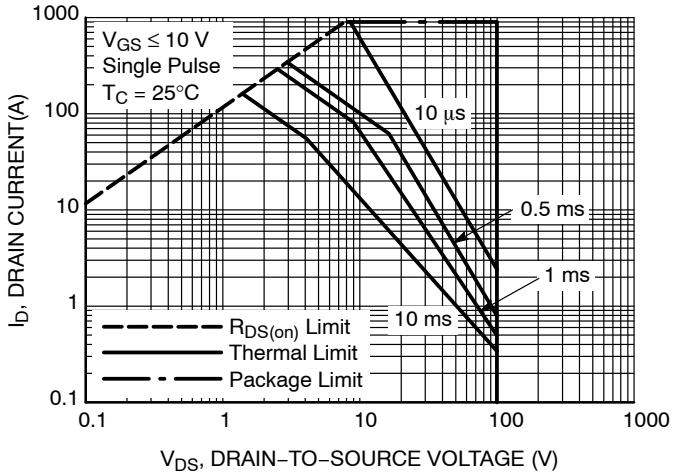


Figure 11. Maximum Rated Forward Biased Safe Operating Area

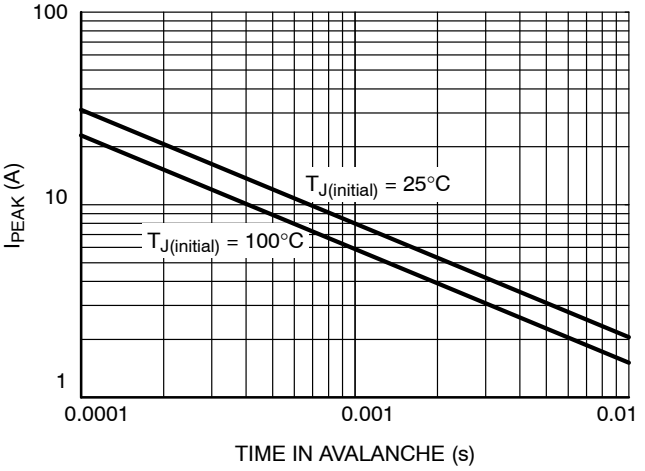


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

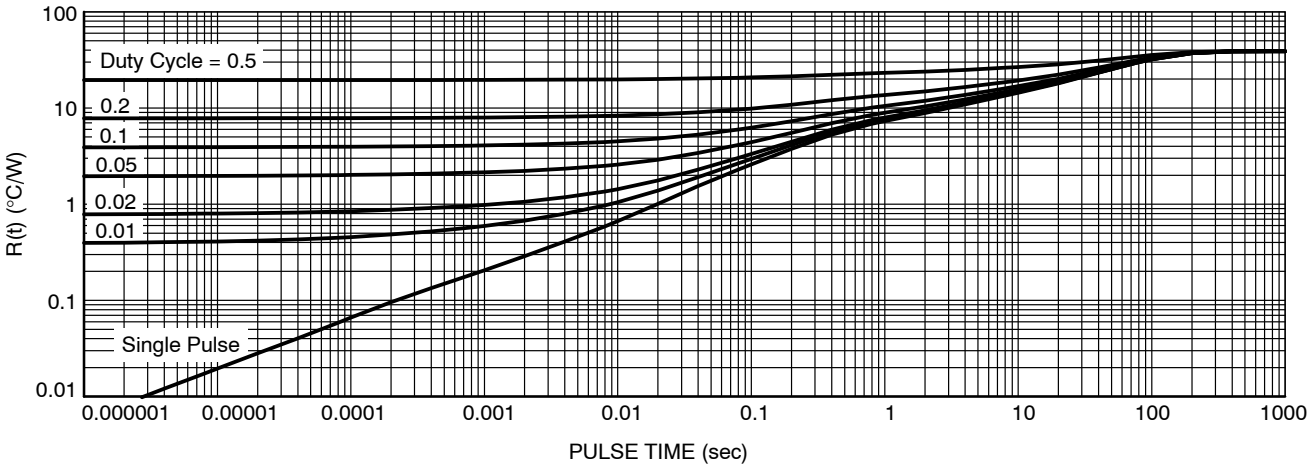
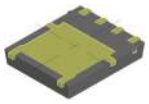


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

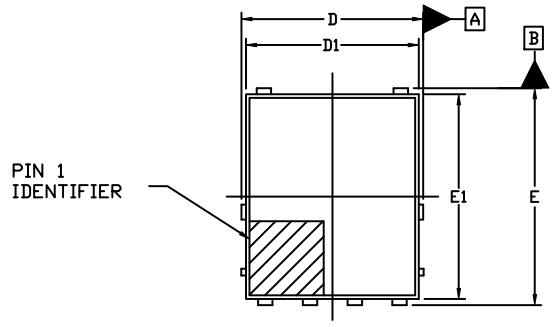
Device	Marking	Package	Shipping†
NVMFWS004N10MCT1G	004W10	Wettable Flank DFN5 (Pb−Free)	1500 / Tape & Reel

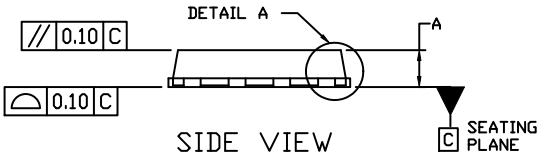
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

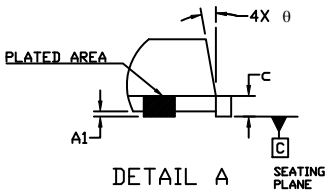


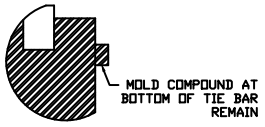
DFNW5 5x6 (FULL−CUT SO8FL WF)
CASE 507BA
ISSUE A

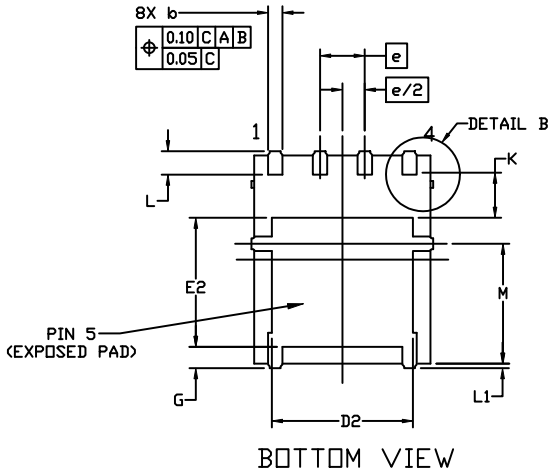
DATE 03 FEB 2021





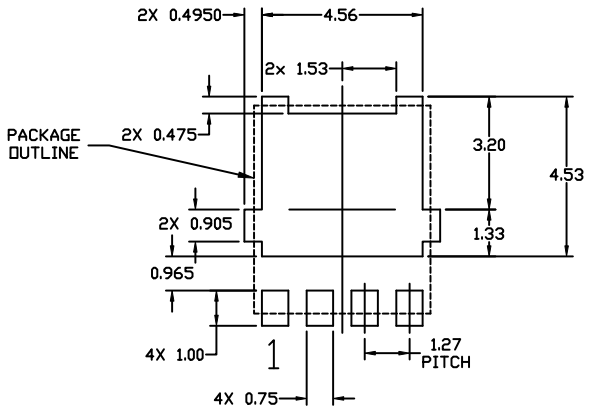






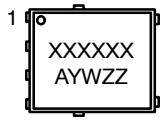
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFNW5 5x6 (FULL−CUT SO8FL WF)**	**PAGE 1 OF 1**

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