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40MHz, PRAM Four Channel Programmable Amplifiers

intercil

The HA-2404 comprise a series of four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

Each channel of the HA-2404 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing signal selection and mathematical function designs. With $30V/\mu s$ slew rate, 40MHz gain bandwidth and $30M\Omega$ input impedance these devices are ideal building blocks for signal generators, active filters and data acquisition designs. Programmability, coupled with 4mV typical offset voltage and 5nA offset current, makes these amplifiers outstanding components for signal conditioning circuits.

During Disable Mode V_{OUT} goes to V-. For high output impedance during Disable, see HA2444.

For further design ideas, see Application Note AN514.

Ordering Information

PART NUMBER	TEMP. RANGE (^o C)	PACKAGE	PKG. DWG. #
HA1-2404-4	-25 to 85	16 Ld CERDIP	F16.3

TRUTH	TABLE

D1	D0	D0 EN SELECTED CHANNEL		D1
L	L	Н	1	L
L	Н	Н	2	L
н	L	Н	3	Н
н	Н	Н	4	Н
Х	Х	L	None, V _{OUT} goes to V-	Х

Features

Programmability

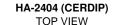
•	High Rate Slew $\ldots \ldots 30 V/\!\mu s$
•	Wide Gain Bandwidth 40MHz
•	High Gain
•	Low Offset Current
•	High Input Impedance $\dots \dots 30 M\Omega$

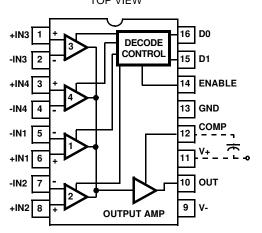
- Single Capacitor Compensation
- DTL/TTL Compatible Inputs

Applications

- · Thousands of Applications; Program
 - Signal Selection/Multiplexing
 - Operational Amplifier Gain
 - Oscillator Frequency
 - Filter Characteristics
 - Add-Subtract Functions
 - Integrator Characteristics
 - Comparator Levels

Pinout





Absolute Maximum Ratings (T_A = 25°C)

Voltage Between V+ and V- Terminals	45.0V
Differential Input Voltage VS	UPPLY
Digital Input Voltage0.76V to -	
Output Current Short Circuit Protected, $I_{SC} < \pm$	33mA)
Internal Power Dissipation (Note 1)	

Operating Conditions

Temperature Range

Thermal Information

Thermal Resistance (Typical, Note 2)	θ _{JA} (^o C/W)	θ _{JC} (^o C/W)
CERDIP Package	75	22
Maximum Junction Temperature (Ceramic		175 ⁰ C
Maximum Junction Temperature (Plastic	Package)	150 ⁰ C
Maximum Storage Temperature Range .	6	5 ^o C to 150 ^o C
Maximum Lead Temperature (Soldering 7	10s)	300 ⁰ C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation including output load, must be designed to maintain the junction temperature below 175°C for the ceramic package, and below 150°C for the plastic packages.

2. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications Test Conditions: $V_{SUPPLY} = \pm 15V$, Unless Otherwise Specified. Digital Inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4$. Limits apply to each of the four channels, when addressed

	TEST	ТЕМР. (^о С)	HA-2404			
PARAMETER	CONDITIONS		MIN	ТҮР	MAX	UNITS
INPUT CHARACTERISTICS						
Offset Voltage		25	-	4	9	mV
		Full	-	-	11	mV
Bias Current (Note 8)		25	-	50	200	nA
		Full	-	-	400	nA
Offset Current (Note 8)		25	-	5	50	nA
		Full	-	-	100	nA
Input Resistance (Note 8)		25	-	30	-	MΩ
Common Mode Range		Full	±9.0	-	-	V
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	$R_L = 2k\Omega$	25	50	150	-	kV/V
	$V_{OUT} = 20V_{P-P}$	Full	25	-	-	kV/V
Common Mode Rejection Ratio	$V_{CM} = \pm 5V$	Full	80	100	-	dB
Gain Bandwidth (Notes 3, 9)		25	20	40	-	MHz
Gain Bandwidth (Notes 4, 9)		25	4	8	-	MHz
Minimum Stable Gain	$(C_{COMP} = 0)$		10	-	-	V/V
OUTPUT CHARACTERISTICS				-1	L	1
Output Voltage Swing	$R_L = 2k\Omega$	Full	±10.0	±12.0	-	V
Output Current		25	10	20	-	mA
Full Power Bandwidth (Notes 3, 10)	$V_{OUT} = 20V_{P-P}$	25	640	950	-	kHz
Full Power Bandwidth (Notes 4, 10)	V _{OUT} = 20V _{P-P}	25	200	250	-	kHz
TRANSIENT RESPONSE (Note 11)				1	I	1
Rise Time (Note 4)	$V_{OUT} = 200 m V_{PEAK}$	25	-	20	45	ns
Overshoot (Note 4)	V _{OUT} = 200mV _{PEAK}	25	-	25	40	%
Slew Rate (Note 3)	V _{OUT} = 10V _{P-P}	25	20	30	-	V/µs
Slew Rate (Notes 4, 9)	V _{OUT} = 10V _{P-P}	25	6	8	-	V/µs

Electrical Specifications Test Conditions: $V_{SUPPLY} = \pm 15V$, Unless Otherwise Specified. Digital Inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4$. Limits apply to each of the four channels, when addressed (Continued)

	TEST CONDITIONS	TEMP.	HA-2404			
PARAMETER		(°C)	MIN	ТҮР	МАХ	UNITS
Settling Time (Notes 4, 5, 9)	$V_{OUT} = 10V_{P-P}$	25	-	1.5	2.5	μS
CHANNEL SELECT CHARACTERISTICS						
Digital Input Current	$V_{IN} = 0V$	Full	-	1	1.5	mA
Digital Input Current	V _{IN} = +5.0V	Full	-	5	-	nA
Output Delay (Notes 6, 9)		25	-	100	250	ns
Crosstalk (Note 7)		25	-80	-110	-	dB
POWER SUPPLY CHARACTERISTICS		1	4	_1		1
Supply Current		25	-	4.8	6.0	mA
Power Supply Rejection Ratio	$V_{S} = \pm 10V$ to $\pm 20V$	Full	74	90	-	dB

NOTES:

3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2k\Omega$, $C_L = 50pF$.

4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2k\Omega$, $C_L = 50pF$.

5. To 0.1% of final value.

6. To 10% of final value; output then slews at normal rate to final value.

7. Unselected input to output; $V_{IN} = \pm 10V_{DC}$.

8. Unselected channels have approximately the same input parameters.

9. Guaranteed by design.

9. Guaranteed by design. 10. Full Power Bandwidth based on slew rate measurement using: $FPBW = \frac{SR}{2\pi V_{PEAK}}$; $V_{PEAK} = 5V$.

11. See Figure 13 for test circuit.

Schematic Diagram

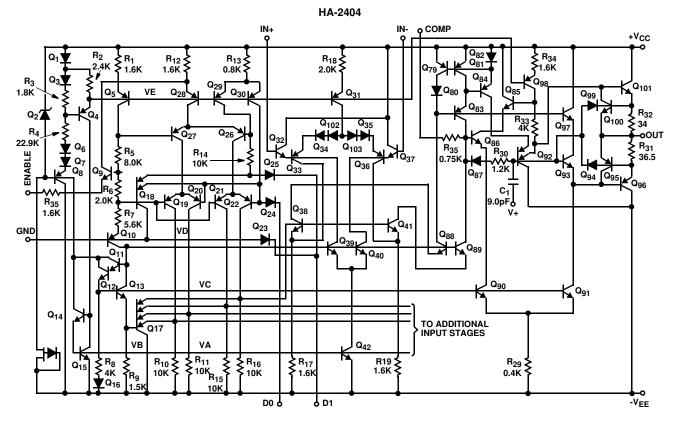
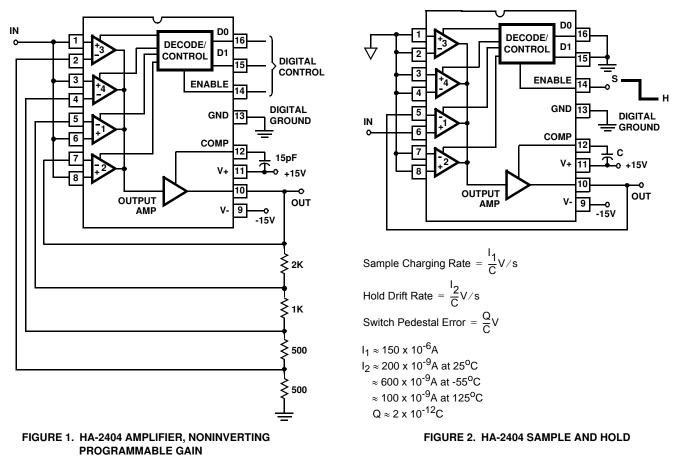
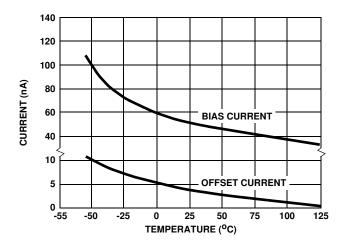


Diagram Includes: One Input Stage, Decode Control, Bias Network, and Output Stage

Typical Applications



For more examples, see Intersil Application Note AN514.



Typical Performance Curves

FIGURE 3. INPUT BIAS CURRENT AND OFFSET CURRENT vs TEMPERATURE

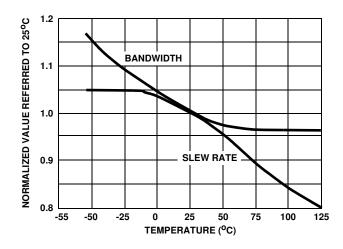


FIGURE 4. NORMALIZED AC PARAMETERS vs TEMPERATURE



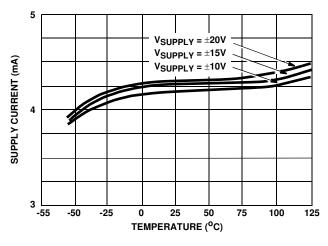


FIGURE 5. POWER SUPPLY CURRENT vs TEMPERATURE

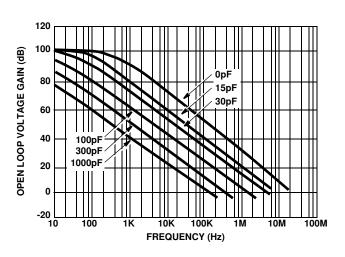


FIGURE 7. FREQUENCY RESPONSE vs C_{COMP}

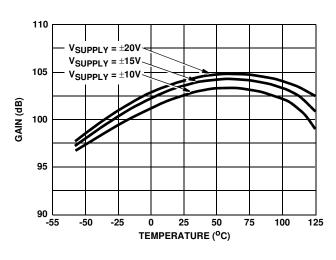


FIGURE 9. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

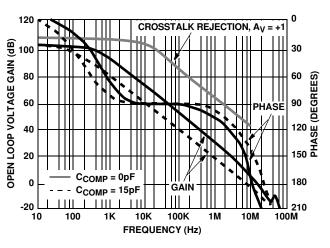
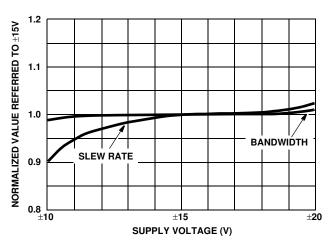


FIGURE 6. OPEN LOOP FREQUENCY AND PHASE RESPONSE





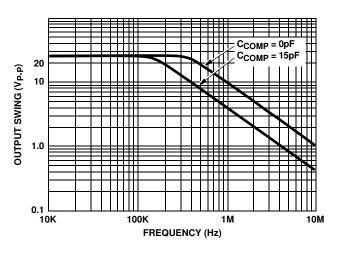
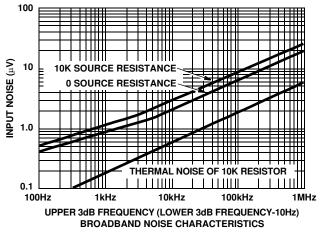
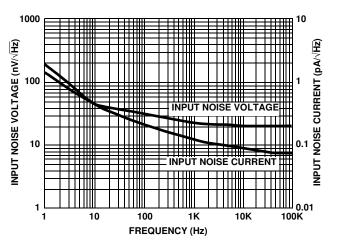


FIGURE 10. OUTPUT VOLTAGE SWING vs FREQUENCY



Typical Performance Curves (Continued)







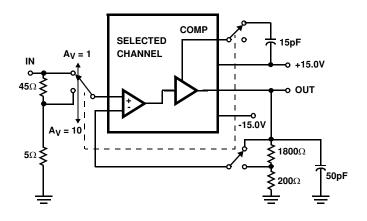
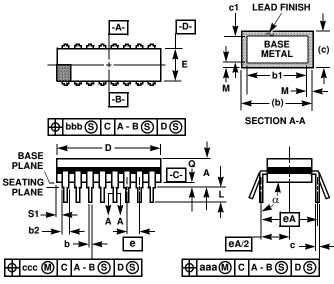


FIGURE 13. SLEW RATE AND TRANSIENT RESPONSE

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

- 1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- 2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
- 3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
- Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
- 5. This dimension allows for off-center lid, meniscus, and glass overrun.
- 6. Dimension Q shall be measured from the seating plane to the base plane.
- 7. Measure dimension S1 at all four corners.
- 8. N is the maximum number of terminal positions.
- 9. Dimensioning and tolerancing per ANSI Y14.5M 1982.
- 10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A) 16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

	INC	INCHES MILLIMETERS		MILLIMETERS		
SYMBOL	MIN	MAX	MIN MAX		NOTES	
А	-	0.200	-	5.08	-	
b	0.014	0.026	0.36	0.66	2	
b1	0.014	0.023	0.36	0.58	3	
b2	0.045	0.065	1.14	1.65	-	
b3	0.023	0.045	0.58	1.14	4	
С	0.008	0.018	0.20	0.46	2	
c1	0.008	0.015	0.20	0.38	3	
D	-	0.840	-	21.34	5	
E	0.220	0.310	5.59	7.87	5	
е	0.100	BSC	2.54 BSC		-	
eA	0.300	0.300 BSC		7.62 BSC		
eA/2	0.150	0.150 BSC		3.81 BSC		
L	0.125	0.200	3.18	5.08	-	
Q	0.015	0.060	0.38	1.52	6	
S1	0.005	-	0.13	-	7	
α	90 ⁰	105 ⁰	90 ⁰	105 ⁰	-	
aaa	-	0.015	-	0.38	-	
bbb	-	0.030	-	0.76	-	
ссс	-	0.010	-	0.25	-	
М	-	0.0015	- 0.038		2, 3	
Ν	1	6	1	8		

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