

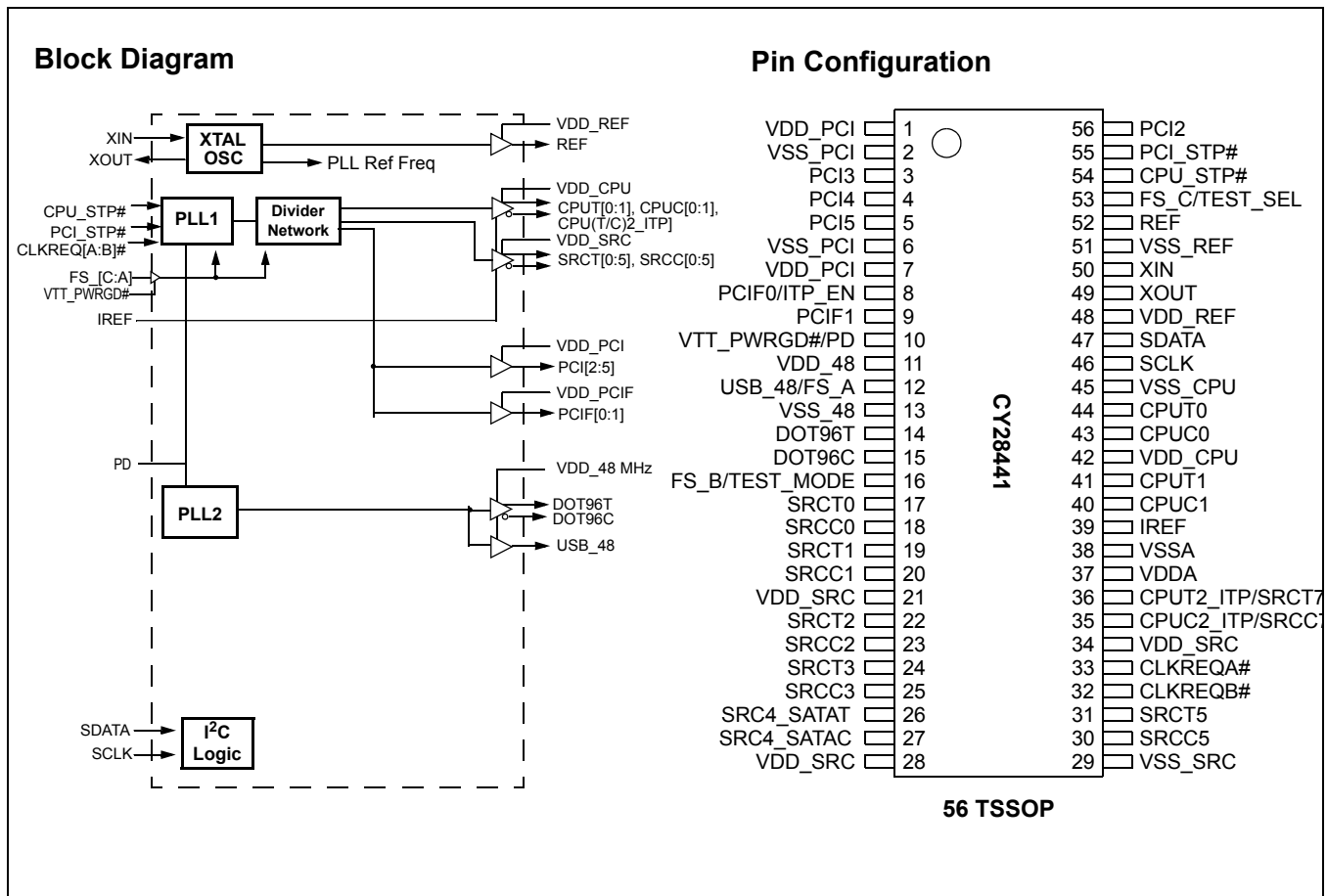


Clock Generator for Intel® Alviso Chipset

Features

- Compliant to Intel® CK410M
- Supports Intel Pentium®-M CPU
- Selectable CPU frequencies
- Differential CPU clock pairs
- 100-MHz differential SRC clocks
- 96-MHz differential dot clock
- 48-MHz USB clocks
- SRC clocks independently stoppable through CLKREQ#[A:B]
- 33-MHz PCI clock
- Low-voltage frequency select input
- I²C support with readback capabilities
- Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- 3.3V power supply
- 56-pin TSSOP package

| CPU | SRC | PCI | REF | DOT96 | USB_48 |
|---------|---------|-----|-----|-------|--------|
| x2 / x3 | x6 / x7 | x 6 | x 1 | x 1 | x 1 |



Pin Description

| Pin No. | Name | Type | Description |
|--|-------------------------------------|---------|--|
| 33, 32 | CLKREQA#, CLKREQB# | I, PU | 3.3V LVTTTL input for enabling assigned SRC clock, active LOW. CLKREQA# defaults to enable/disable SRCT/C4, CLKREQB# defaults to enable/disable SRCT/C5. Assignment can be changed via SMBUS register Byte 8. |
| 54 | CPU_STP# | I, PU | 3.3V LVTTTL input for CPU_STP# active LOW. |
| 44, 43, 41, 40 | CPUT/C | O, DIF | Differential CPU clock outputs. |
| 36, 35 | CPUT2_ITP/SRCT7, CPUC2_ITP/SRCC7 | O, DIF | Selectable differential CPU or SRC clock output. ITP_EN = 0 @ VTT_PWRGD# assertion = SRC7 ITP_EN = 1 @ VTT_PWRGD# assertion = CPU2 |
| 14, 15 | DOT96T, DOT96C | O, DIF | Fixed 96-MHz clock output. |
| 12 | FS_A/USB_48 | I/O, SE | 3.3V-tolerant input for CPU frequency selection/fixed 48-MHz clock output. <i>Refer to DC Electrical Specifications table for V_{IL_FS}, V_{IH_FS} specifications.</i> |
| 16 | FS_B/TEST_MODE | I | 3.3V-tolerant input for CPU frequency selection. Selects Ref/N or Hi-Z when in test mode 0 = Hi-Z, 1 = Ref/N <i>Refer to DC Electrical Specifications table for V_{IL_FS}, V_{IH_FS} specifications.</i> |
| 53 | FS_C/TEST_SEL | I | 3.3V-tolerant input for CPU frequency selection. Selects test mode if pulled to greater than 2.0V when VTT_PWRGD# is asserted low. <i>Refer to DC Electrical Specifications table for V_{IL_FS}, V_{IH_FS} specifications.</i> |
| 39 | IREF | I | A precision resistor is attached to this pin, which is connected to the internal current reference. |
| 56, 3, 4, 5 | PCI | O, SE | 33-MHz clocks. |
| 55 | PCI_STP# | I, PU | 3.3V LVTTTL input for PCI_STP# active LOW. |
| 8 | PCIF0/ITP_EN | I/O, SE | 33-MHz clock/CPU2 select (sampled on the VTT_PWRGD# assertion). 1 = CPU2_ITP, 0 = SRC7 |
| 9 | PCIF1 | O, SE | 33-MHz clock. |
| 52 | REF | O, SE | Reference clock. 3.3V 14.318-MHz clock output. |
| 46 | SCLK | I | SMBus-compatible SCLOCK. |
| 47 | SDATA | I/O | SMBus-compatible SDATA. |
| 26, 27 | SRC4_SATAT, SRC4_SATAC | O, DIF | Differential serial reference clock. Recommended output for SATA. |
| 24, 25, 22, 23, 19, 20, 17, 18, 31, 30 | SRCT/C | O, DIF | Differential serial reference clocks. |
| 11 | VDD_48 | PWR | 3.3V power supply for outputs. |
| 42 | VDD_CPU | PWR | 3.3V power supply for outputs. |
| 1,7 | VDD_PCI | PWR | 3.3V power supply for outputs. |
| 48 | VDD_REF | PWR | 3.3V power supply for outputs. |
| 21, 28, 34 | VDD_SRC | PWR | 3.3V power supply for outputs. |
| 37 | VDDA | PWR | 3.3V power supply for PLL. |
| 13 | VSS_48 | GND | Ground for outputs. |
| 45 | VSS_CPU | GND | Ground for outputs. |
| 2,6 | VSS_PCI | GND | Ground for outputs. |
| 51 | VSS_REF | GND | Ground for outputs. |
| 29 | VSS_SRC | GND | Ground for outputs. |
| 38 | VSSA | GND | Ground for PLL. |
| 10 | VTT_PWRGD#/PD | I | 3.3V LVTTTL input is a level sensitive strobe used to latch the USB_48/FS_A, FS_B, FS_C/TEST_SEL and PCIF0/ITP_EN inputs. After VTT_PWRGD# (active LOW) assertion, this pin becomes a real-time input for asserting power-down (active HIGH). |

Pin Description

| Pin No. | Name | Type | Description |
|---------|------|-------|----------------------------|
| 50 | XIN | I | 14.318-MHz crystal input. |
| 49 | XOUT | O, SE | 14.318-MHz crystal output. |

Frequency Select Pins (FS_A, FS_B and FS_C)

Host clock frequency selection is achieved by applying the appropriate logic levels to FS_A, FS_B, FS_C inputs prior to VTT_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT_PWRGD# being sampled LOW by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS_A, FS_B and FS_C input values. For all logic levels of FS_A, FS_B and FS_C, VTT_PWRGD# employs a one-shot functionality in that once a valid low on VTT_PWRGD# has been sampled, all further VTT_PWRGD#, FS_A, FS_B and FS_C transitions will be ignored, except in test mode. See *Table 1*.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface

initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts Byte Write, Byte Read, Block Write, and Block Read operations from the controller. For Block Write/Read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For Byte Write and Byte Read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The Block Write and Block Read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding Byte Write and Byte Read protocol. The slave receiver address is 11010010 (D2h).

Table 1. Frequency Select Table FS_A, FS_B and FS_C

| FS_C | FS_B | FS_A | CPU | SRC | PCIF/PCI | REF0 | DOT96 | USB |
|------|------|------|-----------------|---------|----------|------------|--------|--------|
| 1 | 0 | 1 | 100 MHz | 100 MHz | 33 MHz | 14.318 MHz | 96 MHz | 48 MHz |
| 0 | 0 | 1 | 133 MHz | 100 MHz | 33 MHz | 14.318 MHz | 96 MHz | 48 MHz |
| 0 | 1 | 1 | RESERVED | | | | | |
| 0 | 1 | 0 | | | | | | |
| 0 | 0 | 0 | | | | | | |
| 1 | 0 | 0 | | | | | | |
| 1 | 1 | 0 | | | | | | |
| 1 | 1 | 1 | | | | | | |

Table 2. Command Code Definition

| Bit | Description |
|-------|---|
| 7 | 0 = Block Read or Block Write operation, 1 = Byte Read or Byte Write operation |
| (6:0) | Byte offset for Byte Read or Byte Write operation. For Block Read or Block Write operations, these bits should be '0000000' |

Table 3. Block Read and Block Write Protocol

| Block Write Protocol | | Block Read Protocol | |
|----------------------|------------------------|---------------------|------------------------|
| Bit | Description | Bit | Description |
| 1 | Start | 1 | Start |
| 8:2 | Slave address – 7 bits | 8:2 | Slave address – 7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 18:11 | Command Code – 8 bits | 18:11 | Command Code – 8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |

Table 3. Block Read and Block Write Protocol (continued)

| Block Write Protocol | | Block Read Protocol | |
|----------------------|-------------------------------|---------------------|-------------------------------------|
| Bit | Description | Bit | Description |
| 27:20 | Byte Count – 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 27:21 | Slave address – 7 bits |
| 36:29 | Data byte 1 – 8 bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 45:38 | Data byte 2 – 8 bits | 37:30 | Byte Count from slave – 8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge |
| | Data Byte /Slave Acknowledges | 46:39 | Data byte 1 from slave – 8 bits |
| | Data Byte N –8 bits | 47 | Acknowledge |
| | Acknowledge from slave | 55:48 | Data byte 2 from slave – 8 bits |
| | Stop | 56 | Acknowledge |
| | | | Data bytes from slave / Acknowledge |
| | | | Data Byte N from slave – 8 bits |
| | | | NOT Acknowledge |
| | | | Stop |

Table 4. Byte Read and Byte Write Protocol

| Byte Write Protocol | | Byte Read Protocol | |
|---------------------|------------------------|--------------------|--------------------------|
| Bit | Description | Bit | Description |
| 1 | Start | 1 | Start |
| 8:2 | Slave address – 7 bits | 8:2 | Slave address – 7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 18:11 | Command Code – 8 bits | 18:11 | Command Code – 8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 27:20 | Data byte – 8 bits | 20 | Repeated start |
| 28 | Acknowledge from slave | 27:21 | Slave address – 7 bits |
| 29 | Stop | 28 | Read |
| | | 29 | Acknowledge from slave |
| | | 37:30 | Data from slave – 8 bits |
| | | 38 | NOT Acknowledge |
| | | 39 | Stop |

Control Registers

Byte 0:Control Register 0

| Bit | @Pup | Name | Description |
|-----|------|------------------------------------|---|
| 7 | 1 | CPUT2_ITP/SRCT7 CPUC2_ITP/SRCC7 | CPU[T/C]2_ITP/SRC[T/C]7 Output Enable 0 = Disable (Hi-Z), 1 = Enable |
| 6 | 1 | RESERVED | RESERVED |
| 5 | 1 | SRC[T/C]5 | SRC[T/C]5 Output Enable 0 = Disable (Hi-Z), 1 = Enable |
| 4 | 1 | SRC[T/C]4 | SRC[T/C]4 Output Enable 0 = Disable (Hi-Z), 1 = Enable |
| 3 | 1 | SRC[T/C]3 | SRC[T/C]3 Output Enable 0 = Disable (Hi-Z), 1 = Enable |

Byte 0: Control Register 0 (continued)

| Bit | @Pup | Name | Description |
|-----|------|-----------|---|
| 2 | 1 | SRC[T/C]2 | SRC[T/C]2 Output Enable 0 = Disable (Hi-Z), 1 = Enable |
| 1 | 1 | SRC[T/C]1 | SRC[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enable |
| 0 | 1 | SRC[T/C]0 | SRC[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enable |

Byte 1: Control Register 1

| Bit | @Pup | Name | Description |
|-----|------|----------------------------------|---|
| 7 | 1 | PCIF0 | PCIF0 Output Enable 0 = Disabled, 1 = Enabled |
| 6 | 1 | DOT_96T/C | DOT_96 MHz Output Enable 0 = Disable (Hi-Z), 1 = Enabled |
| 5 | 1 | USB_48 | USB_48 MHz Output Enable 0 = Disabled, 1 = Enabled |
| 4 | 1 | REF | REF Output Enable 0 = Disabled, 1 = Enabled |
| 3 | 0 | Reserved | Reserved |
| 2 | 1 | CPU[T/C]1 | CPU[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enabled |
| 1 | 1 | CPU[T/C]0 | CPU[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enabled |
| 0 | 0 | CPU/T/C SRCT/C PCIF PCI | Spread Spectrum Enable 0 = Spread off, 1 = Spread on |

Byte 2: Control Register 2

| Bit | @Pup | Name | Description |
|-----|------|----------|---|
| 7 | 1 | PCI5 | PCI5 Output Enable 0 = Disabled, 1 = Enabled |
| 6 | 1 | PCI4 | PCI4 Output Enable 0 = Disabled, 1 = Enabled |
| 5 | 1 | PCI3 | PCI3 Output Enable 0 = Disabled, 1 = Enabled |
| 4 | 1 | PCI2 | PCI2 Output Enable 0 = Disabled, 1 = Enabled |
| 3 | 1 | PCI | PCI Output Drive strength 0 = Low drive 1 = High drive |
| 2 | 1 | Reserved | Reserved, Set = 1 |
| 1 | 1 | Reserved | Reserved, Set = 1 |
| 0 | 1 | PCIF1 | PCIF1 Output Enable 0 = Disabled, 1 = Enabled |

Byte 3: Control Register 3

| Bit | @Pup | Name | Description |
|-----|------|----------|---|
| 7 | 0 | SRC7 | Allow control of SRC[T/C]7 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP# |
| 6 | 0 | RESERVED | RESERVED |
| 5 | 0 | SRC5 | Allow control of SRC[T/C]5 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP# |

Byte 3: Control Register 3 (continued)

| Bit | @Pup | Name | Description |
|-----|------|------|---|
| 4 | 0 | SRC4 | Allow control of SRC[T/C]4 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP# |
| 3 | 0 | SRC3 | Allow control of SRC[T/C]3 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP# |
| 2 | 0 | SRC2 | Allow control of SRC[T/C]2 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP# |
| 1 | 0 | SRC1 | Allow control of SRC[T/C]1 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP# |
| 0 | 0 | SRC0 | Allow control of SRC[T/C]0 with assertion of PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP# |

Byte 4: Control Register 4

| Bit | @Pup | Name | Description |
|-----|------|-----------|---|
| 7 | 0 | Reserved | Reserved, Set = 0 |
| 6 | 0 | DOT96T/C | DOT_PWRDWN Drive Mode 0 = Driven in PWRDWN, 1 = Hi-Z |
| 5 | 0 | Reserved | Reserved, Set = 0 |
| 4 | 0 | PCIF1 | Allow control of PCIF1 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP# |
| 3 | 0 | PCIF0 | Allow control of PCIF0 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP# |
| 2 | 1 | CPU[T/C]2 | Allow control of CPU[T/C]2 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP# |
| 1 | 1 | CPU[T/C]1 | Allow control of CPU[T/C]1 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP# |
| 0 | 1 | CPU[T/C]0 | Allow control of CPU[T/C]0 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP# |

Byte 5: Control Register 5

| Bit | @Pup | Name | Description |
|-----|------|---------------|---|
| 7 | 0 | SRC[T/C][7:0] | SRC[T/C] Stop Drive Mode 0 = Driven when PCI_STP# asserted, 1 = Hi-Z when PCI_STP# asserted |
| 6 | 0 | CPU[T/C]2 | CPU[T/C]2 Stop Drive Mode 0 = Driven when CPU_STP# asserted, 1 = Hi-Z when CPU_STP# asserted |
| 5 | 0 | CPU[T/C]1 | CPU[T/C]1 Stop Drive Mode 0 = Driven when CPU_STP# asserted, 1 = Hi-Z when CPU_STP# asserted |
| 4 | 0 | CPU[T/C]0 | CPU[T/C]0 Stop Drive Mode 0 = Driven when CPU_STP# asserted, 1 = Hi-Z when CPU_STP# asserted |
| 3 | 0 | SRC[T/C][7:0] | SRC[T/C] PWRDWN Drive Mode 0 = Driven when PD asserted, 1 = Hi-Z when PD asserted |
| 2 | 0 | CPU[T/C]2 | CPU[T/C]2 PWRDWN Drive Mode 0 = Driven when PD asserted, 1 = Hi-Z when PD asserted |
| 1 | 0 | CPU[T/C]1 | CPU[T/C]1 PWRDWN Drive Mode 0 = Driven when PD asserted, 1 = Hi-Z when PD asserted |
| 0 | 0 | CPU[T/C]0 | CPU[T/C]0 PWRDWN Drive Mode 0 = Driven when PD asserted, 1 = Hi-Z when PD asserted |

Byte 6: Control Register 6

| Bit | @Pup | Name | Description |
|-----|------|------|---|
| 7 | 0 | | REF/N or Hi-Z Select 0 = Hi-Z, 1 = REF/N Clock |

Byte 6: Control Register 6 (continued)

| Bit | @Pup | Name | Description |
|-----|---------------------|----------------|--|
| 6 | 0 | | Test Clock Mode Entry Control 0 = Normal operation, 1 = REF/N or Hi-Z mode, |
| 5 | 0 | Reserved | Reserved, Set = 0 |
| 4 | 1 | REF | REF Output Drive Strength 0 = 1X, 1 = 2X |
| 3 | 1 | PCIF, SRC, PCI | SW PCI_STP Function 0=SW PCI_STP assert, 1= SW PCI_STP deassert When this bit is set to 0, all STOPPABLE PCI, PCIF and SRC outputs will be stopped in a synchronous manner with no short pulses. When this bit is set to 1, all STOPPED PCI, PCIF and SRC outputs will resume in a synchronous manner with no short pulses. |
| 2 | Externally selected | CPUT/C | FS_C Reflects the value of the FS_C pin sampled on power up 0 = FS_C was low during VTT_PWRGD# assertion |
| 1 | Externally selected | CPUT/C | FS_B Reflects the value of the FS_B pin sampled on power up 0 = FS_B was low during VTT_PWRGD# assertion |
| 0 | Externally selected | CPUT/C | FS_A Reflects the value of the FS_A pin sampled on power up 0 = FS_A was low during VTT_PWRGD# assertion |

Byte 7: Vendor ID

| Bit | @Pup | Name | Description |
|-----|------|---------------------|---------------------|
| 7 | 0 | Revision Code Bit 3 | Revision Code Bit 3 |
| 6 | 0 | Revision Code Bit 2 | Revision Code Bit 2 |
| 5 | 0 | Revision Code Bit 1 | Revision Code Bit 1 |
| 4 | 0 | Revision Code Bit 0 | Revision Code Bit 0 |
| 3 | 1 | Vendor ID Bit 3 | Vendor ID Bit 3 |
| 2 | 0 | Vendor ID Bit 2 | Vendor ID Bit 2 |
| 1 | 0 | Vendor ID Bit 1 | Vendor ID Bit 1 |
| 0 | 0 | Vendor ID Bit 0 | Vendor ID Bit 0 |

BYTE 8: CLKREQ Control Register

| Bit | @Pup | Name | Description |
|-----|------|----------|---|
| 7 | 0 | Reserved | Reserved |
| 6 | 1 | CLKREQ#B | SRC[T/C]5 CLKREQ#B control 1 = SRC[T/C]5 stoppable by CLKREQ#B pin 0 = SRC[T/C]5 not controlled by CLKREQ#B pin |
| 5 | 0 | CLKREQ#B | SRC[T/C]3 CLKREQ#B control 1 = SRC[T/C]3 stoppable by CLKREQ#B pin 0 = SRC[T/C]3 not controlled by CLKREQ#B pin |
| 4 | 0 | CLKREQ#B | SRC[T/C]1 CLKREQ#B control 1 = SRC[T/C]1 stoppable by CLKREQ#B pin 0 = SRC[T/C]1 not controlled by CLKREQ#B pin |
| 3 | 0 | Reserved | Reserved |
| 2 | 1 | CLKREQ#A | SRC[T/C]4 CLKREQ#A control 1 = SRC[T/C]4 stoppable by CLKREQ#A pin 0 = SRC[T/C]4 not controlled by CLKREQ#A pin |
| 1 | 0 | CLKREQ#A | SRC[T/C]2 CLKREQ#A control 1 = SRC[T/C]2 stoppable by CLKREQ#A pin 0 = SRC[T/C]2 not controlled by CLKREQ#A pin |
| 0 | 0 | CLKREQ#A | SRC[T/C]0 CLKREQ#A control 1 = SRC[T/C]0 stoppable by CLKREQ#A pin 0 = SRC[T/C]0 not controlled by CLKREQ#A pin |

Table 5. Crystal Recommendations

| Frequency (Fund) | Cut | Loading | Load Cap | Drive (max.) | Shunt Cap (max.) | Motional (max.) | Tolerance (max.) | Stability (max.) | Aging (max.) |
|------------------|-----|----------|----------|--------------|------------------|-----------------|------------------|------------------|--------------|
| 14.31818 MHz | AT | Parallel | 20 pF | 0.1 mW | 5 pF | 0.016 pF | 35 ppm | 30 ppm | 5 ppm |

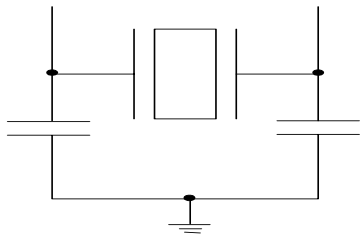
Crystal Recommendations

The CY28441 requires a Parallel Resonance Crystal. Substituting a series resonance crystal will cause the CY28441 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading. See *Table 5*.

Crystal Loading

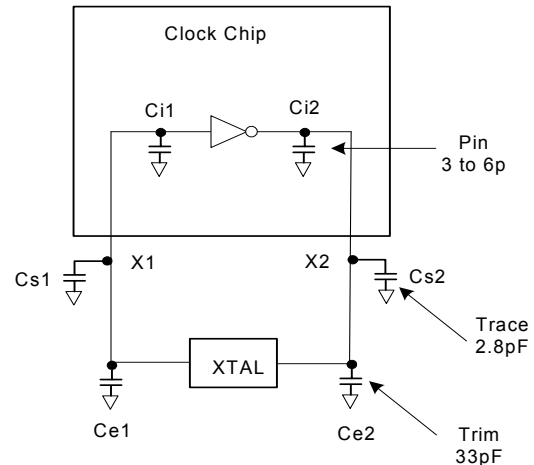
Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.


Figure 2. Crystal Loading Example

As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitance loading on both sides.

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

- CL.....Crystal load capacitance
- CLe.....Actual loading seen by crystal using standard value trim capacitors
- Ce.....External trim capacitors
- Cs.....Stray capacitance (terraced)
- Ci.....Internal capacitance (lead frame, bond wires etc.)

CLK_REQ[0:1]# Description

The CLKREQ#[A:B] signals are active LOW input used for clean enabling and disabling selected SRC outputs. The outputs controlled by CLKREQ#[A:B] are determined by the settings in register byte 8. The CLKREQ# signal is a de-bounced signal in that it's state must remain unchanged during two consecutive rising edges of DIFC to be recognized as a valid assertion or de-assertion. (The assertion and deassertion of this signal is absolutely asynchronous.)

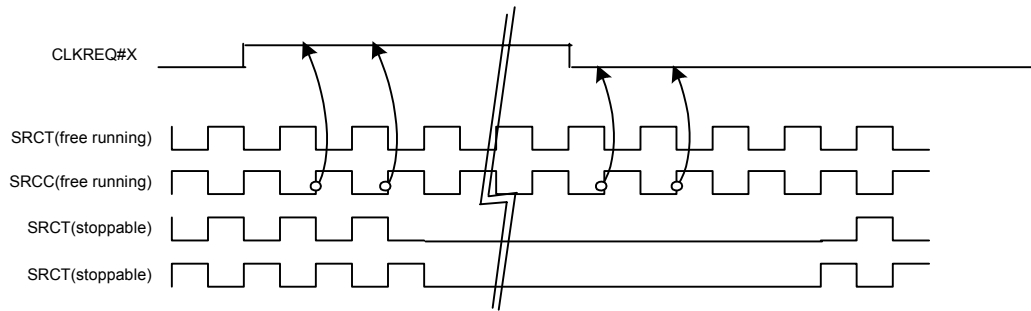


Figure 3. CLK_REQ#[A:B] Deassertion/Assertion Waveform

CLK_REQ#[A:B]# Assertion (CLKREQ# -> LOW)

All differential outputs that were stopped are to resume normal operation in a glitch free manner. The maximum latency from the assertion to active outputs is between 2-6 SRC clock periods (2 clocks are shown) with all SRC outputs resuming simultaneously. All stopped SRC outputs will be driven HIGH within 10 ns of CLKREQ#[1:0] deassertion to a voltage greater than 200 mV.

CLK_REQ#[A:B]# Deassertion (CLKREQ# -> HIGH)

The impact of deasserting the CLKREQ#[A:B] pins is all SRC outputs that are set in the control registers to stoppable via deassertion of CLKREQ#[A:B] are to be stopped after their next transition. The final state of all stopped DIF signals is LOW, both SRCT clock and SRCC clock outputs will not be driven.

PD (Power-down) Clarification

The VTT_PWRGD# /PD pin is a dual-function pin. During initial power-up, the pin functions as VTT_PWRGD#. Once VTT_PWRGD# has been sampled LOW by the clock chip, the pin assumes PD functionality. The PD pin is an asynchronous active HIGH input used to shut off all clocks cleanly prior to shutting off power to the device. This signal is synchronized

internal to the device prior to powering down the clock synthesizer. PD is also an asynchronous input for powering up the system. When PD is asserted HIGH, all clocks need to be driven to a LOW value and held prior to turning off the VCOs and the crystal oscillator.

PD (Power-down) – Assertion

When PD is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs will be held low on their next HIGH to LOW transition and differential clocks must held HIGH or Hi-Zd (depending on the state of the control register drive mode bit) on the next diff clock# HIGH to LOW transition within 4 clock periods. When the SMBus PD drive mode bit corresponding to the differential (CPU, SRC, and DOT) clock output of interest is programmed to '0', the clock output are held with "Diff clock" pin driven HIGH at 2 x Iref, and "Diff clock#" tristate. If the control register PD drive mode bit corresponding to the output of interest is programmed to "1", then both the "Diff clock" and the "Diff clock#" are tristate. Note *Figure 4* shows CPUC = 133 MHz and PD drive mode = '1' for all differential outputs. This diagram and description is applicable to valid CPU frequencies 100 and 133 MHz. In the event that PD mode is desired as the initial power-on state, PD must be asserted HIGH in less than 10 μs after asserting Vtt_PwrGd#.

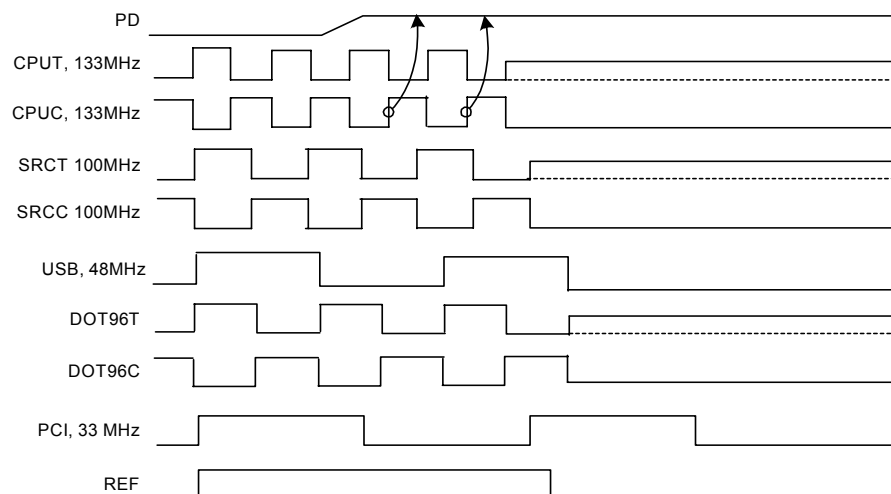


Figure 4. Power-down Assertion Timing Waveform

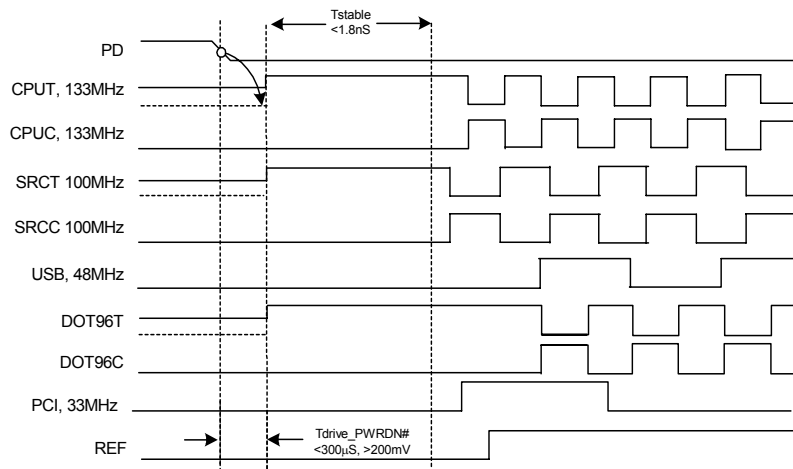


Figure 5. Power-down Deassertion Timing Waveform

PD Deassertion

The power-up latency is less than 1.8 ms. This is the time from the deassertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock chip. All differential outputs stopped in a three-state condition resulting from power down will be driven high in less than 300 μ s of PD deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs will be enabled within a few clock cycles of each other. *Figure 5* is an example showing the relationship of clocks coming up.

CPU_STP# Assertion

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable via assertion of CPU_STP# will be stopped within two–six CPU clock periods after being sampled by two rising edges of the internal CPUC clock. The final states of the stopped CPU signals are CPUT = HIGH and CPUC = LOW. There is no change to the output drive current values during the stopped state. The CPUT is driven HIGH with a current value equal to 6 x (Iref), and the CPUC signal will be Hi-Z.

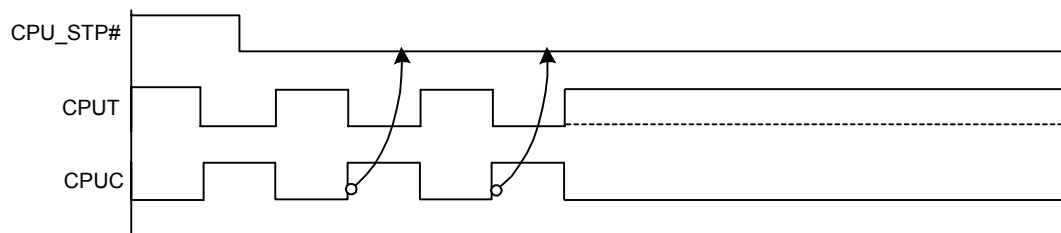


Figure 6. CPU_STP# Assertion Waveform

CPU_STP# Deassertion

The deassertion of the CPU_STP# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner. Synchronous manner meaning that no

short or stretched clock pulses will be produced when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.

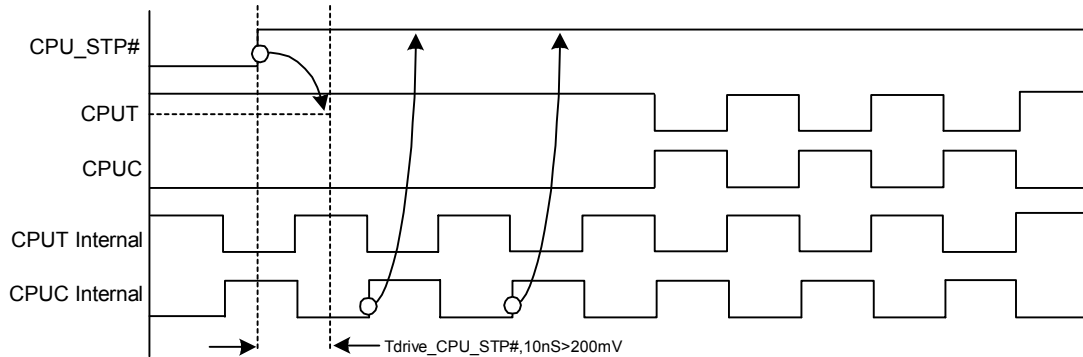


Figure 7. CPU_STP# Deassertion Waveform

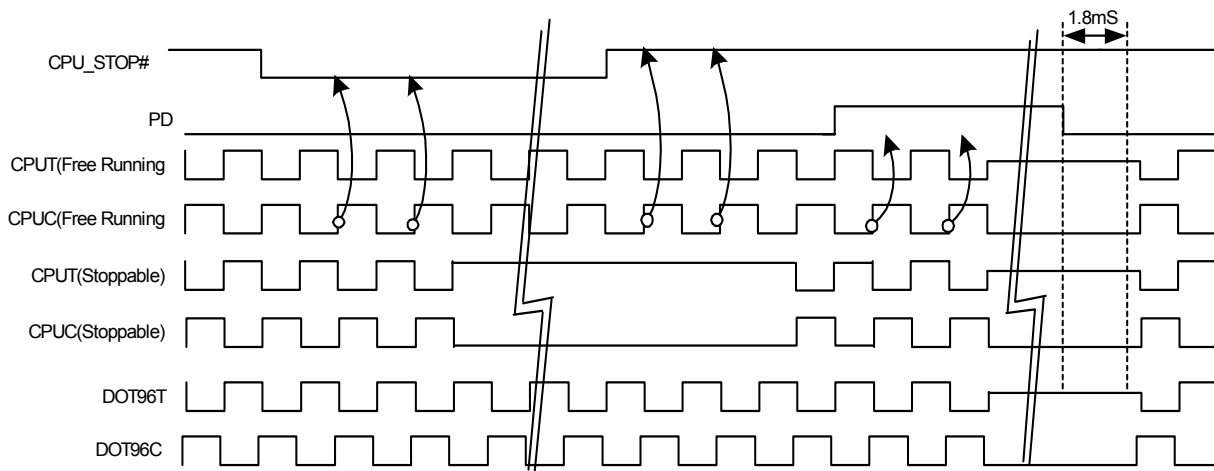


Figure 8. CPU_STP# = Driven, CPU_PD = Driven, DOT_PD = Driven

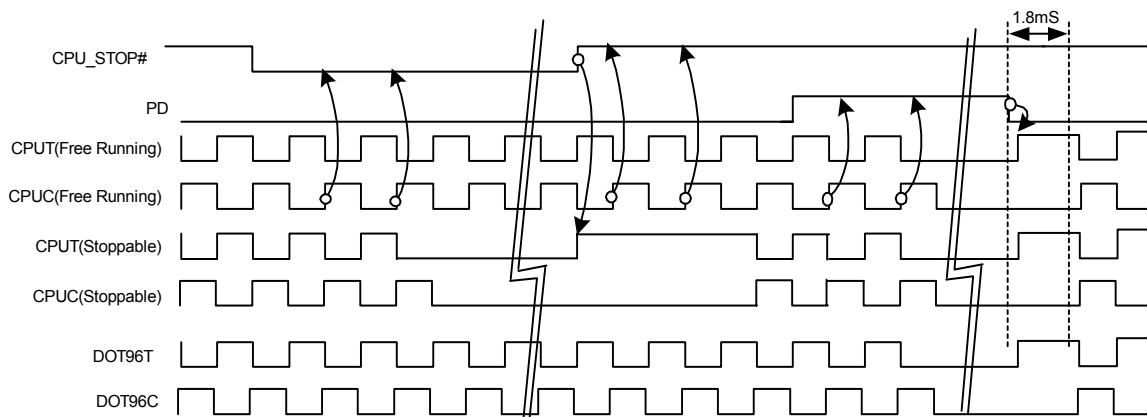


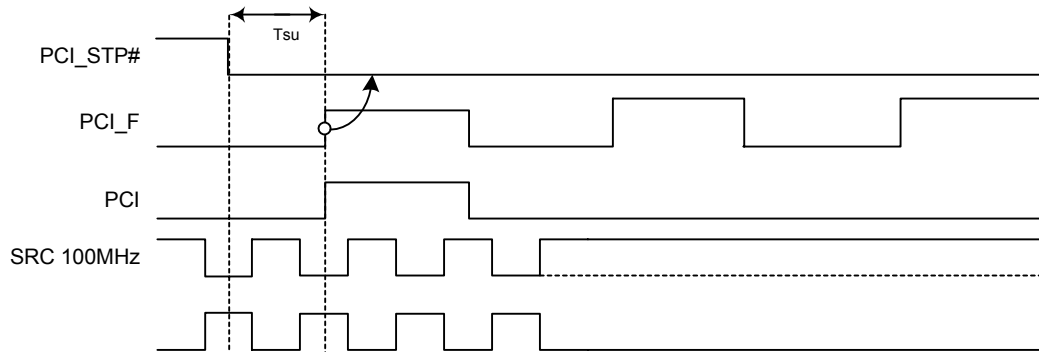
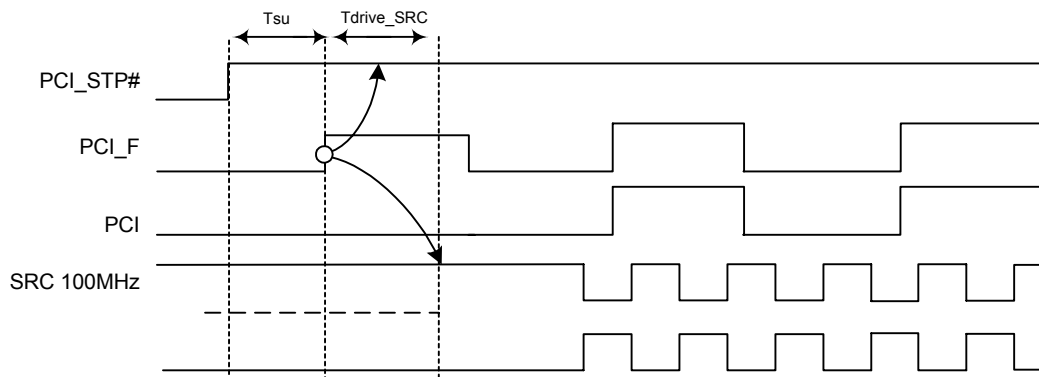
Figure 9. CPU_STP# = Hi-Z, CPU_PD = Hi-Z, DOT_PD = tHi-Z

PCI_STP# Assertion^[1]

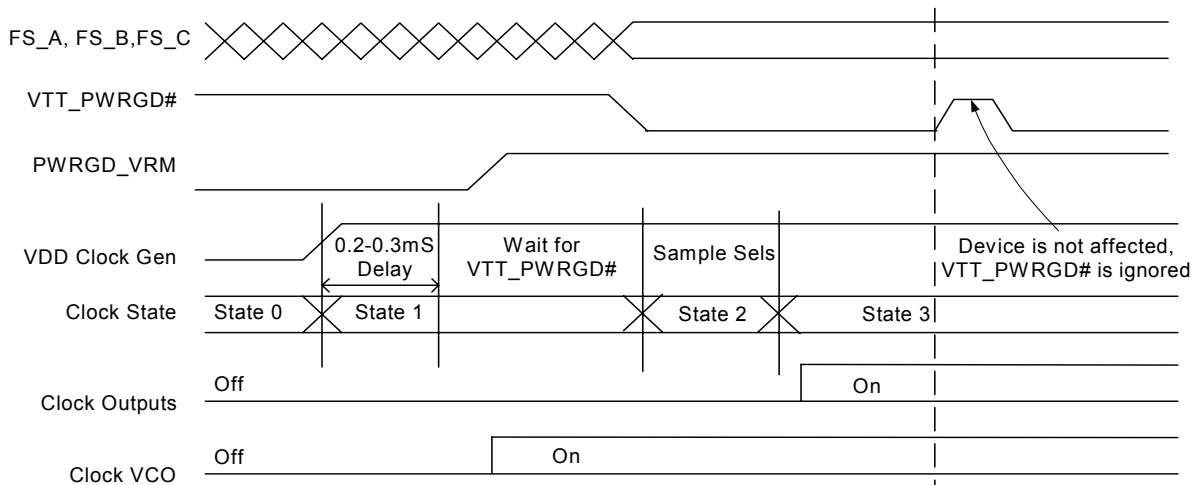
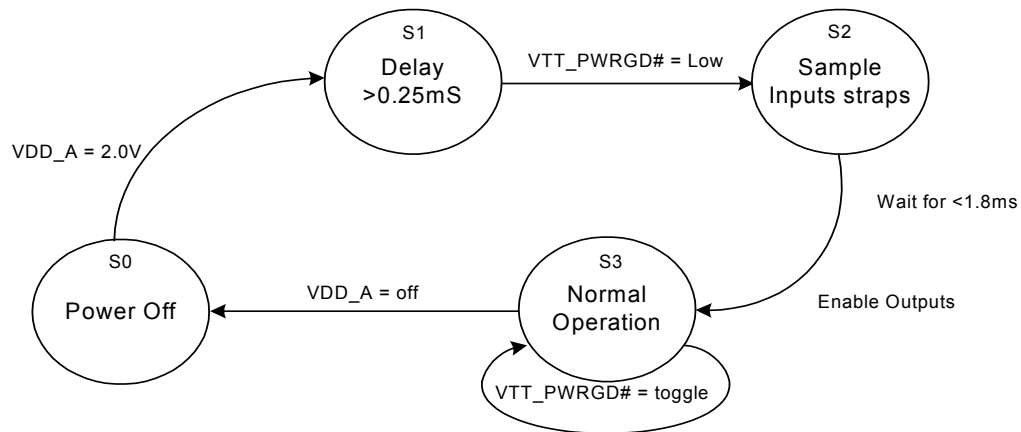
The PCI_STP# signal is an active LOW input used for synchronous stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI_STP# going LOW is 10 ns (t_{SU}). (See *Figure 10.*) The PCIF clocks will not be affected by this pin if their corresponding control bit in the SMBus register is set to allow them to be free running.

PCI_STP# Deassertion

The deassertion of the PCI_STP# signal will cause all PCI and stoppable PCIF clocks to resume running in a synchronous manner within two PCI clock periods after PCI_STP# transitions to a high level. (See *Figure 11.*)


Figure 10. PCI_STP# Assertion Waveform

Figure 11. PCI_STP# Deassertion Waveform
Note:

1. The PCI STOP function is controlled by two inputs. One is the device PCI_STP# pin number 55 and the other is SMBus byte6 bit 3. These two inputs are logically OR'ed. If either the external pin or the internal SMBus register bit is set LOW then the stoppable PCI clocks will be stopped in a logic LOW state.


Figure 12. VTT_PWRGD# Timing Diagram

Figure 13. Clock Generator Power-up/Run State Diagram

Absolute Maximum Conditions

| Parameter | Description | Condition | Min. | Max. | Unit |
|--------------------|-----------------------------------|-----------------------------|------|-----------------------|------|
| V _{DD} | Core Supply Voltage | | -0.5 | 4.6 | V |
| V _{DD_A} | Analog Supply Voltage | | -0.5 | 4.6 | V |
| V _{IN} | Input Voltage | Relative to V _{SS} | -0.5 | V _{DD} + 0.5 | VDC |
| T _S | Temperature, Storage | Non-functional | -65 | 150 | °C |
| T _A | Temperature, Operating Ambient | Functional | 0 | 85 | °C |
| T _J | Temperature, Junction | Functional | - | 150 | °C |
| ∅ _{JC} | Dissipation, Junction to Case | Mil-STD-883E Method 1012.1 | - | 39.56 | °C/W |
| ∅ _{JA} | Dissipation, Junction to Ambient | JEDEC (JESD 51) | - | 45.29 | °C/W |
| ESD _{HBM} | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015 | 2000 | - | V |
| UL-94 | Flammability Rating | At 1/8 in. | V-0 | | |
| MSL | Moisture Sensitivity Level | | 1 | | |

Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|--|-----------------------------------|--|-----------------------|-----------------------|------|
| V _{DD_A} , V _{DD_REF} , V _{DD_PCI} , V _{DD_3V66} , V _{DD_48} , V _{DD_CPU} | 3.3V Operating Voltage | 3.3 ± 5% | 3.135 | 3.465 | V |
| V _{IL2C} | Input Low Voltage | SDATA, SCLK | - | 1.0 | V |
| V _{IH2C} | Input High Voltage | SDATA, SCLK | 2.2 | - | V |
| V _{IL_FS} | FS_A/FS_B/FS_C Input Low Voltage | | V _{SS} - 0.3 | 0.35 | V |
| V _{IH_FS} | FS_A/FS_B/FS_C Input High Voltage | | 0.7 | V _{DD} + 0.5 | V |
| V _{IL} | 3.3V Input Low Voltage | | V _{SS} - 0.5 | 0.8 | V |
| V _{IH} | 3.3V Input High Voltage | | 2.0 | V _{DD} + 0.5 | V |
| I _{IL} | Input Low Leakage Current | Except internal pull-up resistors, 0 < V _{IN} < V _{DD} | -5 | - | μA |
| I _{IH} | Input High Leakage Current | Except internal pull-down resistors, 0 < V _{IN} < V _{DD} | - | 5 | μA |
| V _{OL} | 3.3V Output Low Voltage | I _{OL} = 1 mA | - | 0.4 | V |
| V _{OH} | 3.3V Output High Voltage | I _{OH} = -1 mA | 2.4 | - | V |
| I _{OZ} | High-impedance Output Current | | -10 | 10 | μA |
| C _{IN} | Input Pin Capacitance | | 2 | 5 | pF |
| C _{OUT} | Output Pin Capacitance | | 3 | 6 | pF |
| L _{IN} | Pin Inductance | | - | 7 | nH |
| V _{XIH} | Xin High Voltage | | 0.7V _{DD} | V _{DD} | V |
| V _{XIL} | Xin Low Voltage | | 0 | 0.3V _{DD} | V |
| I _{DD3.3V} | Dynamic Supply Current | At max. load and freq. per <i>Figure 15</i> | - | 380 | mA |
| I _{PD3.3V} | Power-down Supply Current | PD asserted, Outputs driven | - | 70 | mA |
| I _{PD3.3V} | Power-down Supply Current | PD asserted, Outputs Hi-Z | - | 2 | mA |

AC Electrical Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|---------------------------------|--|---|----------|-------------------------|------|
| Crystal | | | | | |
| T _{DC} | XIN Duty Cycle | The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification | 47.5 | 52.5 | % |
| T _{PERIOD} | XIN Period | When XIN is driven from an external clock source | 69.841 | 71.0 | ns |
| T _R / T _F | XIN Rise and Fall Times | Measured between 0.3V _{DD} and 0.7V _{DD} | – | 10.0 | ns |
| T _{CCJ} | XIN Cycle to Cycle Jitter | As an average over 1- μ s duration | – | 500 | ps |
| L _{ACC} | Long-term Accuracy | Over 150 ms | – | 300 | ppm |
| CPU at 0.7V | | | | | |
| T _{DC} | CPUT and CPUC Duty Cycle | Measured at crossing point V _{OX} | 45 | 55 | % |
| T _{PERIOD} | 100-MHz CPUT and CPUC Period | Measured at crossing point V _{OX} | 9.997001 | 10.00300 | ns |
| T _{PERIOD} | 133-MHz CPUT and CPUC Period | Measured at crossing point V _{OX} | 7.497751 | 7.502251 | ns |
| T _{PERIODSS} | 100-MHz CPUT and CPUC Period, SSC | Measured at crossing point V _{OX} | 9.997001 | 10.05327 | ns |
| T _{PERIODSS} | 133-MHz CPUT and CPUC Period, SSC | Measured at crossing point V _{OX} | 7.497751 | 7.539950 | ns |
| T _{PERIODAbs} | 100-MHz CPUT and CPUC Absolute Period | Measured at crossing point V _{OX} | 9.912001 | 10.08800 | ns |
| T _{PERIODAbs} | 133-MHz CPUT and CPUC Absolute Period | Measured at crossing point V _{OX} | 7.412751 | 7.587251 | ns |
| T _{PERIODSSAbs} | 100-MHz CPUT and CPUC Absolute Period, SSC | Measured at crossing point V _{OX} | 9.912001 | 10.13827 | ns |
| T _{PERIODSSAbs} | 133-MHz CPUT and CPUC Absolute Period, SSC | Measured at crossing point V _{OX} | 7.412751 | 7.624950 | ns |
| T _{CCJ} | CPUT/C Cycle to Cycle Jitter | Measured at crossing point V _{OX} | – | 125 | ps |
| T _{CCJ2} | CPU2_ITP Cycle to Cycle Jitter | Measured at crossing point V _{OX} | – | 125 | ps |
| T _{SKEW} | CPUT to CPUC Clock Skew | Measured at crossing point V _{OX} | – | 100 | ps |
| T _{SKEW2} | CPU2_ITP to CPU0 Clock Skew | Measured at crossing point V _{OX} | – | 150 | ps |
| T _R / T _F | CPUT and CPUC Rise and Fall Times | Measured from V _{OL} = 0.175 to V _{OH} = 0.525V | 175 | 700 | ps |
| T _{RFM} | Rise/Fall Matching | Determined as a fraction of $2 \cdot (T_R - T_F) / (T_R + T_F)$ | – | 20 | % |
| ΔT_R | Rise Time Variation | | – | 125 | ps |
| ΔT_F | Fall Time Variation | | – | 125 | ps |
| V _{HIGH} | Voltage High | Math averages <i>Figure 15</i> | 660 | 850 | mV |
| V _{LOW} | Voltage Low | Math averages <i>Figure 15</i> | –150 | – | mV |
| V _{OX} | Crossing Point Voltage at 0.7V Swing | | 250 | 550 | mV |
| V _{OVS} | Maximum Overshoot Voltage | | – | V _{HIGH} + 0.3 | V |
| V _{UDS} | Minimum Undershoot Voltage | | –0.3 | – | V |
| V _{RB} | Ring Back Voltage | See <i>Figure 15</i> . Measure SE | – | 0.2 | V |
| SRC | | | | | |
| T _{DC} | SRCT and SRCC Duty Cycle | Measured at crossing point V _{OX} | 45 | 55 | % |
| T _{PERIOD} | 100-MHz SRCT and SRCC Period | Measured at crossing point V _{OX} | 9.997001 | 10.00300 | ns |
| T _{PERIODSS} | 100-MHz SRCT and SRCC Period, SSC | Measured at crossing point V _{OX} | 9.997001 | 10.05327 | ns |
| T _{PERIODAbs} | 100-MHz SRCT and SRCC Absolute Period | Measured at crossing point V _{OX} | 10.12800 | 9.872001 | ns |
| T _{PERIODSSAbs} | 100-MHz SRCT and SRCC Absolute Period, SSC | Measured at crossing point V _{OX} | 9.872001 | 10.17827 | ns |

AC Electrical Specifications (continued)

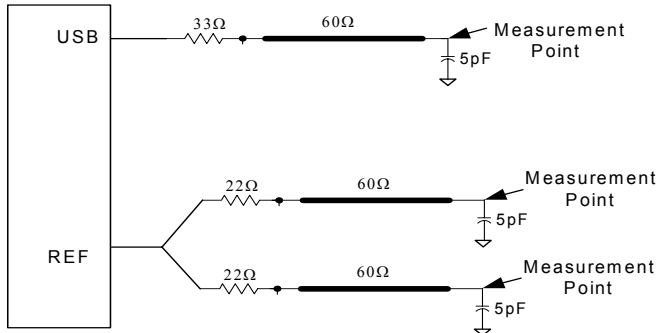
| Parameter | Description | Condition | Min. | Max. | Unit |
|---------------------------------|---------------------------------------|---|----------|-------------------------|------|
| T _{SKEW} | Any SRCT/C to SRCT/C Clock Skew | Measured at crossing point V _{OX} | – | 250 | ps |
| T _{CCJ} | SRCT/C Cycle to Cycle Jitter | Measured at crossing point V _{OX} | – | 125 | ps |
| L _{ACC} | SRCT/C Long Term Accuracy | Measured at crossing point V _{OX} | – | 300 | ppm |
| T _R / T _F | SRCT and SRCC Rise and Fall Times | Measured from V _{OL} = 0.175 to V _{OH} = 0.525V | 175 | 700 | ps |
| T _{RFM} | Rise/Fall Matching | Determined as a fraction of 2*(T _R – T _F)/(T _R + T _F) | – | 20 | % |
| ΔT _R | Rise Time Variation | | – | 125 | ps |
| ΔT _F | Fall Time Variation | | – | 125 | ps |
| V _{HIGH} | Voltage High | Math averages <i>Figure 15</i> | 660 | 850 | mV |
| V _{LOW} | Voltage Low | Math averages <i>Figure 15</i> | –150 | – | mV |
| V _{OX} | Crossing Point Voltage at 0.7V Swing | | 250 | 550 | mV |
| V _{OVS} | Maximum Overshoot Voltage | | – | V _{HIGH} + 0.3 | V |
| V _{UDS} | Minimum Undershoot Voltage | | –0.3 | – | V |
| V _{RB} | Ring Back Voltage | See <i>Figure 15</i> . Measure SE | – | 0.2 | V |
| PCI/PCIF | | | | | |
| T _{DC} | PCI Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| T _{PERIOD} | Spread Disabled PCIF/PCI Period | Measurement at 1.5V | 29.99100 | 30.00900 | ns |
| T _{PERIODSS} | Spread Enabled PCIF/PCI Period, SSC | Measurement at 1.5V | 29.9910 | 30.15980 | ns |
| T _{PERIODAbs} | Spread Disabled PCIF/PCI Period | Measurement at 1.5V | 29.49100 | 30.50900 | ns |
| T _{PERIODSSAbs} | Spread Enabled PCIF/PCI Period, SSC | Measurement at 1.5V | 29.49100 | 30.65980 | ns |
| T _{HIGH} | PCIF and PCI High Time | Measurement at 2.4V | 12.0 | – | ns |
| T _{LOW} | PCIF and PCI Low Time | Measurement at 0.4V | 12.0 | – | ns |
| T _R / T _F | PCIF and PCI Rise and Fall Times | Measured between 0.8V and 2.0V | 0.5 | 2.0 | ns |
| T _{SKEW} | Any PCI clock to Any PCI Clock Skew | Measurement at 1.5V | – | 500 | ps |
| T _{CCJ} | PCIF and PCI Cycle to Cycle Jitter | Measurement at 1.5V | – | 500 | ps |
| DOT | | | | | |
| T _{DC} | DOT96T and DOT96C Duty Cycle | Measured at crossing point V _{OX} | 45 | 55 | % |
| T _{PERIOD} | DOT96T and DOT96C Period | Measured at crossing point V _{OX} | 10.41354 | 10.41979 | ns |
| T _{PERIODAbs} | DOT96T and DOT96C Absolute Period | Measured at crossing point V _{OX} | 10.16354 | 10.66979 | ns |
| T _{CCJ} | DOT96T/C Cycle to Cycle Jitter | Measured at crossing point V _{OX} | – | 250 | ps |
| L _{ACC} | DOT96T/C Long Term Accuracy | Measured at crossing point V _{OX} | – | 300 | ppm |
| T _R / T _F | DOT96T and DOT96C Rise and Fall Times | Measured from V _{OL} = 0.175 to V _{OH} = 0.525V | 175 | 700 | ps |
| T _{RFM} | Rise/Fall Matching | Determined as a fraction of 2*(T _R – T _F)/(T _R + T _F) | – | 20 | % |
| ΔT _R | Rise Time Variation | | – | 125 | ps |
| ΔT _F | Fall Time Variation | | – | 125 | ps |
| V _{HIGH} | Voltage High | Math averages <i>Figure 15</i> | 660 | 850 | mV |
| V _{LOW} | Voltage Low | Math averages <i>Figure 15</i> | –150 | – | mV |
| V _{OX} | Crossing Point Voltage at 0.7V Swing | | 250 | 550 | mV |
| V _{OVS} | Maximum Overshoot Voltage | | – | V _{HIGH} + 0.3 | V |
| V _{UDS} | Minimum Undershoot Voltage | | –0.3 | – | V |
| V _{RB} | Ring Back Voltage | See <i>Figure 15</i> . Measure SE | – | 0.2 | V |

AC Electrical Specifications (continued)

| Parameter | Description | Condition | Min. | Max. | Unit |
|----------------------------------|-----------------------------------|--|----------|----------|------|
| T _{LTJ} | Long Term Jitter @ 10 μs | Measured at crossing point V _{OX} | | 1.1 | ns |
| USB | | | | | |
| T _{DC} | Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| T _{PERIOD} | Period | Measurement at 1.5V | 20.83125 | 20.83542 | ns |
| T _{PERIODAbs} | Absolute Period | Measurement at 1.5V | 20.48125 | 21.18542 | ns |
| T _{HIGH} | USB High Time | Measurement at 2.4V | 8.094 | 10.036 | ns |
| T _{LOW} | USB Low Time | Measurement at 0.4V | 7.694 | 9.836 | ns |
| T _R / T _F | Rise and Fall Times | Measured between 0.8V and 2.0V | 1.0 | 2.0 | ns |
| T _{CCJ} | Cycle to Cycle Jitter | Measurement at 1.5V | – | 350 | ps |
| REF | | | | | |
| T _{DC} | REF Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| T _{PERIOD} | REF Period | Measurement at 1.5V | 69.8203 | 69.8622 | ns |
| T _{PERIODAbs} | REF Absolute Period | Measurement at 1.5V | 68.82033 | 70.86224 | ns |
| T _R / T _F | REF Rise and Fall Times | Measured between 0.8V and 2.0V | 0.5 | 2.0 | V/ns |
| T _{CCJ} | REF Cycle to Cycle Jitter | Measurement at 1.5V | – | 1000 | ps |
| ENABLE/DISABLE and SET-UP | | | | | |
| T _{STABLE} | Clock Stabilization from Power-up | | – | 1.8 | ms |
| T _{SS} | Stopclock Set-up Time | | 10.0 | – | ns |
| T _{SH} | Stopclock Hold Time | | 0 | – | ns |

Test and Measurement Set-up

The following diagram shows the test load configurations for the single-ended USB, and REF output signals



For PCI Single-ended Signals and Reference

Figure 14 shows the test load configuration for single-ended PCI outputs.

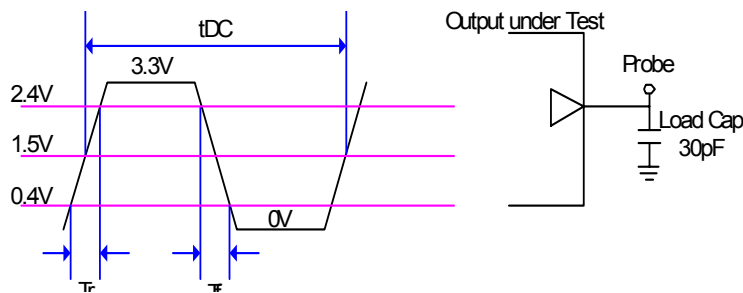


Figure 14. Single-ended Lumped Load Configuration for PCI Outputs

For Differential CPU, SRC and DOT96 Output Signals

Figure 15 shows the test load configuration for the differential CPU and SRC outputs.

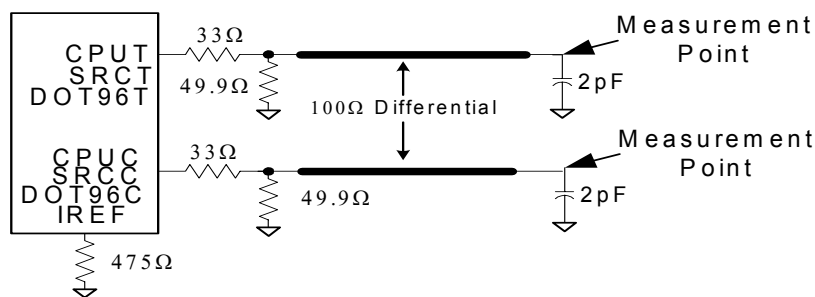


Figure 15. 0.7V Single-ended Load Configuration

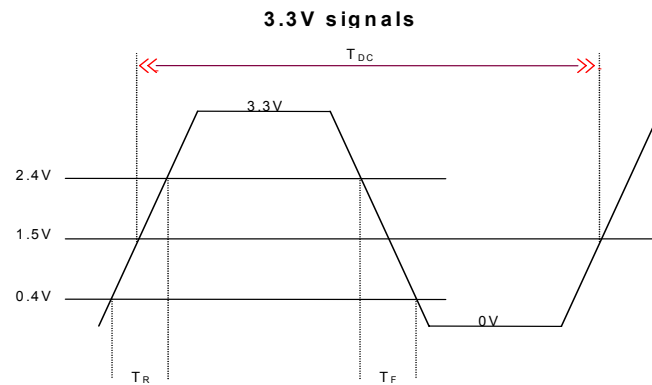


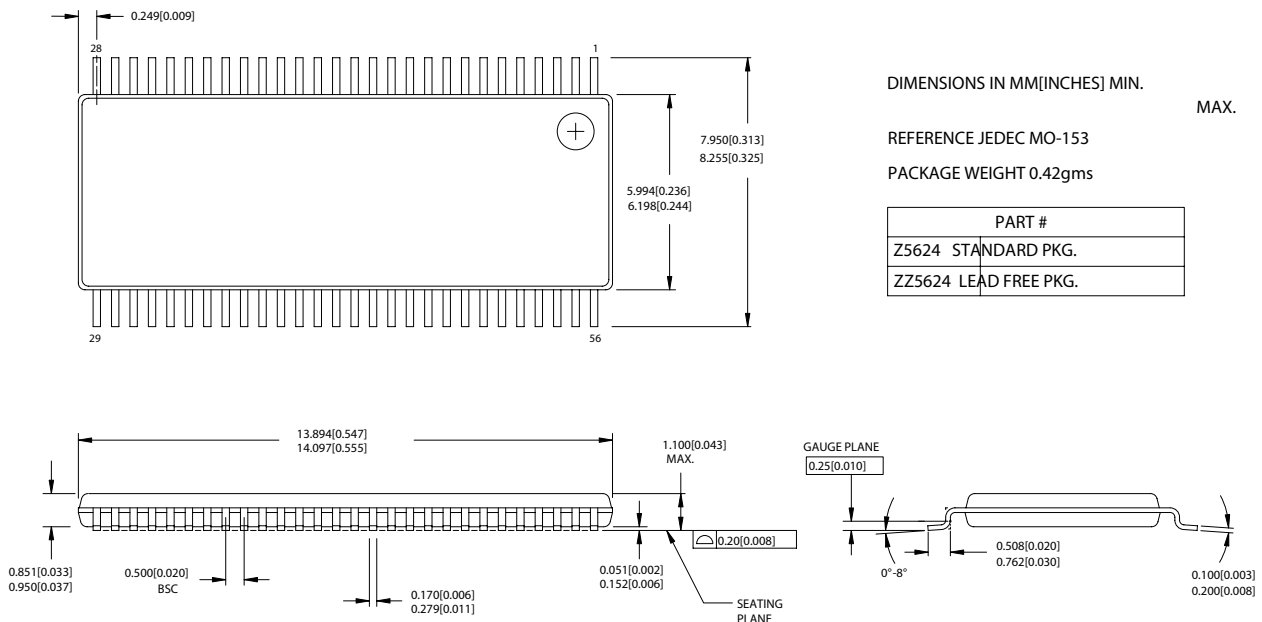
Figure 16. Single-ended Output Signals (for AC Parameters Measurement)

Ordering Information

| Part Number | Package Type | Product Flow |
|------------------|------------------------------|------------------------|
| Lead-free | | |
| CY28441ZXC | 56-pin TSSOP | Commercial, 0° to 85°C |
| CY28441ZXCT | 56-pin TSSOP – Tape and Reel | Commercial, 0° to 85°C |

Package Diagrams

56-Lead Thin Shrunk Small Outline Package, Type II (6 mm x 12 mm) Z56



51-85060-°C

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| ** | 237792 | See ECN | RGL/SDR | New Data Sheet |