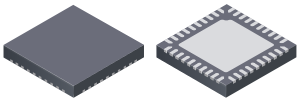
A5990

Quad DMOS Full-Bridge PWM Motor Driver

FEATURES AND BENEFITS

- 40 V output rating
- 4 full bridges
- Dual stepper motor driver
- High-current outputs
- Adaptive fast decay option
- Adjustable off-time
- 3.3 and 5 V compatible logic supply
- Synchronous rectification
- Internal undervoltage lockout (UVLO)
- Thermal shutdown circuitry
- Crossover-current protection
- Overcurrent protection
- Low-power sleep mode
- Low-profile QFN package

PACKAGES



Package EV, 40-pin QFN
0.90 mm nominal height
with exposed thermal pad

Not to scale

DESCRIPTION

The A5990 is a quad DMOS full-bridge driver capable of driving up to two stepper motors or four DC motors. Each full-bridge output is rated up to 1.6 A and 40 V. The A5990 includes fixed off-time pulse-width modulation (PWM) current regulators, along with 2- bit nonlinear DACs (digital-to-analog converters) that allow stepper motors to be controlled in full, half, and quarter steps, and DC motors in forward, reverse, and coast modes. The A5990 PWM current regulator features externally adjustable off-time to adapt the current control to supply voltage and motor parameters (each bridge pair can be adjusted independently). The A5990 also features an adaptive percent fast decay (APFD) option which automatically and continuously adjusts the fast decay portion of the off-time to provide increased step accuracy, lower current ripple, and reduced power dissipation in many conditions. Alternatively, the A5990 can be set to use the Allegro™ patented mixed decay mode, found on the A5988 and A5989, which provides reduced audible motor noise, increased step accuracy, and reduced power dissipation, when compared to a fixed decay mode.

Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation.

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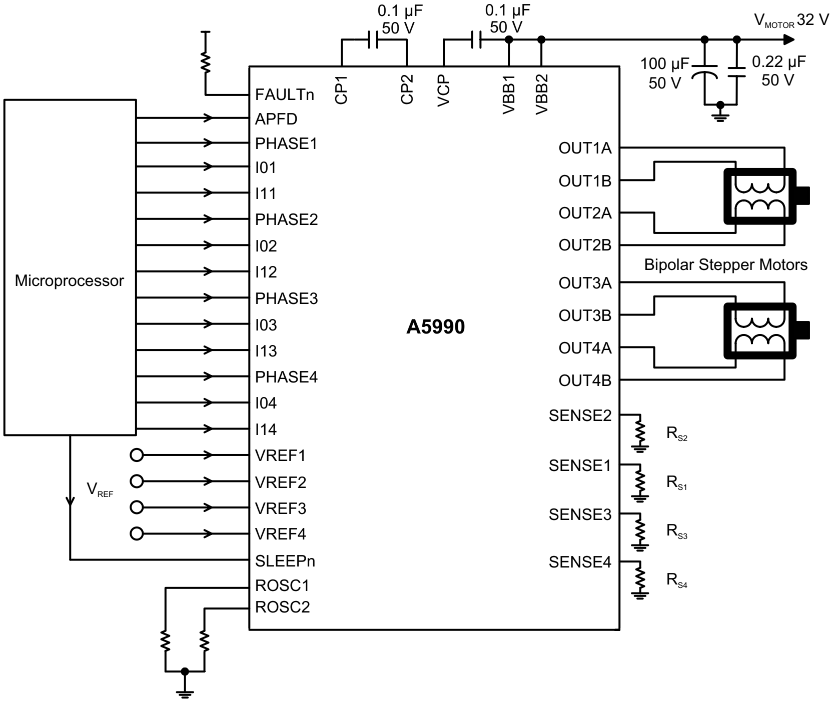


Figure 1: Typical Application Circuit

DESCRIPTION (continued)

Protection features include thermal shutdown with hysteresis, undervoltage lockout (UVLO) and crossover-current protection. Special power-up sequencing is not required.

The A5990 is supplied in the EV package, a 6 mm × 6 mm 40-pin QFN package with a nominal overall package height of 0.90 mm. The packages is lead (Pb) free, with 100% matte-tin leadframe plating.

SELECTION GUIDE

Part Number	Package	Packing
A5990GEVSR-T	40-pin QFN with exposed thermal pad	6000 pieces per reel

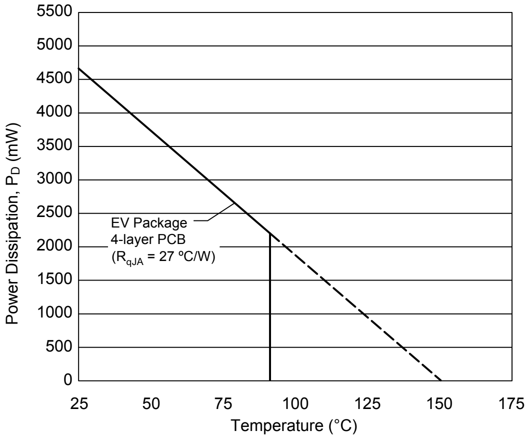
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		–0.5 to 40	V
Output Current	I_{OUT}	May be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a Junction Temperature of 150°C.	1.6	A
Logic Input Voltage Range	V_{IN}		–0.3 to 7	V
SENSE*x* Pin Voltage	V_{SENSEx}		0.5	V
		Pulsed $t_w < 1$ μs	2.5	V
VREF*x* Pin Voltage	V_{REFx}		2.5	V
Operating Temperature Range	T_A	Range G	–40 to 105	°C
Junction Temperature	T_J(max)		150	°C
Storage Temperature Range	T_{stg}		–40 to 125	°C

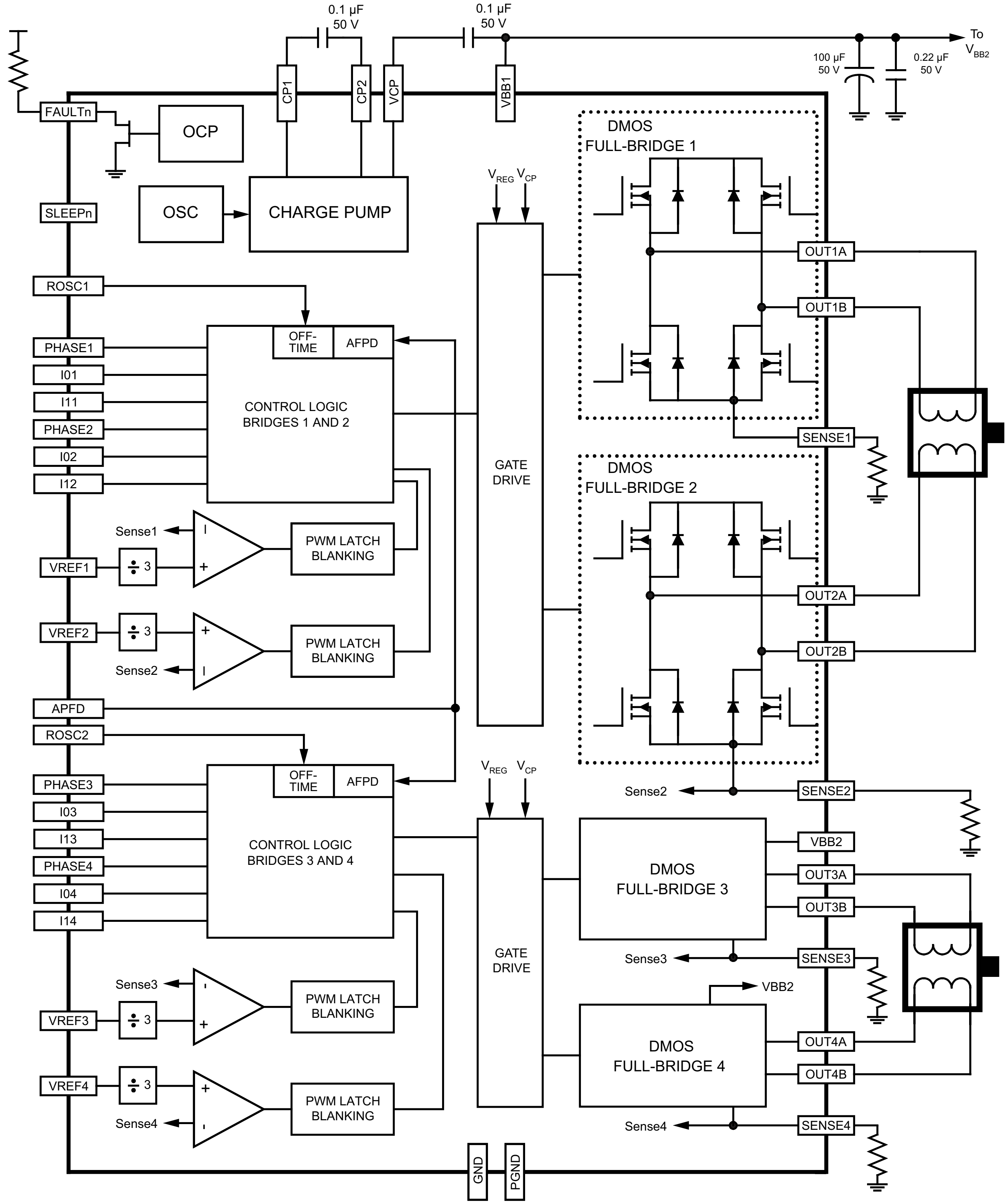
THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	EV package, 4-layer PCB based on JEDEC standard	27	°C/W

Power Dissipation versus Ambient Temperature



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS [1]**: Valid at T_A = 25°C, V_{BB} = 40 V, unless otherwise noted**

Characteristics	Symbol	Test Conditions	Min.	Typ. [2]	Max.	Units
Load Supply Voltage Range	V_{BB}	Operating	8	–	40	V
Output On Resistance	$R_{DS(on)}$	Source driver, I_{OUT} = –1.2 A, T_J = 25°C	–	500	600	mΩ
		Sink driver, I_{OUT} = 1.2 A, T_J = 25°C	–	500	600	mΩ
V_f, Outputs		I_{OUT} = 1.2 A	–	–	1.2	V
Output Leakage	I_{DSS}	Outputs, V_{OUT} = 0 to V_{BB}	–20	–	20	μA
VBB Supply Current	I_{BB}	I_{OUT} = 0 mA, outputs on, PWM = 50 kHz, DC = 50%	–	–	25	mA
		Outputs off	–	14.7	18	mA
		Sleep mode	–10	<1	10	μA
Output Driver Slew Rate	SR_{OUT}	10% to 90%	50	100	150	ns
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		2	–	–	V
	$V_{IN(0)}$		–	–	0.8	V
Logic Input Current	I_{IN}	Except APFD, V_{IN} = 0 to 5 V	–20	<1	20	μA
		APFD, V_{IN} = 0 V	–72	–55	–38	μA
		APFD, V_{IN} = 5 V	–	0	–	μA
Logic Input Hysteresis	V_{hys}		150	300	500	mV
Sleep Rising Threshold			2.5	2.7	2.95	V
Sleep Falling Threshold			–	2.4	–	V
Sleep Hysteresis			250	325	450	mV
Sleep Input Current			–	100	150	μA
Crossover Delay	t_{COD}		250	425	1000	ns
Blank Time	t_{BLANK}		0.7	1	1.3	μs
VREF*x* Pin Input Voltage Range	V_{REFx}	Operating	0.0	–	1.5	V
VREF*x* Pin Reference Input Current	I_{REF}	V_{REF} = 1.5	–	–	±1	μA
Current Trip-Level Error [3]	V_{ERR}	V_{REF} = 1.5, phase current = 100%	–5	–	5	%
		V_{REF} = 1.5, phase current = 67%	–5	–	5	%
		V_{REF} = 1.5, phase current = 33%	–15	–	15	%
Protection Circuits						
VBB UVLO Threshold	$V_{UV(VBB)}$	V_{BB} rising	7.3	7.6	7.9	V
VBB Hysteresis	$V_{UV(VBB)hys}$		400	500	600	mV
Overcurrent Protection Threshold			1.6	–	–	A
Fault Output Voltage		I_{OUT} = 1 mA	–	–	0.5	V
Fault Output Leakage Current		No fault, V_{OUT} = 5 V	–	–	1	μA
Thermal Shutdown Temperature	T_{JTSD}		155	165	175	°C
Thermal Shutdown Hysteresis	$T_{JTSDhys}$		–	15	–	°C

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

[2] Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

[3] $V_{ERR} = [(V_{REF}/3) – V_{SENSE}] / (V_{REF}/3)$.

FUNCTIONAL DESCRIPTION

Device Operation. The A5990 is designed to operate two stepper motors, four DC motors, or one stepper and two DC motors. The currents in each of the output full bridges, all N-channel DMOS, are regulated with fixed off-time pulse-width-modulated (PWM) control circuitry. Each full-bridge peak current is set by the value of an external current sense resistor, R_{Sx}, and a reference voltage, V_{REFx}.

If the logic inputs are pulled up to V_{DD}, it is good practice to use a high-value pull-up resistor to limit current to the logic inputs, should an overvoltage event occur. Logic inputs include: PHASE*x*, I0*x*, and I1*x*.

Internal PWM Current Control. Each full-bridge is controlled by a fixed off-time PWM current control circuit that limits the load current to a desired value, I_{TRIP}. Initially, a diagonal pair of source and sink DMOS outputs are enabled, and current flows through the motor winding and R_{Sx}. When the voltage across the current sense resistor equals the voltage on the VREF*x* pin, the current sense comparator resets the PWM latch, which turns off the source driver.

The maximum value of current limiting is set by the selection of R_S and voltage at the VREF input with a transconductance function, approximated by:

$$I_{TripMax} = V_{REF} / (3 \times R_S)$$

Each current step is a percentage of the maximum current, $I_{TripMax}$. The actual current at each step I_{Trip} is approximated by:

$$I_{Trip} = (\%\ I_{TripMax} / 100) \times I_{TripMax}$$

where % $I_{TripMax}$ is given in the Step Sequencing table.

Note: It is critical to ensure that the maximum rating of ±500 mV on each SENSE*x* pin is not exceeded.

Adaptive Percent Fast-Decay (APFD). The APFD terminal is a logic input used to control the APFD feature. When left floating or tied high, APFD is disabled, and the decay mode is set to fast-decay for 30.1% of the off-time. When tied low, APFD is enabled, and the percent fast-decay is automatically continuously adjusted to the lowest level needed to regulate the winding current at its target level while providing minimal current ripple.

Fixed Off-Time. The internal PWM current control circuitry uses a one-shot circuit to control the time the drivers remain off. The off-time (t_{off}) is set by the ROSCx inputs and is set independently for each bridge pair. If ROSCx is tied to GND, the off-time is set to 8.1 µs. If ROSCx is biased to greater than 3 V, the off-time is set to 30 µs. If ROSC is connected to GND with a resistor, the off-time is set to approximately:

$$t_{off}\ (seconds) = ROSC / 820\ (\mu s)\ .$$

Blanking. This function blanks the output of the current sense comparator when the outputs are switched by the internal current control circuitry. The comparator output is blanked to prevent false detections of overcurrent conditions due to reverse recovery currents of the clamp diodes, or to switching transients related to the capacitance of the load. The stepper blank time, t_{BLANK}, is approximately 1 µs.

Control Logic. Communication is implemented via the industry standard I1, I0, and PHASE interface. This communication logic allows for full, half, and quarter step modes. Each bridge also has an independent V_{REF} input, so higher resolution step modes can be programmed by dynamically changing the voltage on the VREF*x* pins.

Charge Pump (CP1 and CP2). The charge pump is used to generate a gate supply greater than V_{BB} to drive the source-side DMOS gates. A 0.1 µF ceramic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1 µF ceramic capacitor is required between VCP and VBB*x* to act as a reservoir to operate the high-side DMOS devices.

Shutdown. In the event of a fault (excessive junction temperature, or low voltage on VCP), the outputs of the device are disabled until the fault condition is removed. At power-up, the undervoltage lockout (UVLO) circuit disables the drivers.

Synchronous Rectification

When a PWM-off cycle is triggered by an internal fixed off-time cycle, load current will recirculate. The A5990 synchronous rectification feature will turn on the appropriate MOSFETs during the current decay, and effectively short out the body diodes with the low $R_{DS(on)}$ driver. This significantly lowers power dissipation. When a zero current level is detected, synchronous rectification is turned off to prevent reversal of the load current.

Mixed Decay Operation

The bridges operate in mixed decay mode. Referring to Figure 2, as the trip point is reached, the device goes into fast decay mode for 30.1% of the fixed off-time period. After this fast decay portion, t_{FD}, the device switches to slow decay mode for the remainder of the off-time. During transitions from fast decay to slow decay, the drivers are forced off for approximately 600 ns. This feature is added to prevent shoot-through in the bridge. As shown in Figure 2, during this "dead time" portion, synchronous rectification is not active, and the device operates in fast decay and slow decay only.

Sleep Mode

To minimize power consumption when not in use, the A5990 can be put into Sleep Mode by bringing the SLEEPn pin low. Sleep Mode disables much of the internal circuitry, including the charge pump.

Overcurrent Protection

An overcurrent monitor protects the A5990 from damage due to output shorts. If a short is detected, the A5990 latches the fault and disables the outputs. The latched fault can only be cleared by cycling the power to VBB or by putting the device in Sleep Mode. During OCP events, Absolute Maximum Ratings may be exceeded for a short period of time before outputs are latched off.

Fault Output

The open-drain fault output is pulled low when an overcurrent protection event occurs and the outputs are latched off.

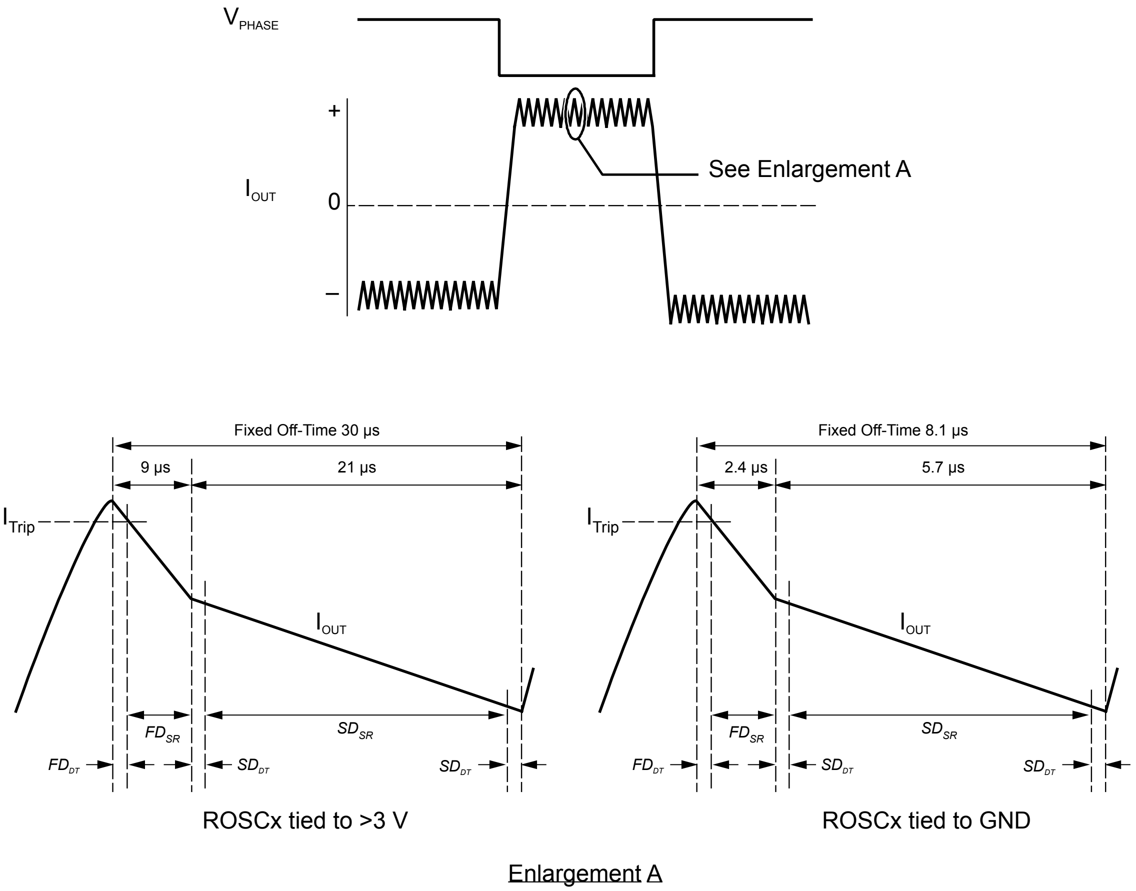


Figure 2: Mixed Decay Mode Operation

STEP SEQUENCING DIAGRAMS

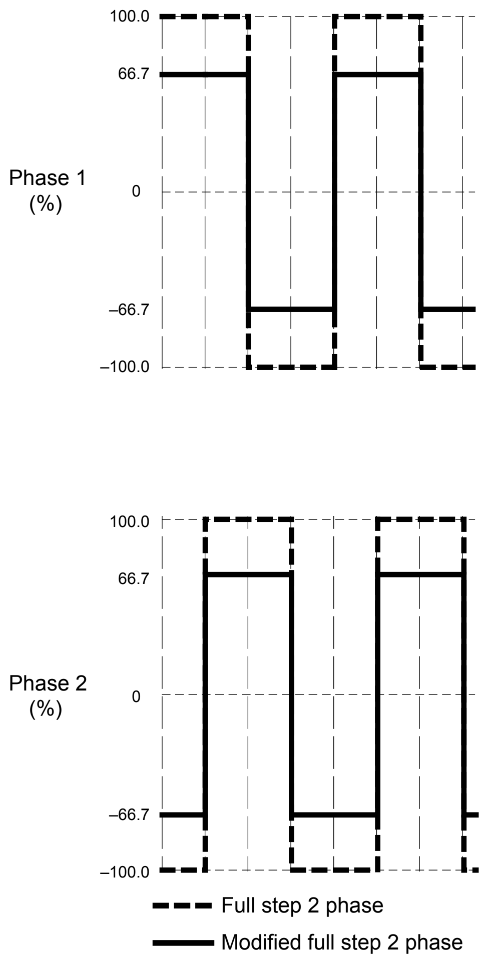


Figure 3: Step Sequencing for Full-Step Increments

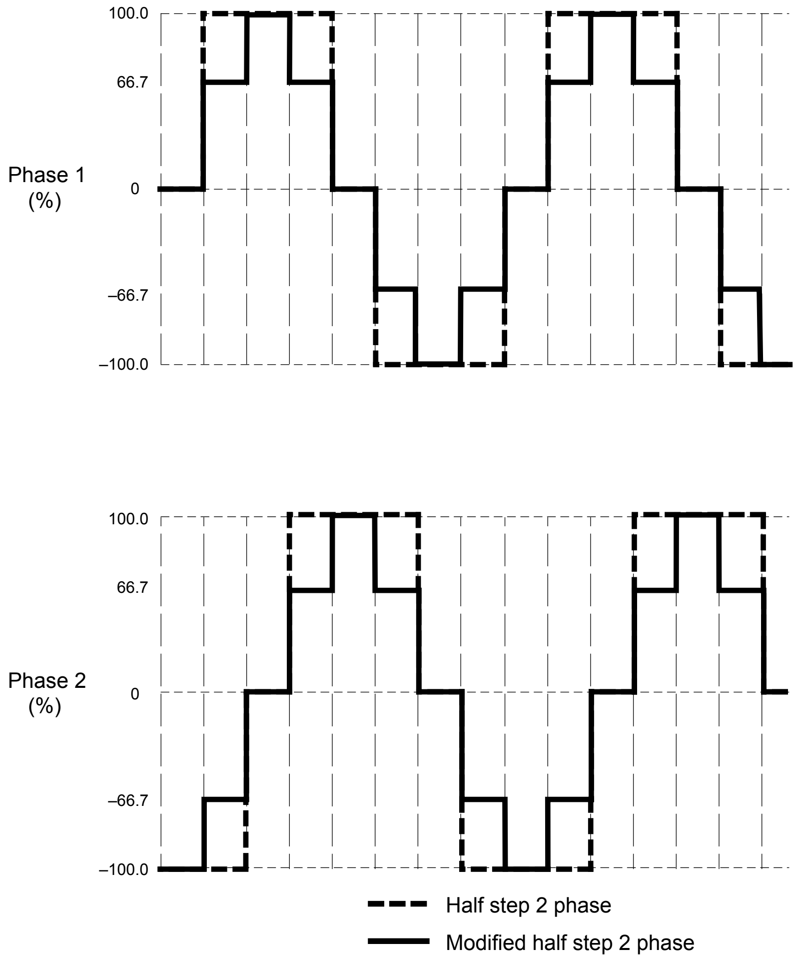


Figure 4: Step Sequencing for Half-Step Increments

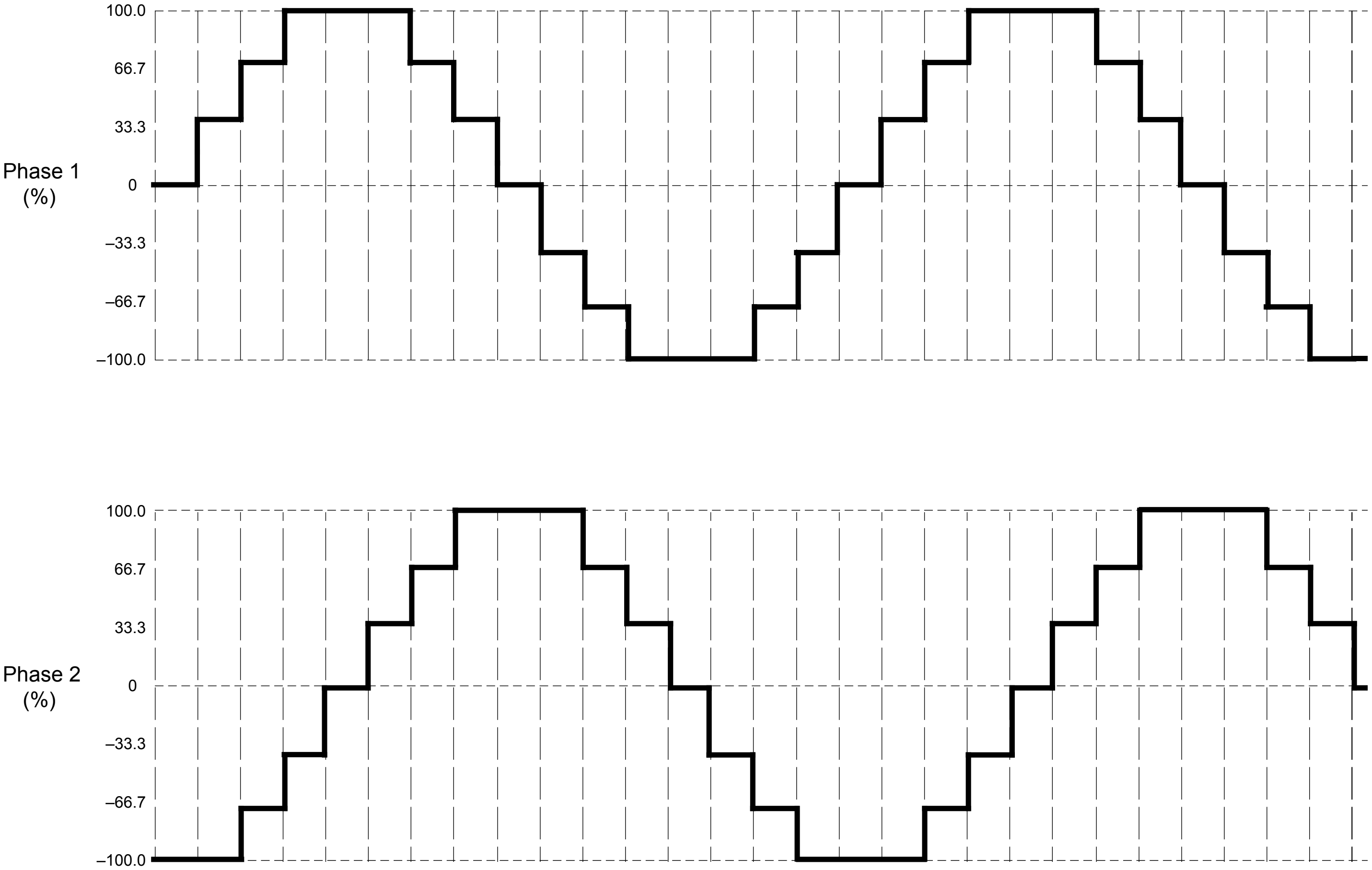


Figure 5: Step Sequence for Quarter-Step Increments

Table 1: Step Sequencing Settings

Full	1/2	1/4	Phase 1 (%$I_{TripMax}$)	I0x	I1x	PHASE	Phase 2 (%$I_{TripMax}$)	I0x	I1x	PHASE
	1	1	0	H	H	x	100	L	L	0
		2	33	L	H	1	100	L	L	0
1	2	3	100/66*	L/H*	L	1	100/66*	L/H*	L	0
		4	100	L	L	1	33	L	H	0
	3	5	100	L	L	1	0	H	H	x
		6	100	L	L	1	33	L	H	1
2	4	7	100/66*	L/H*	L	1	100/66*	L/H*	L	1
		8	33	L	H	1	100	L	L	1
	5	9	0	H	H	x	100	L	L	1
		10	33	L	H	0	100	L	L	1
3	6	11	100/66*	L/H*	L	0	100/66*	L/H*	L	1
		12	100	L	L	0	33	L	H	1
	7	13	100	L	L	0	0	H	H	x
		14	100	L	L	0	33	L	H	0
4	8	15	100/66*	L/H*	L	0	100/66*	L/H*	L	0
		16	33	L	H	0	100	L	L	0

* Denotes modified step mode.

For the APFD feature to operate properly, the A5990 allows for 100 ns jitter between the inputs. Specifically, do not set both I0x = H and I1x = H for longer than 100 ns between states, unless the state is being changed to I0x = H and I1x = H.

APPLICATIONS INFORMATION

DC Motor Control Each of the 4 full bridges has independent PWM current control circuitry that makes the A5990 capable of driving up to four DC motors at currents up to 1.2 A. Control of the DC motors is accomplished by tying the I0*x* and I1*x* pins together, creating an equivalent ENABLE function with maximum current defined by the voltage on the corresponding VREF pin. The DC motors can be driven via a PWM signal on this enable signal, or on the corresponding PHASE pin. Motor control includes forward, reverse, and coast.

Layout The printed circuit board should use a heavy groundplane. For optimum electrical and thermal performance, the A5990 must be soldered directly onto the board. On the underside of the A5990 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

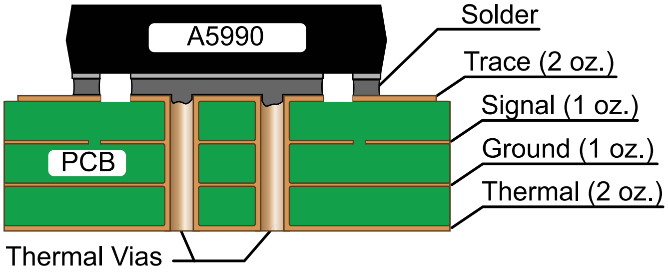
Grounding In order to minimize the effects of ground bounce and offset issues, it is important to have a low-impedance single-point ground, known as a *star ground*, located very close to the device. By making the connection between the exposed thermal pad and the groundplane directly under the A5990, that area becomes an ideal location for a star ground point.

A low-impedance ground will prevent ground bounce during high-current operation and ensure that the supply voltage remains stable at the input terminal. The recommended PCB layout shown in the diagram below illustrates how to create a star ground under the device to serve both as low-impedance ground point and thermal path.

The two input capacitors should be placed in parallel and as close to the device supply pins as possible. The ceramic capacitor should be closer to the pins than the bulk capacitor. This is necessary because the ceramic capacitor will be responsible for delivering the high-frequency current components.

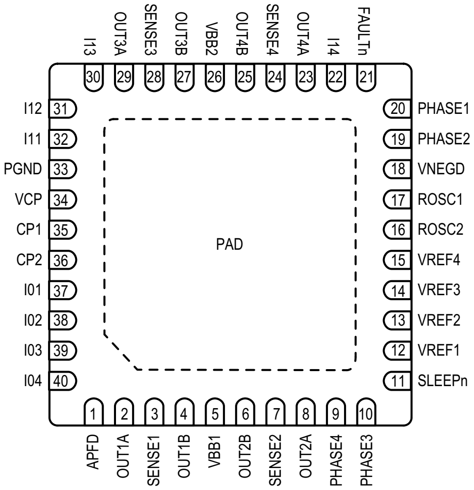
Sense Pins The sense resistors, RS*x*, should have a very low impedance path to ground, because they must carry a large current while supporting very accurate voltage measurements by the current sense comparators. Long ground traces will cause additional voltage drops, adversely affecting the ability of the comparators to accurately measure the current in the windings. The SENSE*x* pins have very short traces to the RS*x* resistors and very thick, low-impedance traces directly to the star ground beneath the device. If possible, there should be no other components on the sense circuits.

Note: When selecting a value for the sense resistors, be sure not to exceed the maximum voltage on the SENSE*x* pins of ±500 mV.



PINOUT DIAGRAM AND TERMINAL LIST TABLE

Package EV



Package not to scale

Terminal List Table

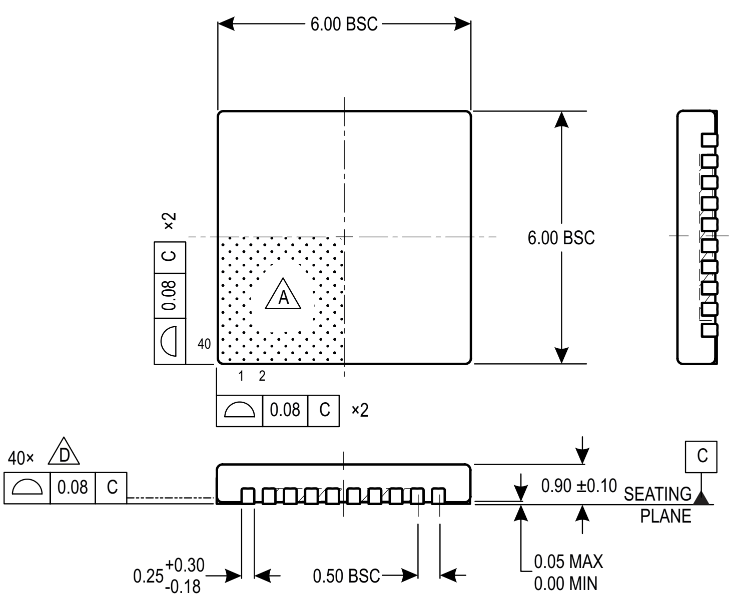
Number	Pin Name	Pin Description
1	APFD	Adaptive Percent Fast-Decay Input
2	OUT1A	DMOS Full-Bridge 1 Output A
3	SENSE1	Sense Resistor Terminal for Bridge 1
4	OUT1B	DMOS Full-Bridge 1 Output B
5	VBB1	Load Supply Voltage
6	OUT2B	DMOS Full-Bridge 2 Output B
7	SENSE2	Sense Resistor Terminal for Bridge 2
8	OUT2A	DMOS Full-Bridge 2 Output A
9	PHASE4	Control Input
10	PHASE3	Control Input
11	SLEEPn	Active Low Sleep Mode Input
12	VREF1	Analog Input
13	VREF2	Analog Input
14	VREF3	Analog Input
15	VREF4	Analog Input
16	ROSC2	Off-Time Input for Bridges 3 and 4
17	ROSC1	Off-Time Input for Bridges 1 and 2
18	GND*	Analog and Digital Ground
19	PHASE2	Control Input
20	PHASE1	Control Input
21	FAULTn	Open Drain Fault Output
22	I14	Control Input
23	OUT4A	DMOS Full-Bridge 4 Output A
24	SENSE4	Sense Resistor Terminal for Bridge 4
25	OUT4B	DMOS Full-Bridge 4 Output B
26	VBB2	Load Supply Voltage
27	OUT3B	DMOS Full-Bridge 3 Output B
28	SENSE3	Sense Resistor Terminal for Bridge 3
29	OUT3A	MOS Full-Bridge 3 Output A
30	I13	Control Input
31	I12	Control Input
32	I11	Control Input
33	PGND*	Power Ground
34	VCP	Reservoir Capacitor Terminal
35	CP1	Charge Pump Capacitor Terminal
36	CP2	Charge Pump Capacitor Terminal
37	I01	Control Input
38	I02	Control Input
39	I03	Control Input
40	I04	Control Input
–	PAD*	Exposed pad for enhanced thermal performance. Should be soldered to the PCB.

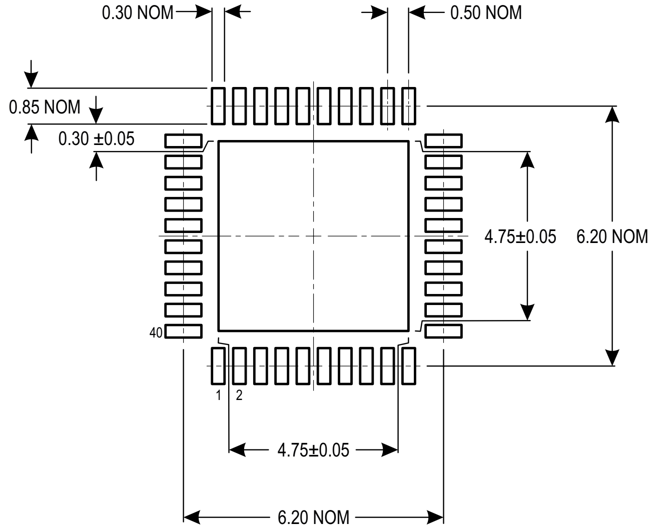
* GND, PGND, and thermal pad must be connected together externally under the device.

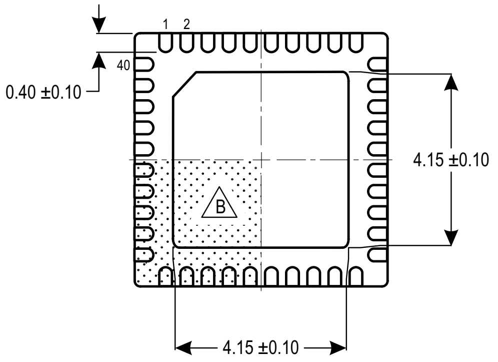
EV PACKAGE, 40-TERMINAL QFN WITH EXPOSED THERMAL PAD

For Reference Only – Not for Tooling Use

(Reference DWG-0000378, Rev. 3)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown







A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P600X600X100-41V5M); adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Revision History

Number	Date	Description
–	March 8, 2017	Initial release
1	November 15, 2018	Corrected Fixed Off-Time functional description (page 5)
2	December 6, 2019	Minor editorial updates
3	January 20, 2021	Updated Package Outline Drawing reference number (page 11)
4	January 31, 2022	Updated Package Outline Drawing (page 11)

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