ON Semiconductor®

AMIS-52150

Low-Power Transceiver with Clock and Data Recovery

1.0 Introduction

The AMIS-52150 is a cost-effective, ultra-low power single-chip wireless transceiver. It combines the proven Amplitude Shift Key/On-Off Key (ASK/OOK) modulation technology of the AMIS-52050 with data clock recovery.

Based on key features, such as dual independent receive channels, Quick Start crystal oscillator, Sniff Mode™ signal acquisition, and data clock recovery, the AMIS-52150 is ideally suited for a wide range of applications, including point-to-point wireless data links, cost-optimized wireless monitor solutions, and very low power remote wireless sensors, among others.

2.0 Key Features

- Data clock recovery
- Auto slicing of data
- Very low-power single-chip transceiver
- Minimal external components
- Low-power RC oscillator
- Quick Start crystal oscillator
- Ultra-low power RF Sniff Mode™, with wake-up on RSSI
- Internal trim functions reduce external component requirements
- I^2C control interface
- Serial TX/RX data port
- Clock generation for an external microprocessor
- Wake-up on RSSI
- Antenna diversity dual receiver
- Internal VCO/PLL tuning varactor
- Wake-up interrupt to external controller

May 2008 – Rev. 7

Publication Order Number:
AMIS52150/D

3.0 Technical Features

- Operating frequency range:
    - Quick Start, from 350MHz to 448MHz
    - Non-Quick Start, from 300MHz to 768MHz
- TX output power: +12dBm
- RX sensitivity:
    - Sniff Mode: -93dBm minimum
    - Receive: -117dBm minimum @ 1Kbps, with CDR
- Data rate:
    - 1-8Kbps with Manchester Coding
    - 1-16Kbps with NRZ data
- Power requirements:
    - Receive: 7.5mA (Continuous)
    - Transmit: 25mA @ full power (50 percent duty-cycle)
    - Sniff Mode: 75uA (One percent duty-cycle)
    - Standby: 500nA (RC oscillator running)
- Operating voltage: 2.3V to 3.6V
- Modulation: ASK/OOK
- Xtal start time: 15us (Quick Start)
- Sniff Mode™ polling: 0.5ms to 16s (0.5ms or 64ms steps)
- PLL lock time: <50us
- Selectable data filter: Up to 20kHz
- Internal trim functions:
    - TX power (-3 to +12dBm)
    - Antenna impedance matching (Two independent channels)
    - Xtal, for frequency and Quick Start
    - RC oscillator frequency
    - Sniff Mode™, for data threshold
    - Data slice
- Clock and data recovery (Reduced data jitter)
- I^2C interface: Control bus
- Serial interface: Data input/output
- Low frequency IF
- Internal IF filtering
- Package: 20-lead, 209mm SSOP

4.0 Functional Block Diagram

The AMIS-52150 is a dual-channel receiver and a transmitter in a single, small outline package (Fig. 1). The receiver provides for two independent receive channels with the signals combined in the data detection circuit. Summing the signals allows the two channels to be used for antenna diversity optimization, without the need for complex protocols to select the strongest channel. The AMIS-52150 can be programmed to be a single channel or a dual-channel receiver, respectively. There exist internal trim functions for the RF receiver frequency, for tuning each input port, for setting the internal filters to match the data rate, and for setting the threshold level for acquiring an incoming signal, respectively. The receiver converts the received RF signal to a low frequency IF. An RSSI circuit determines the strength of the received signal. A level detector samples the RSSI signal level and compares that level to the slice threshold to recover the data. The slice threshold can be either set to a fixed level, or alternately, the transceiver can be configured to automatically set the threshold level based on the incoming data.

The transmitter is a high efficiency power amplifier (PA) that is turned On or Off by the serial data. The output power level is adjustable. The frequency of the RF output can be tuned with an internal crystal trim function, in order to conform to component and manufacturing tolerances. In addition, the design of the transceiver is based on a number of unique features.

The AMIS-52150 can be placed in a very low power state, with the crystal oscillator being Off while the low power RC oscillator maintains the chip operation. In this low power state, the AMIS-52150 remains in the sleep mode until either the wake-up timer or an

external microcontroller wake up the device, respectively. The receiver can be also configured for operation in Sniff Mode™ , where by the device is programmed to wake up at regular intervals to sniff for received RF signals, returning to the sleep mode if a signal is not detected. The AMIS-52150 contains a Quick Start circuit as well, which results in full operation of the crystal oscillator in an extremely short time, in turn leading to much lower power consumption as compared to other transceiver products available in the market. In the AMIS-52150, a programmable PLL is used to synchronize the data clock to the received data. This feature enables reducing much of the jitter in the data signal.

These functions will be described in more detail later in the document.

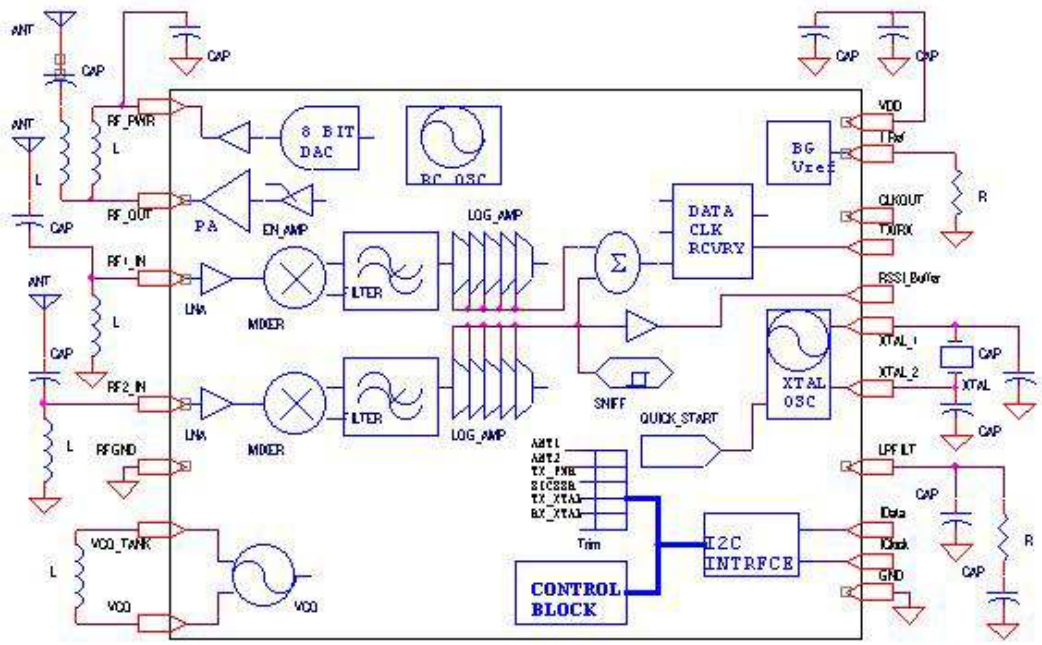

Figure 1: AMIS-52150 Block Diagram

5.0 Operating and Maximum Specifications

Table 1: Operating Conditions

Sym.	Parameter	Min.	Typ.	Max.	Units
VDD	Positive supply	2.3	3	3.6	V
VSS	Ground		0.0	0.1	V
Temp	Temperature range	0	+25	+50	°C

Table 2: Absolute Maximum Ratings

Sym.	Parameter	Min.	Max.	Units
VDD	Positive supply		+4	V
RFin	Max RF input RX1/RX2		+10	dBm
VSS	Ground	0.0	0.1	V
Vin	Logical I/P voltage	-0.3	VDD+ 0.3	V
Tstrg	Storage temperature	-40	+120	°C

Table 3: Absolute Maximum Ratings

Idd (Supply Current)	Typ.	Max.	Units	Conditions
Transmitting	20	25	mA	50% duty cycle
Receiving	7.5	10	mA	
Sniff Mode	75		uA	1% sniff cycle
Off		500	nA	RC OSC Off

Table 4: Electrical Characteristics; Digital Inputs

Parameter	Min.	Typ.	Max.	Units
Vih	0.7*VDD			V
Vil			0.3*VDD	V
Iih			+1.0	uA
Iil	-1.0			uA
I^2C internal pull-up		15	20	KΩ

Table 5: Electrical Characteristics; Digital Outputs

Parameter	Min.	Typ.	Max.	Units
Voh	0.8*VDD			V
Vol			0.4	V
Ioh			-1.0	mA
Iol	+1.0			mA
I^2C internal pull-up		15	20	KΩ

Table 6: Electrical Characteristics; Analog TX

Parameter	Min.	Typ.	Max.	Units	Comments
Frequency range	402	403.5	405	MHz	Targeted
	300		768	MHz	Non-Quick Start
	350		448	MHz	Quick Start
Modulation	1		8	Kbps	Manchester-coded data
	1		16	Kbps	NRZ data
Max. output power	11	12	13	dBm	
On/Off ratio		70		dB	Transmit
VCO gain		75		MHz/V	Kvco
PLL phase noise		-95		dBc/Hz	10kHz
		-97		dBc/Hz	100kHz
Harmonics		-35		dBc	With typical matching components
Crystal freq. spurs		-50		dBc	50kHz PLL loop bandwidth
Time TX to RX			1	ms	

Table 7: Electrical Characteristics; Analog RX

Parameter	Min.	Typ.	Max.	Units	Comments
Frequency range	402	403.5	405	MHz	Targeted
	300		768	MHz	Non-Quick Start
	350		448	MHz	Quick Start
Modulation	1		8	Kbps	Manchester-coded data
	1		16	Kbps	NRZ data
RF input	-117		-10	dBm	
Noise figure		4.5			
RF detect time	100			us	In Sniff Mode™
Time RX to TX			1	ms	

6.0 Pin Definitions

This section describes the pins of the AMIS-52150 package.

Table 8: Pin Description

Pin#	Name	Type	Comments
1	RX1 RF	RF	Receive RF input 1
2	RX2 RF	RF	Receive RF input 2
3	VCO2	Ana	Voltage controlled oscillator 2
4	VCO1	Ana	Voltage controlled oscillator 1
5	LPFILT	Ana	Loop filter
6	RSSI/ Bandgap Out	Ana	Analog RSSI output or bandgap output
7	NC		No electrical connection
8	CREF	Ana	Current bias precision resistor
9	GND	Ana	Analog/digital ground
10	CLKOUT	Dig	RC, XTAL, or data clock output
11	X1	Ana	Xtal input
12	X2	Ana	Xtal output
13	IIC Data	Dig	IIC interface data I/O
14	NC		No electrical connection
15	IIC Clock	Dig	IIC interface clock
16	TX/RX DATA	Dig	Data transmit, data receive or recovered data
17	VDD	Ana	Positive power supply
18	RFPWR	Ana	Regulated voltage Output for RF transmitter circuitry
19	RFOUT RF	RF	Transmit RF output
20	RFGND	Ana	RF ground

7.0 Package Outline

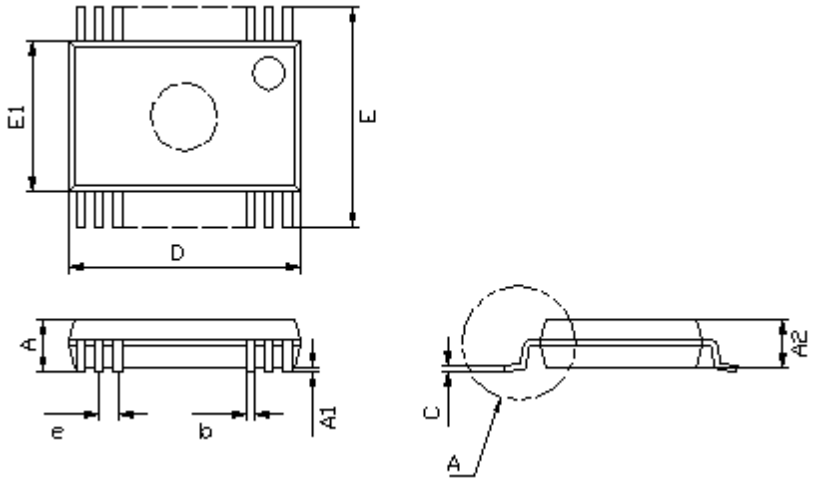

Figure 2: Package Outline

Table 9: Package Dimensions ; 209mil SSOP

	Inches		Millimeters	
Dm	Min.	Max.	Min.	Max.
A	0.068	0.078	1.73	2.00
A1	0.002	.20	0.05	
A2	0.065	0.073	1.65`	1.85
b	0.009	0.015	0.22	0.38
D	0.271	0.295	6.90	7.5
E	0.291	0.323	7.40	0.820
E1	0.197	0.221	5.00	0.560
e	0.026 BSC		0.65 BSC	

8.0 Pin Descriptions

8.1 RX1, RX2, RF Input Pins

RX1 and RX2 are the RF antenna inputs to the AMIS-52150. The internal circuit designs are identical between these inputs. For the AMIS-52150 receiver inputs, RX1 and RX2, external components are required in order to match the low noise amplifier (LNA) to external devices such as antennas. The external components must provide a DC voltage path to the RF ground. Figure 3 suggests an external circuit for the receiver inputs at 403MHz. Each circuit's input impedance can be trimmed internally to compensate for manufacturing and external component tolerances. The circuits employ an LNA, internal filters, a low frequency, intermediate frequency (IF), and a received signal strength indication (RSSI) circuit to recover the ASK/OOK modulated data. The signals in the two input channels are "summed" before the data recovery circuit.

The functions of the receive circuits are controlled by writing to the registers shown in Table 10.

Table 10: Receiver Control Register Description

RX1 or RX2 Receiver Register Control				
Register (HEX)	Name	Bits	States	Comments
0x00	ANT1 Trim	All		Inverse relationship register value to internal capacitance
0x01	ANT2 Trim	All		Inverse relationship register value to internal capacitance
0x0c	ANT1 Enable	0	0	Antenna port is Off
			1	Antenna port is On
	ANT2 Enable	1	0	Antenna port is Off
			1	Antenna port is On

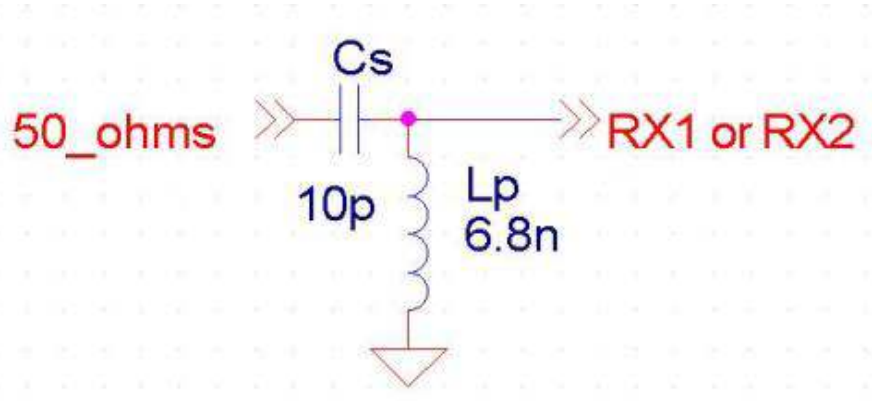

Figure 3: Typical Input Impedance Match to 50Ω (402MHz)

8.2 VCO1, VCO2, Voltage Controlled Oscillator Pins

The VCO1 and VCO2 pins connect a parallel combination of a capacitor and an inductor to the AMIS-52150 internal voltage controlled oscillator (VCO). The external LC (parallel inductor and capacitor) circuit sets the frequency of the internal VCO. The VCO frequency must be set to twice the value of the desired TX or RX frequency. Typical components for the tuning of the VCO at 402MHz are shown in Figure 4. The range of the VCO frequency is from 600MHz to 1536MHz.

The voltage on these pins can be used to determine proper operation of the PLL/VCO circuits. For further details, refer to the application note titled “First Time Users Guide to working with the Transceiver IC”.

Table 11: VCO Control Registers

VCO/PLL Control Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x06	Charge Pump	0,1	00	20uA
			01	25uA
			10	50uA*
			11	100uA
	VCO Current	2,3,4	000	180uA
			001	220uA
			010	260uA
			011	300uA
			100	340uA*
			101	380uA
			110	420uA
			111	460uA
	PLL Divider	7	0	Divider is 64
			1	Divider is 128

*Denotes the normal value

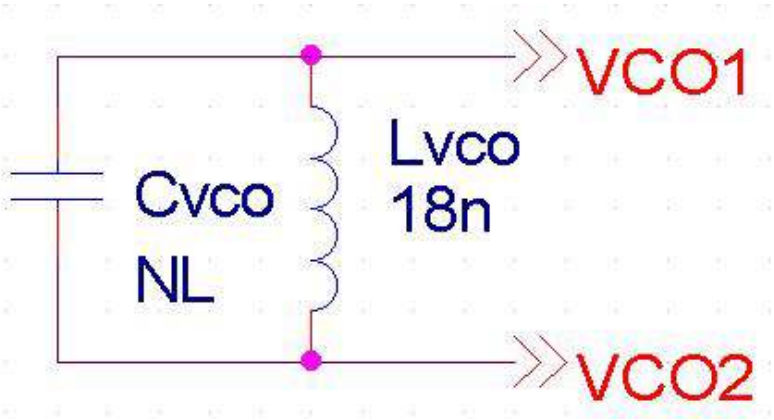

Figure 4: Typical Components for VCO Tuning at 402MHz

8.3 LPFILT, Loop Filter Pin

The LPFILT pin connects the AMIS-52150 internal phase lock loop (PLL) frequency synthesizer to an external loop filter (Fig. 5). An external loop filter allows the system designer to optimize the operation of the AMIS-52150 in order to meet the requirements for a specific end application. For further details, refer to the application note titled “Extending to Frequencies Outside of the 403MHz Target”.

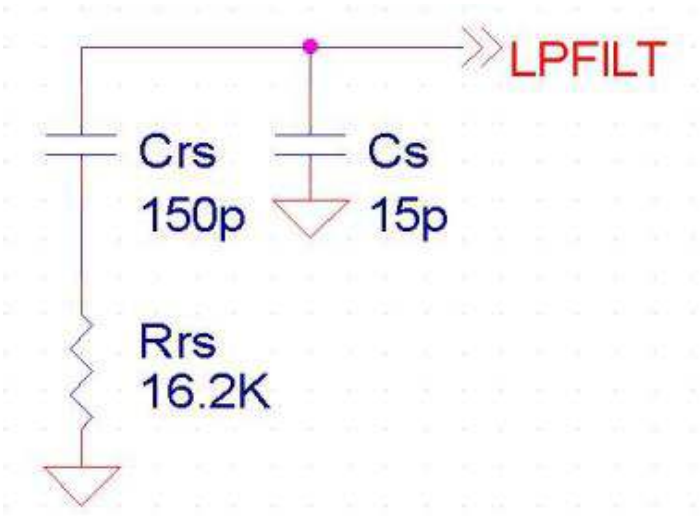

Figure 5: Typical Loop Filter

8.4 RSSI/BG, Analog Output Pin

The RSSI/BG pin is used to output either the signal from the RSSI circuits, or to output the voltage from the bandgap voltage reference or a bypass capacitor node, respectively. The RSSI output is a true analog representation of the received signal level. The pin can also be programmed to output the voltage of the bandgap voltage reference. When using the AMIS-52150 in the clock and data recovery mode, a capacitor needs to be connected from the RSSI/BG pin to ground. A typical value for this capacitor is 2.2nF. Additional information on the CDR function can be found later in this document. Table 12 presents the registers that control the function of the RSSI/BG pin.

Table 12: RSSVBG Pin Control Registers

RSSI Pin Definition Control Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x0e	Bandgap on RSSI	3	0	Normal operation
			1	BG output on RSSI*
0x1e	RSSI Ext Amp	4	0	Tri-stated
			1	RSSI signal

*Note that device needs to be in RX, TX or crystal-on mode for bandgap voltage to be present on pin.

8.5 CREF, Current Reference Bias Pin

A resistor must be connected to the CREF pin to provide a current bias to the internal bandgap voltage reference circuit. It is critical that this resistor value is 33.2KΩ (with one percent or better tolerance) to achieve proper operation of the bandgap voltage reference.

8.6 GND, Ground Pin

The GND pin is the ground connection for the digital and analog circuits.

8.7 CLKOUT, Internal Clock Output Pin

The CLKOUT pin is an output for the RC oscillator, crystal oscillator signal or the recovered data clock, respectively. The crystal oscillator signal output can be divided by 2, 3 or 4. The pin can also be programmed to output the signal from the recovered data clock function. For more information about the clock and data recovery (CDR) function of the AMIS-52150, refer to the section of this document on clock and data recovery.

The CLKOUT pin function control registers are shown in Table 13.

Table 13: Oscillator Output Control Registers

CLKOUT Pin Definition Control Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x0c	CLKOUT enable	7	0	CLKOUT is enabled
			1	CLKOUT is disabled
0x0d	CLKOUT select	4,5	00	Automatic control
			01	RC OSC
			10	Xtal
			11	Off
0x0e	XTAL divide	0,1	00	Divide by 4
			01	Divide by 3
			10	Divide by 2
			11	Divide by 1

8.8 X1, X2, External Crystal Reference Pins

X1 and X2 pins connect a parallel resonance oscillator crystal to the AMIS-52150 internal oscillator circuit. The external crystal should meet the requirements as listed in Table 14. However, the two load capacitors should be sized slightly smaller than the recommended value for the crystal, because of the added capacitance due to the internal trim circuit. For further details, refer to the application note titled “Quick Start Crystal Oscillator Circuit Operation and Set-up”. The crystal parameters are shown in Table 14.

Table 14: External Crystal Parameters

Parameter	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Crystal frequency	12.56		12.65	MHz	Targeted
	9.375		24.0		Non-Quick Start
	10.9		14.0		Quick Start
Crystal ESR			70	Ω	
Crystal tolerance		10		ppm	
Load capacitance	Load capacitors should be smaller than recommended for the crystal to allow for frequency tuning				

8.9 I^2CDATA, I^2CCLK, I^2C Control Interface Bus Pins

The AMIS-52150 implements an I^2C serial 8-bit bi-directional interface with the pins I^2CDATA and I^2CCLK. The device implements the protocol for a slave device. The clock for the interface is generated by the external master device. The interface will support the normal (0 – 100 Kbits/second) or the fast (0 – 400Kbits/second) data modes. The interface conforms to the Phillips specification for the I^2C bus standard. The pins have internal pull-up resistors. See Table 15 and Table 16 for some parameters of this interface.

In addition, Table 17 shows the details of register that controls the I^2C address increment function.

Table 15: Internal I^2C Pull-up Resistors

Pin	Function	Typ.	Units
I²CDATA	Internal pull-up R	15	KΩ
I² CCLK	Internal pull-up R	15	KΩ

Table 16: I²C Bus Device Addressing

Device	Address (Bin)	HEX	Function
AMIS-52150	01101000	68	Device write
AMIS-52150	01101001	69	Device read

Table 17: I²C Control Register

I²C Control Register				
Register (HEX)	Name	Bits	States	Comments
0x0c	I²C address increment	2	0	Increment after write
			1	Do not increment

The I²CDATA and I²CCLK lines are also used to signal to an external controller certain internal activities of the transceiver. The receiver is activated upon detection of RF energy during Sniff Mode™ operation. The wake-up timer can also be configured to wake-up the device in order to alert an external controller to perform specific tasks, as defined by the system designer.

8.10 TX/RX, Data Input/Output Pin

The transmit/receive (TX/RX) pin can be programmed to be either an input for RF transmissions, or an output for RF reception, or the output of the RC oscillator signal, or the output of the recovered data from the CDR circuits, respectively.

In transmit mode, this pin is the digital data input to the AMIS-52150 RF transmit circuit. The digital data results in the On and Off cycling of the output power amplifier (PA). The AMIS-52150 does not perform any protocol conversion on the data bit stream; it is simply a serial bit stream. The state of the TX/RX pin either turns the output amplifier On (enabling RF transmission) or turns the output amplifier Off (disabling RF transmission). The TX/RX input can be inverted which causes the state control of the RF output amplifier to be inverted as well.

In receive mode, this pin is the digital data output from the AMIS-52150 receivers. The received data is recovered as a high/low (digital ones and zeros) serial bit stream; the AMIS-52150 does not modify the received data protocol. The data output state due to the presence of energy in the receiver can be programmed to be either a high level or a low level at the TX/RX pin. An external controller is needed to decode the information in the recovered data bit stream.

When programmed to be an oscillator output, the TX/RX pin outputs the signal from the RC oscillator. This signal can be used to monitor the frequency of the RC oscillator in order to trim the frequency to the desired value.

The TX/RX pin can be programmed to output the recovered data obtained from the clock and data recovery circuits. In this case, the device must be programmed in the CDR mode. More information on CDR will be provided in a later section of this datasheet.

The functions of the TX/RX port are controlled by the values of the register settings, as shown in Table 18.

Table 18: TX/RX Pin Definition Control Registers

Register (HEX)	Name	Bits	States	Comments
0x0e	RC OSC on TX/RX	2	0	RX/TX normal
			1	RC OSC output
0x1e	TX/RX invert	5	0	Normal levels
			1	Inverted

8.11 VDD, Supply Voltage Pin

The VDD pin is the power supply pin for the AMIS-52150. The voltage on this pin is typically 3.0V. Please refer to the section “Operating and Maximum Specifications” of this document for the VDD operating conditions.

8.12 RFPWR, DC Voltage Output Pin

In the AMIS-52150, a regulated DC voltage is generated and outputted at the RFPWR pin. This voltage should be fed through a DC connection to the RFOUT pin in order to power the output stage of the RF PA. The voltage level is adjusted based on the value of the register setting, as shown in Table 19.

Table 19: TX Voltage Control Register

RFPWR Voltage Control Register				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x02	RFPWR trim	All		0xff is highest power

8.13 RFOUT, RF Output Signal Pin

In the AMIS-52150, a high efficiency non-linear output driver is used to produce the high power RF signal. This driver must be connected through a DC connection to the RFPWR pin. External components are required to match the output to a 50Ω load, or to an external antenna, respectively.

Figure 6 shows a typical matching circuit for the RFOUT pin.

8.14 RFGND, RF Ground Pin

The RFGND pin is the ground connection for the RF circuits in the device.

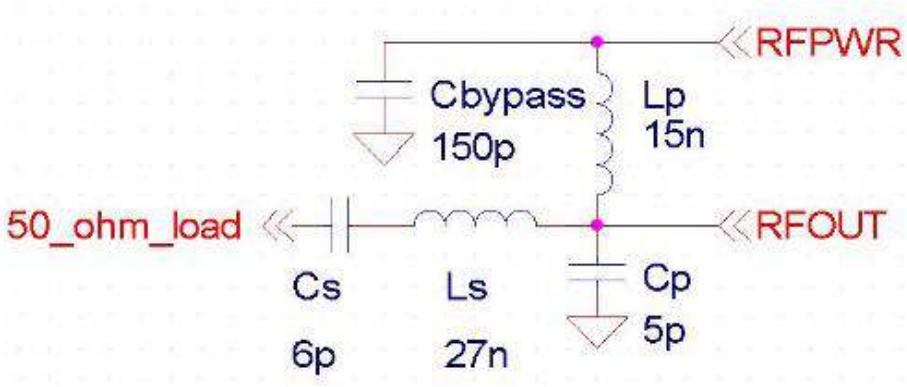

Figure 6: Typical RFOUT Output Impedance Match to 50Ω (402MHz)

9.0 Circuit Functional Description

The functions of the AMIS-52150 are presented in this section. These functions are:

- Receiver
- Transmitter
- Sniff
- Quick Start
- Data detection
- Clock and data recovery
- Application wakeup
- I^2C protocol
- Registers
- Alternative wake-up
- Power-On-Reset/Brown-Out

9.1 Receiver

RF signals often suffer from reflections along the path of propagation. These reflected signals arrive at the receiver antenna with different phases or time delays. The different phases of the reflected signals cause the signal strength at the receiver to vary. This variation can be large enough to cause the receiver to miss information. The AMIS-52150 sums the signals from the dual receiver channels within the data detection circuits. This reduces the effect of multi-path reflections. Proper operation requires a) trimming aimed at minimizing the frequency tolerances, b)tuning of the oscillator frequency, c)selection of the data rate filters, and d)setting of a signal threshold, as shown in Table 20.

Table 21 lists some characteristic parameters for the receivers. Figure 7 shows a typical received data waveform.

Table 20: Receiver Control Registers

RX1 or RX2 Receiver Register Control				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x00	ANT1 trim	All		Inverse relationship register value to internal capacitance
0x01	ANT2 trim	All		Inverse relationship register value to internal capacitance
0x05	RX XTAL tune	All		
0x0a	Data threshold	All		Reference level for detecting data logic state
0x0c	ANT1 enable	0	0	Antenna port is off
			1	Antenna port is on
	ANT2 enable	1	0	Antenna port is off
			1	Antenna port is on
	RX enable	3	0	Receiver is off
			1	Receiver is on
0x0f	Data filter	4,5,6	000	1.1kHz
			001	2.3kHz
			010	5.2kHz
			011	10.4kHz
			100	1.18kHz
			101	2.57kHz
			110	7.0kHz
			111	20.45kHz
0x1e	TX/RX invert	5	0	Normal levels
			1	Inverted

Table 21: RF Input Electrical Characteristics

Specification	Settings	Conditions	Typ.	Max.	Units	Comments
Input resistance			2		KΩ	
Input capacitance	Trim 0x00	Min. tune	3		pFarads	
	Trim 0xff	Max. tune	6		pFarads	
Sensitivity		1 Kbps	-117		dBm	w/CDR
Frequency			403.5		MHz	Target frequency
Max. input				-10	dBm	
IP3			+8		dBm	
IP2			+66		dBm	

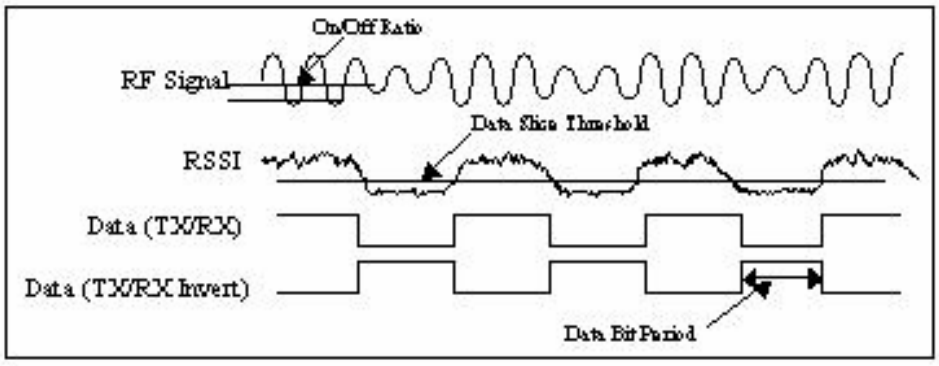

Figure 7: Received Waveform

9.2 Transmitter

The RF transmitter is a non-linear open drain device. It requires a DC signal path to RFPWR, which is the output of the internal power supply to the transmitter. The transmitter is switched On and Off with the serial transmit data stream. To achieve the desired output waveform, a tuned external resonant circuit is required. This resonant circuit should be designed to achieve the desired output frequency. This circuit includes a parallel LC tank (Lp and Cp) tuned to 402MHz (including internal capacitance), as well as a series LC (Ls and Cs) to produce a 403MHz output. The transmitter output is also to be filtered in order to reduce the harmonics to acceptable levels. It is further required that the transmitter output power level is programmed, that the transmit frequency is tuned and that the data rate is selected, respectively (Table 22).

Table 23 lists some characteristic parameters for the transmitter, while a typical transmitter output waveform is shown in Fig. 8.

Table 22: Transmitter Control Registers

TX/RX Definition Control Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x02	TX power	All		
0x04	TX XTAL trim	All		
0x0c	TX enable	4	0	Transmitter is off
			1	Transmitter is on
0x0f	Data filter	4,5,6	000	1.1kHz
			001	2.3kHz
			010	5.2kHz
			011	10.4kHz
			100	1.18kHz
			101	2.57kHz
			110	7.0kHz
			111	20.45kHz
0x1e	TX/RX invert	5	0	Normal levels
			1	Inverted

Table 23: Output Impedance Characteristics

Specification	Settings	Conditions	Min.	Typ.	Max.	Units
Output impedance		Resistance		22		Ω
		Capacitance		3		pFarads
Output power	RFPWR 0x00			-26		dBm
	RFPWR 0xff		11	12	13	dBm
Harmonics		Ext. circuit		-35		dBm
Frequency range		Target	402		405	MHz
		Quick Start	350		448	MHz
		Full range	300		768	MHz
Modulation				ASK/OOK		
On/off ratio	TX output			70		dBm

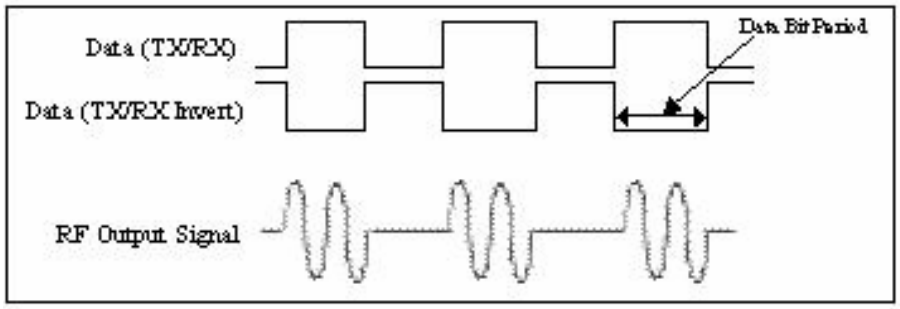

Figure 8: Transmit Waveforms

9.3 Sniff Mode™

Applications based on low power consumption require Sniff Mode™ operation of the AMIS-52150. This mode turns off the receiver and the crystal oscillator during programmable, regular time intervals. At the end of each time interval, the receiver wakes up and sniffs for the incoming RF energy. If energy is detected, the receiver transitions to the full receive mode and starts data recovery from the RF carrier. If energy is not detected, the receiver returns to the low power or “sleep” state. Sniff Mode™ operation is programmable; the “sleep” time as well as multiple delay sequences can be fully programmed. Table 24 lists the Sniff Mode™ control registers.

Typical timing waveforms for operation in Sniff Mode™ are shown in Figure 9 and Figure 10.

Table 24: Sniff Function Control Registers

Control Registers Associated with the Sniff Function				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x0b	SNIFF Threshold	All		Reference level for detected RF
0x0c	WAKE on RSSI	5	0	Do not wake on RSSI
			1	Wake on RSSI > threshold
0x0d	SNIFF TIMER RES	3	0	Resolution is set to 0.5mS per step
			1	Resolution is set to 64mS per step
0x13	DATA FILTER	All		Delay from RX wakeup to data sampled
0x16	IRQ DELAY	All		Time I^2C and TX/RX are active to indicate a wakeup
0x18	RSSI DELAY	All		Delay from wakeup to RSSI being checked
0x19	SNIFF TIMER	All		Time that receiver is off in Sniff Mode
0x1a	OFFSET DWELL	All		Time allowing receiver to power up (typically >40uS)
0x1b	DATA FILTER PRE-DIVIDER	All		Delay from data detection to pre-clock output

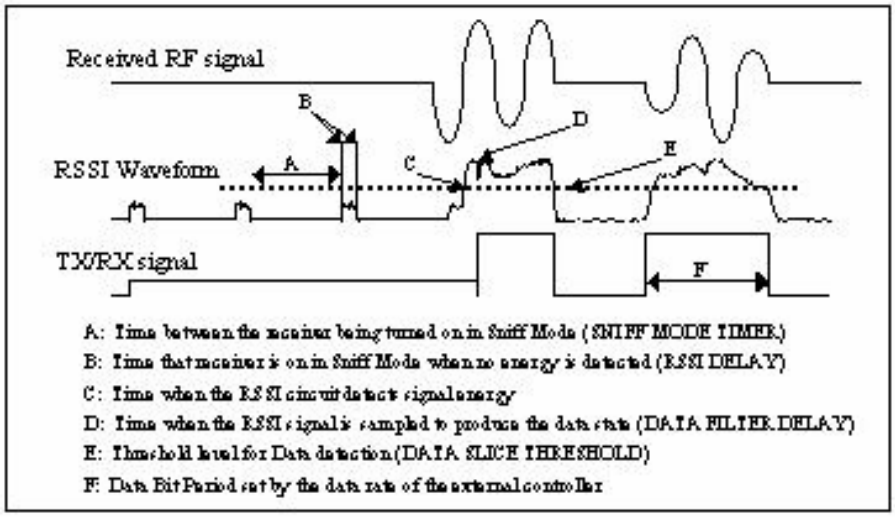

Figure 9: Receiver Data Acquisition in Sniff Mode™

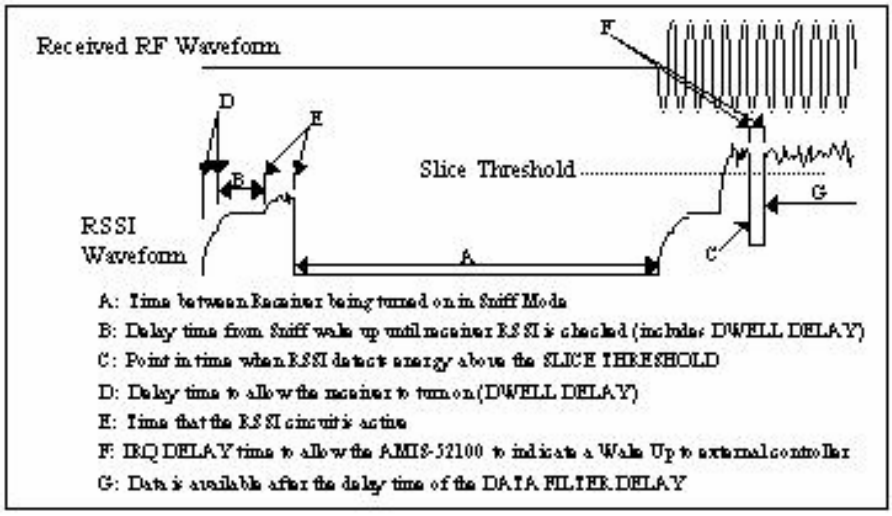

Figure 10: Sniff Timing at RF Energy Detection

9.4 Quick Start

There are two oscillators in the AMIS-52150, a low power 10kHz RC oscillator and a crystal oscillator, respectively.

The RC oscillator is used to keep the AMIS-52150 running in the ultra-low power mode. This oscillator is used to generate the clock signals for the Sniff Mode™ timers as well as the wake-up timers. Figure 11 shows a block diagram of the clocks in the AMIS-52150. The crystal oscillator provides the reference frequency which is used to generate the RF frequencies for transmission and receiving of data. It is also the reference for all the timing functions in the AMIS-52150. The RC oscillator is in turn used to produce a “kicker” signal when the Quick Start function of the crystal oscillator is needed.

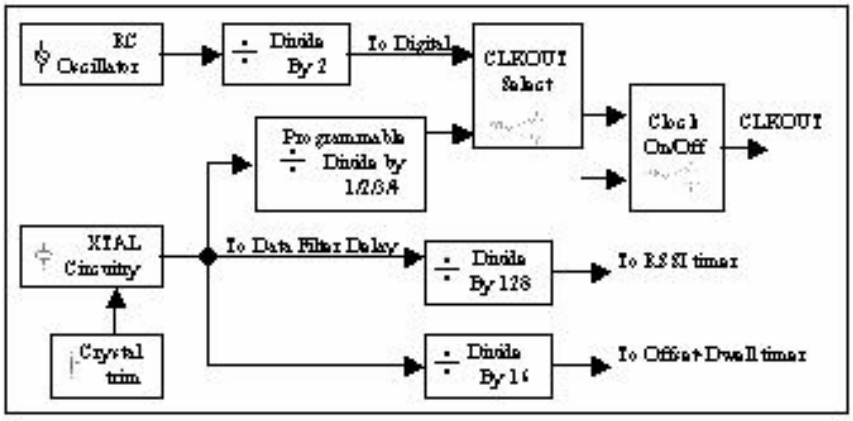

Figure 11: Internal Clocks

A “kicker” circuit stimulates the crystal oscillator circuit with oscillations close to the final frequency. This significantly reduces the time it takes for the oscillator to reach and lock to the final frequency. The Quick Start function is necessary for operation in Sniff Mode™. Table 25 lists the Quick Start control registers. For further details, refer to the application note titled “Quick Start Crystal Oscillator Circuit Operation and Set-up”.

Table 25: Quick Start Control Registers

Quick Start Control Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x03	Kicker Trim	All		Trim the internal RC OSC to form a kick-start to the XTAL oscillator
0x0e	Kick Config1	4	0	Common mode clamp disabled (startup)
			1	Common mode clamp enabled (normal)
	Kick Config2	5	0	Normal operation
			1	Continuous kick On

9.5 Data Detection

The RSSI circuit creates an analog voltage waveform (18mV/dB) that follows the signal strength of the RF signal. The data slice circuit then samples that waveform to create the digitized data. The slice circuit in the AMIS-52150 can be programmed to operate in one of three modes; DAC mode, Average mode or Peak mode. The DAC mode compares a fixed slice threshold value to the level in the slice output. The digital data state is determined by the level of the slice output being above or below that fixed threshold. For further details, refer to the application note titled “Setting Up the AMIS-52150 Data Slicing Modes”. Figure 12 shows a typical waveform for the DAC mode, while Table 26 shows the control registers for the auto slice modes.

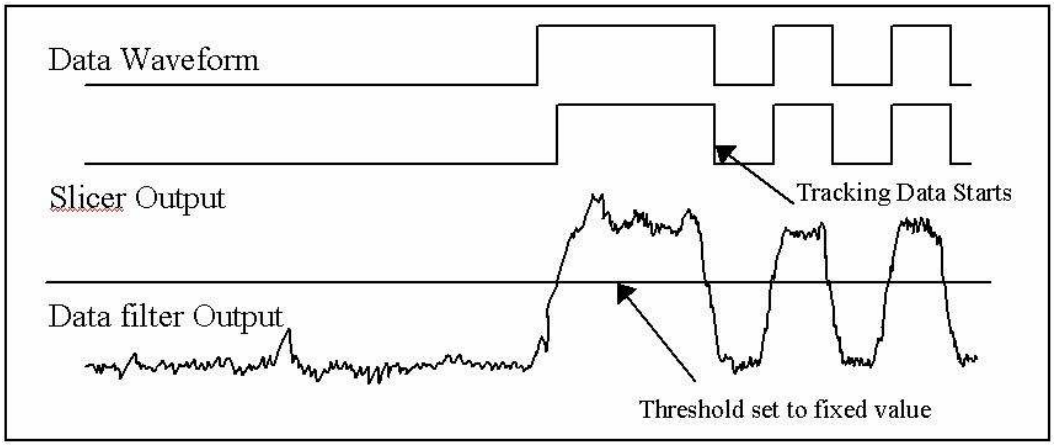

Figure 12: DAC Slice Mode Waveform

In the Average mode, the threshold value is generated automatically. This threshold value is then compared to the output of the slice circuit to re-create the digital data. The slice circuit along with an external capacitor are used to generate a charging time constant which is equal to charging to 95 percent of a bit level in two bit time periods. The data protocol should add a header to the data to allow the slice circuit to determine the average level. For further details, refer to the application note titled “Setting Up the AMIS-52150 Data Slicing Modes”. Figure 13 shows a typical waveform for the Average mode. Table 26 shows the control registers for the auto slice modes.

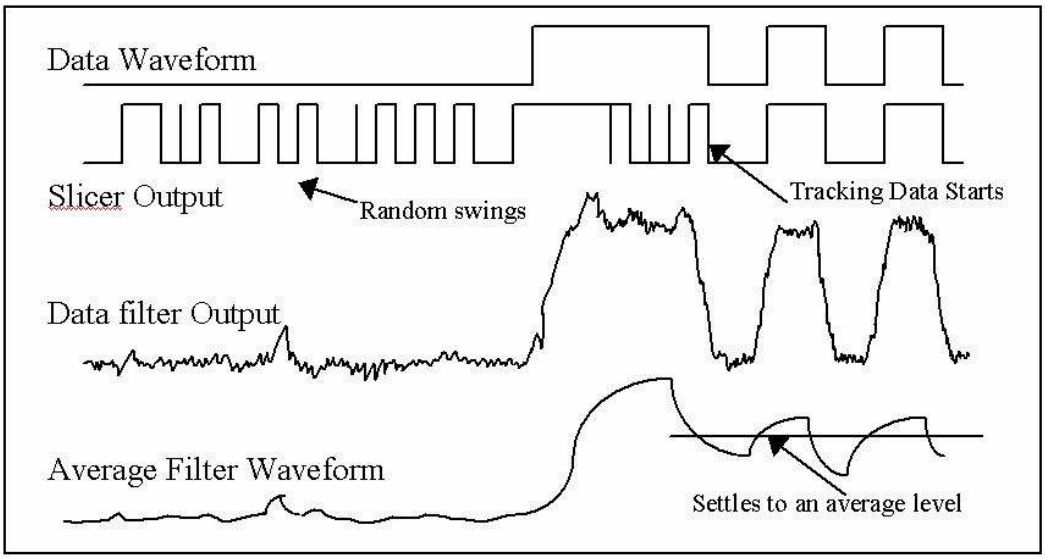

Figure 13: Average Slice Mode Waveform

In the Peak mode, a threshold value is generated automatically as well. This threshold value is then compared to the output of the slice circuit to re-create the digital data. The operation of the slice circuit is based on an external capacitor with an internal peak detector, in order to arrive at the peak value of the data waveform. The threshold value is set 6dB below this peak value. The capacitor value should be selected so that the peak detector does not discharge during periods of continuous zeros, while being small enough to allow the peak detector to reach the peak value quickly. For further details, refer to the application note titled “Setting Up the AMIS-52150 Data Slicing Modes”. Figure 14 shows a typical waveform for the Peak mode.

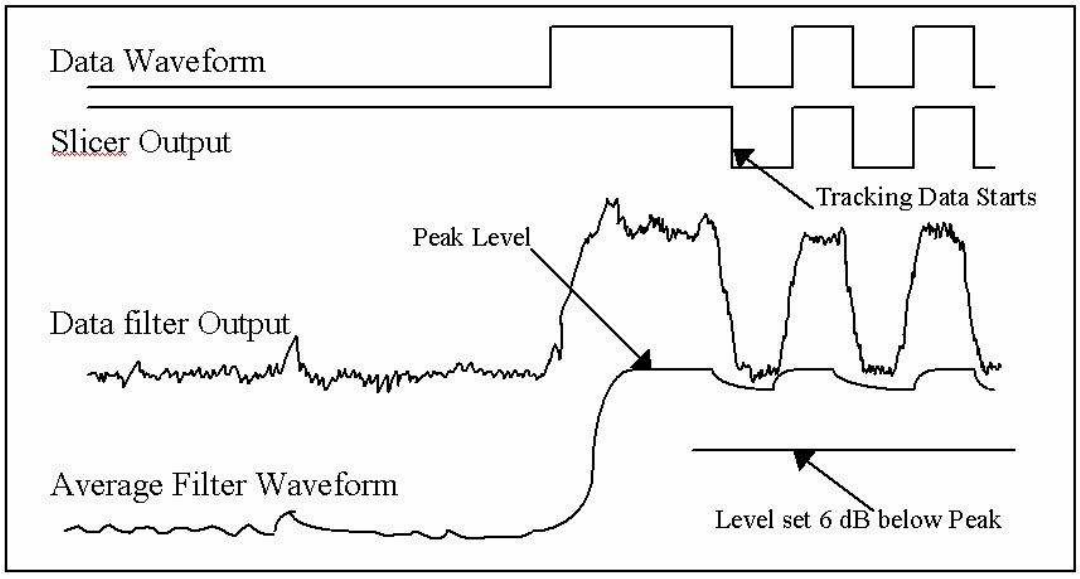

Figure 14: Peak Slice Mode Waveform

Table 26: Auto Slice Control Registers

Auto Slice Control Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x0a	DATA SLICE THRESHOLD	All		Set a fixed reference level for the slice output to be compared to in the DAC mode
0x0f	HYSTERESIS	0,1	00	0mV hysteresis used in the threshold circuit
			01	20mV hysteresis used in the threshold circuit
			10	50mV hysteresis used in the threshold circuit
			11	100mV hysteresis used in the threshold circuit
	AUTOSLICE	2,3	00	DAC mode used for data detection (DEFAULT)
			01	Average mode used for data detection
			10	Peak mode used for data detection
			11	DAC mode used for data detection

9.6 Data and Clock Recovery

Data recovered in a noisy environment or from a weak RF signal is usually jittery. The AMIS-52150 can remove much of that data jitter by recovering a synchronous clock signal from the incoming data. The device can be set to achieve auto slice data detection. The clock and data recovery circuits can be programmed to generate a data clock for synchronously clocking the data output from the transceiver, removing much of the jitter in this process. The AMIS-52150 has an internal PLL that must be programmed to the frequency of the data by setting the values in the FWORD register and setting the coefficients of the filter. If these values are close to the data rate, the device will recover the data clock from the incoming detected data. The CDR circuit can also be set to a given tolerance with respect to the frequency difference between the target data rate and the actual data rate, in order to improve the performance of the CDR function. The CDR circuit can also be configured to reset after a programmed number of data time periods if no data is received. This “stop and check” function allows the CDR circuit to re-acquire the clock data when new data is received, maintaining better clock to data synchronization.

Table 27 lists the registers associated with the data and clock recovery function. For further details, refer to the application note titled “AMIS-52150 Clock and Data Recovery Circuit Operation and Set-Up”.

Table 27: Data and Clock Recovery Control Registers

Data and Clock Recovery Associated Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x07	FWORD LSB	All		Sets the initial internal clock frequency for the clock and data recovery circuits
0x08	FWORD	All		
0x09	FWORD MSB	All		
0x0d	DATA MUX	6	0	TX/RX normal signals
			1	Recovered data on TX/RX
	CLKMUX	7	0	Normal CLKOUT signals
			1	Recovered CLOCK output on CLKOUT
0x10	K_0	0,1,2	000	Filter coefficient gain is 1
			001	Filter coefficient gain is 2
			010	Filter coefficient gain is 4
			011	Filter coefficient gain is 8
			100	Filter coefficient gain is 16
			101	Filter coefficient gain is 32
			110	Filter coefficient gain is 64
			111	Filter coefficient gain is 128
	K_1	4,5,6	000	Filter coefficient gain is 1
			001	Filter coefficient gain is 2
			010	Filter coefficient gain is 4
			011	Filter coefficient gain is 8
			100	Filter coefficient gain is 16
			101	Filter coefficient gain is 32
			110	Filter coefficient gain is 64
			111	Filter coefficient gain is 128
0x11	K_2	0,1,2	000	Filter coefficient gain is 0.125
			001	Filter coefficient gain is 0.250
			010	Filter coefficient gain is 0.500
			011	Filter coefficient gain is 1.000
			100	Filter coefficient gain is 2
			101	Filter coefficient gain is 4
			110	Filter coefficient gain is 8
			111	Filter coefficient gain is 16
	FsDIV	4,5,6	000	Sample frequency divider is 2
			001	Sample frequency divider is 4
			010	Sample frequency divider is 8
			011	Sample frequency divider is 16
			100	Sample frequency divider is 20
			101	Sample frequency divider is 32
			110	Sample frequency divider is 40
			111	Sample frequency divider is 48
0x12	STOP CHECK	0,1	00	StopCheck bits: disabled
			01	StopCheck bits: 2
			10	StopCheck bits: 4
			11	StopCheck bits: 8
	LOOPCLAMP	2,3	00	Loop clamp value is: +-BaudClk/8
			01	Loop clamp value is: +-BaudClk/16
			10	Loop clamp value is: +-BaudClk/32
			11	Loop clamp value is: +-BaudClk/64
	FREERUN	4	0	Phase alignment enabled
			1	Phase alignment disabled
	CRD RESET	5	0	CDR reset disabled
			1	CDR reset enabled
	AUTO/MANUAL RESET	6	0	POR reset (auto)
			1	CDR reset enabled (manual)
	SAMPLE WINDOW	7	00	Sampling starts with bit start edge
			00	Sampling centered around bit center

The clock and data recovery function is dependent on the receiver's ability to recover the data from the incoming RF signal. There exists a technique to test the clock and data recovery function without having to set up the receiver to receive data. This is a test mode that allows an input data stream (square wave at 1/2 the data rate) on the RSSI pin, with the recovered clock data appearing on the CLKOUT pin and the recovered data appearing on the TX/RX pin, respectively. Once the AMIS-52150 is configured for clock and data

recovery (see the application note titled “AMIS-52150 Clock and Data Recovery Circuit Operation and Set-Up”), the register shown in Table 28 can be used to define the test mode operation.

Table 28: Clock and Data Recovery Test Mode

Clock and Data Recovery Test Control Register			
Register (HEX)	**Binary Code**	**HEX Code**	**Comments**
0x1d	00001110	0x0e	Normal RSSI digital input
	00001111	0x0f	CDR start bit digital input to RSSI

9.7 Wake-Up Function

Ultra-low power applications can take advantage of the wake-up function of the AMIS-52150. The AMIS-52150 can be placed in a low power or “sleep” state until an interrupt based on the programmable wake-up timer is generated. This wakes up the transceiver, which then flags the external microcontroller to perform the required application-specific operations. The wake-up interrupt is also generated based on detection of RF energy (Sniff Mode™). Communication with the microcontroller takes place via the I^{2}C bus. In addition, when the AMIS-52150 is in the “sleep’” state, the wake-up signal can be generated by the microcontroller. Table 29 lists the registers associated with the wake-up function.

Table 29: Application Wake-Up Control Registers

Application Wakeup Control Registers				
Register (HEX)	**Name**	**Bits**	**States**	**Comments**
0x14	AW TIMER DIV	All		Divides the RC oscillator to form a clock for the AW
0x15	AW TIMER	All		Number of AW clock periods before a AW wakeup
0x17	PRE/POST AW DELAY	All		Number of CLKOUT clock periods before the TX/RX pin goes low for a AW cycle

9.8 I^{2}C Interface

The I^{2}C is a two pin bi-directional serial interface communication bus, with a data line and a clock line, respectively. Serial data on the data pin is clocked into or out of the AMIS-52150 by the clock pin. The AMIS-52150 is implemented as a slave device, which means that the external controller is the master device. The clock signal for all transmissions between the master (controller) and the slave (AMIS-52150) is generated by the controller. The serial communication bit rate can be as high as 400Kbps. A communication link is initiated based on a start sequence. Bi-directional communication continues as long as the master and slave acknowledge the write or read sequences, and is terminated with a stop sequence. This is illustrated in Figure 15, Figure 16 and Figure 17, respectively.

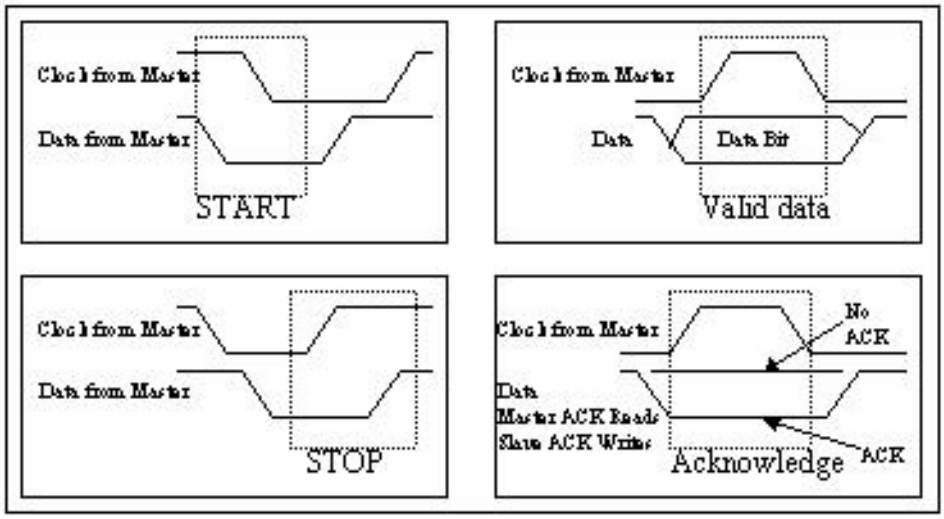

Figure 15: I^2C Valid Control Waveforms

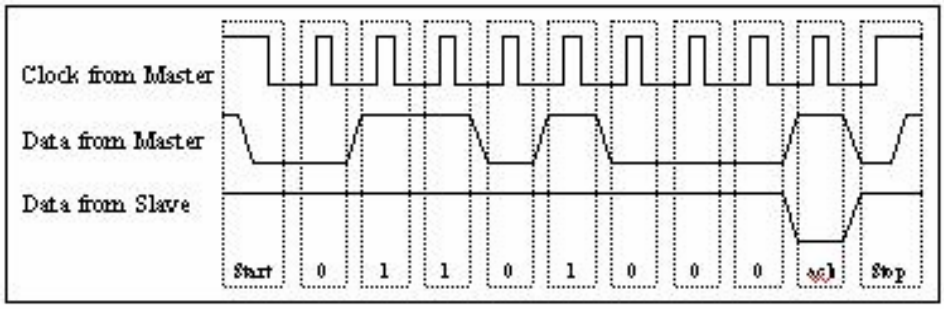

Figure 16: I^2C Protocol in a Write 68 (Hex) or a Data Write Request

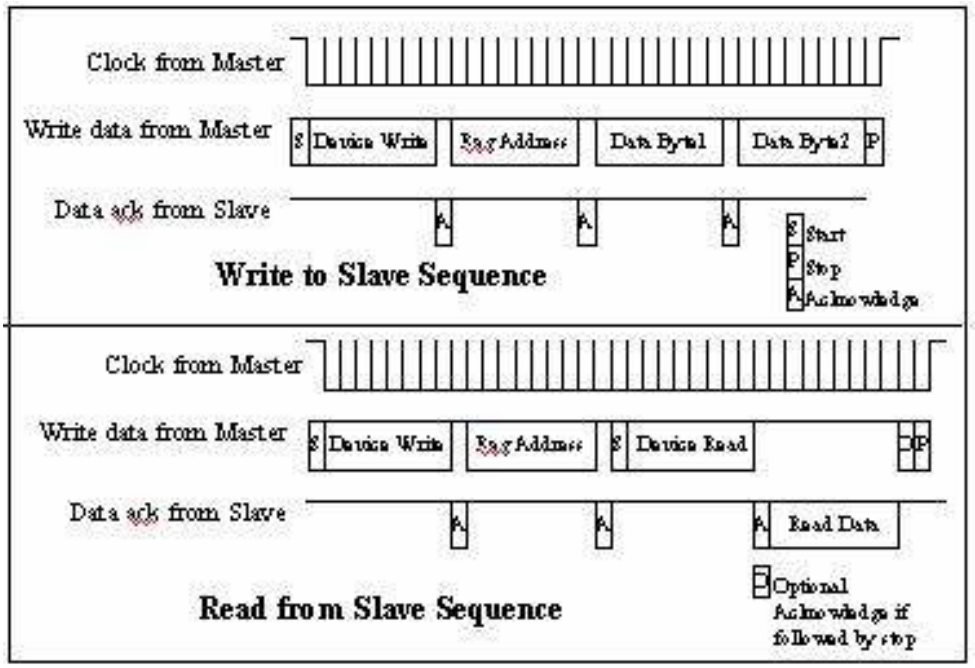

Figure 17: I²C Write and Read Protocol

9.9 Registers

The AMIS-52150 is comprised of 31 registers. For further details, refer to the application note titled “AMIS-52150 Register Definitions and Functions”.

9.10 Power-On-Reset/Brown-Out Detection

The POR/brown-out detection circuit ensures that the AMIS-52150 will be in a reset state when VDD drops below a certain threshold voltage, and remains in this state until VDD rises above another threshold voltage. The characteristics of the POR circuit are shown in Figure 18.

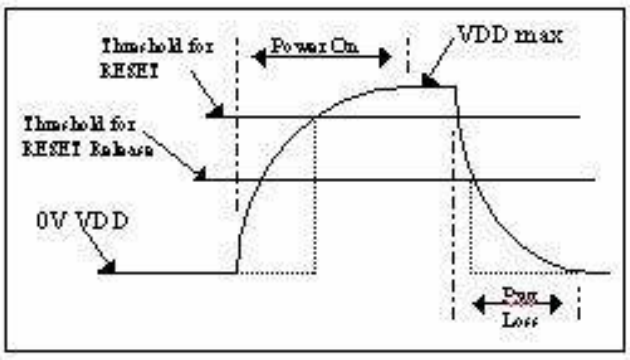

Figure 18: Power-on-Reset Characteristics

9.11 Alternative Wake-Up Functions

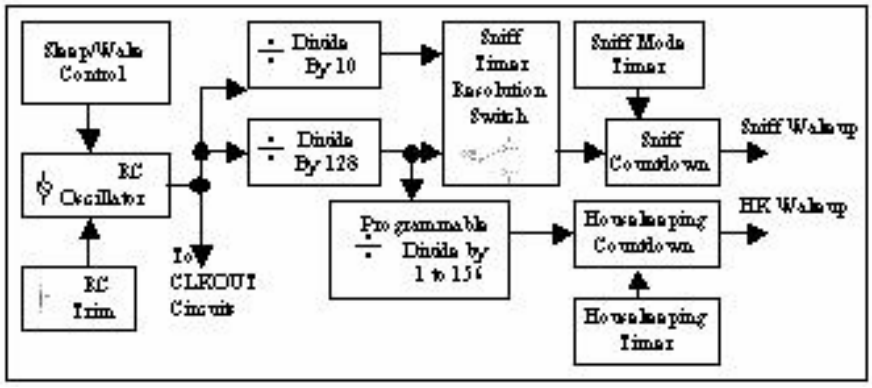

Figure 19: Wakeup Circuits

The AMIS-52150 will wake up from the low power mode upon a) reception of RF energy, b) an interrupt generated by the wake-up timer, or c) an interrupt generated by the external controller. In this low power mode, the RF circuits, the crystal oscillator, and the CLKOUT circuits are shut off, and only the RC oscillator and the wake-up divider circuitry are active. Once the AMIS-52150 receiver detects RF energy and wakes up, the RX/TX pin is set “low” while the I^2CDATA and I^2CCLK pins can remain “high”. In addition, when the wake-up timer wakes up the AMIS-52150 to in turn flag the external controller, the TX/RX and I^2CDATA pins are set “low” while the I^2CCLK pin can remain “high”. The external controller can also signal the AMIS-52150 to wake up by setting both the I^2CDATA and I^2CCLK lines low. These functions are shown in Table 30.

Table 30: Wakeup Truth Table

Wakeup Truth Table					
Wakeup Source	**TX/RX**	**I^2CDATA**	**I^2CCLK**	**CLKOUT**	**Comments**
SNIFF	0	1	1	XTAL out	Wake on RF energy detect
HK Cycle	0	0	1	RC oscillator	Wake due to HK timer timeout
External	1	0	0	Don’t care	Wake due to external controller

10.0 Ordering Information

Part Number	Package Type	Shipping Configuration	Temperature Range
AMIS-52150-XTD	20-pin SSOP (209 mil, shrink small outline package)	Tube/Tray	0°C to 50°C
AMIS-52150-XTP	20-pin SSOP (209 mil, shrink small outline package)	Tape & Reel	0°C to 50°C

11.0 Revision History

Revision	Date	Modification

6	April 2007	Update to new AMIS template
7	May 2008	Update to new ON Semiconductor template

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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