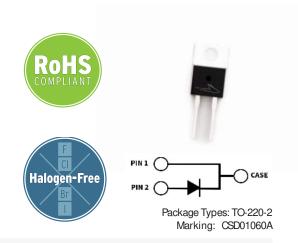


600 V, 1 A Silicon Carbide Schottky Diode

Description

With the performance advantages of a Silicon Carbide (SiC) Schottky Barrier diode, power electronics systems can expect to meet higher e iciency standards than Si-based solutions, while also reaching higher frequencies and power densities. SiC diodes can be easily paralleled to meet various application demands, without concern of thermal runaway. In combination with the reduced cooling requirements and improved thermal performance of SiC products, SiC diodes are able to provide lower overall system costs in a variety of diverse applications.



Features

- Low Forward Voltage $(V_{\scriptscriptstyle F})$ Drop with Positive Temperature Coe icient
- Zero Reverse Recovery Ourrent / Forward Recovery Voltage
- Temperature-Independent Switching Behavior

Applications

- Industrial Switched Mode Power Supplies
- Uninterruptible & AUX Power Supplies
- Boost for PFC & DC-DC Stages
- Solar Inverters

Maximum Ratings ($T_C = 25^{\circ}C$ Unless Otherwise Specified)

Parameter	Symbol	Value	Unit	Test Conditions	Notes	
Repetitive Peak Reverse Voltage	V _{RRM}	600	V			
DC Blocking Voltage	V _{DC}	600	V			
Continuous Forward Current	l _F	4	A	T _J = 25 °C		
		2		T _J = 135 °C	Fig. 3	
		1		T _J = 158 °C		
Repetitive Peak Forward Surge Current	I _{FRM}	7		$T_{\rm C} = 25 {\rm ^{\circ}C}$, $t_{\rm p} = 10 {\rm ms}$, Half Sine Wave		
		5.5		$T_{\rm C} = 110$ °C, $t_{\rm p} = 10$ ms, Half Sine Wave		
Non-Repetitive Forward Surge Current	I _{FSM}	9		$T_{\rm C}$ = 25 °C, $t_{\rm p}$ = 1.5 ms, Half Sine Wave	Fig. 8	
Non-Repetitive Peak Forward Surge Current	l _{F,Max}	32		$T_{\rm C} = 25 {}^{\circ}\text{C}, t_{\rm p} = 10 \mu\text{s}, \text{Pulse}$		
Power Dissipation	P _{tot}	21.4	W	T _J = 25 °C	Fig. 4	
		7.1		T _J = 125 °C		

Electrical Characteristics

Parameter	Symbol	Тур.	Max.	Unit	Test Conditions	Notes
Forward Voltage		1.6	1.8	V	I _F = 1 A, T _j = 25 °C	Fig. 1
	V _F	2.0	2.4		I _F = 1 A, T _j = 175 °C	
Reverse Current		20	100	μА	$V_{R} = 600 \text{ V}, T_{j} = 25 ^{\circ}\text{C}$	Fig. 2
	l _R	40	500		$V_R = 600 \text{ V}, T_j = 175 \text{ °C}$	
Total Capacitive Charge	Q _c	3.3		nC	V _R = 600 V, T _j = 25 °C	Fig. 5
Total Capacitance		80		pF	$V_R = 0 \text{ V}, T_j = 25 \text{ °C}, f = 1 \text{ MHz}$	Fig. 6
	С	11			$V_{R} = 200 \text{ V}, T_{j}$	

Typical Performance

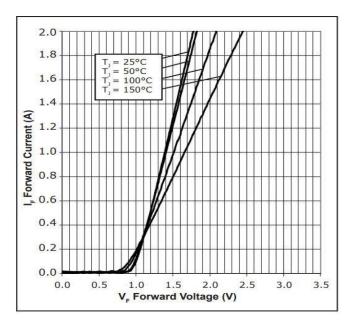


Figure 1Forward Characteristics

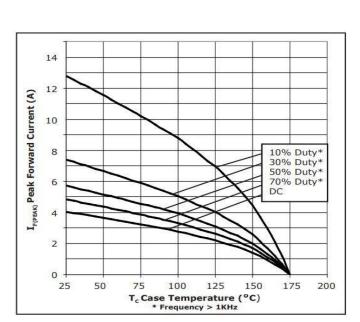


Figure 3Current Derating

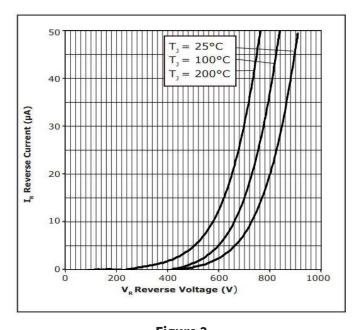


Figure 2Peverse Characteristics

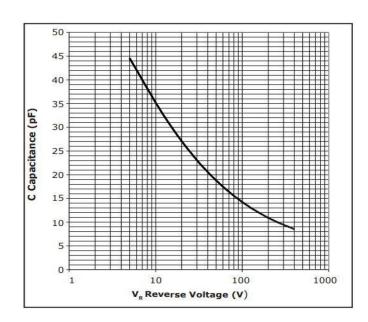


Figure 4Capacitance vs. Reverse Voltage

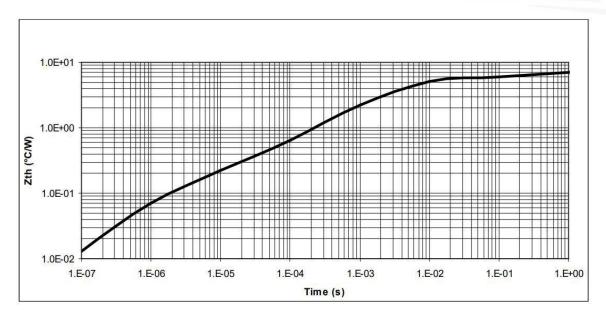


Figure 5
Transient Thermal Impedance

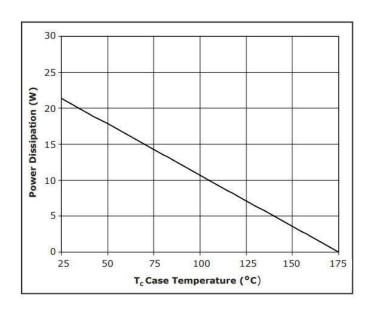


Figure 6Power Derating

Diode Model

$$\begin{array}{c|c} - & & \\ \hline V_T & & R_T \\ \end{array}$$

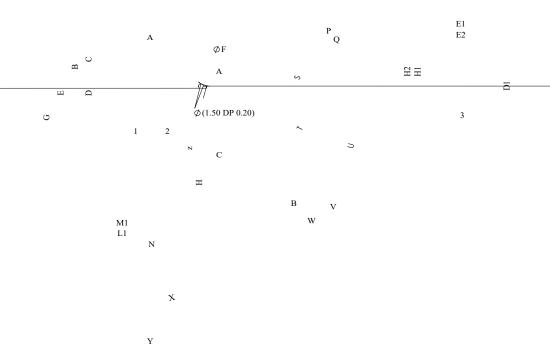
$$Vf_T = V_T + If^*R_T$$

$$\begin{split} V_{T=} \, 0.94 + & \left(T_{\rm j} \, * \, \text{-} 1.2 \, {}^{\text{+}} 10^{\text{-}3} \right) \\ R_{T=} \, 0.015 + & \left(T_{\rm j} \, * \, 6.4 \, {}^{\text{+}} 10^{\text{-}3} \right) \end{split}$$

Note: T_i = Diode Junction Temperature In Degrees Celsius

Package Dimensions & Pin-Out

Package: TO-220-2



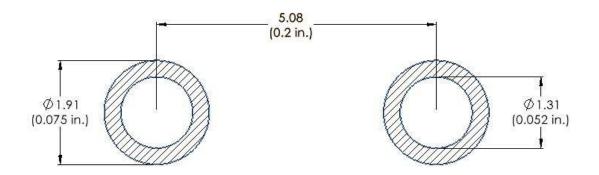
NOTE

- $\begin{array}{l} {\rm 1.\;ALL\;METAL\;SURFACES\;ARE\;TIN\;PLATED\;(MATTE),} \\ {\rm EXCEPT\;AREA\;OF\;CUT.} \end{array}$
- $\begin{tabular}{ll} 2. & DIMENSIONING \& TOLERANCING CONFORM TO \\ & ASME Y14.5M-1994. \end{tabular}$
- 3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
- 4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS



Recommended Solder Pad Layout

Primary dimensions shown in mm.



Product Ordering Information

Order Number	Packing Type
CSD01060A	Tube

Revision History

Document Version	Date of Release	Description of Changes
1	October-2019	Initial Release
18	March-2023	Update Package Drawing Update Landing Pad

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