# NSS30071MR6T1G

# 30 V, 0.7 A, Low $V_{CE(sat)}$ NPN Transistor

ON Semiconductor's $e^2$PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical application are DC−DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows $e^2$PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

- This is a Pb−Free Device

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector−Emitter Voltage | $V_{CEO}$ | 30 | V |
| Collector−Base Voltage | $V_{CBO}$ | 40 | V |
| Emitter−Base Voltage | $V_{EBO}$ | 5.0 | V |
| Collector Current | $I_C$ | 700 | mA |
| Base Current | $I_B$ | 350 | mA |
| Total Power Dissipation @ $T_C$ = 25°C<br>Total Power Dissipation @ $T_C$ = 85°C<br>Thermal Resistance − Junction−to−Ambient (Note 1) | $P_D$<br>$P_D$<br>$R_{\theta JA}$ | 342<br>178<br>366 | mW<br>mW<br>°C/W |
| Total Power Dissipation @ $T_C$ = 25°C<br>Total Power Dissipation @ $T_C$ = 85°C<br>Thermal Resistance − Junction−to−Ambient (Note 2) | $P_D$<br>$P_D$<br>$R_{\theta JA}$ | 665<br>346<br>188 | mW<br>mW<br>°C/W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to +150 | °C |

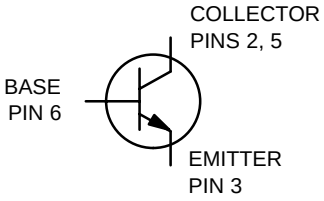
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

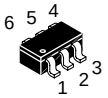
1. Minimum FR−4 or G−10 PCB, Operating to Steady State.
2. Mounted onto a 2″ square FR−4 Board (1″ sq 2 oz Cu 0.06″ thick single sided), Operating to Steady State.

**ON Semiconductor®**

**http://onsemi.com**

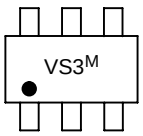
**30 VOLTS**
**0.7 AMPS**
**NPN LOW $V_{CE(sat)}$ TRANSISTOR**
**EQUIVALENT $R_{DS(on)}$ 200 mΩ**




**SC−74**
**CASE 318F**
**STYLE 2**

**DEVICE MARKING**




VS3 = Specific Device Code
M = Date Code

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NSS30071MR6T1G | SC−74 (Pb−Free) | 10000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure. BRD8011/D.





June, 2005 − Rev. 0

Publication Order Number:
NSS30071MR6/D

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Symbol | Characteristic | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $V_{(BR)CBO}$ | Collector−Base Breakdown Voltage | ($I_C$ = 100 μAdc) | 40 | − | − | Vdc |
| $V_{(BR)CEO}$ | Collector−Emitter Breakdown Voltage | ($I_C$ = 10 mAdc) | 30 | − | − | Vdc |
| $V_{(BR)EBO}$ | Emitter−Base Breakdown Voltage | ($I_E$ = 100 μAdc) | 5.0 | − | − | Vdc |
| $I_{CBO}$ | Collector Cutoff Current | ($V_{CB}$ = 25 Vdc, $I_E$ = 0 Adc)<br>($V_{CB}$ = 25 Vdc, $I_E$ = 0 Adc, $T_A$ = 125°C) | −<br>− | −<br>− | 1.0<br>10 | μAdc |
| $I_{EBO}$ | Emitter Cutoff Current | ($V_{EB}$ = 5.0 Vdc, $I_C$ = 0 Adc) | − | − | 10 | μAdc |
| **ON CHARACTERISTICS** | | | | | | |
| $h_{FE}$ | DC Current Gain | ($V_{CE}$ = 3.0 Vdc, $I_C$ = 100 mAdc) | 150 | − | − | Vdc |
| $V_{CE(sat)}$ | Collector−Emitter Saturation Voltage | ($I_C$ = 500 mAdc, $I_B$ = 50 mAdc) | − | − | 0.25 | Vdc |
| $V_{CE(sat)}$ | Collector−Emitter Saturation Voltage | ($I_C$ = 700 mAdc, $I_B$ = 70 mAdc) | − | − | 0.4 | Vdc |
| $V_{BE(sat)}$ | Base−Emitter Saturation Voltage | ($I_C$ = 700 mAdc, $I_B$ = 70 mAdc) | − | − | 1.1 | Vdc |
| $V_{BE(on)}$ | Collector−Emitter Saturation Voltage | ($I_C$ = 700 mAdc, $V_{CE}$ = 1.0 Vdc) | − | − | 1.0 | Vdc |

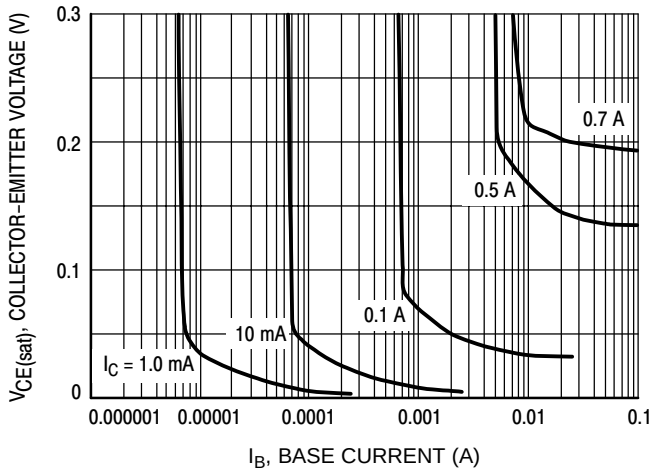



**Figure 1. Collector Saturation Region**

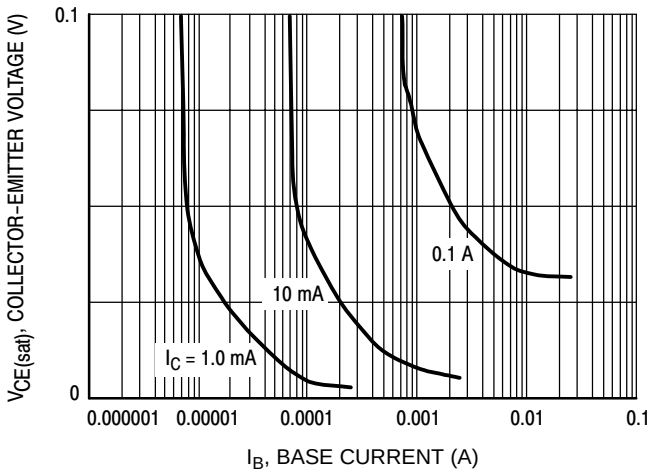



**Figure 2. Collector Saturation Region**

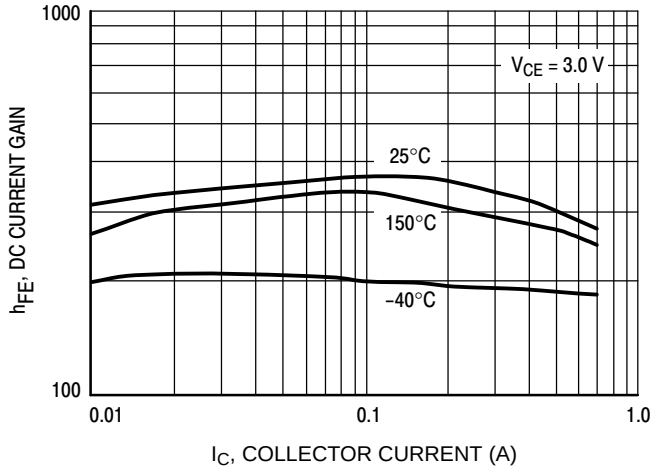



**Figure 3. DC Current Gain**

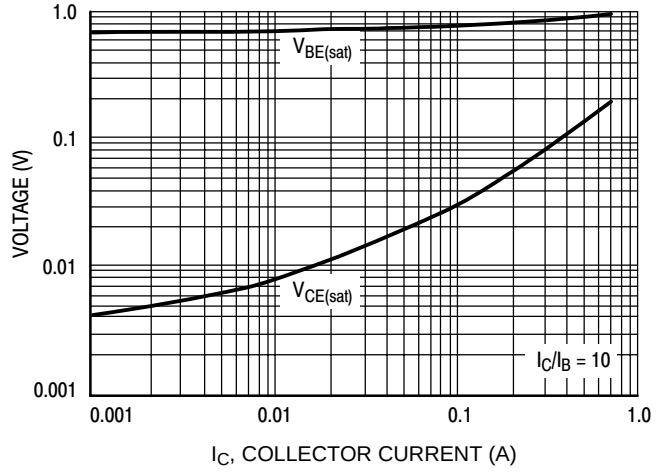



**Figure 4. “ON” Voltages**

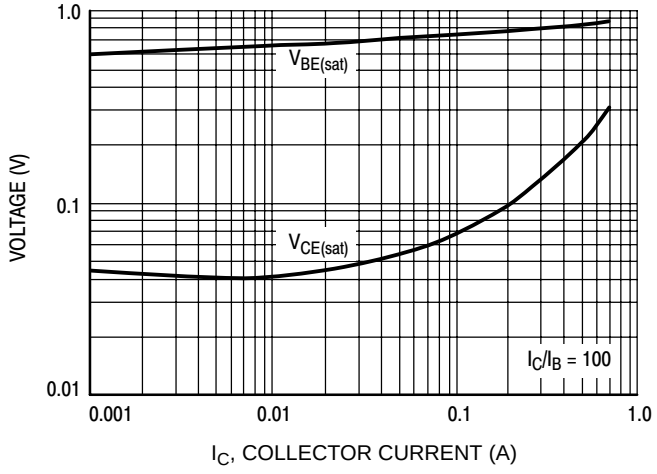



**Figure 5. “ON” Voltages**

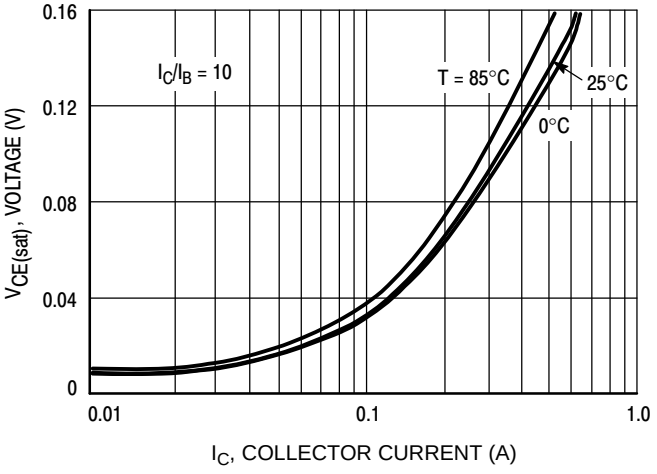



**Figure 6. Collector−Emitter Saturation Voltage**

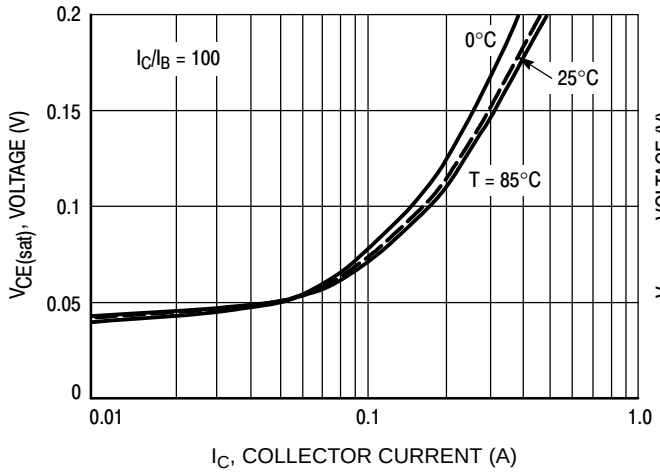



**Figure 7. Collector−Emitter Saturation Voltage**

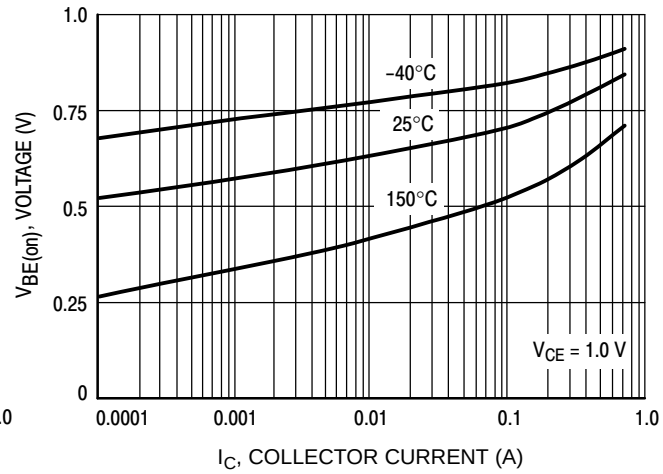



**Figure 8. $V_{BE(on)}$ Voltage**

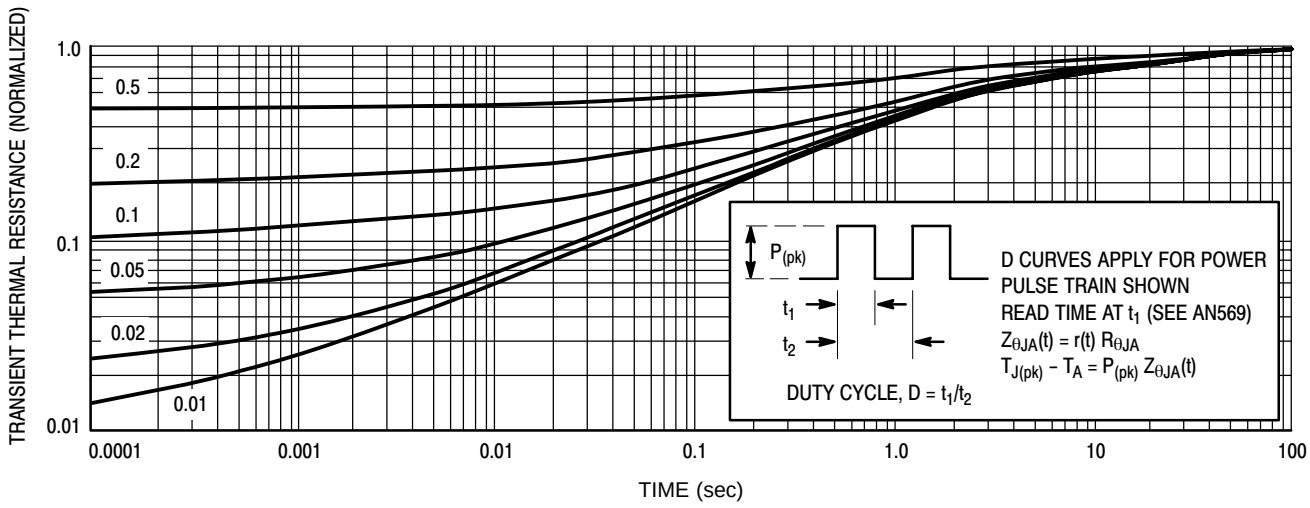
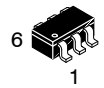



**Figure 9. Thermal Response Curve**

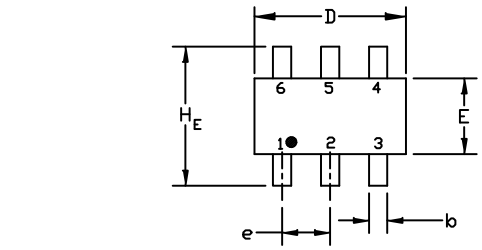
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



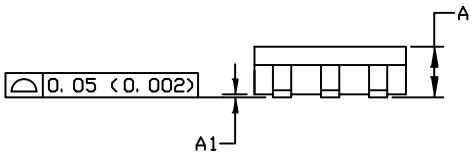
**SCALE 2:1**

**SC−74**
CASE 318F
ISSUE P

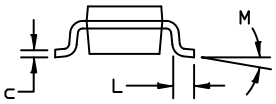
DATE 07 OCT 2021




TOP VIEW




SIDE VIEW

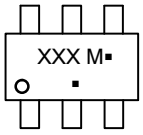



END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994
2. CONTROLLING DIMENSION: INCHES
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.90 | 1.00 | 1.10 | 0.035 | 0.039 | 0.043 |
| A1 | 0.01 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| b | 0.25 | 0.37 | 0.50 | 0.010 | 0.015 | 0.020 |
| c | 0.10 | 0.18 | 0.26 | 0.004 | 0.007 | 0.010 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E | 1.30 | 1.50 | 1.70 | 0.051 | 0.059 | 0.067 |
| e | 0.85 | 0.95 | 1.05 | 0.034 | 0.037 | 0.041 |
| $H_E$ | 2.50 | 2.75 | 3.00 | 0.099 | 0.108 | 0.118 |
| L | 0.20 | 0.40 | 0.60 | 0.008 | 0.016 | 0.024 |
| M | 0° | --- | 10° | 0° | --- | 10° |

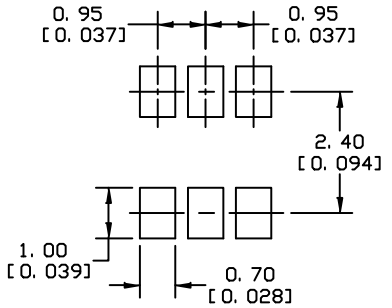
### GENERIC MARKING DIAGRAM*




XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.




* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOLDERING FOOTPRINT

STYLE 1:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 2:
PIN 1. NO CONNECTION
2. COLLECTOR
3. EMITTER
4. NO CONNECTION
5. COLLECTOR
6. BASE

STYLE 3:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 4:
PIN 1. COLLECTOR 2
2. EMITTER 1/EMITTER 2
3. COLLECTOR 1
4. EMITTER 3
5. BASE 1/BASE 2/COLLECTOR 3
6. BASE 3

STYLE 5:
PIN 1. CHANNEL 1
2. ANODE
3. CHANNEL 2
4. CHANNEL 3
5. CATHODE
6. CHANNEL 4

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 8:
PIN 1. EMITTER 1
2. BASE 2
3. COLLECTOR 2
4. EMITTER 2
5. BASE 1
6. COLLECTOR 1

STYLE 9:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 10:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 11:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SC−74** | **PAGE 1 OF 1** |

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