Evaluating the ADN4693E-1 3.3 V, 200 Mbps, Full-Duplex, High Speed M-LVDS Transceiver

FEATURES

- Easy evaluation of the ADN4693E-1 200 Mbps, full-duplex, M-LVDS transceiver
- Board layout optimized for high speed signaling
- Matched track lengths on M-LVDS differential pairs with controlled 100 Ω differential impedance
- Matched track lengths on high speed DI and RO logic signals with controlled 50 Ω impedance to GND
- SMA jacks for connecting to high speed DI and RO logic signals and the M-LVDS A, B, Y, and Z signals
- Optional screw terminal connectors for accessing the RO, $\overline{RE}$, DE, and DI logic signals
- Power and ground connections through screw terminal blocks
- Jumper-selectable driver enable and receiver enable via the $\overline{RE}$ and DE pins
- Test points for measuring all signals and multiple ground points to facilitate probing of multiple signals
- 100 Ω termination resistors across A and B signals and Y and Z signals to simulate a terminated bus

EQUIPMENT NEEDED

- A 4 channel oscilloscope
- A signal generator
- A 3.0 V to 3.6 V power supply

EVALUATION KIT CONTENTS

- EVAL-ADN4693E-1EBZ

GENERAL DESCRIPTION

The EVAL-ADN4693E-1EBZ allows quick and easy evaluation of the ADN4693E-1 200 Mbps, full-duplex, multipoint, low voltage differential signaling (M-LVDS) transceiver. The EVAL-ADN4693E-1EBZ allows the input and output functions of the transceiver to be exercised without the need for external components. Subminiature A (SMA) connectors provide convenient connections for high speed logic and the M-LVDS bus signals. Screw terminal blocks are available to access power, ground, and digital signals. Jumper options allow control of the driver and receiver enable pins of the transceiver.

The EVAL-ADN4693E-1EBZ is optimized for high speed signaling. The differential M-LVDS signal traces on the board are routed as length matched 100 Ω differential pairs. The EVAL-ADN4693E-1EBZ features a solid ground and power plane for optimum power integrity.

The EVAL-ADN4693E-1EBZ has a footprint for the ADN4693E-1 full-duplex transceiver in a 4 mm × 4 mm, 16-lead, lead frame chip scale package (LFCSP).

For full details on the ADN4693E-1, see the ADN4693E-1 data sheet, which must be used in conjunction with this user guide when using the EVAL-ADN4693E-1EBZ.

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REVISION HISTORY

3/2022—Revision 0: Initial Version

EVAL-ADN4693E-1EBZ EVALUATION BOARD PHOTOGRAPH

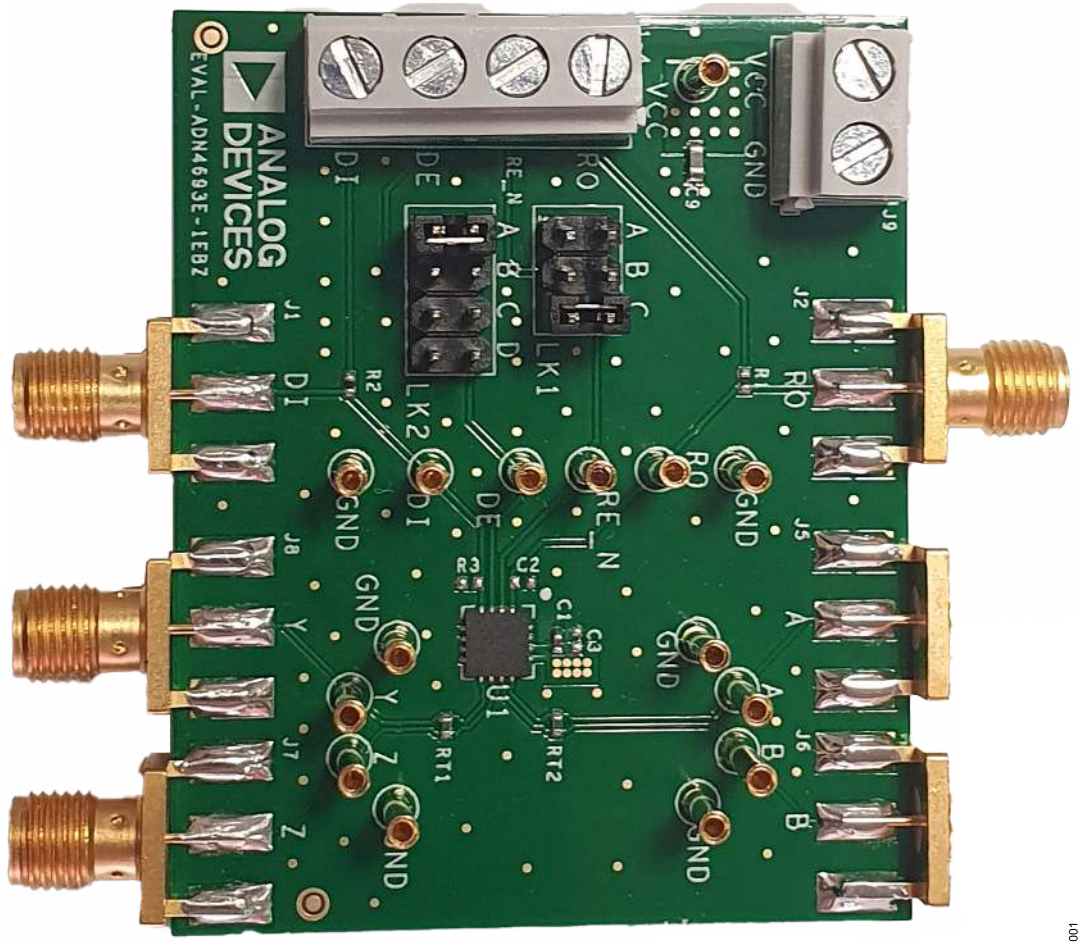

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Figure 1.

EVALUATION BOARD CONFIGURATION

SETTING UP THE EVALUATION BOARD

The EVAL-ADN4693E-1EBZ allows the ADN4693E-1 to be quickly and easily evaluated. The EVAL-ADN4693E-1EBZ allows all of the input and output functions to be exercised without the need for external components. Jumper configurations are shown in Table 3.

The EVAL-ADN4693E-1EBZ is powered by connecting a 3.3 V power supply to the VCC and GND connections of the J9 screw terminal block. The supply current is typically 1 mA with the driver and receiver disabled. A 10 µF decoupling capacitor, C9, is fitted at the VCC connector. A 100 nF decoupling capacitor, C1, is included at the supply pins of the ADN4693E-1, with a placeholder for an additional capacitor, C3.

The ADN4693E-1 full-duplex transceiver contains both a driver and receiver that can be individually enabled or disabled via jumper options. The driver can be enabled or disabled by setting the driver enable signal, DE, via the LK2 jumper. The receiver can be enabled or disabled by setting the $\overline{RE}$ signal, via the LK1 jumper. The DE and $\overline{RE}$ signals can also be accessed via the J1-4 screw terminal block for dynamic control via a processor or a signal generator.

For optimum signal integrity, the ADN4693E-1 digital input signal, DI, and receiver output signal, RO, are routed to the SMA connectors, J1 and J2, respectively. Alternatively the J1-4 screw terminal connectors can be used to access the DI and RO signals for easy wire connections to a microprocessor. The connections to the J1-4 screw terminal block are made via 0 Ω resistors, which can be removed to eliminate any stub lengths along the interconnect. The DI input is terminated to GND with a 50 Ω resistor, R3. The RO trace includes an optional placeholder for a load capacitor at C2.

The M-LVDS input signals, A and B, and M-LVDS output signals, Y and Z, are accessed via the J5, J6, J8, and J7 SMA connectors, respectively. These A and B signals and Y and Z signals are routed as two differential pairs with a differential characteristic impedance of 100 Ω. The M-LVDS input signals are terminated at the A and B pins of the ADN4693E-1 with the 100 Ω resistor, RT2. The M-LVDS output signals are terminated at the Y and Z pins of the ADN4693E-1 with the 100 Ω resistor, RT1.

An example evaluation of the ADN4693E-1 driver and receiver is shown in Figure 2. A signal generator is connected to the DI pin via the J1 SMA connector, with an input signal of 100 MHz, a 50% duty cycle, and a swing of between 0 V and 3.3 V. To enable both the driver and the receiver, the LK1 jumper is set to Position C, and the LK2 jumper is set to Position A. The J8 SMA connector for Pin Y is connected to the J5 SMA connector for Pin A, and the J7 SMA connector for Pin Z is connected to the J6 SMA connector for Pin B. This setup connects the M-LVDS driver and receiver together in a point to point loopback network. In addition, oscilloscope probes are connected to the DI, A, B, and RO testpoints.

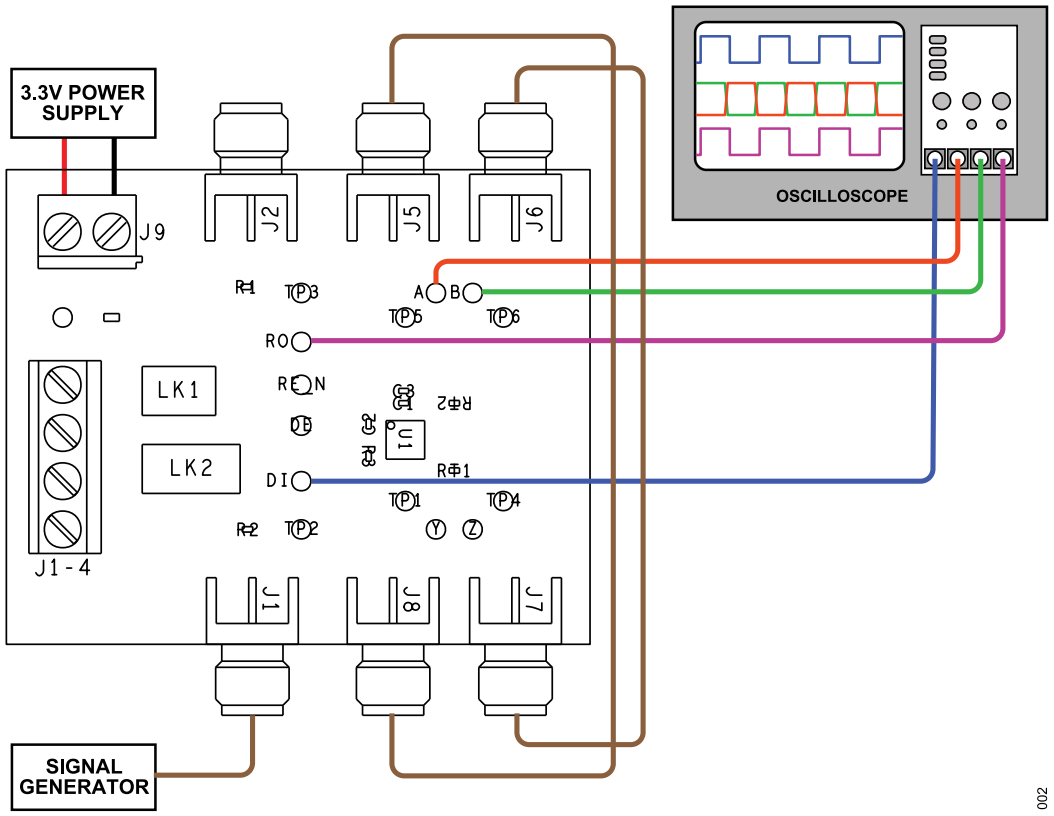

Figure 2. Example Evaluation of the ADN4693E-1 Driver and Receiver

EVALUATION BOARD CONFIGURATION

INPUT AND OUTPUT CONNECTIONS

Table 1 details the digital input and output connections, and Table 2 details the M-LVDS input and output connections.

Table 1. Digital I/O Connections

Connection	DI	RO
SMA Connector	J1	J2
Terminal Connector	J1-4 via R2	J1-4 via R1
Load Capacitor	None	C2 (not populated)
Termination Resistor	R3	None

Table 2. M-LVDS Input and Output Connections

	Receiver		Transmitter	
Connection	A	B	Y	Z
SMA Connector	J5	J6	J8	J9
Termination Resistor	RT2		RT1	

JUMPER CONNECTIONS

Table 3 details the jumper configurations.

Table 3. Jumper Configurations

Jumper	Position	Description
LK1	A	Connects the $\overline{RE}$ pin of the ADN4693E-1 to VCC, which disables the receiver. This places the RO output into a high impedance state.
	B	Connects the $\overline{RE}$ pin of the ADN4693E-1 to the $\overline{RE}$ connection on the J1-4 screw terminal connector.
	C	Connects the $\overline{RE}$ pin of the ADN4693E-1 to GND, which enables the receiver.
LK2	A	Connects the DE pin of the ADN4693E-1 to VCC, which enables the driver.
	B	Connects the DE pin of the ADN4693E-1 to the DE connection on the J1-4 screw terminal connector.
	C	Connects the DE pin of the ADN4693E-1 to GND, which disables the driver. This places the Y and Z outputs into a high impedance state.
	D	Connects the DE pin of the ADN4693E-1 to the $\overline{RE}$ pin of the ADN4693E-1. Set the state of both the DE and $\overline{RE}$ signals using the LK1 jumper.

EVALUATION BOARD SCHEMATIC AND LAYOUT

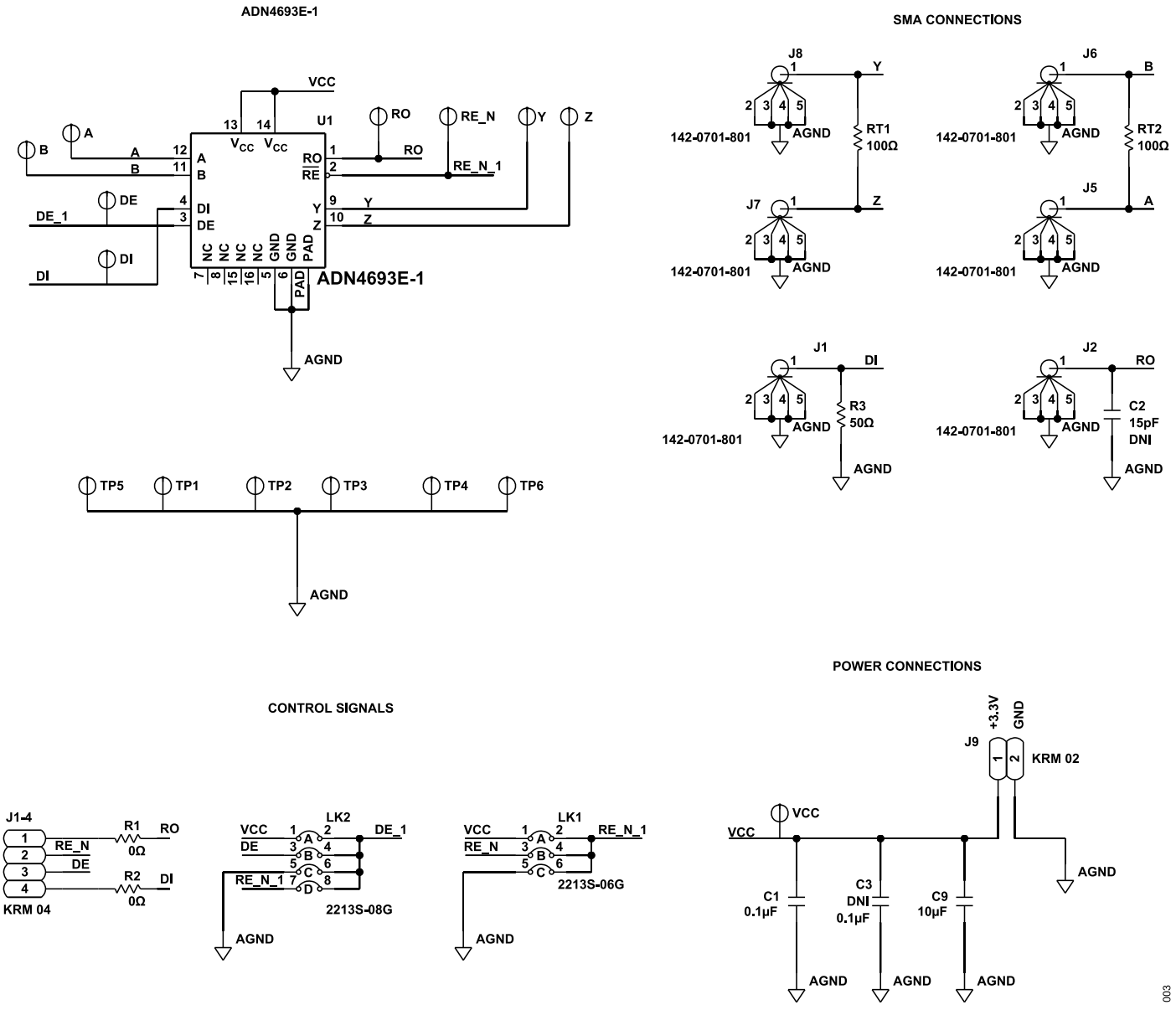

Figure 3. EVAL-ADN4693E-1EBZ Schematic

EVALUATION BOARD SCHEMATIC AND LAYOUT

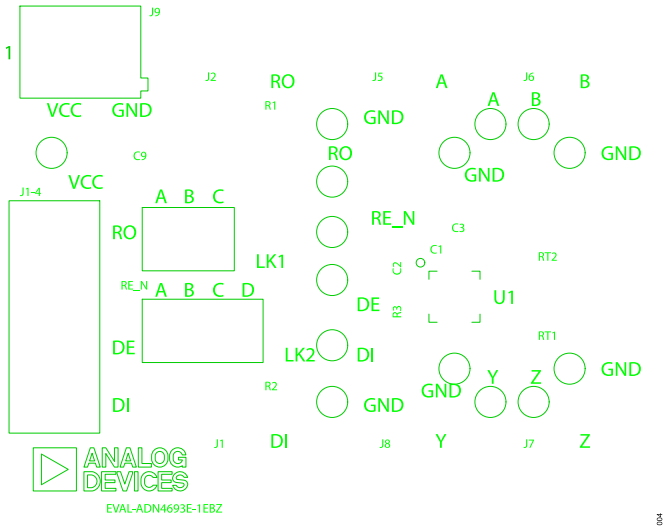

Figure 4. EVAL-ADN4693E-1EBZ Silkscreen

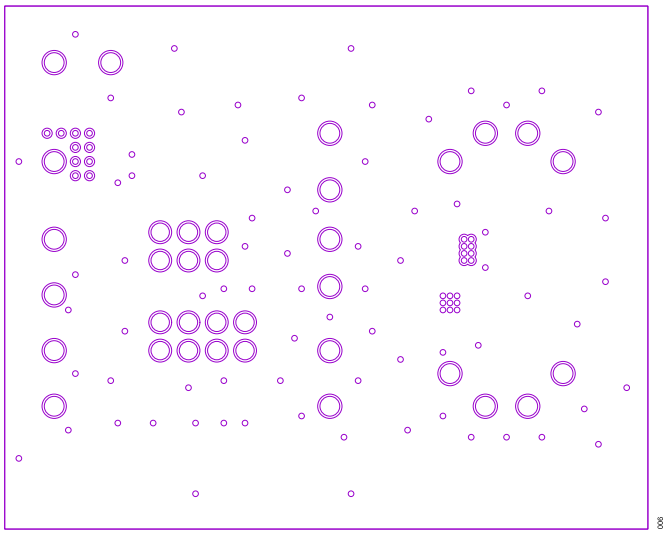

Figure 6. EVAL-ADN4693E-1EBZ Internal Layer 2 (GND)

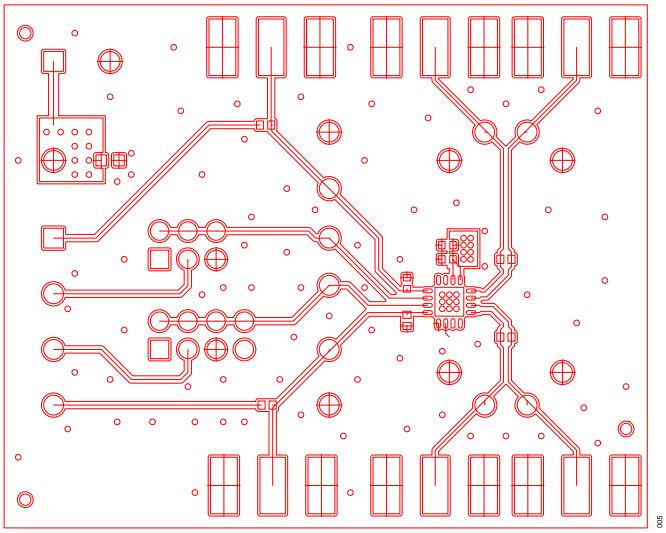

Figure 5. EVAL-ADN4693E-1EBZ Component Side

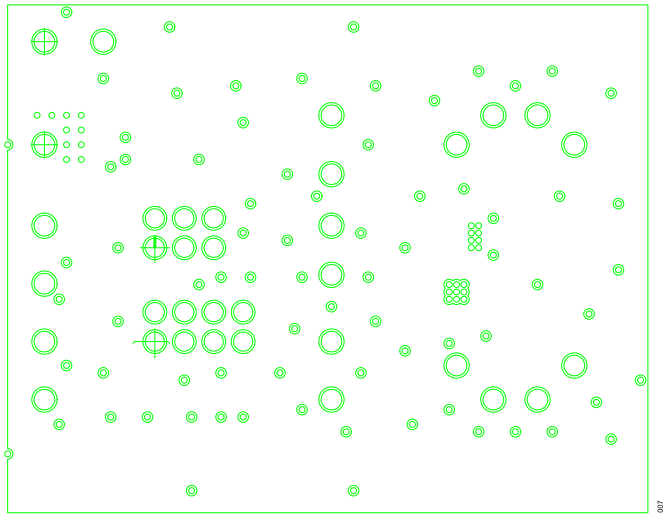

Figure 7. EVAL-ADN4693E-1EBZ Internal Layer 3 (VCC)

EVALUATION BOARD SCHEMATIC AND LAYOUT

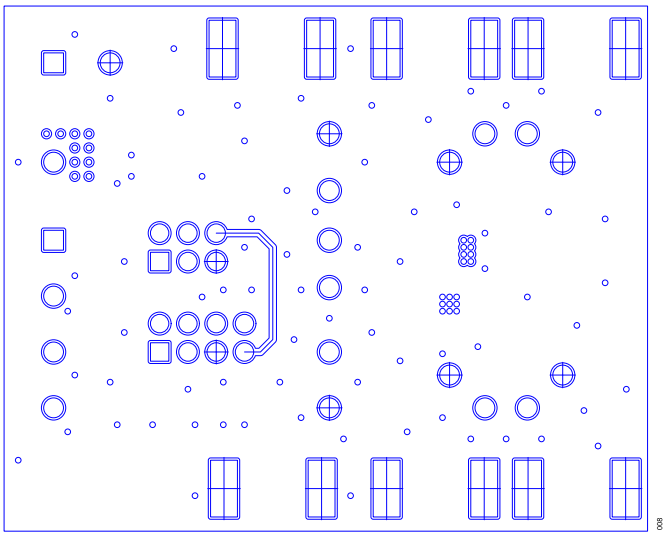

Figure 8. EVAL-ADN4693E-1EBZ Solder Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Quantity	Reference Designator	Description	Supplier and Part Number
6	J1, J2, J5, J6, J7, J8	Coaxial side launch SMA connectors	Cinch Connectivity 142-0701-801
1	C1	Capacitor, 0.1 µF, 0402	ATC 530L104KT16T
1	C9	Capacitor, 10 µF, 0603	Murata GRM188R60J106ME47D
1	LK1	3-pin (3 × 2), 0.1 inch header and shorting block	Multicomp 2213S-06G
1	LK2	4-pin (4 × 2), 0.1 inch header and shorting block	Multicomp 2213S-08G
1	J1-4	4-way terminal block	Lumberg Automation KRM 04
1	J9	2-way terminal block	Lumberg Automation KRM 02
2	RT1, RT2	Resistors, 100 Ω, 0402	Vishay FC0402E1000BST1
1	R3	Resistor, 49.9 Ω, 0402	FC0402E50R0BST1
2	R1, R2	Resistors, 0 Ω, 0402	Yageo RC0402JR-070RL
15	TP1 to TP6, A, B, DE, DI, RE_N, RO, VCC, Y, Z	Test points	Mill-Max Mfg. 0319-1-15-15-18-27-04-0
1	U1	200 Mbps, full-duplex, M-LVDS transceiver, 16-lead LFCSP	Analog Devices, Inc., ADN4693E-1BCPZ
2	C2, C3	Capacitors, do not install, 0402	Not applicable

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.