Reference Manual

VCM-DAS-1/2

Analog & Digital
Input/Output Module for
the PC/104 Bus

VERSALOGIC CORPORATION

VCM-DAS-1/2

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the PC/104 Bus

Model VCM-DAS-1/2

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REFERENCE MANUAL

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Table of Contents

Other References

Burr-Brown Corp., (800) 548-6132, http://www.burr-brown.com/
ADS7805 16-Bit A/D Converter

Analog Devices Inc., (800) 262-5643, http://www.analog.com/
AD8522 12-Bit D/A Converter
AD976 16-Bit A/D Converter (alternate vendor)

Integrated Device Technology Inc., (800) 345-7015, http://www.idt.com
74FCT16652T Parallel Port Interface Chip

PC/104 Consortium, (650) 903-8304, http://www.controlled.com/pc104
PC/104 Resource Guide

VersaLogic Corporation, (800) 824-3163, http://www.versalogic.com
Embedded PCI (PC/104-Plus*) Specification. Available on web site.*

Overview 1

This chapter introduces the VCM-DAS-1/2 Analog and Digital I/O Module, lists its features and specifications, and provides a brief overview of the installation and configuration process.

Using This Manual

Each chapter in this manual corresponds to a step in the installation and operation of the module.

Chapter 1 – Overview

Lists basic information, specifications, and system requirements. Use this chapter to familiarize yourself with the module and it's capabilities.

Chapter 2 – Configuration

Describes how to jumper the module.

Chapter 3 – Installation

Describes how to install the VCM-DAS-1/2. Also provides information on the external connections.

Chapter 4 – Registers

Provides programming details and register descriptions.

Chapter 5 – Operation

Provides details on how to operate the Analog Input, Analog Output, Digital I/O, Digital Pots, and EEPROM circuits. Some software examples are given.

Chapter 6 – Calibration and Diagnostics

Describes the procedure for calibrating the module and running the included diagnostic software.

Appendix A – Schematics

Circuit diagrams.

Introduction

The VCM-DAS-1/2 module provides 16 single-ended analog input channels, featuring fast 10 µs conversion times and ±5V or ±10V input ranges. Throughput up to 200 kHz may be realized with repeat conversions on one channel; up to 67KHz when scanning from channel to channel.

The VCM-DAS-1/2 also includes two 12-bit analog output channels. These channels may be jumpered independently for 0 to 5V or 0 to 10V output at 5 ma each. Digital data is written in a serial fashion to update the analog values.

Digital pots are used for calibrating the analog circuits. A 1K EEPROM is included to store the calibration values, and there is plenty of extra space in the EEPROM for general purpose use. The digital pots must be initialized whenever the computer system is reset.

In addition to the analog sections, the module also includes 16 digital I/O lines. These digital lines feature TTL type outputs with readback, and are compatible with optically isolated modular I/O racks.

Features

GENERAL

- +5V and ±12V supplies required
- Uses four electronic digital adjustment pots instead of manual pots
- Digital Pot settings are stored in an on-board 128 x 16 EEPROM
- Compatible with the industry standard 5B series of signal conditioners

ANALOG INPUT

- 16 channels
- 16-bit input resolution
- Single ended, high impedance inputs
- Electronic digital calibration
- Up to 200K samples/second (VCM-DAS-2), up to 100K samples/second (VCM-DAS-1)
- ±5V and ±10V input ranges
- On board timer for periodic readings
- Auto retrigger mode
- Auto Channel Increment Mode
- DMA support
- Compatible with industry standard 5B01 series signal conditioners

ANALOG OUTPUT

- 2 channels
- 12-bit resolution
- Electronic digital calibration
- 0-5V and 0-10V output range
- 40 µS update time
- Short circuit proof, 5ma output current

DIGITAL I/O

- Two 8-bit ports
- ±24 ma output drive
- Programmable read-only or read/write
- Opto 22 compatible
- EEPROM storage for user data

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Size: 3.8" x 3.6" (PC/104 standard)
0.6" component height

Storage Temperature:
–40°C to 85°C

Free Air Operating Temperature:
0°C to +60°C

Power Requirements: *(all digital outputs low [no external load], both analog outputs sourcing or sinking 5 ma ea.)*
5V ±5% @ 510 ma typ.
±12V ±5% @ ±20 ma typ.

Analog Input:

Channels:	16
Resolution:	16 bits, no missing codes
Accuracy:	±0.003% (±3 LSBs)
Input Mode:	Single ended
Range:	±5V or ±10V (jumper selectable, all channels the same)
Conversion Time:	10 μS (VCM-DAS-1), 5 μS (VCM-DAS-2)
Settling Time:	5 μS (applies only when switching channels)
Protection:	±35V overvoltage protection
Impedance:	$>10^{10}\Omega$, 20 pF
Retrigger Timer:	Programmable 20 μS, 50 μS, 100 μS, 250 μS, 500 μS, or 1 mS
Access:	Direct I/O

Analog Output:

Channels:	2
Range:	0 to 5V or 0 to 10V (jumper selectable, each channel independent)
Resolution:	12 bits
Accuracy:	±1.5 LSB
Update Time:	40 μS
Output Drive:	5 ma, 200 pF (each channel)
Access:	Bitwise serial

Digital I/O:

Channels:	16 (non-inverting)
Input Threshold:	TTL compatible
Architecture:	Totem pole output with readback
Output Drive (H):	–24ma @ 2.4V
Output Drive (L):	+24ma @ 0.55V
Signal Direction:	Byte programmable as input or output with readback
Short Protection:	Short circuit to ground, indefinite duration
Access:	Direct I/O

Digital Pots:

Organization:	4 pots used to calibrate analog section
Resolution:	256 settings
Access:	Serial

EEPROM:

Organization:	Sixty-four 16-bit words
Allocation:	Two words used for digital pots, 62 words available for general purpose storage
Access:	Bitwise serial

Bus Interface:

I/O Ports:	Occupies 16 ports on any 16-bit address boundary
Interrupt Channel:	IRQ10, IRQ11, or IRQ12
DMA Channel:	DMA5, DMA6, or DMA7

External Connectors:

Analog In/Out:	26-pin .1" dual-row header
Opto 22:	34-pin .1" dual-row header

Compatibility:

PC/104:	Full compliance, 16-bit data bus

Specifications are subject to change without notice.

Technical Support

If you have problems that this manual can't help you solve, contact VersaLogic for technical support at **(800) 824-3163 or (503) 747-2261**. You can also reach VersaLogic by e-mail at Support@versalogic.com.

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (800) 824-3163. Our standard turn-around time for repairs is five working days after we receive the product.

Please provide the following information:

- Your name, the name of your company, and your phone number
- The name of a technician or engineer who we can contact if we have questions
- Quantity of items being returned
- The model and serial number of each item (the serial number is a 5 digit bar code)
- A description of the problem
- Steps you have taken to resolve or repeat the problem
- The return shipping address

Warranty Repair All charges are covered, including UPS Ground shipping charges for return back to your facility.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges, and return shipping fees. We will need to know what shipping method you prefer for return back to your facility, and we will need to secure a purchase order number for invoicing the repair.

Note! Please mark the RMA number clearly on the outside of the box before returning.

2 Configuration

This chapter describes how to configure the on-board options for the VCM-DAS-1/2 module. Configuration involves both hardware (jumper) and software configuration. The jumpers set the base address for the module and configure the analog circuitry for various modes of operation. Software configuration completes the process by initializing the analog calibration pots every time the card is reset.

Warning! The VCM-DAS-1/2 module requires +5V, +12V, and –12V for normal operation. These voltages must be supplied through the PC/104 connector. Damage to on-board components will occur if all three voltages are not present at the same time.

Hardware Jumper Summary

Hardware option configuration is accomplished by installing or removing jumper plugs. In this chapter, the term “in” is used to indicate an installed jumper and “out” is used to indicate a removed jumper.

Use the following key to interpret the jumper diagrams used in this manual:

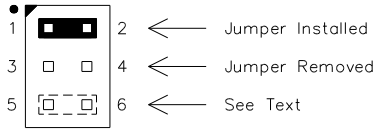


Figure 1. Jumpering Key

JUMPER BLOCK LOCATIONS

Note Jumpers are shown in as-shipped configuration.

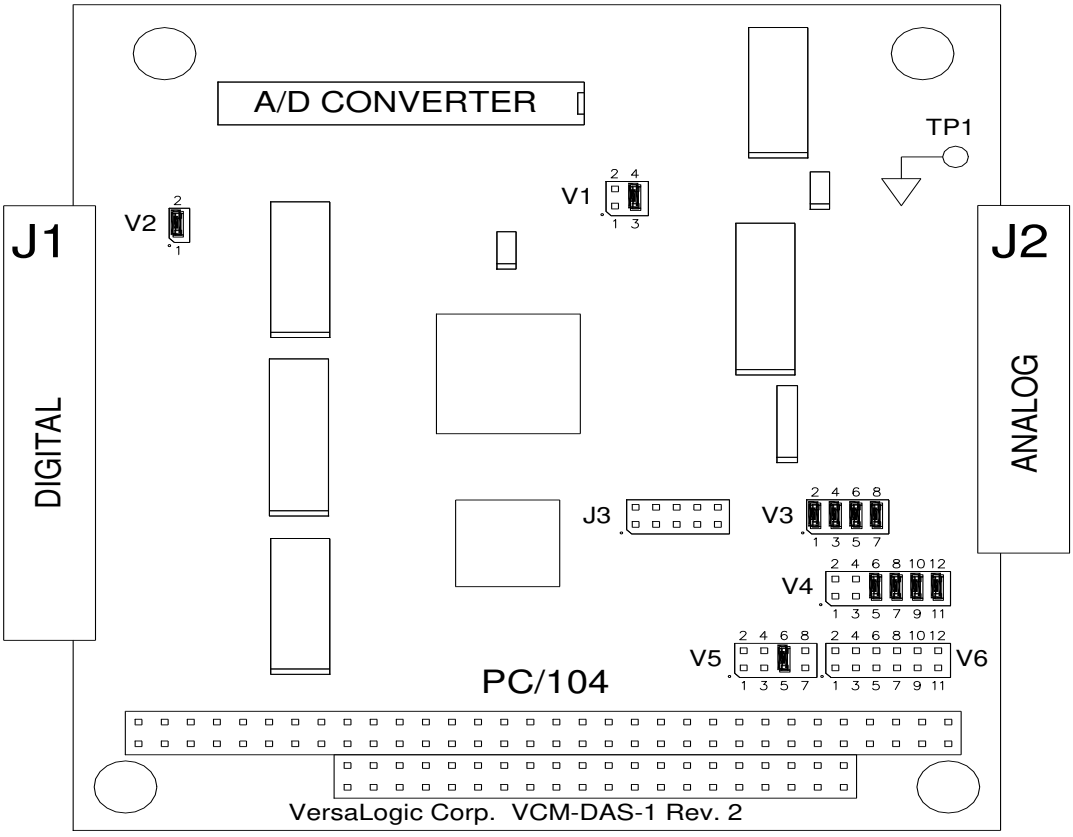
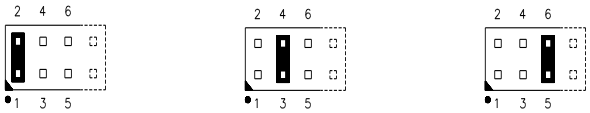
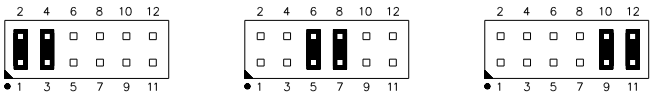


Figure 2. Jumper Block Locations

Table 1: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1[1-2]	**Input Voltage Range** In — ±5V Input Range Out — ±10V Input Range	Out	9
V1[3-4]	**Input Low Pass Filter** In — Enabled Out — Disabled	In	9
V2	**Opto 22 I/O Rack Power** In — I/O rack power provided by analog board Out — I/O rack power provided externally	In	13
V3[1-2]	**Analog Loopback (Channel 0)** In — Connects DAC 0 output to ADC 14 input for diagnostic loopback Out — Circuits operate independently	In	11
V3[3-4]	**Analog Output 0 Voltage Range** In — 0 to 10V Out — 0 to 5V	In	10
V3[5-6]	**Analog Output 1 Voltage Range** In — 0 to 10V Out — 0 to 5V	In	10
V3[7-8]	**Analog Loopback (Channel 1)** In — Connects DAC 1 output to ADC 15 input for diagnostic loopback Out — Circuits operate independently	In	11
V4	**Address Select (A4 – A9)** V4[1-2] In – A9 Decoded Low Out – A9 Decoded High V4[3-4] In – A8 Decoded Low Out – A8 Decoded High V4[5-6] In – A7 Decoded Low Out – A7 Decoded High V4[7-8] In – A6 Decoded Low Out – A6 Decoded High V4[9-10] In – A5 Decoded Low Out – A5 Decoded High V4[11-12] In – A4 Decoded Low Out – A4 Decoded High	300h	8
V5[1-2] V5[3-4] V5[5-6]	**Interrupt Request Select** IRQ 10 IRQ 11 IRQ 12 	IRQ 12	14
V5[7-8]	**Shared Interrupt Configuration** In — Shared interrupts Out — Normal interrupts	Out	
V6	**DMA Channel Select** DMA 5 DMA 6 DMA 7 	None	16

Module Addressing

As shipped, the module is configured for a base address of 300h. The card occupies 16 consecutive I/O addresses (0300h to 030Fh). Ten of these addresses are mapped to control, data, and status registers. The remaining six addresses occupy positions in I/O space, but are not assigned to registers. See the Registers description section on page 23 for further register information.

The base address can range from 000h to 3F0h on any 10h address boundary. Use the table below to select the jumpering for the appropriate upper and middle hex digits of the three digit base address (i.e., "1" and "4" = 140h).

Note The lower digit is always "0".

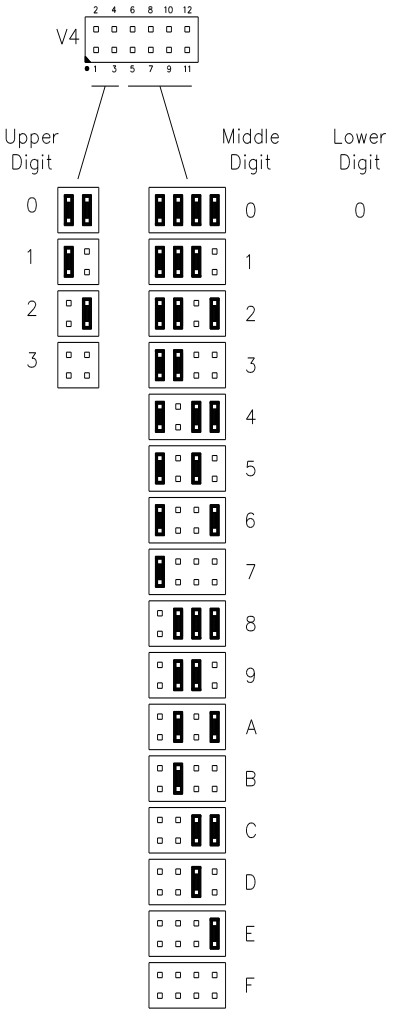


Figure 3. Jumper Block Locations

Analog Input Configuration

INPUT RANGE

The module may be operated with an input range of ±5 volts or ±10 volts. To achieve the maximum digital resolution and to prevent saturation, the range which most closely matches the input signal should be chosen. All channels operate with the same input range.

As shipped, the board is configured for ±5 volt input.

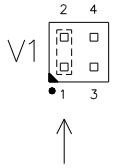


Table 2: Input Range Jumper

Jumper Block	Description	As Shipped
V1[1-2]	**Input Voltage Range** In — ±5V Input Range Out — ±10V Input Range	Out

LOW PASS FILTER

A 1 MHz low pass filter between the instrumentation amplifier and the A/D converter can be selected to reject high frequency noise.

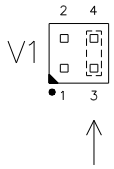


Table 3: Low Pass Filter Jumper

Jumper Block	Description	As Shipped
V1[3-4]	**Input Low Pass Filter** In — Enabled Out — Disabled	In

Analog Output Configuration

The VCM-DAS-1/2 module features two unipolar analog output channels. Both channels are single-ended and are referenced to analog ground. The digital data format is straight binary.

OUTPUT RANGE

Each output channel can be configured independently to produce a unipolar output voltage range of 0-5 volts or 0-10 volts as shown below.

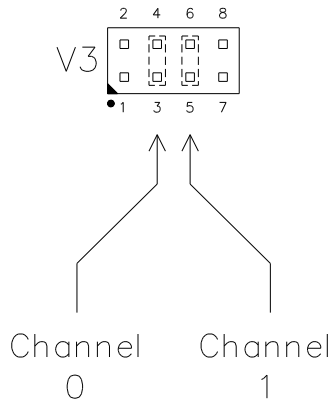


Table 4: Output Range Jumpers

Jumper Block	Description	As Shipped
V3[3-4]	**Analog Output Voltage Range (Channel 0)** In — 0 to 10V Out — 0 to 5V	In
V3[5-6]	**Analog Output Voltage Range (Channel 1)** In — 0 to 10V Out — 0 to 5V	In

ANALOG LOOPBACK

The two output channels can be connected (looped back) to two input channels for a direct readback of the voltage, or to provide analog output to a 5B01 signal conditioning rack. Analog loopback is also useful for diagnostic and calibration purposes.

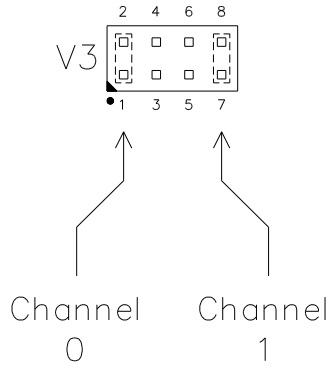


Table 5: Analog Loopback Jumpers

Jumper Block	Description	As Shipped
V3[1-2]	**Analog Loopback (Channel 0)** In — Connects DAC 0 output to ADC 14 input for diagnostic loopback Out — Circuits operate independently	In
V3[7-8]	**Analog Loopback (Channel 1)** In — Connects DAC 1 output to ADC 15 input for diagnostic loopback Out — Circuits operate independently	In

5B01 Analog Signal Conditioning Rack

When using a 5B01 series analog signal conditioning rack, the input range should be set to ±5V. If output channels are used, the Analog Loopback jumpers must be inserted and the output range configured for ±5V operation.

Note: It is important to configure your 5B01 signal conditioning rack so that analog ground on the rack is connected to the eight analog ground signals on the interface connector. Most racks include a jumper or cutable trace for this purpose, which must be installed (shown as "A" below).

To prevent ground loops, it is important that analog and digital grounds be connected together at only one point in the system. The VCM-DAS-1/2 brings these grounds together on the module circuitry itself, therefore any external connections between the two ground systems must be avoided. Most racks include a jumper or cutable trace that must be removed (shown as "D" below).

Warning! To prevent analog output channel 0 from shorting to ground, it is very important to properly configure your 5B01 signal conditioning rack so that pin 25 is disconnected. Most racks include jumpers or cuttable traces that must be removed to leave pin 25 floating (shown as "B" and "C" below).

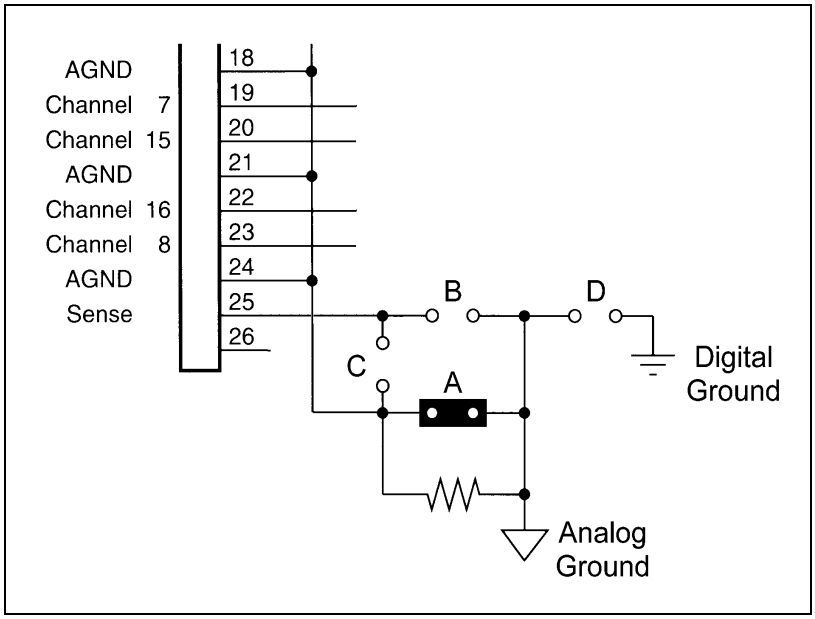


Figure 4. 5B01 Analog Signal Conditioning Rack

Digital Input/Output Configuration

The VCM-DAS-1/2 has 16 digital I/O lines that can be programmed in groups of eight as inputs or outputs with readback. The I/O connector is compatible with 8 and 16 position modular I/O racks.

RACK POWER CONTROL

The VCM-DAS-1/2 module includes provisions for powering the external I/O rack assembly with +5 volts at 500 ma.

When jumper V2 is installed, the I/O rack power line (I/O rack pin 49) is connected directly to +5 volts on the PC/104 Bus. If the I/O rack is powered by a separate external supply, either a jumper from the I/O rack or the V2 jumper must be removed.

Warning! The +5 volt power output from the VCM-DAS-1/2 card can be shorted to ground if the connector is not correctly oriented at either end of the interface cable. The use of keys in the connectors, or very clear markings on the connectors, is recommended to prevent backwards connection of the cable.

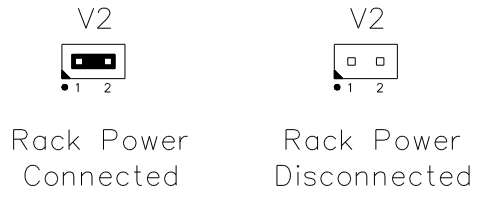


Table 6: Opto 22 Rack Power Jumper

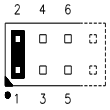
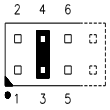
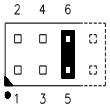
Jumper Block	Description	As Shipped
V2	**Opto 22 I/O Rack Power** In — I/O rack power provided by analog board Out — I/O rack power provided externally	In

Interrupt Configuration

IRQ SELECTION

Jumper V5 connects the interrupt request signal (analog input conversion complete) to one of three PC/104 Bus interrupt request lines. The choice of which jumper position to choose depends upon the capabilities of the CPU or interrupt controller used in the system.

Table 7: Interrupt Request Jumpers

Jumper Block	Description	As Shipped
V5[1-2] V5[3-4] V5[5-6]	**Interrupt Request Select** IRQ 10  IRQ 11  IRQ 12 	IRQ 12

SHARED INTERRUPT CONFIGURATION

Jumper V5[7-8] inserts a 1KΩ pull-down resistor into the IRQ circuit for applications using shared IRQs.

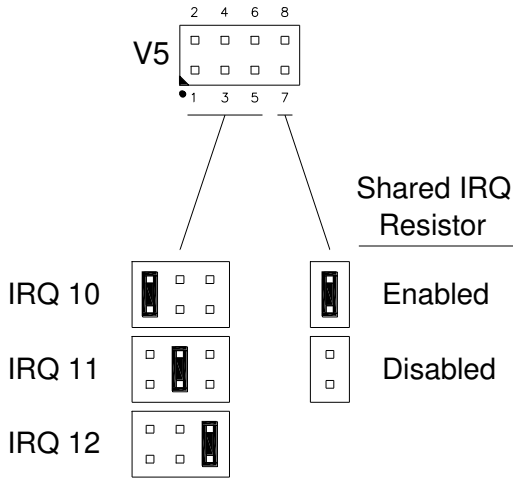


Table 8: Shared Interrupt Jumper

Jumper Block	Description	As Shipped
V5[7-8]	**Shared Interrupt Configuration** In — Shared interrupts Out — Normal interrupts	Out

ABOUT SHARED INTERRUPTS

REGULAR INTERRUPTS

- Sources are totem-pole drivers
- Interrupt controller is set to edge trigger mode
- Interrupts are requested by driving the IRQ line from low-to-high (positive edge triggering)
- The CPU has a 4.7K pull-up resistor on each IRQ line to prevent stray interrupts on unused inputs. Unused IRQ lines assume a high state.
- Only one interrupt source per IRQ line
- The IRQ line can be left in a high or low state when not requesting interrupts. It is common practice, however, to leave the line in the low state.
- A new interrupt is requested by lowering the IRQ line and raising it again

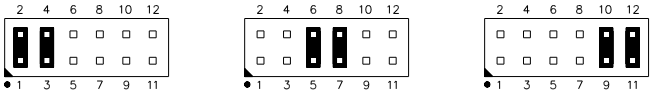
SHARED INTERRUPTS

- Sources are tri-statable, totem-pole drivers with the input tied high
- Interrupt controller is set to level trigger mode
- The CPU has a 4.7K pull-up resistor on each IRQ line to prevent stray interrupts on unused inputs. Unused IRQ lines assume a high state.
- Each source has a 1K pull-down resistor tied to the IRQ line through a series jumper. Only one shared device per IRQ line should have the jumper installed. The pull-down resistor fights against the 4.7K pull-up resistor on the CPU, but the 1K wins, causing the IRQ line to assume a low state.
- Interrupts are requested by enabling the tri-state driver. This drives the IRQ line from low-to-high.
- The source must work against the pull-down resistor
- Multiple sources are allowed per IRQ line. Software must distinguish which device made the interrupt request by polling the hardware within the Interrupt Service Routine.
- When not requesting an interrupt, the tri-statable driver must be disabled. This leaves the IRQ line in a low state, allowing other sources on the same IRQ line to make requests of their own.

DMA Configuration

The VCM-DAS-1/2 can be setup to generate a DMA transfer request upon analog input conversion complete. These requests can be routed to DMA channel 5, 6, or 7 depending upon the configuration of jumper V6.

Table 9: DMA Channel Selection Jumpers

Jumper Block	Description	As Shipped
V6	**DMA Channel Select** DMA 5 DMA 6 DMA 7 	None

Installation 3

Handling

After removing the module from its protective wrapper, place the module on a grounded, static-free surface, component side up. Use an anti-static foam pad if available. Do not slide the board over any surface.

The module should also be protected during shipment or storage with anti-static foam and conductive bubble wrap.

Warning! The VCM-DAS-1/2 is designed for reliability, however, electrostatic discharge (ESD) can damage on-board components. When handling the module, standard ESD procedures should be observed. If an ESD station is not available, you can provide some ESD protection by wearing a grounded antistatic wrist strap.

Arranging the PC/104 Stack

1. Turn the system power off. Installing or removing modules from the PC/104 stack while the power is on may damage the system.
2. The VCM-DAS-1/2 module can occupy any stack position, however, if the stack contains PC/104-Plus modules, the VCM-DAS-1/2 module should be plugged on top of these cards.
3. Additional stack-through modules can be stacked on top of the VCM-DAS-1/2. Up to six PC/104 modules can be added. If a non-stack-through module is used, it must be topmost module on the stack.

Signal Levels

Connector J1 is the digital input/output connector. Each circuit is a tri-statable totem-poll TTL driver with a 10K ohm pull up resistor to +5V. Input gates are attached to each output signal for read-back. Signal direction is determined by the DIRHI and DIRLO bits in the CONTROL register. External equipment attached to connector J1 must be able to sink 500 µA @ 5V per channel. The maximum non-destructive input voltage applied to any channel is +5V.

Connector J2 is the analog input and output connector. All analog input signals are single ended analog level signals measured with respect to analog ground. The maximum non-destructive input voltage applied to any of the inputs is ±16.5V. Each analog channel presents a minimum input impedance of 16K ohms.

External Connectors

CONNECTOR FUNCTIONS

Table 10: Connector Functions

Connector	Function
J1	Digital I/O Connector
J2	Analog I/O Connector

CONNECTOR LOCATIONS

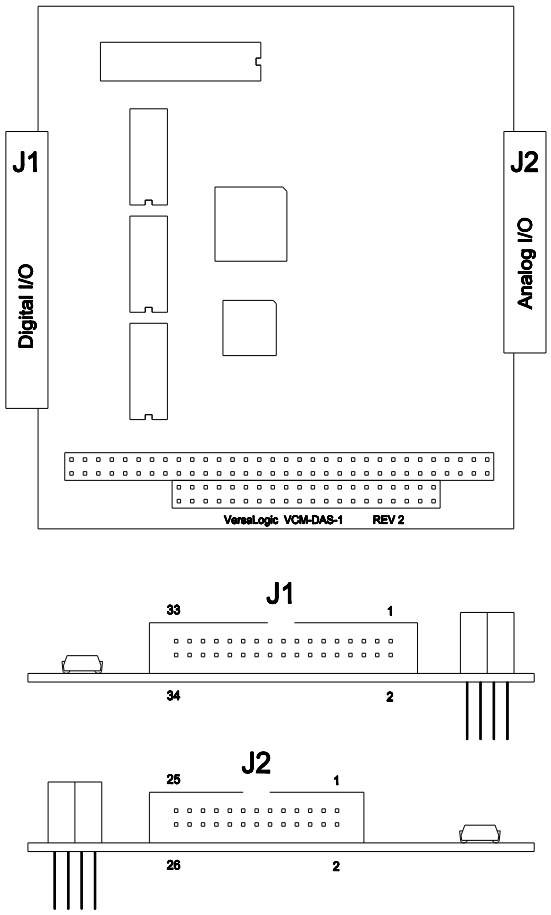


Figure 5. Connector Locations

MATING CONNECTORS AND CABLE ASSEMBLIES

Connections to the VCM-DAS-1/2 can be made using 0.05" pitch flat ribbon cable with 0.1" mass-terminated mating connectors. One cable for J2 is available from VersaLogic for development work, however, you will probably want to make your own custom cable to more closely match the requirements of your embedded computer project.

Table 11: Mating Connectors and Cable Assemblies

Connector	Mating Connector
J1 (Digital I/O)	Std. 34-pin 0.1 in. IDC header, 3M 3414-6634 or equivalent
J2 (Analog I/O)	Std. 26-pin 0.1 in. IDC header, 3M 3399-6626 or equivalent

J1 – DIGITAL I/O CONNECTOR

Table 12: Digital I/O Connector Pinout

J1 Pin	Signal Name	Opto 22 Function
1	DIO0	MOD15*
2	Digital Ground	Digital Ground
3	DIO1	MOD14*
4	Digital Ground	Digital Ground
5	DIO2	MOD13*
6	Digital Ground	Digital Ground
7	DIO3	MOD12*
8	Digital Ground	Digital Ground
9	DIO4	MOD11*
10	Digital Ground	Digital Ground
11	DIO5	MOD10*
12	Digital Ground	Digital Ground
13	DIO6	MOD9*
14	Digital Ground	Digital Ground
15	DIO7	MOD8*
16	Digital Ground	Digital Ground
17	DIO8	MOD7*
18	Digital Ground	Digital Ground
19	DIO9	MOD6*
20	Digital Ground	Digital Ground
21	DIO10	MOD5*
22	Digital Ground	Digital Ground
23	DIO11	MOD4*
24	Digital Ground	Digital Ground
25	DIO12	MOD3*
26	Digital Ground	Digital Ground
27	DIO13	MOD2*
28	Digital Ground	Digital Ground
29	DIO14	MOD1*
30	Digital Ground	Digital Ground
31	DIO15	MOD0*
32	Digital Ground	Digital Ground
33	Power	Power
34	Digital Ground	Digital Ground

MOD0* – MOD15*. Opto 22 bi-directional interface signals. Each signal consists of a tri-statable totem-poll TTL driver with a 10KΩ pull up resistor to +5V. Input gates are attached to each output signal for read-back. Signal direction is determined by the DIRHI and DIRLO bits in the CONTROL register.

Power. +5V power output. When jumper V5 is installed, up to 500 mA can be drawn from this +5V output to power the Opto 22 interface rack or other external equipment. If the I/O rack is powered by a separate external supply, the power jumper on the I/O rack or the V2 jumper must be removed. See page 13 for further information.

Digital Ground. All signals on connector J1 are referenced to these digital ground connections. The use of all ground connections is recommended to maintain a high degree of signal integrity.

J2 – ANALOG I/O CONNECTOR

Table 13: Analog I/O Connector Pinout

J2 Pin	Signal Name	Function
1	CH0	Channel 0 Input
2	CH8	Channel 8 Input
3	AGND	Analog Ground
4	CH9	Channel 9 Input
5	CH1	Channel 1 Input
6	AGND	Analog Ground
7	CH2	Channel 2 Input
8	CH10	Channel 10 Input
9	AGND	Analog Ground
10	CH11	Channel 11 Input
11	CH3	Channel 3 Input
12	AGND	Analog Ground
13	CH4	Channel 4 Input
14	CH12	Channel 12 Input
15	AGND	Analog Ground
16	CH13	Channel 13 Input
17	CH5	Channel 5 Input
18	AGND	Analog Ground
19	CH6	Channel 6 Input
20	CH14	Channel 14 Input
21	AGND	Analog Ground
22	CH15	Channel 15 Input
23	CH7	Channel 7 Input
24	AGND	Analog Ground
25	DA0V	Channel 0 Output
26	DA1V	Channel 1 Output

Channel 0 to 15 Input. Analog voltages are applied to these inputs for A/D conversion. All inputs are single-ended, and are referenced to Analog Ground.

Analog Ground. This signal is the on-board analog ground. All signals on J2 are referenced to this signal. The use of multiple Analog Ground signals is recommended to maintain a high degree of signal integrity.

Channel 0 & 1 Output. Analog voltage outputs referenced to analog ground. Each signal can source or sink up to 5 mA.

4 Registers

Introduction

This section includes information about registers, control and status bits, and data formats. It focuses primarily on the individual registers, the bits contained within them, and their functional descriptions. The VCM-DAS-1/2 contains two different sets of registers, those that occupy standard I/O ports, and those that are part of an on-board Serial Peripheral Interface (SPI) bus. Devices on the SPI bus include both analog output channels, the EEPROM, and four digital calibration pots.

I/O Port Mapping

The VCM-DAS-1/2 occupies 16 ports in the I/O map. Ten I/O ports are mapped to functional registers, the remaining six I/O ports are decoded by the board, and cannot be used by other PC/104 Modules.

Table 14: I/O Port Addresses

Write Register	Read Register	I/O Port Address	As Shipped Address
—	—	Board Address + 15	030Fh
—	—	Board Address + 14	030Eh
—	—	Board Address + 13	030Dh
—	—	Board Address + 12	030Ch
—	—	Board Address + 11	030Bh
—	—	Board Address + 10	030Ah
SPIWDAT	SPIRDAT	Board Address + 9	0309h
SPISEL	—	Board Address + 8	0308h
PARWHI	PARRHI	Board Address + 7	0307h
PARWLO	PARRLO	Board Address + 6	0306h
—	ADCHI	Board Address + 5	0305h
—	ADCLO	Board Address + 4	0304h
ADCPTR	—	Board Address + 3	0303h
ADCCVT	—	Board Address + 2	0302h
ADCSEL	—	Board Address + 1	0301h
CONTROL	ADCSTAT	Board Address + 0	0300h

I/O PORT REGISTER FUNCTIONS

The following table lists the functions assigned to each read and write I/O port register.

Table 15: Register Functions

Write Register	Description	Page
SPIWDAT	Write Data to Analog Output Channels, Digital Pots, and EEPROM	27
SPISEL	Serial Peripheral Interface (SPI) Chip Select Register and DAC Load	28
PARWHI	Parallel Port Data High (Opto 22 Modules 0-7)	47
PARWLO	Parallel Port Data Low (Opto 22 Modules 8-15)	47
ADCPTR	Analog Input Periodic Trigger Rate	30
ADCCVT	Triggers Analog Input Conversion, Clears Done Bit	31
ADCSEL	Analog Input Channel Select, Scan Range Limit	32
CONTROL	Analog Input Interrupt, DMA, Trigger Modes, Auto Increment, Parallel Port Direction	34

Read Register	Description	Page
SPIRDAT	Read Data from EEPROM	–
PARWHI	Parallel Port Data High (Opto 22 Modules 0-7)	47
PARWLO	Parallel Port Data Low (Opto 22 Modules 8-15)	47
ADCHI	Analog Input High Data Byte	37
ADCLO	Analog Input Low Data Byte	38
ADCSTAT	A/D Busy, A/D Done	36

Serial Port Interface (SPI) Register Functions

The following table lists the functions assigned to each register accessible through the Serial Port Interface (SPI). These registers are accessed in a serial fashion by manipulating the SPIWDAT, SPISEL, and SPIRDAT registers.

Table 16: Register Functions

Write Register	Description	
ADOFSET	Analog Input Offset Digital Pot	(DPOT#1)
DA0GAIN	Analog Output Channel 0 Gain Digital Pot	(DPOT#2)
ADGAIN	Analog Input Gain Digital Pot	(DPOT#3)
DA1GAIN	Analog Output Channel 1 Gain Digital Pot	(DPOT#4)
DA0DATA	Analog Output Channel 0 Data Register	
DA1DATA	Analog Output Channel 1 Data Register	
WDATA	Data to be stored in EEPROM	
ADDRESS	EEPROM address	
OPCODE	Operation code used to specify EEPROM read, write, and erase functions.	

Read Register	Description
RDATA	Data read from EEPROM

SPI READ DATA REGISTER

SPIRDAT (READ) 0309h

D7	D6	D5	D4	D3	D2	D1	D0
—	—	—	—	—	—	—	RDATA

This register is used to read data from the serial EEPROM. Operational details regarding the serial EEPROM chip exceed the scope of this manual. The user is encouraged to use the C/C++ software functions provided with the VCM-DAS-1/2 to access EEPROM contents.

Table 17: SPIRDAT Bit Assignments

Bit	Mnemonic	Description
D7-D1	—	**Unused** — These bits have no function.
D0	RDATA	**Read Data** — Serial read data from the SPI. Data read from this bit returns stored information from the EEPROM. In certain modes, this bit is also used to indicate EEPROM busy status.

SPI WRITE DATA REGISTER

SPIWDAT (WRITE) 0309h

D7	D6	D5	D4	D3	D2	D1	D0
—	—	—	—	—	—	—	WDATA

This register is used to write data to the various devices on the serial peripheral interface. Each device contains a shift register which receives data written to the WDATA bit. You must first select which chip is to receive the data by writing to the SPISEL register.

Table 18: SPIWDAT Bit Assignments

Bit	Mnemonic	Description
D7-D1	—	**Unused** — These bits have no function.
D0	WDATA	**Write Data** — Serial write data to the SPI. Data written to this bit is clocked into the shift register of the selected SPI device.

SPI SELECT REGISTER

SPISEL (WRITE) 0308H

D7	D6	D5	D4	D3	D2	D1	D0
—	—	—	—	DACLOAD	EESEL	DPOTSEL	DACSEL

This register is used to select which device on the serial peripheral interface (SPI) bus should receive data written to the SPIWDAT register. Bit D3 (DACLOAD) is used to transfer the contents of the analog output shift register(s) to the A/D converter(s), causing an output voltage update.

Table 19: SPISEL Bit Assignments

Bit	Mnemonic	Description
D7-D4	—	**Unused** — These bits have no function.
D3	DACLOAD	**Analog Output Data Load** — This control bit is used to transfer the analog output data from the DAC shift register to the D/A converters. Data is transferred on the 0 to 1 transition of this bit. DACLOAD = 0 Both analog output channels remain stable. DACLOAD = 1 The Analog Output Data stored in the Analog Output Shift Register (DACSR) is transferred to the appropriate D/A converter(s) as determined by the A and B bits in DACSR. Output voltage change(s) occurs immediately. **NOTE:** The update occurs when DACLOAD changes from 0 to 1. DACLOAD should be reset to "0" prior to loading new data into the DACSR register.
D2	EESEL	**EEPROM Chip Select** — This control bit selects the EEPROM chip for serial data transfer. EESEL = 0 EEPROM chip ignores the serial data interface. EESEL = 1 EEPROM chip responds to serial data interface reads and writes.
D1	DPOTSEL	**Digital Pot Chip Select** — This control bit selects the digital pot chip for serial data transfer. DPOTSEL = 0 Digital pot chip ignores the serial data interface. DPOTSEL = 1 Digital pot chip responds to serial data interface reads and writes.
D0	DACSEL	**Analog Output Chip Select** — This control bit selects the analog output chip for serial data transfer. DACSEL = 0 Analog output chip ignores the serial data interface.. DACSEL = 1 Analog output chip responds to serial data interface writes.

Analog Input Registers

The following table lists the functions assigned to each analog input read and write register.

Table 20: Register Functions

Write Register	Description	Page
ADCPTR	Analog Input Periodic Trigger Rate	30
ADCCVT	Triggers Analog Input Conversion, Clears Done Bit	31
ADCSEL	Analog Input Channel Select, Scan Range Limit	32
CONTROL	Analog Input Interrupt, DMA, Trigger Modes, Auto Increment, Parallel Port Direction	34

Read Register	Description	Page
ADCHI	Analog High Data Byte	37
ADCLO	Analog Low Data Byte	38
ADCSTAT	A/D Busy, A/D Done	36

ADC PERIODIC TRIGGER RATE REGISTER

ADCPTR (WRITE) 0303H

D7	D6	D5	D4	D3	D2	D1	D0
—	—	—	—	—	TR2	TR1	TR0

This register specifies the periodic trigger rate for applications which need analog input conversions at predetermined intervals.

Table 21: ADCPTR Bit Assignments

Bit	Mnemonic	Description
D7-D3	—	**Unused** — These bits have no function.
D2-D0	TR2-TR0	**Trigger Rate** — These bits set the periodic trigger rate. **TR2 TR1 TR0 Counts Triggering Rate** 0 0 0 128 15.3 Microseconds 0 0 1 256 30.4 Microseconds 0 1 0 512 60.9 Microseconds 0 1 1 1024 122.2 Microseconds 1 0 0 2048 244.5 Microseconds 1 0 1 4096 491.5 Microseconds 1 1 0 8192 982.9 Microseconds **Note:** The triggering rate is determined by counting PC/104 bus clocks (which are supplied by the CPU). The times given above are based on an 8.333 MHz bus clock.

ADC CONVERT REGISTER

ADCCVT (WRITE) 0302H

D7	D6	D5	D4	D3	D2	D1	D0
—	—	—	—	—	—	—	CMD

The ADCCVT register is a write register which is used to trigger an A/D conversion under software control.

Note: A word-wide output instruction to the ADCSEL register (out dx,ax) also writes into the ADCCVT register causing channel addressing and triggering with one CPU instruction.

Table 22: ADCCVT Bit Assignments

Bit	Mnemonic	Description
D7-D1	—	**Unused** — These bits have no function.
D0	CMD	**Command** — This control bit has two functions. CMD = 0 Clears the BUSY bit in the ADCSTAT register and cancels the interrupt request signal. Normally this is a seldom used function because reading data from the ADCHI register performs these actions. The most common use of this command is to remove the interrupt request signal when operating the board in DMA mode. CMD = 1 Triggers (starts) an A/D conversion. Writing a 1 to this bit causes an A/D conversion to start. It is not necessary to write a 0 before triggering the next conversion. **Note:** Proper operation dictates that A/D conversions should only be triggered when the A/D converter is idle (i.e., the BUSY bit in the ADCSTAT register = 0). Retriggering a conversion while one is underway is not recommended.

ADC SELECT REGISTER

ADCSEL (WRITE) 0301H

D7	D6	D5	D4	D3	D2	D1	D0
—	—	SL1	SL0	SEL3	SEL2	SEL1	SEL0

This register is used to select the analog channel to use for A/D conversion. It is also used to limit the number of scanned channels in auto-increment mode.

Table 23: ADCSEL Bit Assignments

Bit	Mnemonic	Description
D7-D6	—	**Unused** — These bits have no function.
D5-D4	SL1-SL0	**Scan Range Limit** — These two bits define and restrict the number of channels scanned in auto-increment mode. This allows for faster throughput when fewer than 16 analog inputs are used. A board reset selects (00) so that applications which do not use auto-increment mode are not restricted to a limited set of channels. **SL1 SL0 Scan Range** 0 0 **Channels 0 to 15** – This selection does not restrict the number of channels accessed in auto-increment mode. Allows access to all channels. 0 1 **Channels 0 to 3** – This selection causes the first four channels to be accessed in auto-increment mode. Channels 0 through 3 are accessed in sequence, and then repeated. 1 0 **Channels 0 to 7** – This selection causes the first eight channels to be accessed in auto-increment mode. Channels 0 through 7 are accessed in sequence, and then repeated. 1 1 **Unused** – This combination is invalid.

Table 23: ADCSEL Bit Assignments (cont.)

Bit	Mnemonic	Description
D3-D0	SEL	**Channel Select** — These bits select the analog channel to use for A/D conversion. In auto-increment mode, the channel address changes after each A/D conversion. In all other cases the channel remains static.

SEL3	SEL2	SEL1	SEL0	Selected Channel
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Note: The Scan Range Limit bits in the Control register affect the number stored in this register. A settling delay of approximately 5 microseconds is inserted whenever this register changes.

CONTROL REGISTER

CONTROL (WRITE) 0300H

D7	D6	D5	D4	D3	D2	D1	D0
DIRHI	DIRLO	DMAEN	AINCR	ATRIG	PTRIG	SHARE	INTEN

This register is used to set various operating modes of the VCM-DAS-1/2. A board reset sets this register to 00h.

Table 24: CONTROL Bit Assignments

Bit	Mnemonic	Description
D7	DIRHI	**Parallel Port Direction** — This bit controls the direction of the upper half of the parallel I/O port (DIO8–DIO15). DIRHI = 0 Input DIRHI = 1 Output
D6	DIRLO	**Parallel Port Direction** — This bit controls the direction of the lower half of the parallel I/O port (DIO0–DIO7). DIRLO = 0 Input DIRLO = 1 Output
D5	DMAEN	**Direct Memory Access Enable** — Enables or disables analog input DMA. DMAEN = 0 Disables DMA transfers. DMAEN = 1 Enables analog input DMA transfers. In this mode a DMA transfer request is made whenever an A/D conversion is complete.
D4	AINCR	**Auto Increment Enable** — Enables or disables auto increment mode. AINCR = 0 Disables auto increment. The Channel Select bits retain their value. AINCR = 1 Enables auto increment. In this mode the Channel Select bits in the ADCSEL register increment by one after the ADCHI register is read, allowing the next channel in sequence to be converted. The channel number will increment to a maximum value set by the Scan Range Limit bits (in the ADCSEL register), and then repeat starting again with channel 0. A five microsecond settling delay is inserted after each increment. Auto increment is compatible with manual and auto-trigger modes.

Table 24: Control Bit Assignments (cont.)

Bit	Mnemonic	Description
D3	ATRIG	**Auto Trigger Enable** — Enables or disables auto trigger mode. ATRIG = 0 Disables auto trigger mode. ATRIG = 1 Enables auto trigger mode. In this mode a new A/D conversion is triggered immediately after the ADCHI register is read, eliminating the need to trigger a conversion by writing to the ACDCVT register. To use auto-triggering, set this bit to "1," start the first conversion "manually" by writing to the ADCCVT register, wait until Done, then read the ADCLO and ADCHI registers. From this point on, just wait until DONE and read data.
D2	PTRIG	**Periodic Trigger Enable** — Enables or disables periodic trigger mode. PTRIG = 0 Disables periodic trigger mode. PTRIG = 1 Enables periodic trigger mode. In this mode a new A/D conversion is triggered automatically at a rate determined by the ADCPTR register. This mode is typically used in conjunction with interrupt or DMA based data transfers.
D1	SHARE	**Shared Interrupt Enable** — Enables or disables shared interrupt mode. SHARE = 0 Disabled shared interrupt mode. This mode configures the interrupt driver for totem-pole operation, and is used when the VCM-DAS-1/2 is not sharing interrupts with other devices in the system. SHARE = 1 Enables shared interrupt mode. This mode configures the interrupt driver for open-collector operation, and is used when the VCM-DAS-1/2 is to share it's interrupt request line with other devices.
D0	INTEN	**A/D Interrupt Enable** — Enables or disables interrupt mode. INTEN = 0 Disables interrupts. INTEN = 1 Enables interrupts. The behavior of the interrupt request depends upon the DMAEN bit: DMAEN = 0 In this mode, an interrupt request is sent to the CPU when the A/D conversion is complete, The interrupt request goes away when the ADCHI register is read or by writing 00h to the ADCCVT register. DMAEN = 1 In this mode, an interrupt request is sent to the CPU when the DMA controller (located on the CPU board) indicates a Terminal Count condition. The interrupt request goes away by writing 00h to the ADCCVT register.

ADC STATUS REGISTER

ADCSTAT (READ) 0300H

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	DONE	—	—	—	—	—	—

This register is used to determine if an A/D conversion is complete.

Table 25: ADCSTAT Bit Assignments

Bit	Mnemonic	Description
D7	BUSY	**Analog Input Conversion** / **Settling Time In Progress** — This status bit indicates the status of the A/D converter and the settling delay circuits. BUSY = 0 Analog input circuits idle. BUSY = 1 Indicates the following conditions: • The five microsecond settling time is currently in progress. (The delay starts when the channel number is switched by writing to the ADCSEL register or by the auto-increment mode.) • The ten microsecond A/D conversion process is currently in process (begins when an A/D conversion is triggered). **Note:** This bit is used for factory testing.
D6	DONE	**Analog Input Conversion Complete** — This status bit is used to determine when it is OK to read data from the A/D converter. DONE = 0 There is no unread data waiting for pickup. Done is reset to "0" when the ADCHI register is read. DONE = 1 Analog input conversion has completed. Valid data is available to be read from the ADCLO and ADCHI registers. When interrupts are enabled, the A/D interrupt request signal goes active when Done is set.
D5-D0	—	**Unused** — These bits have no function.

ADC DATA HIGH REGISTER

ADCHI (READ) 0305H

D7	D6	D5	D4	D3	D2	D1	D0
D15	D14	D13	D12	D11	D10	D9	D8

The ADCHI register is a read register containing the upper 8 bits of data from the A/D conversion results. It is used in conjunction with the ADCLO register to read the complete 16-bit data word.

When reading data, the ADCLO register should be read first, followed by the ADCHI register.

When the ADCHI register is read the following events occur:

- The DONE bit in the ADCSTAT register is reset to "0".
- If DMA mode is not being used, the A/D interrupt request signal is cleared.
- The next channel in sequence is selected if auto-increment mode enabled.
- A new A/D conversion is triggered if auto-trigger mode is enabled.

Table 26: ADCHI Bit Assignments

Bit	Mnemonic	Description
D15-D8	ADCDATA	**A/D Input Data (Most Significant Byte)** — These bits contain data bits D15 through D8 of the conversion results.

ADC DATA LOW REGISTER

ADCLO (READ) 0304H

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

The ADCLO register is a read register containing the lower 8 bits of data from the A/D conversion results. It is used in conjunction with the ADCHI register to read the complete 16-bit data word.

After a conversion is complete (as reported by the DONE bit in the ADCSTAT register) the ADCLO register should be read first, followed by the ADCHI register. A word-wide input instruction from the ADCLO register (in ax,dx) will fetch data from both registers in the proper sequence.

The data registers are located on an even address boundary to facilitate efficient single-cycle reading of the A/D data.

Table 27: ADCLO Bit Assignments

Bit	Mnemonic	Description
D7-D0	ADCDATA	**A/D Input Data (Least Significant Byte)** — These bits contain data bits D7 through D0 of the conversion results.

ANALOG INPUT DATA REPRESENTATION

The VCM-DAS-1/2 converts applied analog voltages into 16-bit, two's complement digital words. The full applied analog input range is divided into 65536 steps. The output code (0000h) is associated with a mid-range analog value of 0 Volts (ground). Positive analog values are represented by positive binary numbers, whereas negative analog values are represented by negative binary numbers, i.e., –1 = FFFFh.

The formulas for calculating analog or 16-bit two's complement digital values are given by:

$$Digital = \left[\frac{Analog}{Step} \right] \qquad Analog = Step \times Digital$$

Where:

Analog = Applied voltage

Digital = A/D Conversion Data

Step = 0.0003051757813 (±10V Range)
0.0001525878907 (±5V Range)

Sample two's complement values are shown in the table below:

Table 28: Two's Complement Data Format

±5V Input Voltage	±10V Input Voltage	Hex	Decimal	Comment
+5.000000	+10.000000	—	—	Out of range
+4.999847	+9.999695	7FFFh	32767	Maximum positive voltage
+2.500000	+5.000000	4000h	16384	Positive half scale
+1.250000	+2.500000	2000h	8192	Positive quarter scale
+0.000153	+0.000305	0001h	1	Positive 1 LSB
0.000000	0.000000	0000h	0	Zero (ground input)
–0.000153	–0.000305	FFFFh	-1	Negative 1 LSB
–1.250000	–2.500000	E000h	-8192	Negative quarter scale
–2.500000	–5.000000	C000h	-16384	Negative half scale
–5.000000	–10.000000	8000h	-32768	Maximum negative voltage

ADC OFFSET DIGITAL POT REGISTER

ADOFSET (WRITE) SPI DPOT #1

D7	D6	D5	D4	D3	D2	D1	D0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

This register is used to control the setting for the digital potentiometer assigned to analog input offset calibration.

Table 29: ADOFSET Bit Assignments

Bit	Mnemonic	Description
D7-D0	DATA7-DATA0	**Analog Input Offset Pot Wiper Position** — This 8-bit value controls the position of the wiper contact of potentiometer #1 (inside U2). Changing the value in this register is analogous to rotating the control shaft of a regular pot with a screwdriver, and will have the effect of shifting the Analog Input transfer function up or down along the Y (digital) axis. The overall adjustment range of this pot will affect the analog input readings by approximately ±00B0h. Data format is offset binary. Some sample values are shown below: **DATA** — **Wiper Position** — **Approximate Offset** FFh — Full CCW — –00B0h C0h — Half CCW — –0058h 80h — Middle Position — 0000h 40h — Half CW — +0058h 00h — Full CW — +00B0h **NOTE:** This register is reset to 80h (middle position) by a board reset.

ADC GAIN DIGITAL POT REGISTER

ADGAIN (WRITE) SPI DPOT #3

D7	D6	D5	D4	D3	D2	D1	D0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

This register is used to control the setting for the digital potentiometer assigned to analog input gain calibration.

Table 30: ADGAIN Bit Assignments

Bit	Mnemonic	Description
D7-D0	DATA7-DATA0	**Analog Input Gain Pot Wiper Position** — This 8-bit value controls the position of the wiper contact of potentiometer #3 (inside U2). Changing the value in this register is analogous to rotating the control shaft of a regular pot with a screwdriver, and will change the slope of the Analog Input transfer function. The overall adjustment range of this pot will affect the analog input readings by approximately ±.05% (±20h at full-scale). Data format is offset binary. Some sample values are shown below: **DATA** — **Wiper Position** — **Approximate Gain (Slope)** FFh — Full CCW — .90 C0h — Half CCW — .95 80h — Middle Position — 1.00 40h — Half CW — 1.05 00h — Full CW — 1.10 **NOTE:** This register is reset to 80h (middle position) by a board reset.

ACCESS EXAMPLE

The following code example will set the ADGAIN register to 44h.

```
OUTPUT  SPISEL,02h     ;Route SPI traffic to Digital Pot chip

OUTPUT  SPIWDAT,01h    ;ADDR1 = 1  DPOT#3 ADDR=2
OUTPUT  SPIWDAT,00h    ;ADDR0 = 0

OUTPUT  SPIWDAT,00h    ;DATA7 = 0  ADGAIN=44h
OUTPUT  SPIWDAT,01h    ;DATA6 = 1
OUTPUT  SPIWDAT,00h    ;DATA5 = 0
OUTPUT  SPIWDAT,00h    ;DATA4 = 0
OUTPUT  SPIWDAT,00h    ;DATA3 = 0
OUTPUT  SPIWDAT,01h    ;DATA2 = 1
OUTPUT  SPIWDAT,00h    ;DATA1 = 0
OUTPUT  SPIWDAT,00h    ;DATA0 = 0
```

Analog Output Registers

The following table lists the functions assigned to each analog output write register.

Table 31: Register Functions

Write Register	Description	
DA0GAIN	Analog Output Channel 0 Gain Digital Pot	(DPOT#2)
DA1GAIN	Analog Output Channel 1 Gain Digital Pot	(DPOT#4)
DA0DATA	Analog Output Channel 0 Data Register	
DA1DATA	Analog Output Channel 1 Data Register	

ANALOG OUTPUT GAIN DIGITAL POT REGISTERS

DA0GAIN (WRITE) SPI DPOT #2 – Analog Output Channel 0
DA1GAIN (WRITE) SPI DPOT #4 – Analog Output Channel 1

D7	D6	D5	D4	D3	D2	D1	D0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

These registers are used to control the settings for the digital potentiometers used to calibrate analog output channels 0 and 1.

Table 32: Bit Assignments

Bit	Mnemonic	Description
D7-D0	DATA7-DATA0	**Analog Output Gain Pot Wiper Position** — The value stored in this register controls the position of the wiper contact of potentiometer #2 or #4 (inside U2). Changing the value is analogous to rotating the control shaft of a regular pot with a screwdriver, and will change the slope of the Analog Output transfer function. The overall adjustment range of this pot will affect the analog output voltages by approximately ±.05%. Data format is offset binary. Some sample values are shown below: **DATA** — **Wiper Position** — **Approximate Gain (Slope)** FFh — Full CCW — .90 C0h — Half CCW — .95 80h — Middle Position — 1.00 40h — Half CW — 1.05 00h — Full CW — 1.10 **NOTE:** These registers are reset to 80h (middle position) by a board reset.

ACCESS EXAMPLE

The following code example will set the DA0GAIN register to 15h.

```
OUTPUT  SPISEL,02h     ;Route SPI traffic to Digital Pot chip

OUTPUT  SPIWDAT,00h    ;ADDR1 = 0  DPOT#2 ADDRESS=1 (DPOT#4 ADDRESS=3)
OUTPUT  SPIWDAT,01h    ;ADDR0 = 1

OUTPUT  SPIWDAT,00h    ;DATA7 = 0  DA0GAIN=15h
OUTPUT  SPIWDAT,00h    ;DATA6 = 0
OUTPUT  SPIWDAT,00h    ;DATA5 = 0
OUTPUT  SPIWDAT,01h    ;DATA4 = 1
OUTPUT  SPIWDAT,00h    ;DATA3 = 0
OUTPUT  SPIWDAT,01h    ;DATA2 = 1
OUTPUT  SPIWDAT,00h    ;DATA1 = 0
OUTPUT  SPIWDAT,01h    ;DATA0 = 1
```

ANALOG OUTPUT SHIFT REGISTER

DACSR (WRITE) SPI

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SHL	B	A	—	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

This shift register is used to control the voltages on analog output channels 0 and 1. After writing the desired digital value into the shift register, bit D3 (DACLOAD) in the SPISEL register must be set to transfer the data to the analog converter.

Table 33: Bit Assignments

Bit	Mnemonic	Description
D15	SHL	**Software/Hardware Load** — This control bit determines how the DACA and DACB converters are loaded with new data. SHL = 0 **Hardware Mode** – A and B bits are ignored. Both DACA and DACB are loaded with data from DB11-DB0 when bit D3 (DACLOAD) in the SPISEL register is changed from "0" to "1". SHL = 1 **Software Mode** – When DACLOAD is activated, A and B bits are examined to determine which DAC channel should receive data from DB11-DB0. This is the normal mode of operation for the VCM-DAS-1/2.
D14	B	**Analog Output Channel 1 Load** — This control bit is used to load the analog output data into the channel 1 D/A converter. B = 0 Data will not transfer to DACB when bit D3 (DACLOAD) in the SPISEL register is set. B = 1 Loads DACB (channel 1) with data from DB11–DB0 when bit D3 (DACLOAD) in the SPISEL register is set. **NOTE:** The above descriptions assume SHL=1.
D13	A	**Analog Output Channel 0 Load** — This control bit is used to load the analog output data into the channel 0 D/A converter. A = 0 Data will not transfer to DACA when bit D3 (DACLOAD) in the SPISEL register is set. A = 1 Loads DACA (channel 0) with data from DB11–DB0 when bit D3 (DACLOAD) in the SPISEL register is set. **NOTE:** The above descriptions assume SHL=1.
D12	—	**Unused** — This bit has no function. This bit should be written as a "0".
D11-D0	DB11-DB0	**Analog Output Data** — The data written to these bits forms the 12-bit digital value to be converted to an analog output voltage. See page 45 for a discussion of data format. **NOTE:** The analog output voltage does not update until bit D3 (DACLOAD) in the SPISEL register is changed from 0 to 1.

ACCESS EXAMPLE

The following code example will set Analog Output Channel 0 to a mid-scale value.

```
OUTPUT  SPISEL,01h     ;Route SPI traffic to DAC chip

OUTPUT  SPIWDAT,01h    ;D15 1 SHL        = Software
OUTPUT  SPIWDAT,00h    ;D14 0 B          = Disable
OUTPUT  SPIWDAT,01h    ;D13 1 A          = Enable
OUTPUT  SPIWDAT,00h    ;D12 0 Unused Bit = Zero
OUTPUT  SPIWDAT,01h    ;D11 1 DB11       = 800h (Mid Scale)
OUTPUT  SPIWDAT,00h    ;D10 0 DB10       =   "
OUTPUT  SPIWDAT,00h    ;D9  0 DB9        =   "
OUTPUT  SPIWDAT,00h    ;D8  0 DB8        =   "
OUTPUT  SPIWDAT,00h    ;D7  0 DB7        =   "
OUTPUT  SPIWDAT,00h    ;D6  0 DB6        =   "
OUTPUT  SPIWDAT,00h    ;D5  0 DB5        =   "
OUTPUT  SPIWDAT,00h    ;D4  0 DB4        =   "
OUTPUT  SPIWDAT,00h    ;D3  0 DB3        =   "
OUTPUT  SPIWDAT,00h    ;D2  0 DB2        =   "
OUTPUT  SPIWDAT,00h    ;D1  0 DB1        =   "
OUTPUT  SPIWDAT,00h    ;D0  0 DB0        =   "

OUTPUT  SPISEL,08h     ;D3  1 DACLOAD    = Active
OUTPUT  SPISEL,00h     ;D3  0 DACLOAD    = Inactive
```

ANALOG OUTPUT DATA REPRESENTATION

The VCM-DAS-1/2 converts 12-bit, straight binary digital words into 0 to +5V or 0 to +10V output signals. The output range is divided into 4096 steps. The code 000h produces an analog output of 0 Volts (ground).

The formulas for calculating analog or straight binary digital values are given by:

$$Digital = \left[\frac{Analog}{Step} \right] \qquad Analog = Step \times Digital$$

Where:

Analog = Applied voltage

Digital = A/D Conversion Data

Step = 0.00244140625 (0 to +10V Range)
0.00122070313 (0 to +5V Range)

Sample values are shown in the table below:

Table 34: Straight Binary Data Format

±5V Output Voltage	±10V Output Voltage	Hex	Decimal	Comment
+4.9976	+9.9951	FFFh	4095	Maximum positive voltage
+2.5000	+5.0000	800h	2048	Positive half scale
+1.2500	+2.5000	400h	1024	Positive quarter scale
+0.00122	+0.00244	001h	1	Positive 1 LSB
0.0000	0.0000	000h	0	Zero (ground output)

Digital I/O Registers

PORT DIRECTION

The two 8-bit parallel ports can be configured as inputs or outputs by setting or clearing the DIRHI and/or DIRLO bits in the CONTROL register.

When the system is powered up, or a system reset occurs, both ports are reset to inputs which causes the signal lines to go high.

REGISTER FUNCTIONS

The following table lists the functions assigned to the parallel port interface.

Table 35: Register Functions

Write Register	Description	Page
PARWHI	Parallel Port Data High (Opto 22 Modules 0-7)	47
PARWLO	Parallel Port Data Low (Opto 22 Modules 8-15)	47

Read Register	Description	Page
PARRHI	Parallel Port Data High (Opto 22 Modules 0-7)	48
PARRLO	Parallel Port Data Low (Opto 22 Modules 8-15)	48

DIGITAL OUTPUT REGISTERS

PARWLO (WRITE) 0306h

D7	D6	D5	D4	D3	D2	D1	D0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0

PARWHI (WRITE) 0307h

D7	D6	D5	D4	D3	D2	D1	D0
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8

These registers are used to write data to the output port signal lines DIO0 through DIO15.

Table 36: Bit Assignments

Bit	Mnemonic	Description
D7-D0	DIO0-DIO7 DIO15-DIO8	**Digital Output Data** — Data written to these registers is driven onto the parallel port data signals DIO15–DIO0 on connector J1. Data is not inverted; when a bit is set to 1 the signal line is driven high, when a bit is reset to 0 the signal line is driven low. **NOTE:** You must first set the direction of the appropriate port to output by setting the DIRHI and/or DIRLO bits in the CONTROL register.

DIGITAL INPUT REGISTERS

PARRLO (READ) 0306h

D7	D6	D5	D4	D3	D2	D1	D0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0

PARRHI (READ) 0307h

D7	D6	D5	D4	D3	D2	D1	D0
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8

These registers are used to read data from the input port signal lines DIO0 through DIO15.

Table 37: Bit Assignments

Bit	Mnemonic	Description
D7-D0	DIO0-DIO7 DIO15-DIO8	**Digital Input Data** — Data read from this register returns the current input state of the digital port signals DIO15–DIO0 on connector J1. Data is not inverted; when a signal line is high the bit reads as 1; when a signal line is low the bit reads as 0. **NOTE:** To operate the port in input mode you must first set the direction of the appropriate port to input by clearing the DIRHI and/or DIRLO bits in the CONTROL register. If the port is operated in output mode, the PARRLO/PARRHI registers can be used to readback the logic state of the output lines. Normally the data read would be the same as the data written to the PARWLO/PARHI registers, however, if an output line is stuck high or shorted to ground, the fault will be reflected in feedback data.

Operation 5

This section describes how to operate the VCM-DAS-1/2. Analog input, analog output, and digital I/O are discussed.

Analog Input – Polled Mode

Polled mode operation is the simplest method of analog input. In this mode, software is in control of the analog input process at all times. It is the responsibility of the CPU to start each new A/D conversion as desired, and to read the digital results upon completion.

POLLED MODE STEPS

- Channel selection
- Trigger A/D conversion
- Wait until done
- Read data

CHANNEL SELECTION

Output the desired channel number to the SEL bits in the ADCSEL register. See page 32 for further information.

After the first channel selection, this step can be skipped for multiple conversions of the same channel. This will eliminate the settling delay which is inserted every time the ADCSEL register is written to.

Note: A word-wide output instruction to the ADCSEL register (out dx,ax) also writes into the ADCCVT register causing channel addressing and triggering with one CPU instruction.

TRIGGER A/D CONVERSION

Output 01h to the ADCCVT register. See page 31 for further information.

WAIT UNTIL DONE

Read the ADCSTAT register repeatedly until the DONE bit is set to "1". See page 36 for further information.

READ DATA

Input from the ADCLO register first, followed by the ADCHI register. A word-wide input instruction from the ADCLO register (in ax,dx) will fetch data from both the registers in the proper sequence. See page 38 for further information.

Analog Input – Interrupt Mode

Interrupt mode eliminates the need to repeatedly poll the ADCSTAT register for DONE status. This frees up the CPU to execute unrelated code while the VCM-DAS-1/2 is busy with an A/D conversion. This is especially useful for handling auto triggered and periodic trigger applications.

INTERRUPT MODE STEPS

- Interrupt Service Routine
- Initialize VCM-DAS-1/2 for interrupt mode
- Initialize VCM-DAS-1/2 for Auto-trigger (if desired)
- Initialize interrupt controller
- Initialize CPU to receive interrupt
- Channel selection
- Initialize VCM-DAS-1/2 for Auto-increment (if desired)
- Trigger A/D conversion

INTERRUPT SERVICE ROUTINE

The interrupt service routine reads A/D conversion results from the VCM-DAS-1/2 and stores the data somewhere. Data is input from the ADCLO register first, followed by the ADCHI register. A word-wide input instruction from the ADCLO register (in ax,dx) will fetch data from both registers in the proper sequence. Reading the ADCHI register clears the interrupt request.

The interrupt service routine can be written to select a different channel or trigger a new conversion.

INITIALIZE VCM-DAS-1/2 FOR INTERRUPT MODE

Set bit D0 (INTEN) in the ADCSEL register. See page 32 for further information.

INITIALIZE VCM-DAS-1/2 FOR AUTO-TRIGGER (IF DESIRED)

Set bit D3 (ATRIG) in the ADCSEL register. See page 32 for further information.

Auto-trigger mode is optional when using interrupts. Use it when you want to perform a continuous stream of analog input conversions. Auto-trigger mode eliminates the CPU overhead of writing to the ADCCVT register.

INITIALIZE INTERRUPT CONTROLLER

This involves setting up interrupt vector registers, priority, and unmasking. See the Interrupt Controller section of your CPU instruction manual for further information.

INITIALIZE CPU TO RECEIVE INTERRUPTS

This involves preparing the interrupt vector table, and enabling interrupts. See your CPU instruction manual for further information.

CHANNEL SELECTION

Output the desired channel number to the ADCSEL register. See page 32 for further information.

INITIALIZE VCM-DAS-1/2 FOR AUTO-INCREMENT (IF DESIRED)

Set bit D4 (AINCR) in the CONTROL register. See page 34 for further information.

Auto-increment mode is optional when using interrupts. Use it when you want to convert a series of analog input channels beginning with the channel in the ADCSEL register. Auto-increment mode eliminates the CPU overhead of writing to the ADCSEL register. When disabled, the VCM-DAS-1/2 will convert one channel repeatedly without a settling delay penalty.

TRIGGER A/D CONVERSION

Write 01h to the ADCCVT register to begin. An interrupt is generated when the VCM-DAS-1/2 completes an A/D conversion.

Analog Output

Writing to a VCM-DAS-1/2 analog output channel is involves writing to the SPI (Serial Peripheral Interface) one bit at a time. A 16-bit serial "frame" of data is written to the DAC chip which defines the analog output data, channel address, and loading mode. After the serial data is written, bit D3 (DACLOAD) in the SPISEL register is set to update the analog output channel(s).

- Route SPI data to DAC chip and clear DACLOAD
- Write DAC data frame
- Execute DACLOAD to update analog output

ROUTE SPI DATA TO DAC CHIP AND CLEAR DACLOAD

The first step is to initialize the Serial Peripheral Interface (SPI) and to clear the DACLOAD bit which was left set by the previous analog output operation.

Output 01h to the SPISEL register. This will cause two things to happen:

- Data written to the SPIWDAT register will be routed to the DAC chip.
- The DACLOAD bit will be cleared.

See page 28 for further information on the SPISEL register.

WRITE DAC DATA FRAME

Execute sixteen output operations to the SPIWDAT register to setup the Analog Output Shift Register (DACSR). See page 44 for further information.

EXECUTE DACLOAD TO UPDATE ANALOG OUTPUT

The final step is to transfer the data from the shift register to the D/A converter(s).

Output 08h to the SPISEL register. This will trigger a DACLOAD which updates the analog output channel(s) specified by the A/B bits in the DACSR register.

See page 28 for further information on the SPISEL register and operation of the DACLOAD bit.

Digital I/O

SIGNAL DIRECTION

The sixteen parallel port signals on the VCM-DAS-1/2 can be configured as inputs or outputs, in groups of eight, by manipulating the DIRLO and DIRHI bits in the CONTROL register (page 34).

The logic state of any channel can be read by reading the PARRHI or PARRLO registers (this includes the state of any output line). The logic level on any output channel can be manipulated by writing a 1 or 0 to the appropriate bit in the PARWHI or PARWLO register.

SIGNAL POLARITY

All parallel port circuits on the VCM-DAS-1/2 board are non-inverting, true logic. A high logic level on connector J3 is represented by a 1 in the parallel port data registers, and a low logic level is represented by a 0.

Since Opto 22 modules invert the logic sense of signals passed through them, the register-to-module interface is negative logic. The resulting data interface levels between the VCM-DAS-1/2 and I/O rack modules are shown below.

Data Written	I/O Pin	Output Modules	Input Modules	I/O Pin	Data Read
0	(Low)	Power On	Voltage Present	(Low)	0
1	(High)	Power Off	Voltage Absent	(High)	1

DIGITAL INPUT

The logic state of the parallel input channels can be read at any time by reading the PARRLO or PARRHI registers. Simply choose the correct register and read it as an 8-bit quantity. If desired, both registers can be read with a single 16-bit input transaction (in ax,dx) by addressing PARRLO. This data transfer will take a single bus cycle.

DIGITAL OUTPUT

The logic state of any parallel output channel can be manipulated at any time by writing to the PARWLO or PARWHI registers. Simply choose the correct register and write the digital value as an 8-bit quantity. If desired, both registers can be written to with a single 16-bit output transaction (out dx,ax) by addressing PARWLO. This data transfer will take a single bus cycle.

System Reset

When the card is powered up, or a system reset occurs, the following happens:

- Analog input channel address is reset to zero.
- Analog input status flags are cleared.
- Analog outputs are reset to 0 volts.
- Digital outputs are reset to their inactive high states.

Calibration 6

Required equipment

- Computer with PC/104 expansion site
- Precision Voltmeter
- Hand Calculator
- Utility Disk

Preparation

- Place the VCM-DAS-1/2 on the PC/104 computer

ISOLATE ANALOG CARD

- Unplug ribbon cable from connector J2. There shouldn't be any external equipment attached to the VCM-DAS-1/2 card during calibration.

JUMPER CONFIGURATION

- Jumper the VCM-DAS-1 in the as shipped factory default configuration shown on page 6.
- Make sure the base address of the VCM-DAS-1/2 does not conflict with any other I/O devices used in the system. Change jumper V4 if necessary.

  Note: The VCM-DAS-1/2 is shipped with a default base address of 300h.

CALIBRATION UTILITY PROGRAM

- Run DASxxx.EXE.

  Note: Substitute xxx for the base address (in hex). Five different versions of the program have been compiled for your convenience, each uses a different base address. If another address is used, the DAS.C program will need to be recompiled to reflect the new base address. Change line 86 as appropriate and recompile.

```
unsigned int base_addr = 0x300;     /* As shipped address = 0x300 */
```

- You will be presented with a prompt "<1>" which increments with each command typed in.
- Type "?" to see a list of commands

Calibrating Analog Input

ANALOG INPUT OFFSET

- Use a 0.1" jumper block to short J2[1] to J2[3]. This places AGND (0.000V) on input channel 0.
- Type "AICO 0"
- If successful, the program will say "Offset calibration complete"
- If not successful, the program will say "Digital pot setting out of range."

ANALOG INPUT GAIN

- Analog output channel #0 will be used to generate a voltage close to +9.75V. This voltage will appear on analog input channel #14 because voltage loopback jumper V3[1-2] = IN.
- Type "DP 1 0". This reduces the gain on AOUT0 to the absolute minimum. This ensures that we will not exceed +10.0V when we command AOUT0 to a full scale value in the next step.
- Type "AO 0 4095". This commands AOUT0 to a output a full scale value. On a normally calibrated board this would produce about +10V, however, since the gain is turned down, the output will be about +9.8V
- Connect the precision voltmeter to analog input channel 14 to monitor the applied voltage. Positive lead on J2[20], negative lead to J2[21].
- Make note of the reading on the precision voltmeter. Call this value VOM.

CALCULATE

X = 20/65536 Y = (VOM) / X

Note: Round Y to the nearest whole number.

- Type "AICG 14 Y". Note: Substitute Y for the value calculated above. Y will vary depending upon the VOM reading, but should be between 30000 and 32760.

  Example: AICG 14 32300
- If successful, the program will say "Gain calibration complete"
- If not successful, the program will say "Gain calibration failed with Error Code: X"

Save Calibration Values to EEPROM

- Type "SC"

Calibrating Analog Output

Calibration of the analog output channels depends upon a properly calibrated analog input. You must first follow the instructions above.

CALIBRATE ANALOG OUTPUT CHANNEL #0

- Type "AOCG 0 14"
- If successful, the program will say "Gain calibration complete"
- If not successful, the program will say "Gain calibration failed with Error Code: X"

CALIBRATE ANALOG OUTPUT CHANNEL #1

- Type "AOCG 1 15"

SAVE CALIBRATION VALUES TO EEPROM

- Type "SC"

Confirmation Of Calibration

RELOAD CALIBRATION PARAMETERS.

- Turn power off for 5 seconds
- Turn power on
- Run DASxxx.EXE
- Type "LC"

CHECK ANALOG OUTPUT CHANNEL #0

- Attach voltmeter to analog output channel 0. Positive lead on J2[25], negative lead on J2[24].
- Type "AO 0 4095". Voltmeter should read +10.000V
- Type "AO 0 2048". Voltmeter should read +5.000V

CHECK ANALOG OUTPUT CHANNEL #1

- Attach voltmeter to analog output channel 1. Positive lead on J2[26], negative lead on J2[24].
- Type "AO 1 4095". Voltmeter should read +10.000V
- Type "AO 1 2048". Voltmeter should read +5.000V

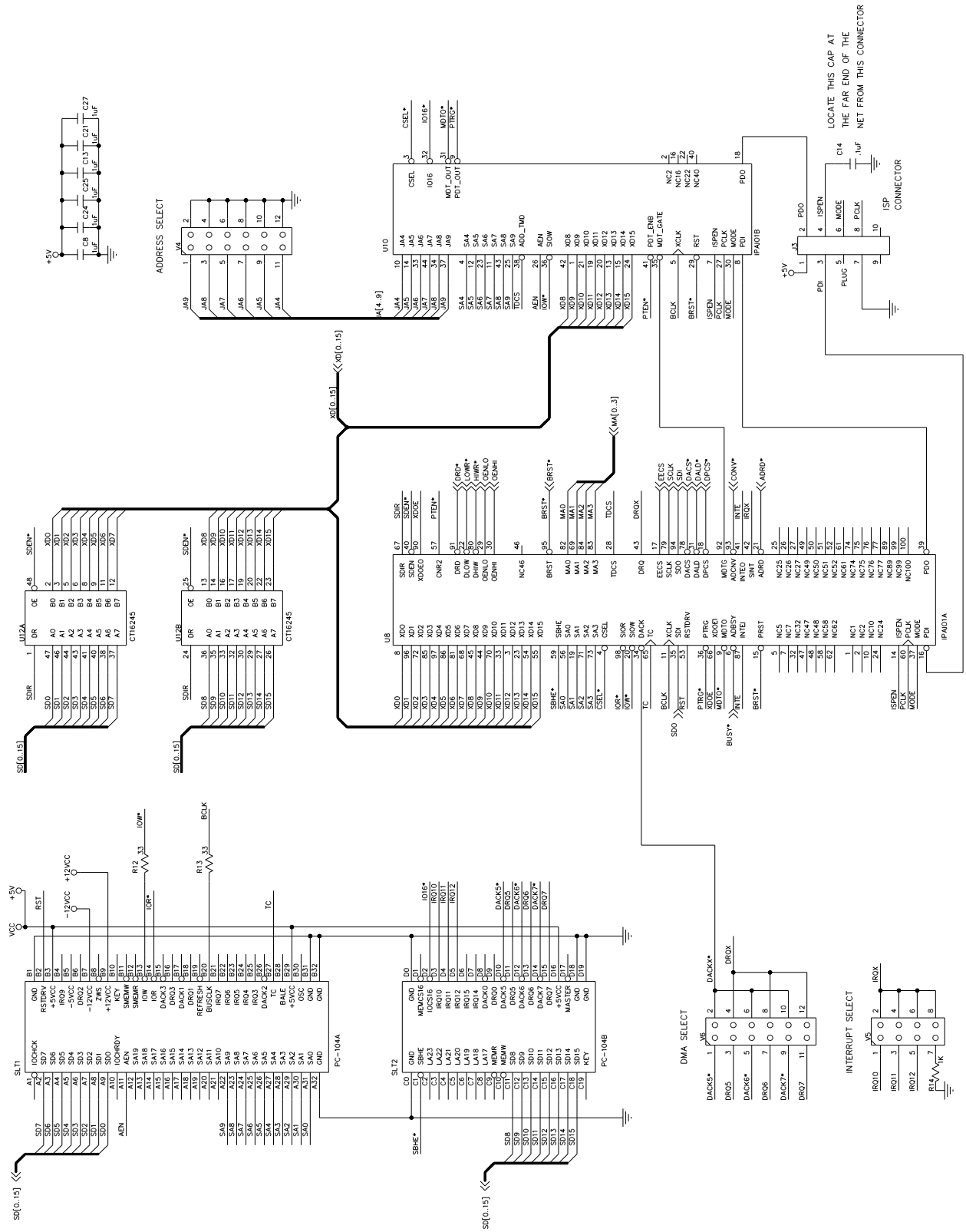
CHECK ANALOG INPUT

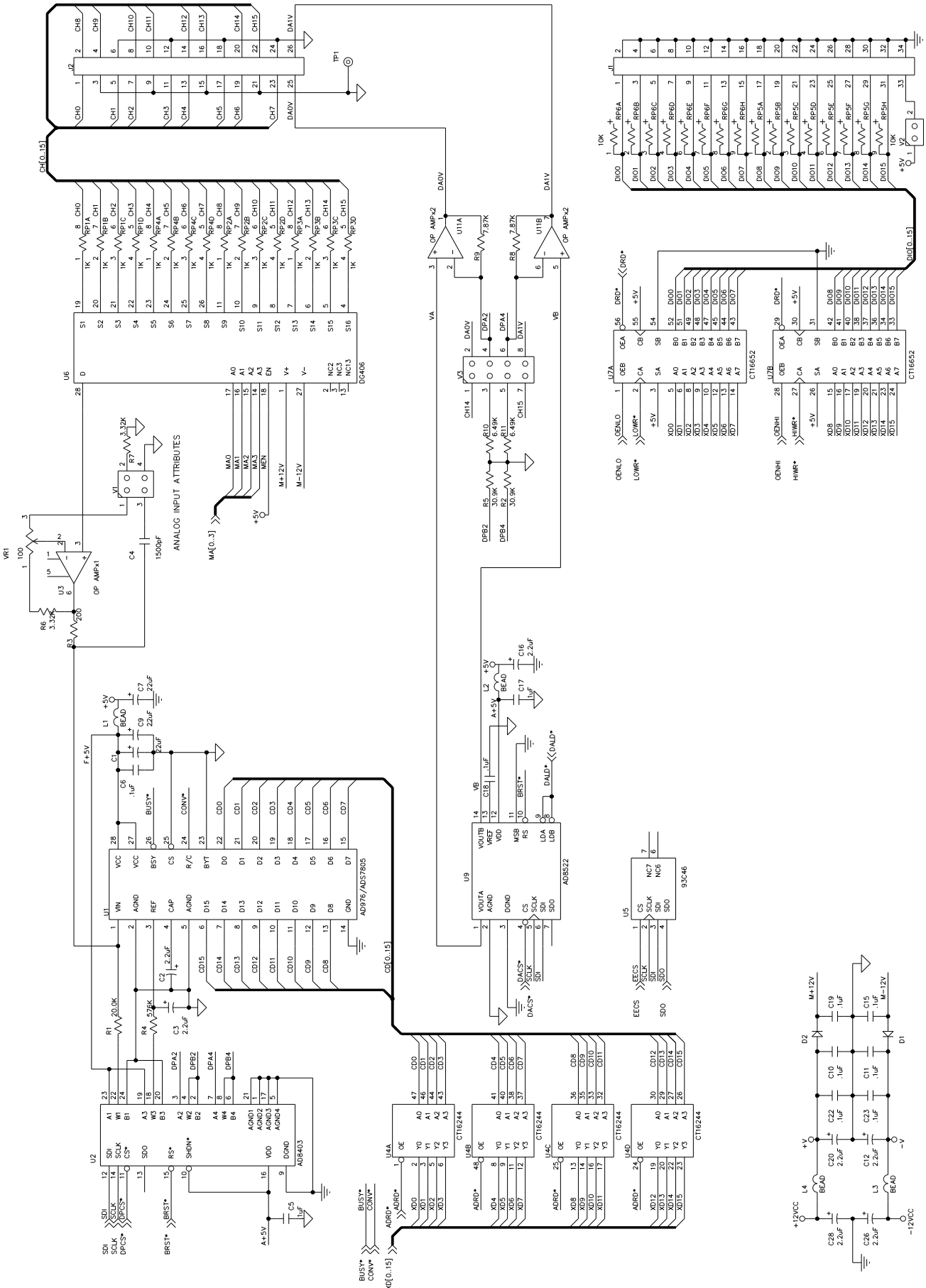
- Type "AI 0 80". Digital values should be 0 +/-6
- Type "AO 0 2048"
- Type "AI 14 80". Digital values should be 4000h +/-6

Finishing Up

- Make sure the AOUT0 and AOUT1 feedback jumpers are restored
- Remove shorting jumper from J2[1-3]
- Reconnect external cable to J2

Appendix A — Schematics




ANALOG INPUT ATTRIBUTES
AD976/ADS7805
AD8522
AD8403
93C46
CT16244
CT16652
DG406
OP AMPx1
OP AMPx2
CH[0..15]
MA[0..3]
XD[0..15]
DIO[0..15]
F+5V
A+5V
+12VCC
-12VCC
M+12V
M-12V