Data Sheet

ADN4680E

250 Mbps, Half-Duplex, Quad M-LVDS Transceivers

FEATURES

- Four M-LVDS transceivers (driver and receiver pairs)
- Switching rate: 250 Mbps (125 MHz)
- Independent pin select for each receiver, two modes:
  - Type 1: input hysteresis of 15 mV typical
  - Type 2: differential input threshold voltage offset by 100 mV to support open-circuit, short-circuit, and bus idle fail-safe
- Compatible with the TIA/EIA-899 standard for M-LVDS
- Glitch free power-up/power-down on the M-LVDS bus
- Controlled transition times on the driver output
- Common-mode range: −1 V to +3.4 V, allowing communication with ±2 V of ground noise
- Driver outputs high-Z when disabled or powered off
- Independent enable pins for each driver and receiver
- Enhanced ESD protection on bus pins
  - ≥±15 kV HBM, air discharge
  - ≥±8 kV HBM, contact discharge
  - ≥±10 kV IEC 61000-4-2, air discharge
  - ≥±8 kV IEC 61000-4-2, contact discharge
- Enhanced ±8 kV HBM ESD protection for all pins, contact discharge
- Operating temperature range: −40°C to +105°C
- Available in 48-lead, 7 mm x 7 mm LFCSP

APPLICATIONS

- Backplane and cable multipoint data transmission
- Multipoint clock distribution
- Low power, high speed alternative to shorter RS-485 links
- Networking and wireless base station infrastructure
- Grid infrastructure and relay protection systems
- Differential extension of SPI networks

FUNCTIONAL BLOCK DIAGRAM

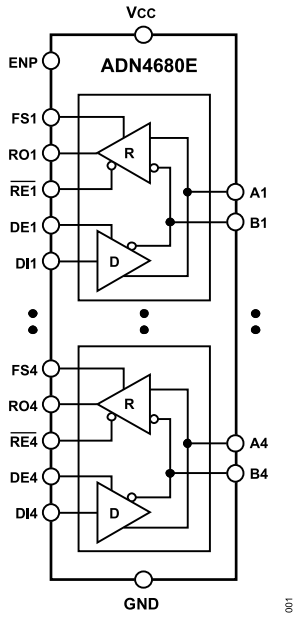

Figure 1.

GENERAL DESCRIPTION

The ADN4680E comprises four multipoint, low voltage differential signaling (M-LVDS) transceivers (driver and receiver pairs) that can operate at up to 125 MHz, or 250 Mbps nonreturn to zero (NRZ). The driver and receiver of each transceiver are connected in half-duplex configuration, which allows each transceiver to be configured via independent enable pins for either sending or receiving data. Electrostatic discharge (ESD) protection of up to ±15 kV is implemented on the bus pins. The transceivers are optimized for low dynamic power consumption for use in high density applications. The ADN4680E is designed to the TIA/EIA-899 standard for use in M-LVDS networks and complement TIA/EIA-644 LVDS devices with additional multipoint capabilities.

The receivers detect the bus state with a differential input of as little as ±50 mV over a common-mode voltage range of −1 V to +3.4 V. Each receiver can be independently pin selectable as a Type 1 or Type 2 receiver. Type 1 receivers have 15 mV of hysteresis so that slow changing signals or loss of input does not lead to output oscillations. Type 2 receivers exhibit an offset threshold, guaranteeing the output state when the inputs are open (open circuit fail-safe), the bus is idle (bus idle or terminated fail-safe), or when the inputs are hard short circuited.

The device is available in a compact 48-lead, 7 mm × 7 mm LFCSP and operates over a temperature range of −40°C to +105°C.

Rev. 0

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REVISION HISTORY

9/2021—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V, load resistance (R_L) = 50 Ω, and T_A = −40°C to +105°C, unless otherwise noted. All typical values are given for V_{CC} = 3.3 V and T_A = 25°C.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY						
Supply Current	I_{CC}					125 MHz clock on DI1 to DI4 or A1 to A4 and B1 to B4, ENP high, and other pins open, unless stated otherwise
Only Driver Enabled			65	75	mA	DE1 to DE4, $\overline{RE1}$ to $\overline{RE4}$ = V_{CC}, R_L = 50 Ω
Both Driver and Receiver Disabled			8	10	mA	DE1 to DE4 = 0 V, $\overline{RE1}$ to $\overline{RE4}$ = V_{CC}
Both Driver and Receiver Enabled			115	140	mA	DE1 to DE4 = V_{CC}, $\overline{RE1}$ to $\overline{RE4}$ = 0 V, R_L = 50 Ω, load capacitance (C_L) = 15 pF
Only Receiver Enabled			60	75	mA	DE1 to DE4, $\overline{RE1}$ to $\overline{RE4}$ = 0 V, C_L = 15 pF
Power-Down Supply Current	I_{CCPD}			4.5	mA	ENP low
DRIVER						
Differential Outputs						
Differential Output Voltage Magnitude	$\lvert V_{OD}\rvert$	450	550	650	mV	See Figure 24
Δ$\lvert V_{OD}\rvert$ for Complementary Output States	Δ$\lvert V_{OD}\rvert$	−50	0	+50	mV	See Figure 24
Common-Mode Output Voltage (Steady State)	$V_{OS(SS)}$	0.7	0.9	1.1	V	See Figure 25 and Figure 28
$\Delta V_{OS(SS)}$ for Complementary Output States	$\Delta V_{OS(SS)}$	−50	0	+50	mV	See Figure 25 and Figure 28
Peak-to-Peak V_{OS}	$V_{OS(PP)}$		100		mV	See Figure 25 and Figure 28
Maximum Steady-State Open-Circuit Output Voltage	$V_{A(O)}$ and $V_{B(O)}$	0		2.4	V	See Figure 26
Voltage Overshoot[1]						
Low to High	V_{PH}			1.2 V_{SS}	V	See Figure 29 and Figure 30
High to Low	V_{PL}	−0.2 V_{SS}			V	See Figure 29 and Figure 30
Output Current, Short-Circuit	$\lvert I_{OS}\rvert$			24	mA	See Figure 27
Logic Inputs (DIx, DEx, and ENP)						
Input High Voltage	V_{IH}	2		V_{CC}	V	
Input Low Voltage	V_{IL}	GND		0.8	V	
Input Current	I_I	0		10	μA	Input voltage (V_I) = GND to V_{CC}
Input Capacitance	C_{IN}		5			V_I = 0.4 sin(30 × 10^6πt) V + 0.5 V[2]
RECEIVER						
Differential Inputs						
Differential Input Threshold Voltage						See Table 2 and Figure 39
Type 1 Receiver	V_{TH}	−50		+50	mV	FSx = GND
Type 2 Receiver	V_{TH}	50		150	mV	FSx = V_{CC}
Input Hysteresis						
Type 1 Receiver	V_{HYS}		15		mV	FSx = GND
Type 2 Receiver	V_{HYS}		0		mV	FSx = V_{CC}
Differential Input Voltage Magnitude	$\lvert V_{ID}\rvert$	0.05		V_{CC}	V	
Logic Output ROx						
Short-Circuit Current	I_{OS}	–65		+65	mA	$\overline{REx}$= GND, ROx = V_{CC} or GND
Output Voltage						
High	V_{OH}	2.4			V	Output high current (I_{OH}) = –8 mA
Low	V_{OL}			0.4	V	Output low current (I_{OL}) = 8 mA
High Impedance Output Current	I_{OZ}	−10		+15	μA	Output voltage (V_O) = 0 V or 3.6 V
Logic Input ($\overline{REx}$) and FSx)						
Input Voltage						
High	V_{IH}	2		V_{CC}	V	

SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Low	V_{IL}	GND		0.8	V	
Input Current	I_I	−10		0	µA	V_I = GND to V_{CC}
BUS INPUT AND OUTPUT						
Input Current						
Ax (Receiver or Transceiver with Driver Disabled)	I_A	0		16	µA	Bx voltage (V_B) = 1.2 V and Ax voltage (V_A) = 3.8 V
		−10		+10	µA	V_B = 1.2 V and V_A = 0 V or 2.4 V
		−16		0	µA	V_B = 1.2 V and V_A = −1.4 V
Bx (Receiver or Transceiver with Driver Disabled)	I_B	0		16	µA	V_A = 1.2 V and V_B = 3.8 V
		−10		+10	µA	V_A = 1.2 V and V_B = 0 V or 2.4 V
		−16		0	µA	V_A = 1.2 V and V_B = −1.4 V
Differential (Receiver or Transceiver with Driver Disabled)	I_{AB}	−4		+4	µA	V_A = V_B and 1.4 V ≤ V_A ≤ 3.8 V
Power-Off Input Current						0 V ≤ V_{CC} ≤ 1.5 V
Ax	$I_{A(OFF)}$	0		16	µA	V_B = 1.2 V and V_A = 3.8 V
		−10		+10	µA	V_B = 1.2 V and V_A = 0 V or 2.4 V
		−16		0	µA	V_B = 1.2 V and V_A = −1.4 V
Bx	$I_{B(OFF)}$	0		16	µA	V_A = 1.2 V and V_B = 3.8 V
		−10		+10	µA	V_A = 1.2 V and V_B = 0 V or 2.4 V
		−16		0	µA	V_A = 1.2 V and V_B = −1.4 V
Differential	$I_{AB(OFF)}$	−4		+4	µA	V_A = V_B and 1.4 ≤ V_A ≤ 3.8 V
Input Capacitance (Transceiver with Driver Disabled)	C_A or C_B		13		pF	V_A or V_B = 0.4 sin(30e^{6}πt) V + 0.5 V, [2] other input = 1.2 V, DEx = 0 V
Differential Input Capacitance (Transceiver with Driver Disabled)	C_{AB}		6.5		pF	Ax – Bx voltage (V_{AB}) = 0.4 sin(30× 10^{6}πt) V,[2] DEx = 0 V
Input Capacitance Balance (C_A/C_B) (Transceiver with Driver Disabled)	$C_{A/B}$		1 ± 0.01			DEx = 0 V

[1] These specifications are guaranteed by design and characterization

[2] HP4194A impedance analyzer (or equivalent).

RECEIVER INPUT THRESHOLD TEST VOLTAGES

$\overline{REx}$ = 0 V.

Table 2. Test Voltages for Type 1 Receiver (FSx = GND)

Applied Voltages (V)		Input Voltage (V)		
V_A	V_B	Differential, V_{ID}	Common-Mode, V_{IC}	ROx (V)
+2.4	0	+2.4	+1.2	High
0	+2.4	−2.4	+1.2	Low
+3.4	+3.35	+0.05	+3.375	High
+3.35	+3.4	−0.05	+3.375	Low
−1.35	−1.4	+0.05	−1.375	High
−1.4	−1.35	−0.05	−1.375	Low

Table 3. Test Voltages for Type 2 Receiver (FSx = V_{CC})

Applied Voltages (V)		Input Voltage (V)		
V_A	V_B	Differential, V_{ID}	Common-Mode V_{IC}	ROx (V)
+2.4	0	+2.4	+1.2	High
0	+2.4	−2.4	+1.2	Low
+3.4	+3.25	+0.15	+3.325	High

SPECIFICATIONS

Table 3. Test Voltages for Type 2 Receiver (FSx = V_{CC})

Applied Voltages (V)		Input Voltage (V)		
V_A	V_B	Differential, V_{ID}	Common-Mode V_{IC}	ROx (V)
+3.4	+3.35	+0.05	+3.375	Low
−1.25	−1.4	+0.15	−1.325	High
−1.35	−1.4	+0.05	−1.375	Low

TIMING SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V and T_A = –40°C to +105°C, unless otherwise noted. All typical specifications are given for V_{CC} = 3.3 V and T_A = 25°C.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate[1]		250			Mbps	T_A = −40°C to +85°C
		100			Mbps	T_A = −40°C to +105°C
Propagation Delay[1]	t_{PLH}, t_{PHL}	1.5	1.9	2.4	ns	See Figure 29 and Figure 30
Differential Output Rise and Fall Time[1]	t_R, t_F	1	1.3	1.6	ns	See Figure 29 and Figure 30
Output Skew (Channel to Channel)[1, 2]	$t_{SK(O)}$			100	ps	See Figure 29 and Figure 30
Pulse Skew $\lvert t_{PHL} - t_{PLH} \rvert$[1]	t_{SK}		0	135	ps	See Figure 29 and Figure 30
Part to Part Skew[1, 3]	$t_{SK(PP)}$			350	ps	See Figure 29 and Figure 30
Period Jitter, RMS (1 Standard Deviation)	$t_{JIT(PER)}$		3		ps	125 MHz clock input[4, 5] (see Figure 33)
Cycle to Cycle Jitter, RMS	$t_{JIT(CYC)}$		5		ps	125 MHz clock input[4, 5] (see Figure 33)
Random Jitter, RMS	$t_{JIT(RJ)}$		2		ps	250 Mbps 2^{15} − 1 PRBS input[4] (see Figure 33)
Deterministic Jitter[6]	$t_{JIT(DJ)}$		110		ps	250 Mbps 2^{15} − 1 PRBS input [4](see Figure 33)
Disable Time[1]						
From High Level	t_{PHZ}			7	ns	See Figure 31 and Figure 32
From Low Level	t_{PLZ}			7	ns	See Figure 31 and Figure 32
Enable Time[1]						
To High Level	t_{PZH}			6	ns	See Figure 31 and Figure 32
To Low Level	t_{PZL}			6	ns	See Figure 31 and Figure 32
RECEIVER						
Maximum Data Rate[1]		250			Mbps	T_A = −40°C to +85°C
		100			Mbps	T_A = −40°C to +105°C
Propagation Delay[1]	t_{PLH}, t_{PHL}	3	4	5	ns	C_L = 15 pF (see Figure 34 and Figure 35)
Rise and Fall Time[1]	t_R, t_F	0.65		2.3	ns	C_L = 15 pF (see Figure 34 and Figure 35)
Output Skew (Channel to Channel)[1, 2]	$t_{SK(O)}$			300	ps	C_L = 15 pF (see Figure 34 and Figure 35)
Pulse Skew $\lvert t_{PHL} - t_{PLH} \rvert$[1]	t_{SK}					C_L = 15 pF (see Figure 34 and Figure 35)
Type 1 Receiver			100	350	ps	FSx = GND
Type 2 Receiver			300	500	ps	FSx = V_{CC}
Part to Part Skew[1, 3]	$t_{SK(PP)}$			820	ps	C_L = 15 pF (see Figure 34 and Figure 35)
Period Jitter, RMS (1 Standard Deviation)	$t_{JIT(PER)}$		4		ps	125 MHz clock input[4, 5] (see Figure 38)
Cycle to Cycle Jitter, RMS	$t_{JIT(CYC)}$		7		ps	125 MHz clock input[4, 5] (see Figure 38)
Deterministic Jitter[6]	$t_{JIT(DJ)}$					250 Mbps 2^{15} − 1 PRBS input[4] (see Figure 38)
Type 1 Receiver			150		ps	FSx = GND, $\lvert V_{ID} \rvert$ = 400 mV, V_{IC} = 1 V
Type 2 Receiver			150		ps	FSx = V_{CC}, $\lvert V_{ID} \rvert$ = 400 mV, V_{IC} = 1 V
Random Jitter, RMS	$t_{JIT(RJ)}$					250 Mbps 2^{15} − 1 PRBS input[4] (see Figure 38)
Type 1 Receiver			3			FSx = GND, $\lvert V_{ID} \rvert$ = 400 mV, V_{IC} = 1 V
Type 2 Receiver			3			FSx = V_{CC}, $\lvert V_{ID} \rvert$ = 400 mV, V_{IC} = 1 V
Disable Time[1]						
From High Level	t_{PHZ}			10	ns	See Figure 36 and Figure 37

SPECIFICATIONS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
From Low Level	t_{PLZ}			10	ns	See Figure 36 and Figure 37
Enable Time[1]						
To High Level	t_{PZH}			15	ns	See Figure 36 and Figure 37
To Low Level	t_{PZL}			15	ns	See Figure 36 and Figure 37

[1] Timing parameters are guaranteed by design and characterization. Values do not include stimulus jitter.

[2] $t_{SK(O)}$ is defined as the difference in propagation delay between the fastest and slowest channel on the same device.

[3] $t_{SK(PP)}$ is defined as the difference between the propagation delays of two devices between any specified terminals. This specification applies to devices at the same V_{CC} and temperature and with identical packages and test circuits.

[4] $t_R = t_F$ = 0.5 ns (10% to 90%)

[5] 50 ± 1% duty cycle, measured over 30,000 samples.

[6] Deterministic jitter includes jitter due to pulse skew (t_{SK}).

ABSOLUTE MAXIMUM RATINGS

$T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 5.

Parameter	Rating
V_{CC}	−0.5 V to +4 V
Digital Inputs ($\overline{RE1}$ to $\overline{RE4}$, FS1 to FS4, and ENP)	−0.5 V to +4 V
Digital Inputs (DE1 to DE4 and DI1 to DI4)	−0.5 V to +4.5 V
Receiver Inputs and Driver Outputs (A1 to A4 and B1 to B4)	−1.8 V to +4 V
Receiver Output (RO1 to RO4)	−0.3 V to +4 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operation environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
CP-48-5[1]	30.2	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no bias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2

ESD Ratings for ADN4680E

Table 7. ADN4680E, 48-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	≥±8,000 (contact discharge)	3B[1]
	≥±15,000 (air discharge)	3B[2]
FICDM	≥±1,250	C5[1]
IEC	≥±8,000 (contact discharge)	Level 4[2]
	≥±10,000 (air discharge)	Level 3[2]

[1] This class is for all pins.

[2] This class is for the A1 to A4 and B1 to B4 pins only.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

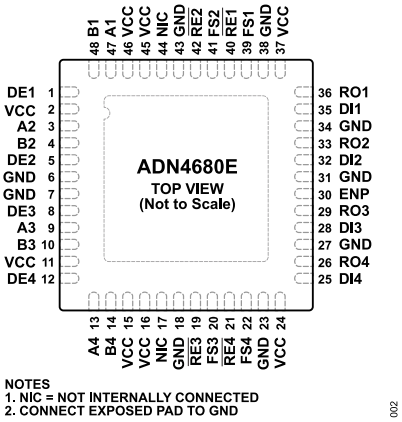


Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5, 8, 12	DE1 to DE4	Driver Output Enable. A logic high on the DE1 to DE4 pins enables the corresponding driver differential outputs. A logic low on the DE1 to DE4 pins places the corresponding driver differential outputs in a high impedance state. If left floating, the DE1 to DE4 pins are internally pulled to logic low.
2, 11, 15, 16, 24, 37, 45, 46	V_{CC}	Power Supply (3.3 V ± 0.3 V). All V_{CC} pins must be connected externally to the supply. Decouple the V_{CC} pins to GND with 0.1 µF capacitors.
3, 9, 13, 47	A2, A3, A4, A1	Noninverting Receiver Input A and Noninverting Driver Output A for Each Transceiver.
4, 10, 14, 48	B2, B3, B4, B1	Inverting Receiver Input B and Inverting Driver Output B for Each Transceiver.
6, 7, 18, 23, 27, 31, 34, 38, 43	GND	Ground. All GND pins must be externally connected to ground.
17, 44	NIC	Not Internally Connected. The NIC pins are not internally connected.
19, 21, 40, 42	$\overline{RE3}$, $\overline{RE4}$, $\overline{RE1}$, $\overline{RE2}$	Receiver Output Enable. A logic low on the $\overline{RE1}$ to $\overline{RE4}$ pins enables the corresponding receiver output. A logic high on the $\overline{RE1}$ to $\overline{RE4}$ pins places the corresponding receiver output in a high impedance state. If left floating, the $\overline{RE1}$ to $\overline{RE4}$ pins are internally pulled to logic high.
20, 22, 39, 41	FS3, FS4, FS1, FS2	Receiver Fail-Safe Enable. A logic high on the FS1 to FS4 pins enables Type 2 receiver functionality for the corresponding receiver inputs (offset threshold). A logic low on the FS1 to FS4 pins enables Type 1 receiver functionality (symmetrical thresholds). If left floating, the FS1 to FS4 pins are internally pulled to logic high.
25, 28, 32, 35	DI4, DI3, DI2, DI1	Driver Inputs. When enabled (the corresponding DE1 to DE4 pins are logic high, and ENP is logic high): A logic low on the DI1 to DI4 pins forces the corresponding noninverting driver output low and inverting output high, whereas a logic high on the DI1 to DI4 pins forces the noninverting output high and inverting output low. If left floating, the DI1 to DI4 pins are internally pulled to logic low.
26, 29, 33, 36	RO4, RO3, RO2, RO1	Receiver Outputs. When the receiver is enabled (the corresponding $\overline{RE1}$ to $\overline{RE4}$ pins are logic low, and ENP is logic high), the following results: In Type 1 receiver mode (the corresponding FS1 to FS4 pins are logic low), if Ax − Bx ≥ +50 mV, the output is logic high, and if Ax − Bx ≤ −50 mV, the output is logic low. In Type 2 receiver mode (the corresponding FS1 to FS4 pins are logic high), if Ax − Bx ≥ +150 mV, the output is logic high, and if Ax − Bx ≤ +50 mV, the output is logic low. The receiver outputs are undefined outside of these conditions.
30	ENP	Global Device Power Enable Pin. The device is active when logic high is applied to the ENP pin. Power-down mode when logic low is applied (overrides all other enable pins for the global device low power shutdown). If left floating, the ENP pin is internally pulled to logic low.
	EPAD	Exposed Pad. The exposed pad must be connected to ground for proper operation.

TYPICAL PERFORMANCE CHARACTERISTICS

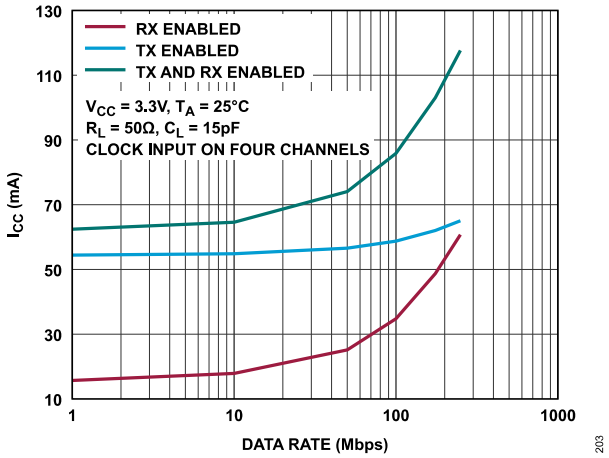


Figure 3. I_{CC} vs. Data Rate (Receiver V_{ID} = 400 mV and V_{IC} = 1 V)

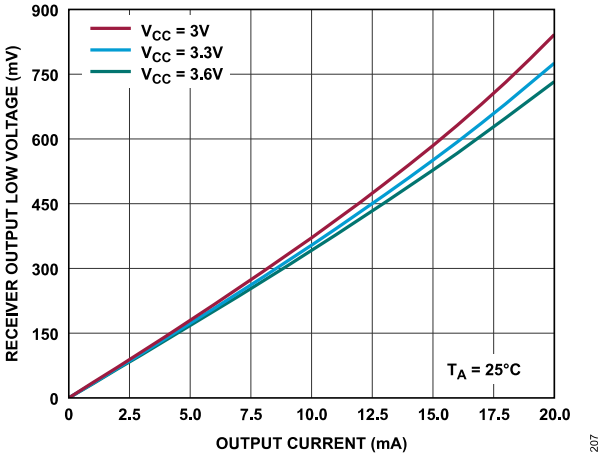


Figure 6. Receiver Output Low Voltage vs. Output Current

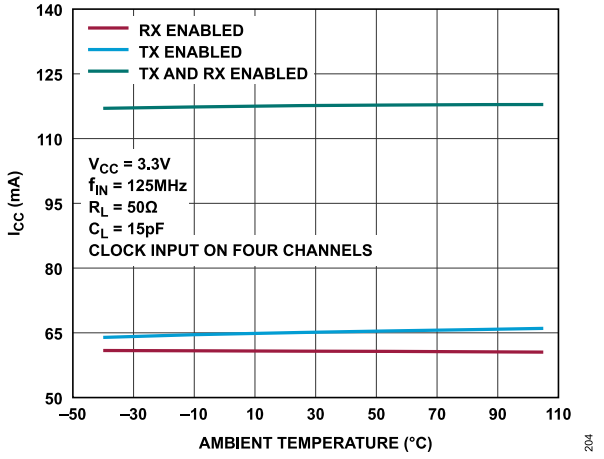


Figure 4. I_{CC} vs. Ambient Temperature (Receiver V_{ID} = 400 mV and V_{IC} = 1 V)

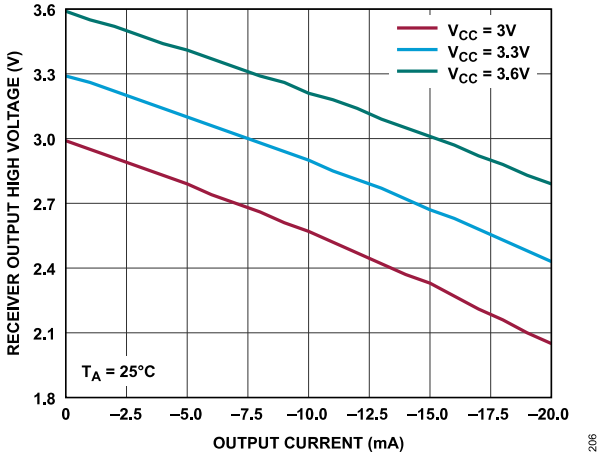


Figure 7. Receiver Output High Voltage vs. Output Current

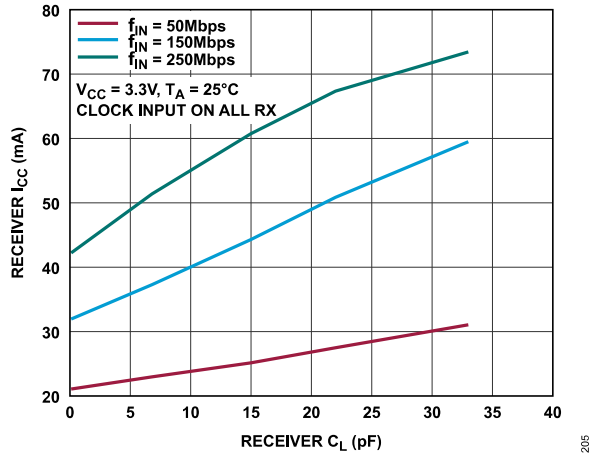


Figure 5. Receiver I_{CC} vs. Receiver C_L (Receiver V_{ID} = 400 mV and V_{IC} = 1 V)

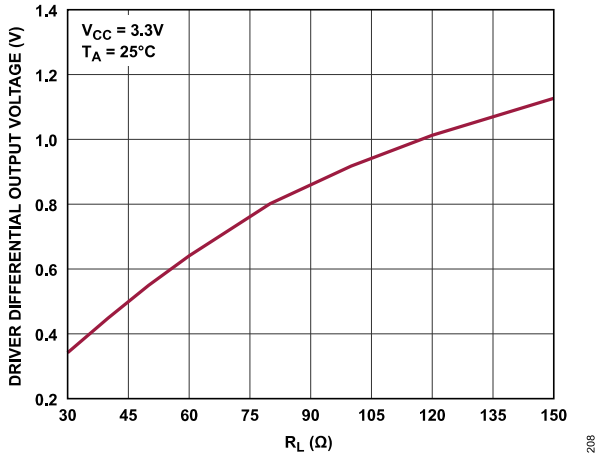


Figure 8. Driver Differential Output Voltage vs. R_L

TYPICAL PERFORMANCE CHARACTERISTICS

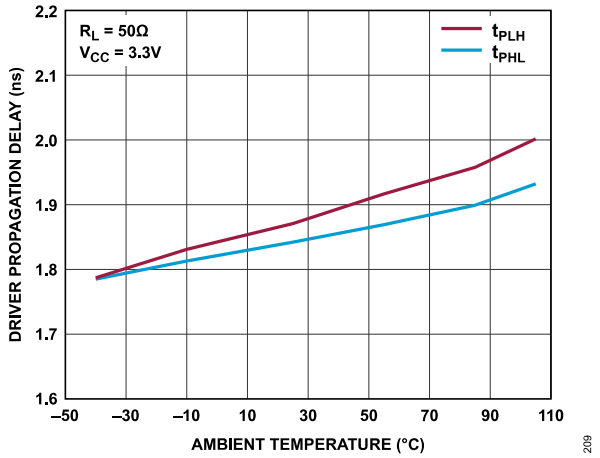


Figure 9. Driver Propagation Delay vs. Ambient Temperature

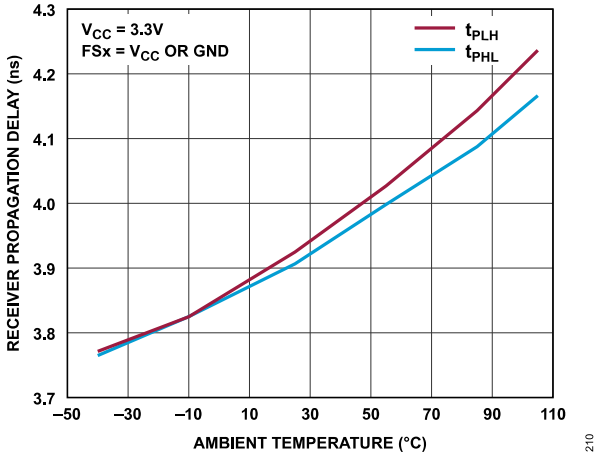


Figure 10. Receiver Propagation Delay vs. Ambient Temperature (V_{ID} = 400 mV and V_{IC} = 1.1 V)

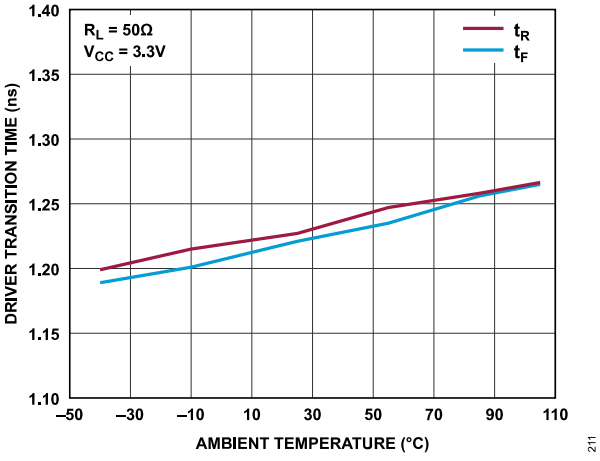


Figure 11. Driver Transition Time vs. Ambient Temperature

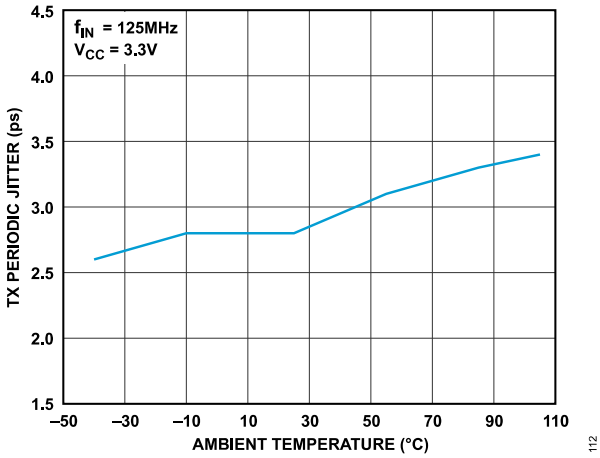


Figure 12. Transmitter Periodic Jitter, RMS vs. Ambient Temperature

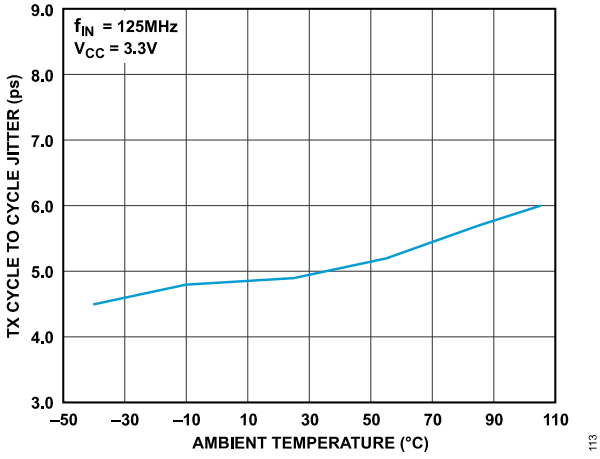


Figure 13. Transmitter Cycle to Cycle Jitter, RMS vs. Ambient Temperature

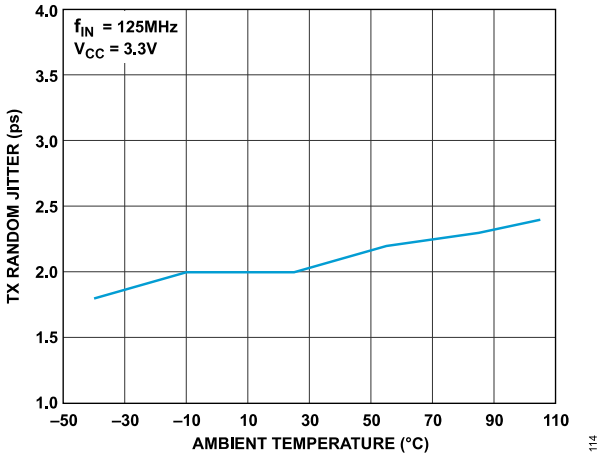


Figure 14. Transmitter Random Jitter, RMS vs. Ambient Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

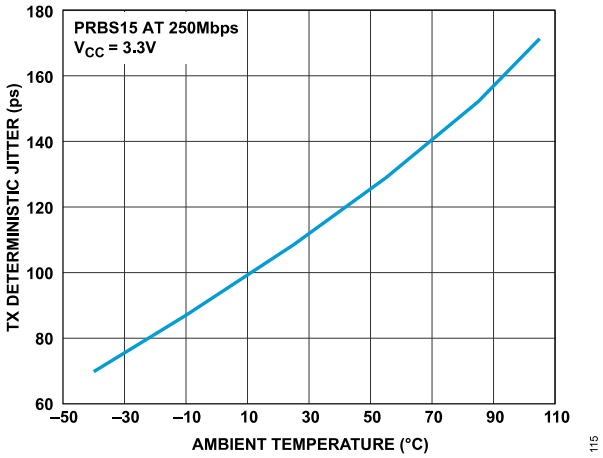


Figure 15. Transmitter Deterministic Jitter vs. Ambient Temperature (R_L = 50 Ω)

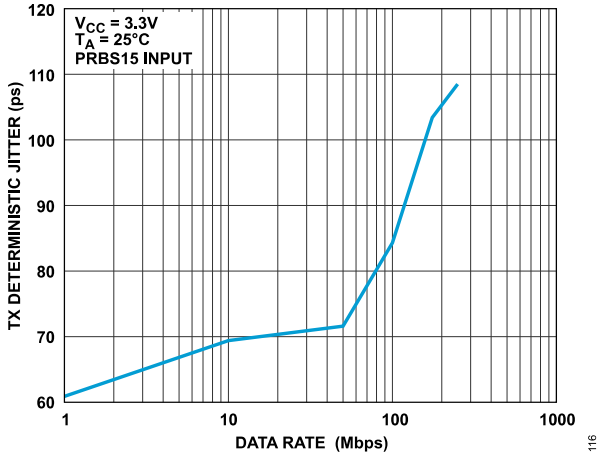


Figure 16. Transmitter Deterministic Jitter vs. Data Rate (R_L = 50 Ω)

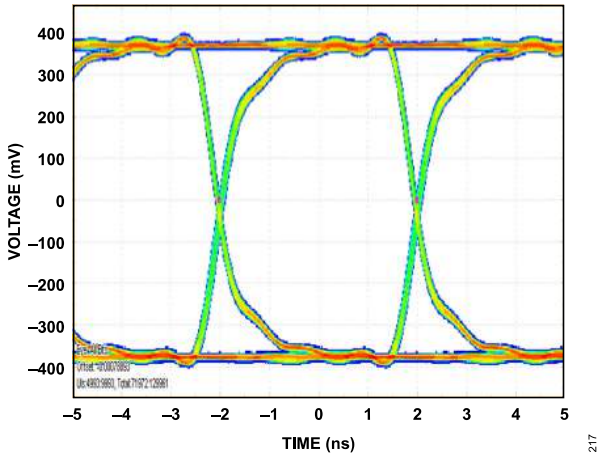


Figure 17. Driver Output Eye Pattern (V_{CC}= 3.3 V, T_A= 25°C, Data Rate = 250 Mbps, PRBS15 Input, and R_L = 50 Ω)

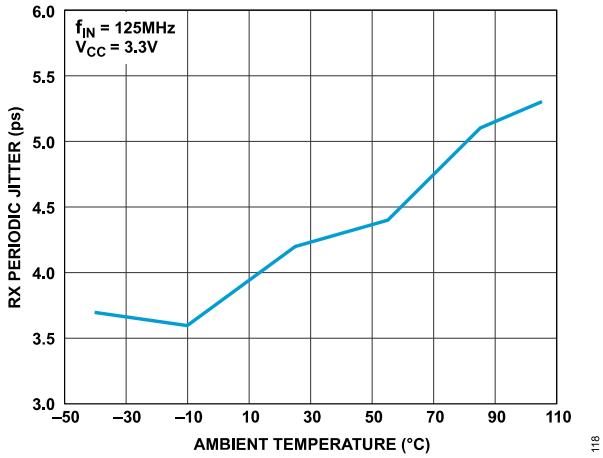


Figure 18. Receiver Periodic Jitter, RMS vs. Ambient Temperature (V_{ID} = 400 mV and V_{IC} = 1.1 V)

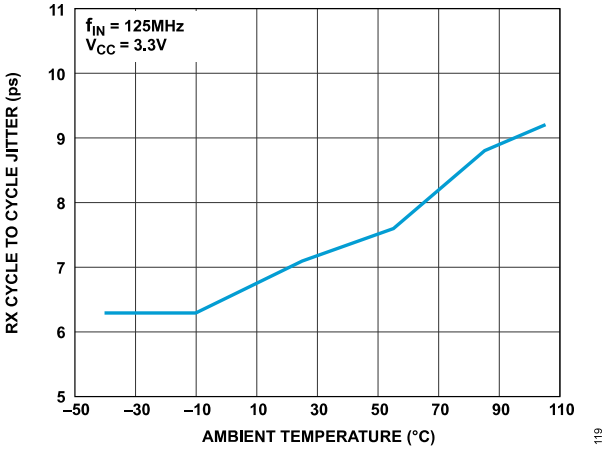


Figure 19. Receiver Cycle to Cycle Jitter, RMS vs. Ambient Temperature (V_{ID} = 400 mV and V_{IC} = 1.1 V)

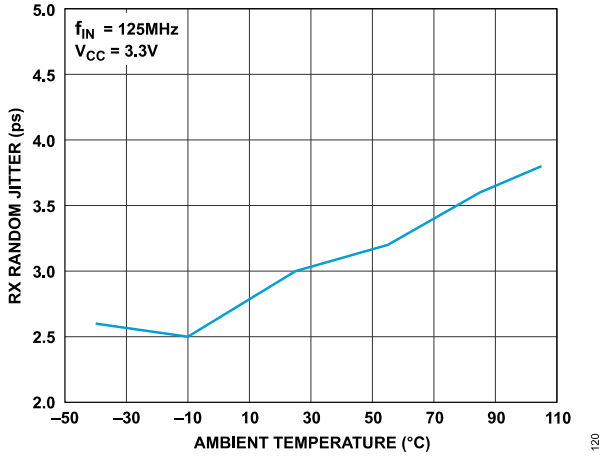


Figure 20. Receiver Random Jitter, RMS vs. Ambient Temperature (V_{ID} = 400 mV and V_{IC} = 1.1 V)

TYPICAL PERFORMANCE CHARACTERISTICS

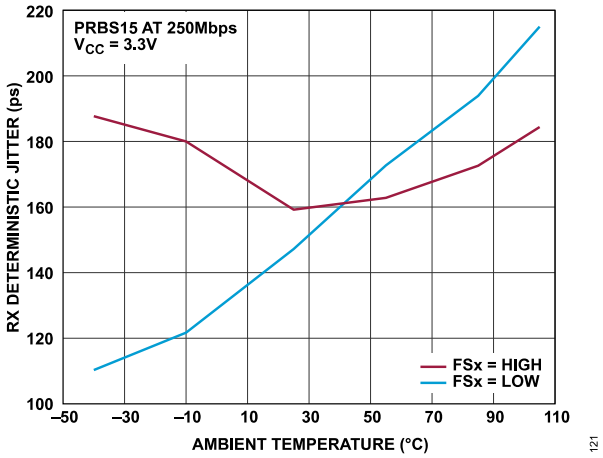


Figure 21. Receiver Deterministic Jitter vs. Ambient Temperature (V_{ID} = 400 mV and V_{IC} = 1.1 V)

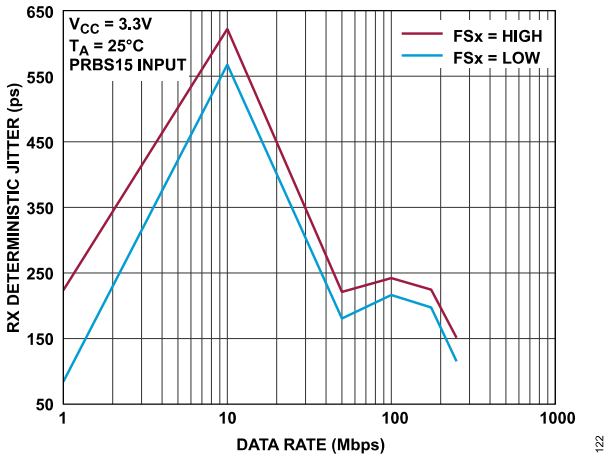


Figure 22. Receiver Deterministic Jitter vs. Data Rate (V_{ID} = 400 mV and V_{IC} = 1.1 V)

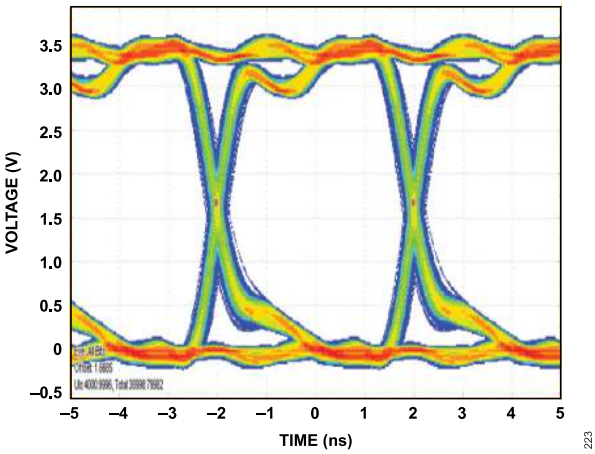


Figure 23. Receiver Output Eye Pattern (V_{CC}= 3.3 V, T_A= 25°C, Data Rate = 200 Mbps, PRBS15 Input, and C_L = 15 pF)

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

DRIVER VOLTAGE AND CURRENT MEASUREMENTS

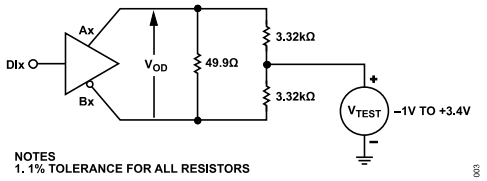


Figure 24. Driver Differential Output Voltage Measurement over Common-Mode Range (V_{TEST} Is the Test Voltage)

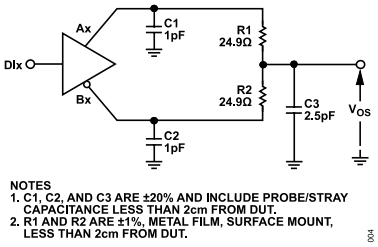


Figure 25. Driver Common-Mode Output Voltage Measurement

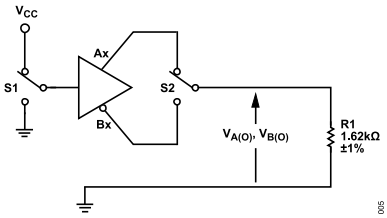


Figure 26. Maximum Steady-State Output Voltage Measurement (S1 Is Switch 1)

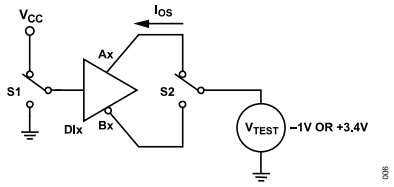


Figure 27. Driver Short Circuit

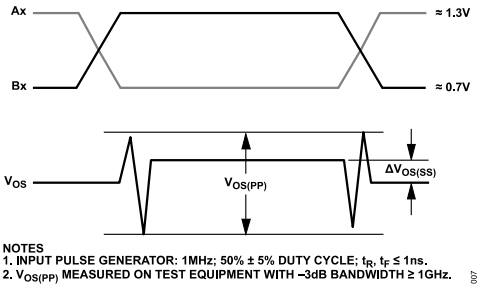
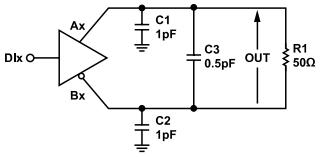


Figure 28. Driver Common-Mode Output Voltage (Steady State)

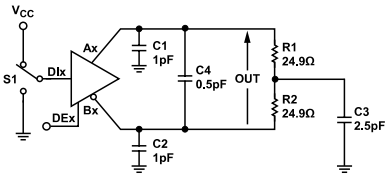
TEST CIRCUITS AND SWITCHING CHARACTERISTICS

DRIVER TIMING MEASUREMENTS



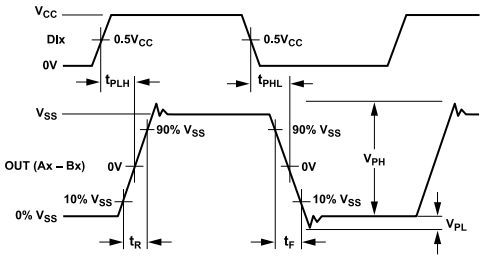
NOTES
1. C1, C2, AND C3 INCLUDE PROBE/STRAY CAPACITANCE.
2. R1 IS ±1%, METAL FILM, SURFACE MOUNT.

Figure 29. Driver Timing Measurement Circuit



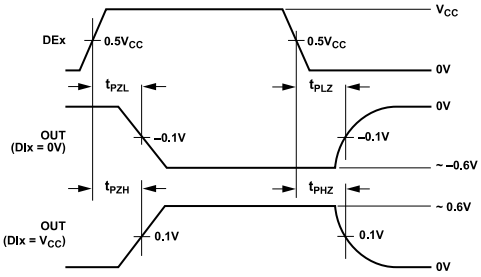
NOTES
1. C1, C2, C3, AND C4 INCLUDE PROBE/STRAY CAPACITANCE.
2. R1 AND R2 ARE METAL FILM, SURFACE MOUNT.

Figure 31. Driver Enable and Disable Time Circuit



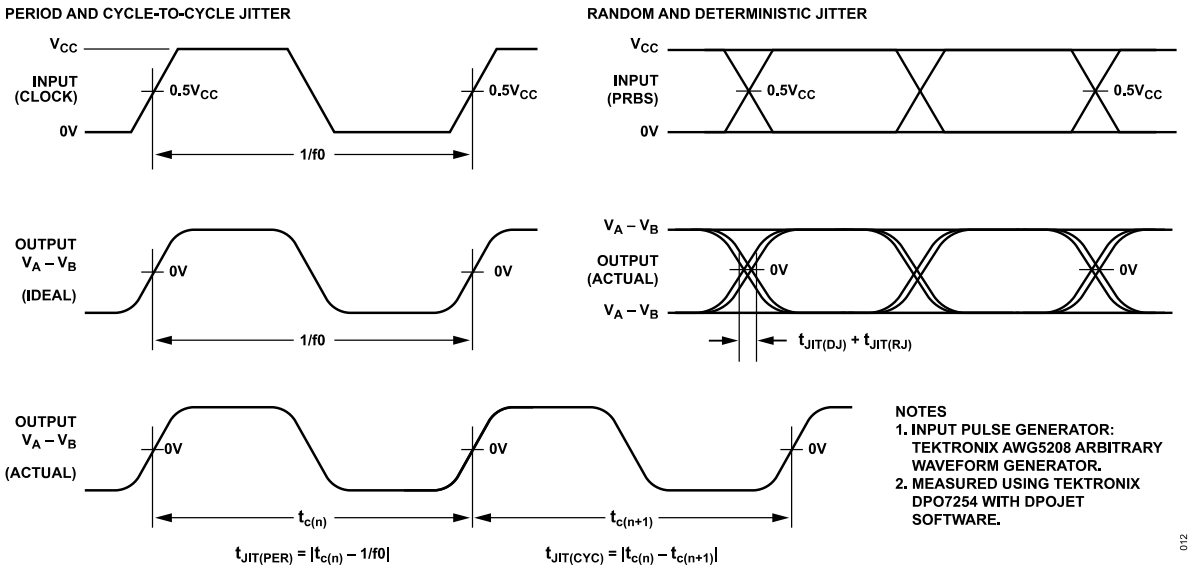
NOTES
1. INPUT PULSE GENERATOR: 125MHz; 50% ± 5% DUTY CYCLE; t_R, t_F ≤ 1ns.
2. MEASURED ON TEST EQUIPMENT WITH –3dB BANDWIDTH ≥ 1GHz.

Figure 30. Driver Propagation, Rise and Fall Times and Voltage Overshoot



NOTES
1. INPUT PULSE GENERATOR: 2MHz; 50% ±5% DUTY CYCLE; t_R, t_F ≤ 1ns.
2. MEASURED ON TEST EQUIPMENT WITH –3dB BANDWIDTH ≥ 1GHz.

Figure 32. Driver Enable and Disable Times



NOTES
1. INPUT PULSE GENERATOR: TEKTRONIX AWG5208 ARBITRARY WAVEFORM GENERATOR.
2. MEASURED USING TEKTRONIX DPO7254 WITH DPOJET SOFTWARE.

Figure 33. Driver Period, Cycle to Cycle, Random and Deterministic Jitter Characteristics

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

RECEIVER TIMING MEASUREMENTS

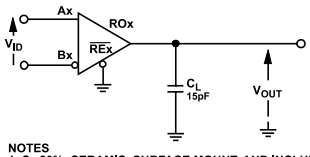


Figure 34. Receiver Timing Measurement Circuit

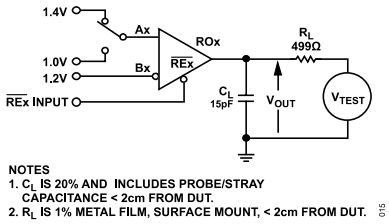


Figure 36. Receiver Enable and Disable Time Circuit

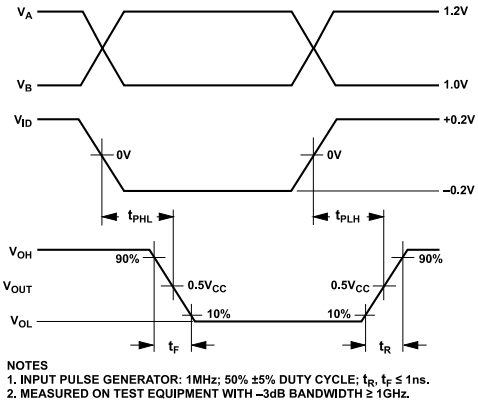


Figure 35. Receiver Propagation and Rise and Fall Times

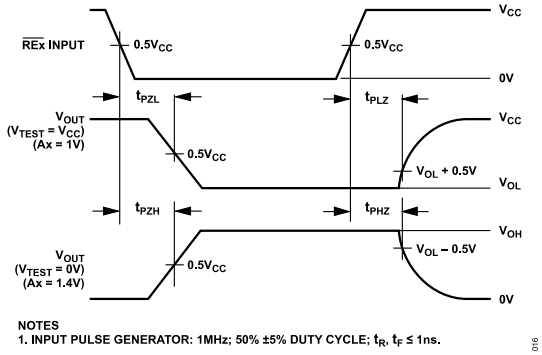


Figure 37. Receiver Enable and Disable Times

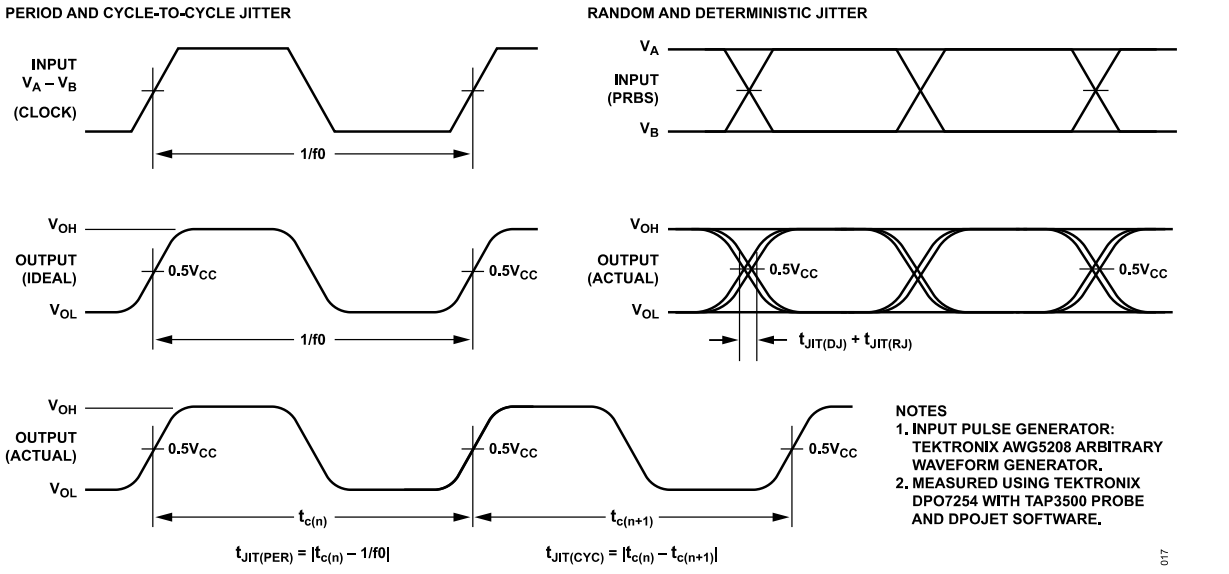


Figure 38. Receiver Period, Cycle to Cycle, Deterministic and Random Jitter Characteristics

THEORY OF OPERATION

The ADN4680E comprises four transceivers for transmitting and receiving M-LVDS at high data rates of up to 250 Mbps NRZ. Each device has a differential line driver and a differential line receiver, allowing each device to send and receive data. The drivers and receivers are connected in half-duplex configuration, allowing a transceiver to transmit or to receive but not simultaneously. Figure 40 shows a typical half-duplex bus topology for M-LVDS.

M-LVDS expands on the established LVDS method by allowing bidirectional communication between more than two nodes. Up to 32 nodes can connect to a standard M-LVDS bus. The ADN4680E is optimized for low dynamic power consumption in applications that utilize multiple high speed M-LVDS lanes.

THREE-STATE BUS CONNECTION

The outputs of the device can be placed in a high impedance state by disabling the driver or the receiver. Placing the driver in a high impedance state allows several driver outputs to connect to a single M-LVDS bus. Note that, on each bus line, only one driver can be enabled at a time, but many receivers can be enabled simultaneously.

Each driver can be enabled or disabled using the driver enable pins (DE1 to DE4). The DEx pins enable the driver outputs when driven logic high. When driven logic low, the DEx pins put the driver outputs into a high impedance state. Similarly, active low receiver enable pins ($\overline{RE1}$ to $\overline{RE4}$) control each receiver. Driving an $\overline{REx}$ pin low enables the corresponding receiver output, whereas driving an $\overline{REx}$ pin high puts the corresponding receiver output into a high impedance state. The M-LVDS driver outputs remain in a high impedance state while the transceiver is not powered.

Truth tables for driver and receiver output states under various conditions are shown in Table 10 and Table 11.

TRUTH TABLES

Table 9. Truth Table Abbreviation Definitions

Abbreviation	Description
H	High level
L	Low level
X	Don't care
I	Indeterminate
Z	High impedance (off)
NC	Disconnected/no input

Table 10. Each Driver (See Table 9 for the Abbreviation Definitions)

	Inputs			Outputs	
V_{CC}	ENP	DEx	DIx	Ax	Bx
On	H	H	H	H	L
On	H	H	L	L	H
On	H	H	NC	L	H
On	X	L or NC	X	Z	Z
On	L or NC	X	X	Z	Z
Off	X	X	X	Z	Z

Table 11. Each Receiver (see Table 9 for the Abbreviation Definitions)

	Inputs					
V_{CC}	ENP	$\overline{REx}$	FSx	Ax − Bx	Receiver Mode	ROx
On	H	L	L	≥+50 mV	Type 1	H
On	H	L	L	≤−50 mV	Type 1	L
On	H	L	L	−50 mV < A − B < +50 mV	Type 1	I
On	H	L	L	NC	Type 1	I
On	H	L	L	Short circuit	Type 1	I
On	H	L	H or NC	≥+150 mV	Type 2	H
On	H	L	H or NC	≤+50 mV	Type 2	L
On	H	L	H or NC	50 mV < A − B < 150 mV	Type 2	I
On	H	L	H or NC	NC	Type 2	L
On	H	L	H or NC	Short circuit	Type 2	L
On	X	H or NC	X	X	X	Z
On	L or NC	X	X	X	X	Z
Off	X	X	X	X	X	I

THEORY OF OPERATION

GLITCH FREE POWERING UP AND POWERING DOWN

To minimize disruption to the bus when adding or removing nodes from the network, the M-LVDS outputs of the device are kept glitch free when the device is powering up or powering down. This feature allows insertion of a device onto a live M-LVDS bus because the bus outputs are not switched on before the device is fully powered. In addition, all outputs are placed in a high impedance state when the device is powered off.

FAULT CONDITIONS

The ADN4680E contains short-circuit current protection that protects the device under fault conditions in case of short circuits on the bus. This protection limits the transmitter output current in a fault condition to 24 mA for short-circuit faults between −1 V and +3.4 V. Any network fault must be cleared to avoid data transmission errors and to ensure reliable operation of the data network and of any devices that are connected to the network.

RECEIVER INPUT THRESHOLDS AND FAIL-SAFE

Two receiver types are pin-selectable using the FSx pins for each receiver. Protection against short circuits is integrated into each receiver.

Type 1 receivers (configured with FSx low) incorporate 15 mV of hysteresis to ensure that slow changing signals or a loss of input does not result in the oscillation of the receiver output. Type 1 receiver thresholds are ±50 mV. Therefore, the state of the receiver output is indeterminate if the differential between Ax and Bx is approximately 0 V. This state occurs if the bus is idle (approximately 0 V on both Ax and Bx), with no drivers enabled on the attached nodes.

Type 2 receivers (configured with FSx high or open) have an open-circuit, short-circuit, and bus idle (terminated) fail-safe. The input threshold is offset by 100 mV to ensure that a logic low is present on the receiver output during the bus idle or receiver open-circuit conditions.

The different receiver thresholds for the two receiver types are illustrated in Figure 39. See Table 11 for the receiver output states under various conditions.

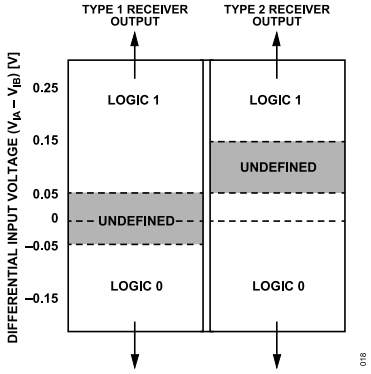


Figure 39. Input Threshold Voltages (V_{IA} Is the Voltage Input on Pin Ax, and V_{IB} Is the Voltage Input on Pin Bx.)

SIXTY-FOUR TRANSCEIVERS ON A NETWORK

The TIA/EIA-899 standard specifies a maximum of 32 M-LVDS transceivers connected to the same differential pair. The ADN4680E receiver exceeds these requirements by a factor of two, with a reduced input current allowing more devices to be connected to the network without excessively loading a transmitter. Up to 64 transceivers from the ADN4680E can be connected to a single network. The ac loading effects of any M-LVDS transceivers on the network must also be considered. See the M-LVDS Design Considerations section for more details.

APPLICATIONS INFORMATION

M-LVDS extends the low power, high speed, differential signaling of LVDS to multipoint systems where multiple nodes are connected over short distances in a bus topology network.

With M-LVDS, a transmitting node drives a differential signal across a transmission medium such as a twisted pair cable. The transmitted differential signal allows other receiving nodes that are connected along the bus to detect a differential voltage that can then be converted back into a single-ended logic signal by the receiver.

The communication line is typically terminated at both ends by resistors (R_T), the value of which is chosen to match the characteristic impedance of the medium (typically 100 Ω). For half-duplex multipoint applications such as the one shown in Figure 40, only one driver can be enabled at any time.

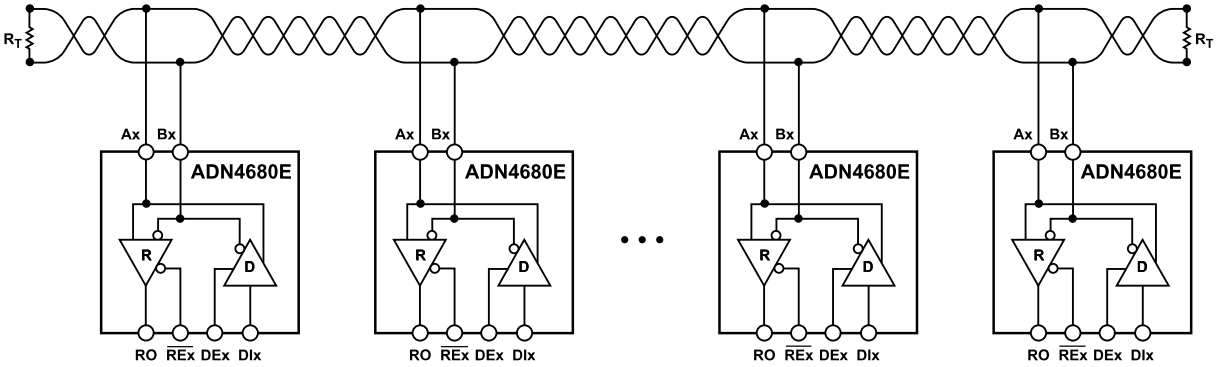


Figure 40. Typical Half-Duplex M-LVDS Network

APPLICATIONS INFORMATION

PCB LAYOUT

The ADN4680E must be adequately decoupled with 0.1 µF capacitors between the V_{CC} and GND pins.

The RO1 to RO4 pins of the ADN4680E output a 3.3 V single-ended signal with fast switching edges of approximately 1 ns. Keep these traces short and routed over a continuous reference plane to minimize radiated emissions. Edge coupling to the reference plane helps minimize fringing electric fields.

The RO1 to RO4 trace capacitance affects the switching supply current drawn from the V_{CC} supply. In applications where the low power consumption is desired, minimize the RO1 to RO4 trace length and capacitance (see Figure 5).

For optimum thermal performance, the exposed pad of the LFCSP must be connected to GND and connected to a solid reference plane through an array of 16 vias with diameter of 0.3 mm, or similar.

M-LVDS DESIGN CONSIDERATIONS

In a backplane or cabled M-LVDS network, the signal integrity is dependent on good design practices. Follow these guidelines to minimize adverse effects on noise margin caused by reflections:

- Route the M-LVDS signals as an impedance controlled differential pair, as either an edge-coupled microstrip or an embedded edge-coupled stripline. The stripline is the preferred method.
- A differential characteristic impedance of between 100 Ω and 130 Ω is recommended. In heavily loaded M-LVDS networks, a larger characteristic impedance gives the best noise margin.
- Maintain a uniform impedance across the M-LVDS network where possible. Avoid unnecessary discontinuities, such as vias or large test points, along the M-LVDS signals.
- Place M-LVDS transceiver modules at uniform distances across the transmission line where possible.
- Place termination resistors within 2.5 cm of the end of the cable or backplane.
- Keep any stub lengths off the main cable or backplane to less than 2.5 cm.
- Minimize connector capacitance where possible.
- Note that Type 2 receivers include fail-safe functionality but have reduced noise margin when receiving data. Configure receivers as Type 1 where receiver fail-safe functionality is not required.
- In heavily loaded M-LVDS networks with multiple devices, match the termination resistors to the effective impedance (Z_{EFF}) of the network. The effective impedance of the network is determined by the capacitance of the network, the capacitance of each transceiver module, and the distance between them as follows:

$$Z_{EFF} = \sqrt{\frac{L_0}{C_0 + \frac{C_L}{D}}} = Z_0 \sqrt{\frac{1}{1 + \frac{C_L}{C_0 D}}} \quad (1)$$

where:
Z_{EFF} is the effective characteristic impedance.
Z_0 is the characteristic impedance of the M-LVDS signals.
L_0 is the inductance per unit length of the M-LVDS signals.
C_0 is the differential capacitance per unit length of the M-LVDS signals.
C_L is the differential capacitance of the load (the transceiver module).
D is the distance between the loads.

EXTENDING THE SPI OVER M-LVDS

The ADN4680E can extend the reach and reliability of a serial peripheral interface (SPI). At a high clock rate and transmission distance, the single-ended signals used in the SPI suffer from poor electromagnetic compatibility (EMC). Differential extenders are commonly used to allow the reliable transmission of the SPI over longer distances. The ADN4680E has several features that make it well suited for this:

- A data rate of up to 125 MHz supports the highest SPI clock rates with minimal added skew and jitter.
- A quad channel transceiver that allows a single device to extend the CLK, MOSI, MISO, and SS signals of the SPI.
- A half-duplex configuration allows for configurable channel directionality.
- The low propagation delay of the transceiver minimizes the impact on transmission distance at higher SPI clock frequencies.
- The robust EMC protection on the M-LVDS input and output pins is suitable for operation in harsh environments.
- The M-LVDS common-mode range allows communication in the presence of up to ±2 V of ground offset.

In Figure 41, the CLK, MOSI, and MISO signals of the SPI are extended over several meters between a processor and a remote device. The same schematic can function as either a master or a remote interface, selectable via a single logic pin (M/#R). The fourth transceiver of the ADN4680E is not shown and can be used to extend the other SPI signals, such as the chip select line or an interrupt from the remote device to the microcontroller unit (MCU).

APPLICATIONS INFORMATION

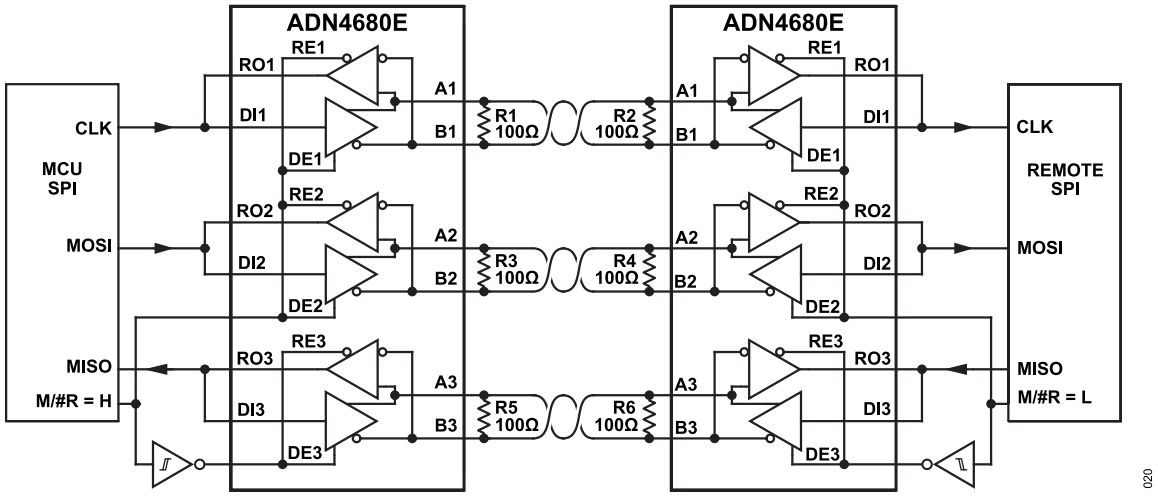


Figure 41. SPI over M-LVDS with ADN4680E

A requirement of the SPI is that the round-trip time delay between the master and the peripheral is less than half the SPI clock period. This requirement places a restriction on the allowed latency, which in turn, limits the maximum cable distance between the master and the peripheral. Devices placed within the signal path, such as transceivers, digital isolators, and level translators, add further propagation delay, which reduces the maximum cable length. The ADN4680E features 10× lower propagation delay than similar RS-485-based solutions, allowing a 10 MHz SPI to operate over several meters of Category 5e (Cat 5e) cabling.

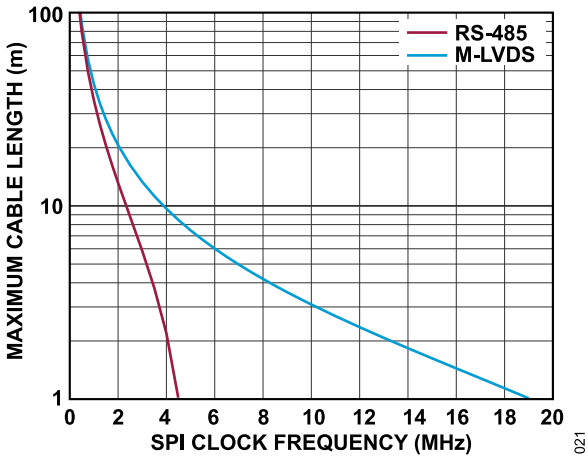
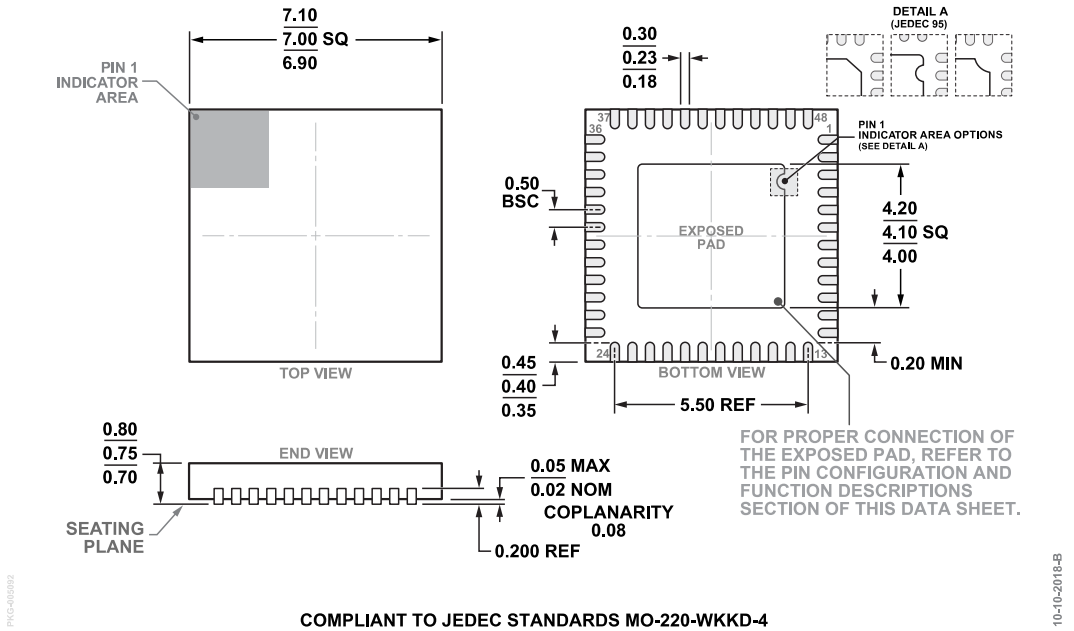


Figure 42. Maximum Cable Length vs. SPI Clock Frequency

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD-4

Figure 43. 48-Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-5)
Dimensions Shown in Millimeters

Updated: September 09, 2021

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADN4680EBCPZ	–40°C to +105°C	48-Lead LFCSP (7 mm × 7 mm with EPAD)	Tray, 0	CP-48-5
ADN4680EBCPZ-RL	–40°C to +105°C	48-Lead LFCSP (7 mm × 7 mm with EPAD)	Reel, 2500	CP-48-5

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model	Description
EVAL-ADN4680EEBZ[1]	ADN4680E Evaluation Board

[1] Z = RoHS Compliant Part.