

Q

# High Speed CMOS 9-Bit Parity Generator/Checker

QS54/74FCT280T

QS54/74FCT1280T

## FEATURES/BENEFITS

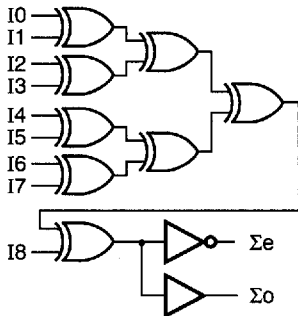
- QSFCT280BT faster than FAST™
- QSFCT1280T has I8 enable, registered outputs
- $I_{OL} = 48 \text{ mA COM}, 32 \text{ mA MIL}$
- TTL-compatible input and output levels
- Military product compliant with MIL-STD 883
- 6.3 ns delay,  $I_x$  to  $\Sigma e$  for QSFCT280BT
- 2 ns setup,  $I_x$  to reg clock for QSFCT1280BT
- CMOS power levels <7.5 mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- JEDEC standard pinouts

## DESCRIPTION

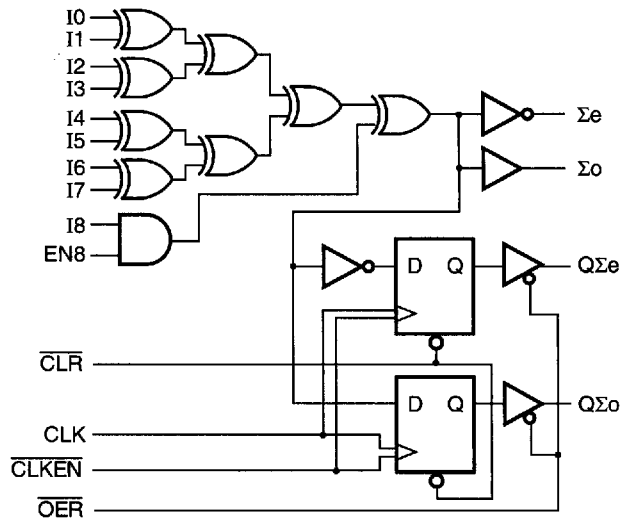
The QSFCT280/AT/BT and QSFCT1280/AT/BT are high-speed CMOS TTL-compatible 9-bit parity generator-checkers. Both odd and even parity outputs are available for generating or checking odd or even parity. The 1280 has I8 enable for parity bit generation and registered odd and even outputs for parity check on the following cycle. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

## FUNCTIONAL BLOCK DIAGRAM

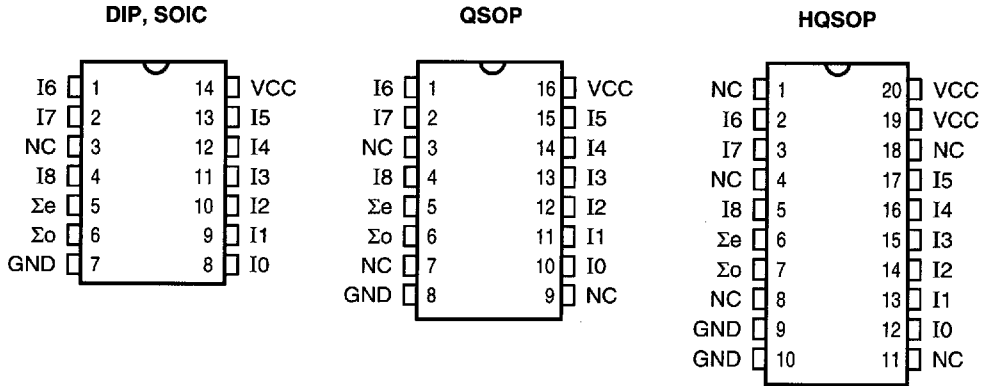
FCT280



FCT1280



FCT280 PIN CONFIGURATIONS (All Pins Top View)

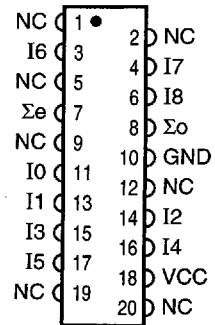


**Note:**  
14-Pin SOIC is 150 mil wide (package code S1).

PIN DESCRIPTION

Name	I/O	Description
I8-I0	I	Data Inputs
Σe	O	Even Parity Out
Σo	O	Odd Parity Out

ZIP

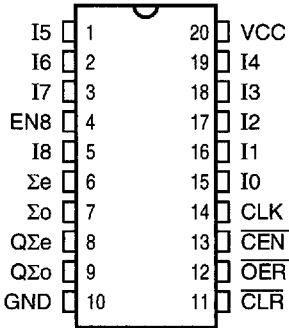


FUNCTION TABLE

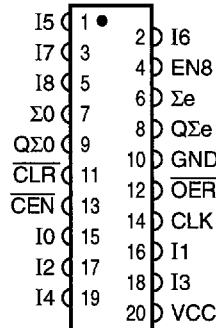
Inputs I8-I0	Outputs		Function
	Σ even	Σ odd	
Number of Bits at TTL High = 0,2,4,6,8	H	L	Parity is Even
Number of Bits at TTL High = 1,3,5,7,9	L	H	Parity is Odd

FCT1280 PIN CONFIGURATIONS (All Pins Top View)

PDIP, SOIC, QSOP, HQSOP



ZIP



PIN DESCRIPTION

Name	I/O	Description
I8-I0	I	Data Inputs
EN8	I	Enable I8
CLK	I	Clock
$\overline{\text{CEN}}$	I	Clock Enable
$\overline{\text{CLR}}$	I	Clear
$\overline{\text{OER}}$	I	Reg. Out Enable
$\Sigma e$	O	Even Parity Out
$\Sigma o$	O	Odd Parity Out
QΣe	O	Reg. Even Parity
QΣo	O	Reg. Odd Parity

FUNCTION TABLE

	Inputs		Outputs	
	I7-I0	I8 EN8	$\Sigma e$	$\Sigma o$
Number of Bits at TTL High = 0,2,4,6,8	X L H	L H H	H H L	L L H
Number of Bits at TTL High = 1,3,5,7,9	X L H	L H H	L L H	H H L

Inputs				Outputs		Function
$\overline{\text{OER}}$	$\overline{\text{CEN}}$	$\overline{\text{CLR}}$	CLK	QΣe	QΣo	
H	X	X	X	Hi-Z	Hi-Z	Disable
L	X	L	X	L	L	Clear
L	H	H	↑	QΣen-1	QΣon-1	No Change
L	L	H	↑	$\Sigma e$ -1	$\Sigma o$ -1	Load $\Sigma e, \Sigma o$

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage to Ground .....	-0.5V to +7.0V
DC Output Voltage $V_{OUT}$ .....	-0.5V to +7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to +7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20 mA
DC Output Diode Current with $V_{OUT} < 0$ .....	-50 mA
DC Output Current Max. Sink Current/Pin .....	120 mA
Maximum Power Dissipation .....	0.5 watts
$T_{STG}$ Storage Temperature .....	-65° to +150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

**FCT280 CAPACITANCE**

$T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins (14-Pin Package)	SOIC	QSOP	PDIP	ZIP	Unit
1, 2, 4, 8-13	4	4	5	7	pF
5, 6	6	6	7	9	pF
—	8	8	9	10	pF

**FCT1280 CAPACITANCE**

$T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1-5, 11-19	4	4	5	7	pF
6-9	6	6	7	9	pF
—	8	8	9	10	pF

**Note:** Capacitance is characterized but not tested.

## QSFACT280T, 1280T

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	$\mu\text{A}$
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$	—	—	5	$\mu\text{A}$
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}, T_A = 25^\circ\text{C}^{(3)}$	—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -12 \text{ mA (MIL)}$ $I_{OH} = -15 \text{ mA (COM)}$	2.4 2.4	—	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $I_{OL} = 32 \text{ mA (MIL)}$ $I_{OL} = 48 \text{ mA (COM)}$	— —	—	0.50 0.50	V

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

### POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, \text{freq} = 0$ $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$\Delta I_{CC}$	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}, V_{IN} = 3.4\text{V}, \text{freq} = 0^{(2)}$	—	2.0	mA
$Q_{CCd}$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}, \text{Outputs Open and Enabled}$ One BitToggling @ 50% Duty Cycle Other Inputs at GND or $V_{CC}^{(3,4)}$	—	0.25	mA/ MHz

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ).
3. For flip-flops,  $Q_{CCd}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4.  $I_C$  can be computed using the above parameters as explained in the Technical Overview section.

## QSFCT280T, 1280T

### FCT280 SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{ pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description		280T		280AT		280BT		Unit
			Min	Max	Min	Max	Min	Max	
tPHLE	Propagation Delay	Com	—	10	—	7.5	—	6.3	ns
tPLHE	I8-I0 to $\Sigma$ even	Mil	—	11	—	9	—	7.5	
tHPLO	Propagation Delay	Com	—	10	—	7.5	—	6.3	ns
tPLHO	I8-I0 to $\Sigma$ odd	Mil	—	11	—	9	—	7.5	

### FCT1280 SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{ pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description		1280T		1280AT		1280BT		Unit
			Min	Max	Min	Max	Min	Max	
tPHLE	Propagation Delay	Com	—	10	—	7.5	—	6.3	ns
tPLHE	I8-I0 to $\Sigma$ even	Mil	—	11	—	9	—	7.5	
tPHLO	Propagation Delay	Com	—	10	—	7.5	—	6.3	ns
tPLHO	I8-I0 to $\Sigma$ odd	Mil	—	11	—	9	—	7.5	
toE	Output Enable Time $\overline{\text{OER}}$ to $Q\Sigma e$ , $Q\Sigma o$	Com <sup>(1)</sup>	1.5	12.5	1.5	10	1.5	7.5	ns
		Mil <sup>(1)</sup>	1.5	14	1.5	12	1.5	8.5	
toZ	Output Disable Time $\overline{\text{OER}}$ to $Q\Sigma e$ , $Q\Sigma o$	Com <sup>(2)</sup>	1.5	8	1.5	7	1.5	6.5	ns
		Mil <sup>(2)</sup>	1.5	8	1.5	7	1.5	6.5	
tcPQ	Clock to Output $Q\Sigma e$ , $Q\Sigma o$	Com	—	10	—	9	—	7.5	ns
		Mil	—	11	—	10	—	8.5	
tCLR	$\overline{\text{CLR}}$ to Output $Q\Sigma e$ , $Q\Sigma o$	Com	—	13	—	11	—	8	ns
		Mil	—	15	—	13	—	10	
tcs	$\overline{\text{CEN}}$ Setup Time $\overline{\text{CEN}}$ to CLK	Com	2.5	—	2	—	2	—	ns
		Mil	2.5	—	2	—	2	—	
tch	$\overline{\text{CEN}}$ Hold Time $\overline{\text{CEN}}$ to CLK	Com	3	—	2.5	—	2	—	ns
		Mil	3	—	2.5	—	2.5	—	
ts	Data Setup Time Ix to CLK	Com	2.5	—	2	—	2	—	ns
		Mil	2.5	—	2	—	2	—	
th	Data Hold Time Ix to CLK	Com	3	—	2.5	—	2	—	ns
		Mil	3	—	2.5	—	2.5	—	
tw	Clock Pulse Width HIGH or LOW	Com <sup>(2)</sup>	7	—	7	—	5	—	ns
		Mil <sup>(2)</sup>	7	—	7	—	6	—	

**Notes:**

1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.