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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E30RA-FW400-N

Overview:

- 3.0-inch TFT (42.04x73.67 [illegible])
- 480 [illegible] 854 [illegible]
- 3SPI & [illegible]
- [illegible]
- All View
- Transmissive
- No Touch Panel
- 400 NITS
- Controllers: ST7701S
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT-LCD Panel, driver circuit and a backlight unit. The resolution of the 3,0" TFT-LCD contains 480(RGB)x854 pixels and can display up to 16.7M colors.

TFT Features

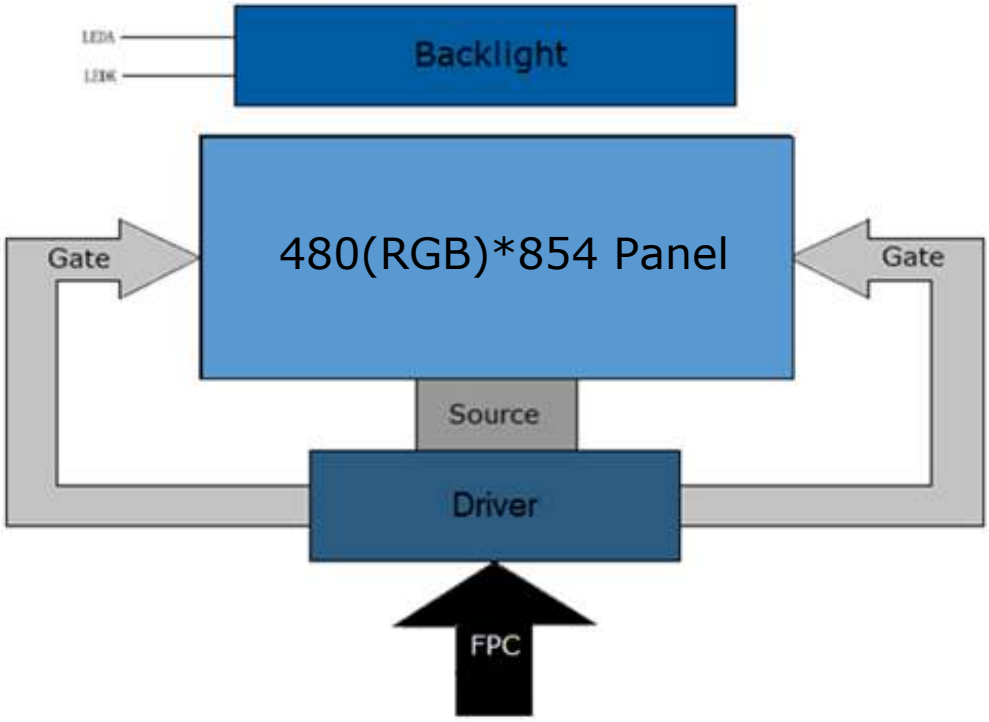
Low Input Voltage: 3.3V
Display Colors: 16.7M colors
TFT Interfaces: 3-wire SPI, 16/18/24-bit RGB

General Information Items	Specification	Unit	Note
	Main Panel		
TFT Display area (AA)	36.72 (H) x 65.28 (V) (2.95 inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	16.7M	colors	-
Number of pixels	480(RGB)x854	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.0765 (H) x 0.07644 (V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ST7701S	-	-
LCM Interface	3SPI+16/18/24-bit RGB	-	-
Display mode	Transmissive/ Normally Black	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

Mechanical Information

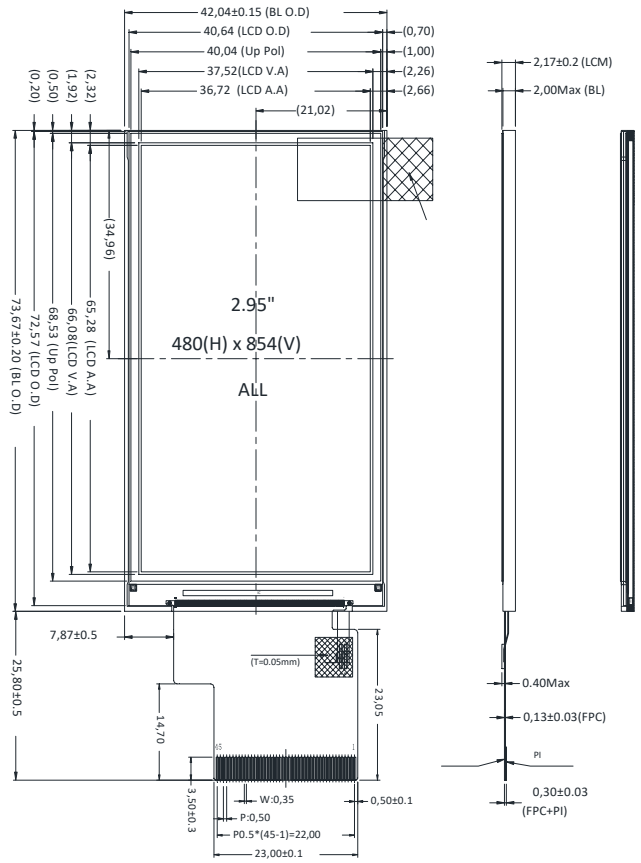
Item		Min	Typ.	Max	Unit	Note
Module size	Height (H)	--	42.04	--	mm	-
	Vertical (V)	--	73.67	--	mm	-
	Depth (D)	--	2.17	--	mm	-
Weight		--	10	--	g	-

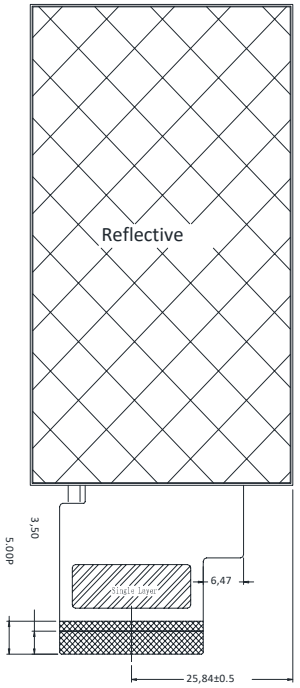
1. Block Diagram

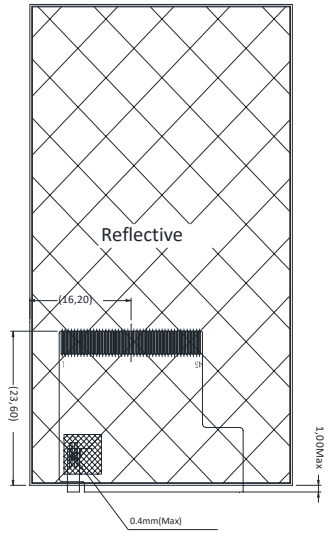


2. Outline Dimensions

ReV.	Revision content description	Date
V0	First Issue	2019. 06. 27
V1		





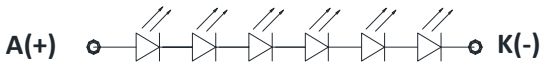


FPC

NO.	Pin Name
1	XR(NC)
2	YD(NC)
3	XL(NC)
4	YU(NC)
5	GND
6	GND
7	VCI
8	IOVCC
9	SDO
10	SDI
11	SCL
12	CS
13	RESET
14	DB23(R7)
15	DB22(R6)
16	DB21(R5)
17	DB20(R4)
18	DB19(R3)
19	DB18(R2)
20	DB17(R1)
21	DB16(R0)
22	DB15(G7)
23	DB14(G6)
24	DB13(G5)
25	DB12(G4)
26	DB11(G3)
27	DB10(G2)
28	DB9(G1)
29	DB8(G0)
30	DB7(B7)
31	DB6(B6)
32	DB5(B5)
33	DB4(B4)
34	DB3(B3)
35	DB2(B2)
36	DB1(B1)
37	DB0(B0)
38	DE
39	PCLK
40	HSYNC
41	VSYNC
42	NC
43	LEDK
44	NC
45	LEDA

NOTES:

1. DISPLAY TYPE: 3.0", TFT-LCD,
2. DISPLAY MODE: IPS NORMALLY BLACK
3. VIEWING DIRECTION: ALL
4. DRIVER IC: ST7701S (COG)
5. VCI: 3.3V
6. CTP SURFACE HARDNESS: 6H
7. OPERATING TEMP: -20°C TO 70°C
   STORAGE TEMP: -30°C TO 80°C
8. BACK LIGHT: LED WHITE, 6 LED, 20mA, 19.2±0.3V
9. RoHS COMPLIANT.



CIRCUIT DIAGRAM

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		PARTS NO.	E30RA-FW400-N	
TOLERANCE UNLESS	X.X±0.3	Drawn		Unit
OTHERWISE SPECIFIED	X.XX±0.2	Checked		mm
Scale 1:1		Approve		Page 1/1

3. Input Terminal Pin Assignment

Recommended Connector: FH12S-45S-0.5SH(55)

NO.	Symbol	Description	I/O
1	XR (NC)	Touch panel right glass terminal. Leave open when not used.	A/D
2	YD (NC)	Touch panel bottom film terminal. Leave open when not used.	A/D
3	XL (NC)	Touch panel left glass terminal. Leave open when not used.	A/D
4	YU (NC)	Touch panel top film terminal. Leave open when not used.	A/D
5	GND	Ground	P
6	GND	Ground	P
7	VCI	Supply voltage (3.3V)	P
8	IOVCC	Supply voltage (1.8-3.3V)	P
9	SDO	Serial data output pin for the SPI interface. Leave this pin open when not used.	O
10	SDI	Serial data input pin for SPI interface.	I/O
11	SCL	Serial clock input pin for SPI interface.	I
12	CS	Chip select pin for SPI interface. Low: the chip is selected and accessible. High: the chip is not selected and not accessible.	I
13	RESET	External reset signal. Initialized the chip with a low input. Execute a power on reset after supplying power.	I
14-37	DB23-DB0	24-bit parallel data bus for RGB interface. Fix to IOVCC or GND when not used.	I/O
38	DE	Data enable signal for RGB interface. Low: access enabled. High: access not enabled. Fix to IOVCC or GND when not used.	I
39	PCLK	Dot clock signal for RGB interface.	I
40	HSYNC	Line synchronizing signal for RGB interface.	I
41	VSYNC	Frame synchronizing signal for RGB interface.	I
42	NC	Not connected	
43	LEDK	Cathode pin of the backlight	P
44	NC	Not connected	
45	LEDA	Anode pin of the backlight	P

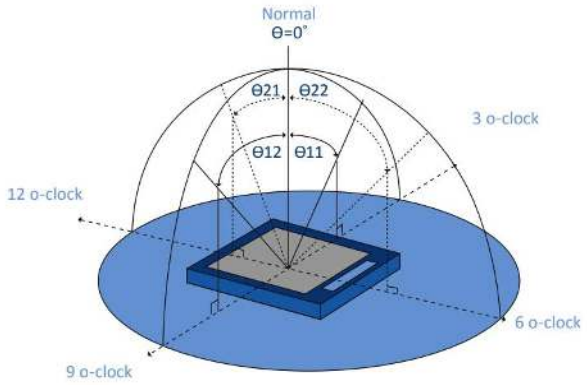
4. LCD Optical Characteristics

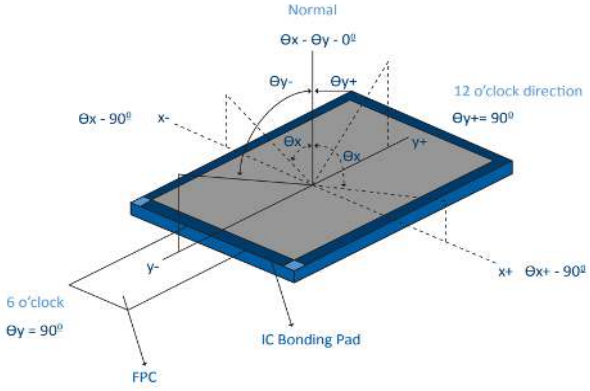
4.1 Optical Specifications

Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Color Gamut		S%		49	54	--	%	(5)
Contrast Ratio		CR	θ=0 Normal viewing angle	1000	1500	--	%	(2)
Response Time	Rising	TR+TF		--	25	35	ms	(4)
	Falling							
Color Filter Chromaticity	White	W_X		0.2669	0.3069	0.3469		(5)(6)
		W_Y		0.2937	0.3337	0.3737		
	Red	R_X		0.5499	0.6099	0.6499		
		R_Y		0.3301	0.3701	0.4101		
	Green	G_X		0.2917	0.3317	0.3717		
		G_Y		0.5291	0.5691	0.6097		
	Blue	B_X		0.1078	0.1478	0.1878		
		B_Y		0.0467	0.0867	0.1267		
Viewing Angle	Hor.	ΘL	CR≥10	80	85	--	degree	(1)(6)
		ΘR		80	85	--		
	Ver.	ΘT		80	85	--		
		ΘB		80	85	--		
Option View Direction		ALL						(1)

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.



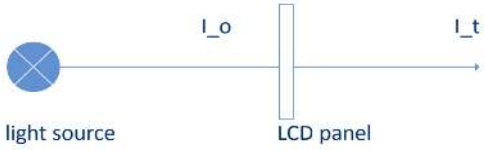


(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$\mathrm{Cr} = \frac{\mathrm{Lw}}{\mathrm{Ld}}$$

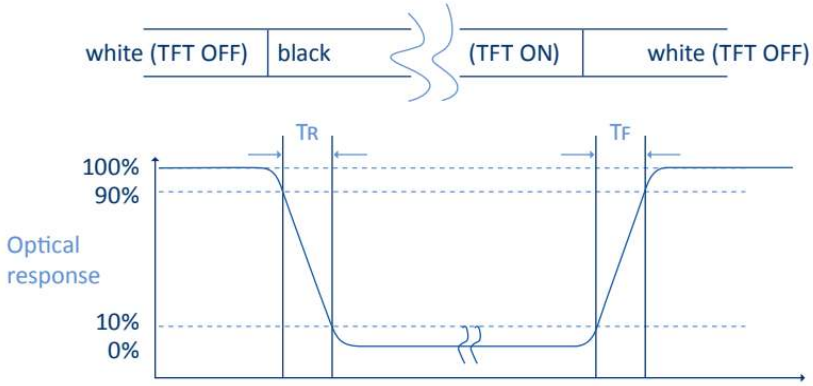
(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving. The equation for transmittance Tr is:

$$\mathrm{Tr} = \frac{\mathrm{It}}{\mathrm{Io}}\ x\ 100\%$$



Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut:
Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.The color chromaticity shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

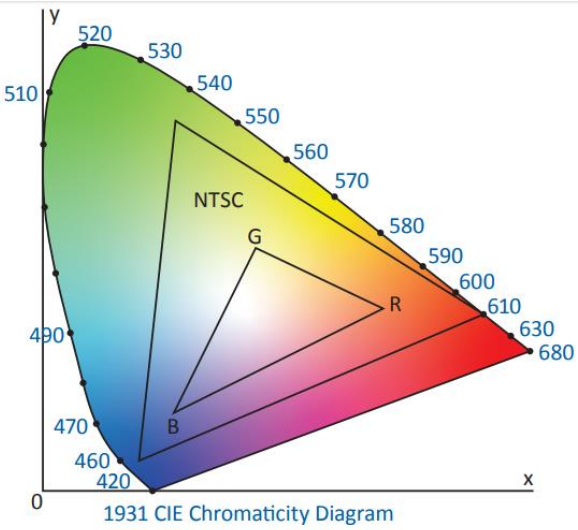
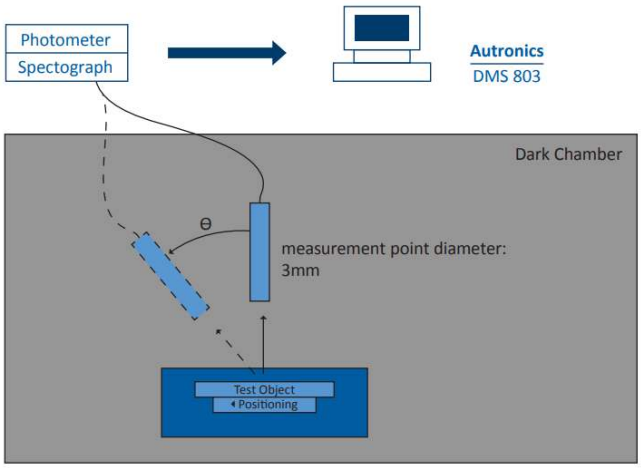


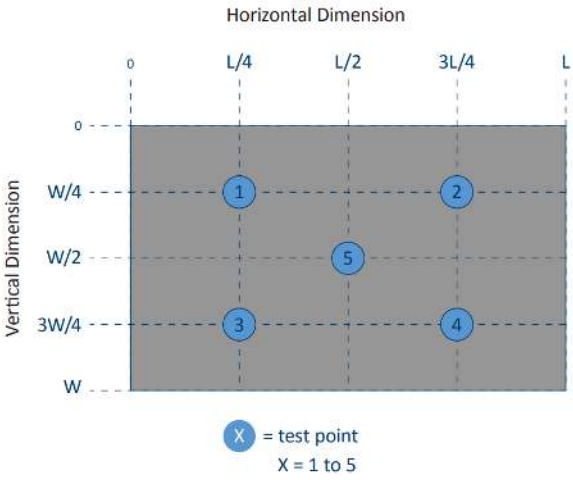
Fig. 1931 CIE chromacity diagram

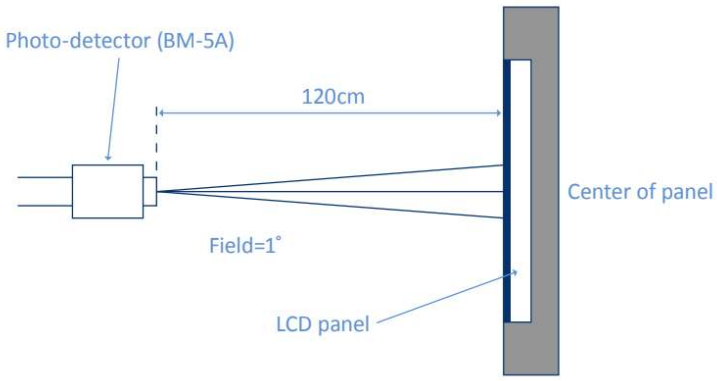
Color gamut: $S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$

(6) Definition of Optical Measurement Setup:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.







5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 ˚C, VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VCI	-0.3	4.6	V
Digital Interface Supply Voltage	IOVCC	-0.3	4.6	V
Operating Temperature	TOP	-20	+70	℃
Storage Temperature	TST	-30	+80	℃

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Digital Supply Voltage	VCI	2.5	3.3	3.6	V	
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.3	V	
Normal Mode Current	ICC	--	38	76	mA	
Level Input Voltage	VIH	0.7IOVCC	--	IOVCC	V	
	VIL	GND	--	0.3IOVCC	V	
Level Output Voltage	VOH	0.8IOVCC	--	IOVCC	V	
	VOL	GND	--	0.2IOVCC	V	

5.3 LED Backlight Characteristics

The backlight system is edge lighting type with 6 chips

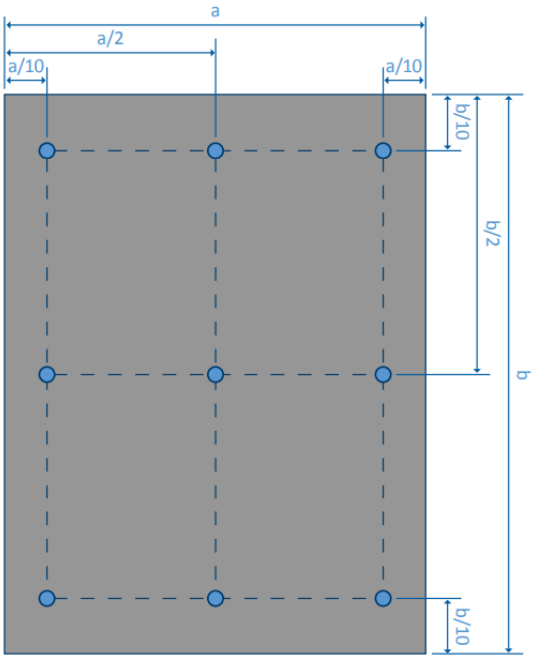
Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	I_F	15	20	--	mA	
Forward Voltage	V_F	--	ろ	--	V	
LCM Luminance	LV	35れ	400	--	cd/m2	Note 3
LED lifetime	Hr	50000	--	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25 ±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL = 20mA

Backlight LED Circuit

Note 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Luminance} = \frac{\text{(Total Luminance of 9 points)}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

6. AC Characteristic

6.1 Parallel RGB Interface Characteristics

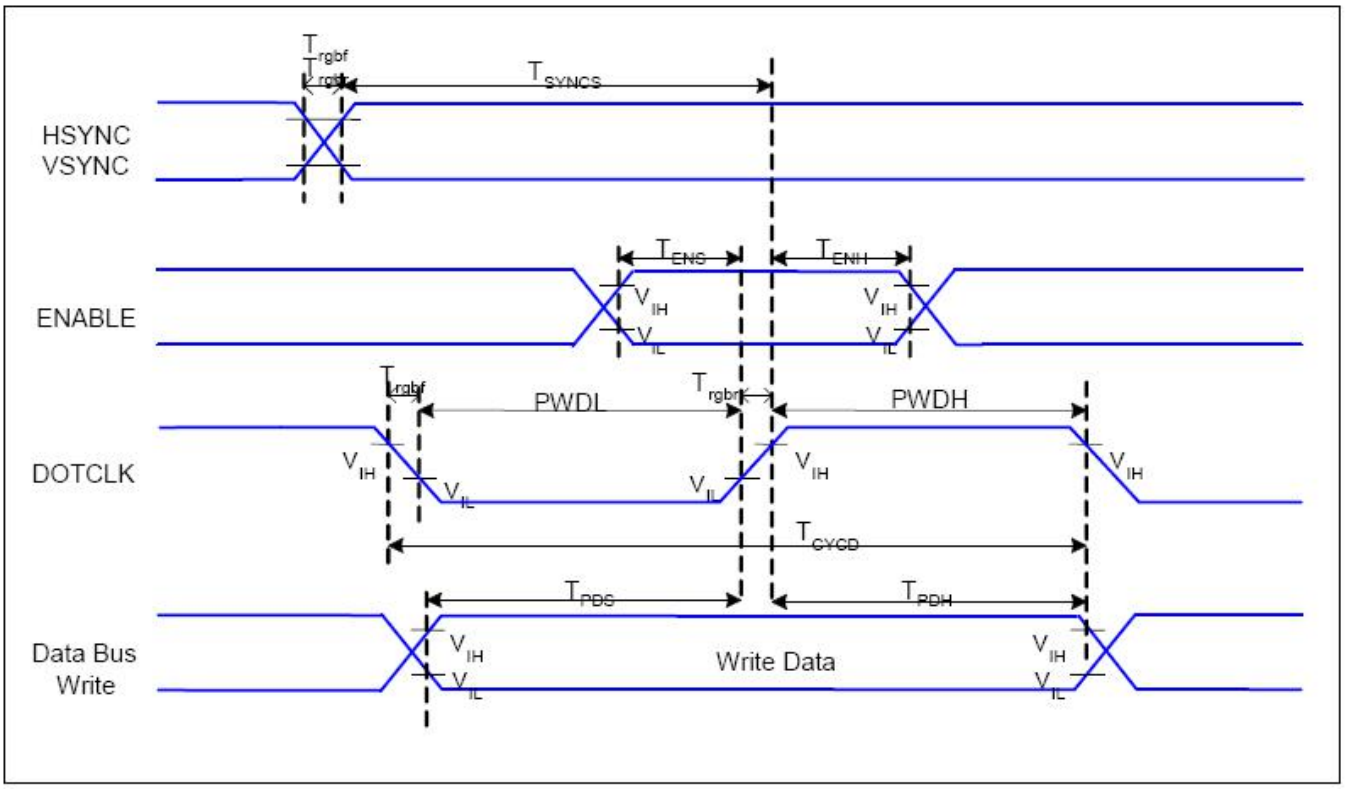


Figure 6.1: Parallel RGB Interface Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	5	-	ns	
	T_{ENH}	Enable Hold Time	5	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	33	-	ns	
	T_{RGHR}, T_{RGHF}	DOTCLK Rise/Fall Time	-	15	ns	
DE	T_{PDS}	PD Data Setup Time	5	-	ns	
	T_{PDH}	PD Data Hold Time	5	-	ns	

Table 6.1: Parallel RGB Interface Timing Characteristics

6.2 Display Serial Interface Characteristics (3-line SPI system)

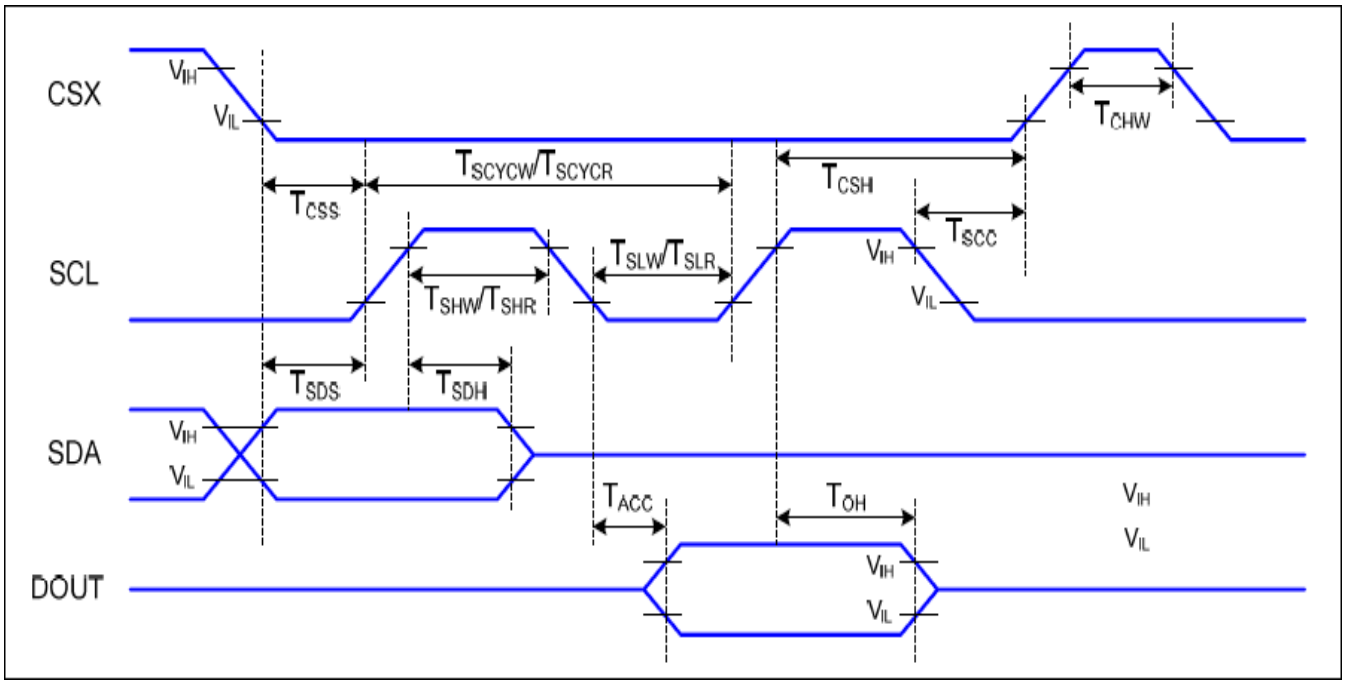


***Figure 6.2: Serial Interface* 3-SPI Timing Diagram**

IOVCC=1.8V, VCI=2.8V Ta=-30 to 70 C°

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	60		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	66		ns	
	T_{SHW}	SCL “H” pulse width (write)	15		ns	
	T_{SLW}	SCL “L” width (write)	15		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	
	T_{SHR}	SCL “H” pulse width (read)	60		ns	
	T_{SLR}	SCL “L” pulse width (read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10			

Table 6.2: 3-line Serial Interface Timing Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

6.3 Reset Timing

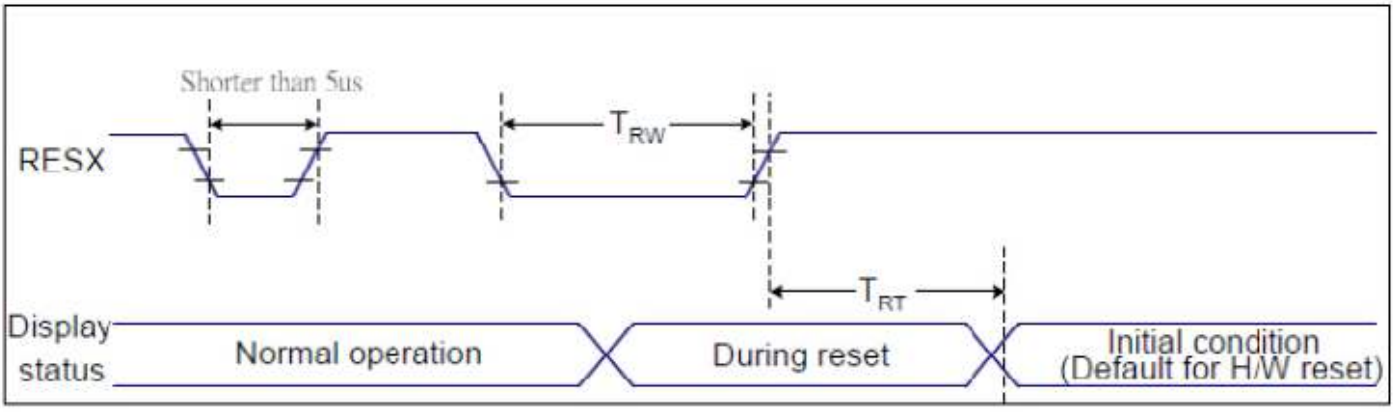


Figure 6.3: Reset Timing Diagram

Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

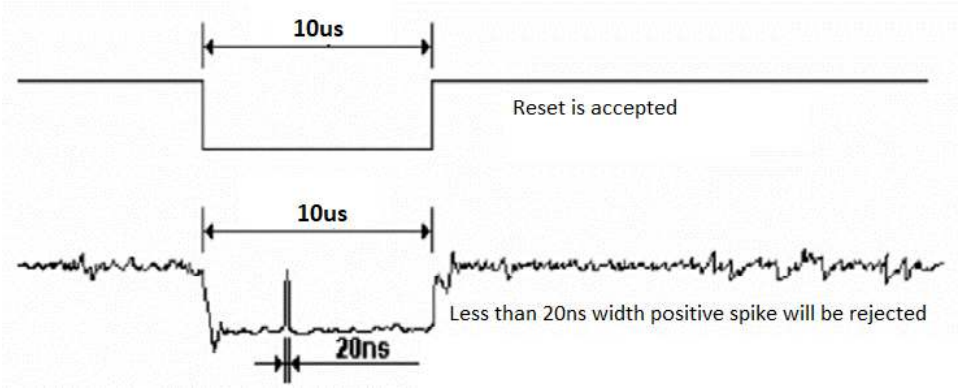
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

7. RGB Interface

The ST7701 support RGB interface Mode 1 and Mode 2. The interface signals as shown in ST7701S datasheet table 6.3.1.The Mode 1 and Mode 2 function is select by setting in the Command 2, please reference application note. In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D[23:0]), when DE is high state. The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer

PCLK, VS and HS signal to ST7701.In RGB Mode 2, back porch of Vsync is defined by VBP[5:0] of RGBPRCTR command. And back porch of Hsync is defined by HBP[5:0] of RGBPRCTR command. Front porch of Vsync is defined by VFP[5:0] of RGBPRCTR command. And front porch of Hsync is defined by HFP[5:0] of RGBPRCTR command.

7.1 DC Electrical Characteristics

RGB I/F Mode	PCLK	DE	VS	HS	DB[23:0]	Register for Blanking Porch Setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

Symbol	Name	Description
PCLK	Pixel Clock	Pixel clock for capturing pixels at display interface
HS	Horizontal Sync	Horizontal synchronizing timing signal
VS	Vertical Sync	Vertical synchronizing timing signal
DE	Data Enable	Data enable singal (assertion indicates valid pixels)
DB[23:0]	Pixel Data	Pixel data in 16/18/24-bit formal

7.2 RGB Interface Mode Selection

ST7701 supports two kinds of RGB interface, DE mode and HV mode. The table shown below uses command C3h to select RGB interface mode. DE/Sync = 0, DE RGB Mode selected. DE/Sync = 1, HV RGB mode is selected.

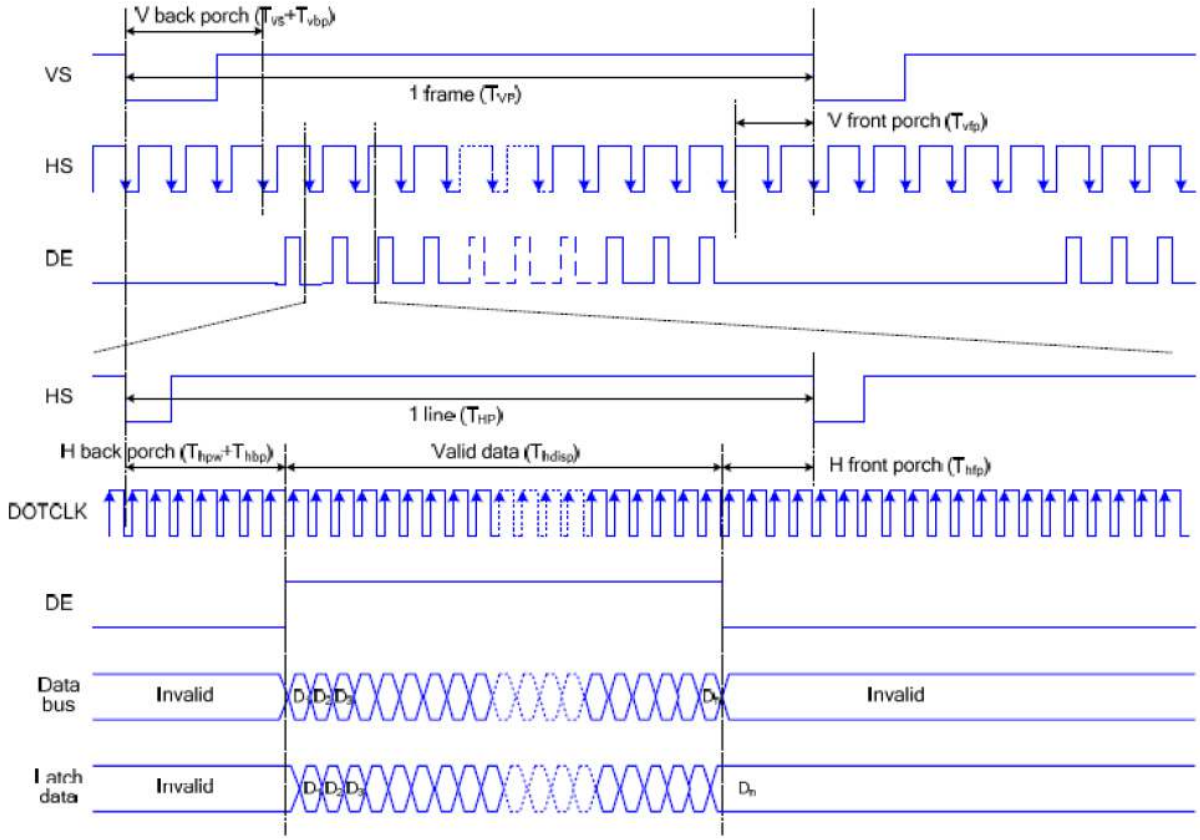
7.3 RGB Color Format

ST7701 supports two kinds of RGB interface, DE mode (mode 1) and HV mode (mode 2), and 16bit/18bit and 24-bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D[17:0] pins can be used; when HV mode is selected and the VSYNC, HSYNC, DOTCLK, D[17:0] pins can be used. When using RGB interface, only serial interface can be selected. Below is a table of the color mapping for the data transmission of the RGB interface.

Pad name	24 bits configuration VIPF[3:0]=0111	18 bits configuration VIPF[3:0]=0110		16 bits configuration VIPF[3:0]=0101
		MDT=0	MDT=1	
DB[23]	R7	Not used	Not used	Not used
DB[22]	R6	Not used	Not used	Not used
DB[21]	R5	R5	Not used	Not used
DB[20]	R4	R4	Not used	R4
DB[19]	R3	R3	Not used	R3
DB[18]	R2	R2	Not used	R2
DB[17]	R1	R1	R5	R1
DB[16]	R0	R0	R4	R0
DB[15]	G7	Not used	R3	Not used
DB[14]	G6	Not used	R2	Not used
DB[13]	G5	G5	R1	G5
DB[12]	G4	G4	R0	G4
DB[11]	G3	G3	G5	G3
DB[10]	G2	G2	G4	G2
DB[09]	G1	G1	G3	G1
DB[08]	G0	G0	G2	G0
DB[07]	B7	Not used	G1	Not used
DB[06]	B6	Not used	G0	Not used
DB[05]	B5	B5	B5	Not used
DB[04]	B4	B4	B4	B4
DB[03]	B3	B3	B3	B3
DB[02]	B2	B2	B2	B2
DB[01]	B1	B1	B1	B1
DB[00]	B0	B0	B0	B0

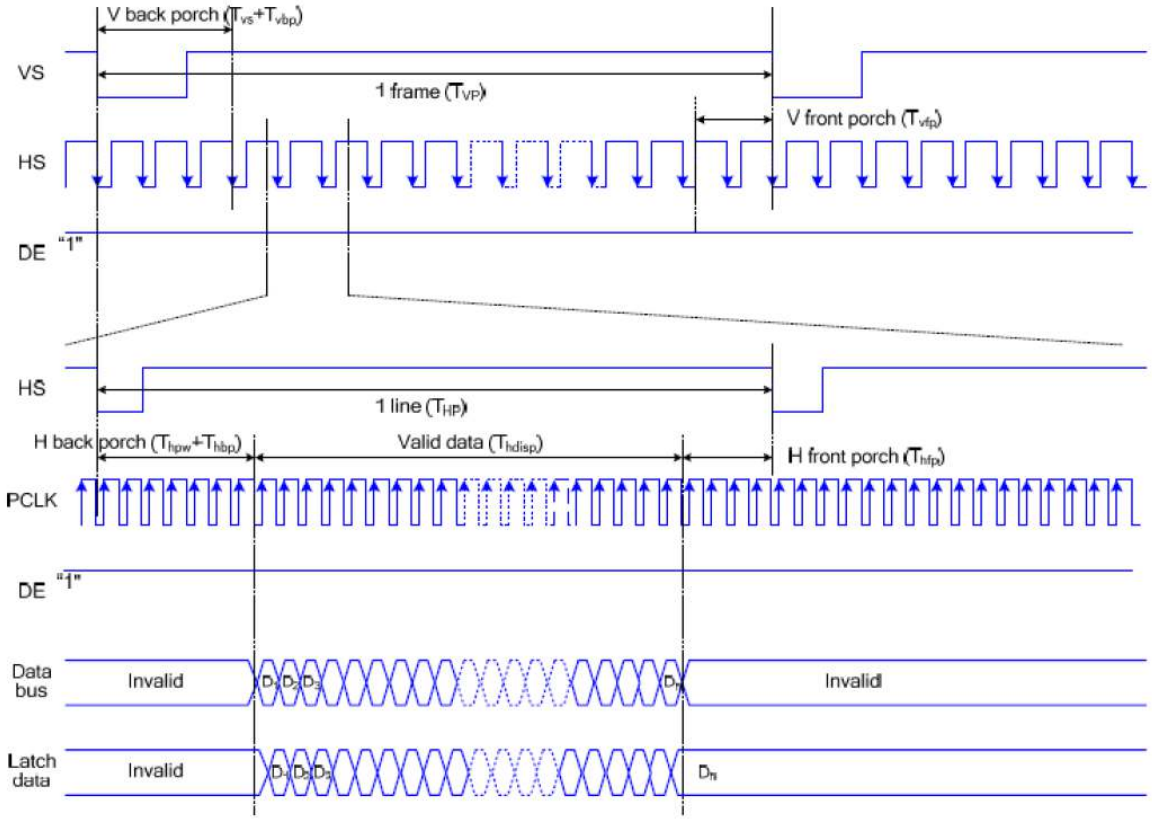
7.4 RGB Interface Timing Diagram

DE Mode



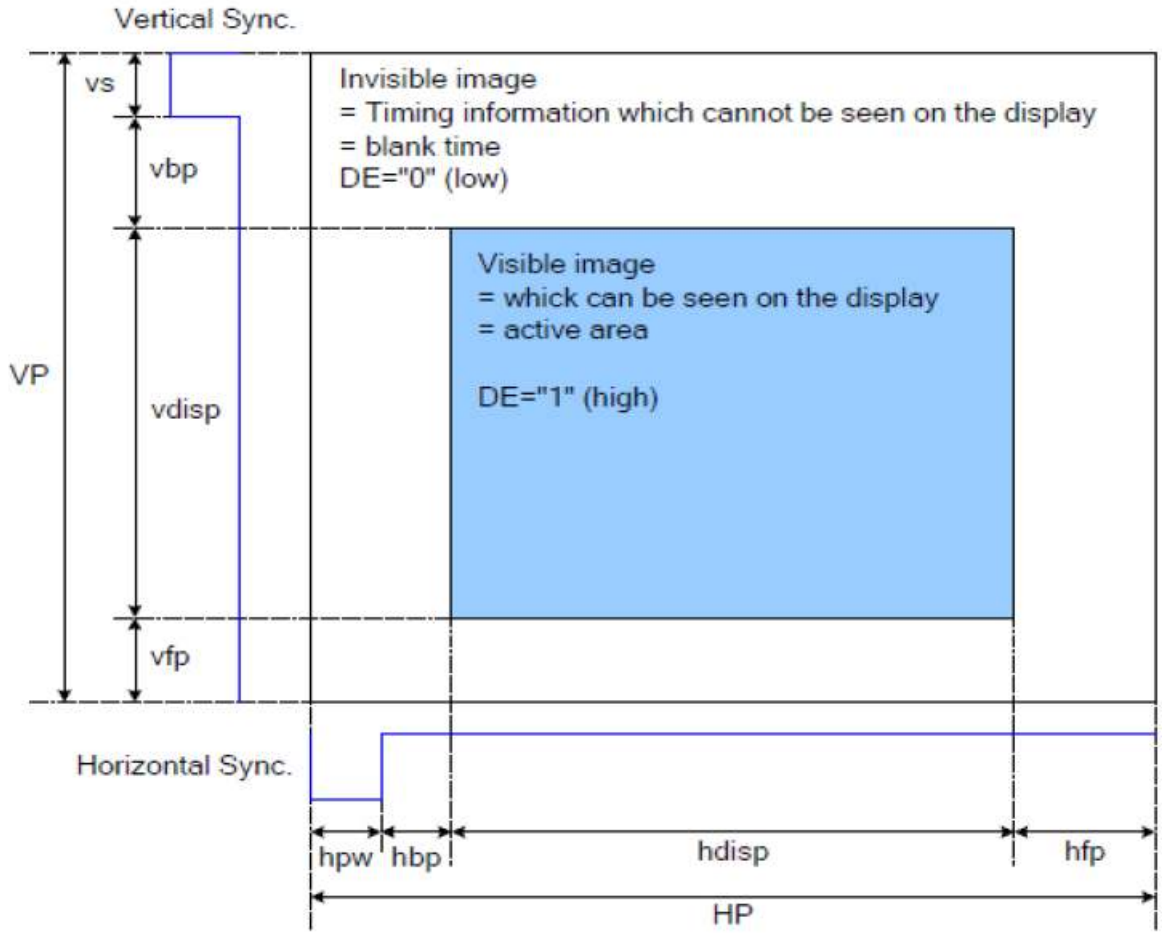
Note: The setting of front porch and back porch in host must match that in IC as this mode.

HV Mode



7.5 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC and DOTCLK signals. The data can be written only within the specified area with low power consumption by using the window address function. The back porch and front porch are used to set the RGB interface timing signals.



Parameter	Symbol	Condition	Min	Typ	Max	Unit
DCLK frequency	fclk		--	17	--	MHz
Horizontal sync width	hpw		1	8	255	Clock
Horizontal back porch	hbp		1	50	255	Clock
Horizontal front porch	hfp		1	10	--	Clock
Vertical sync width	vs		1	8	254	Line
Vertical back porch	vbp		1	20	254	Line
Vertical front porch	vfp		1	21	--	Line

8. Cautions and Handling Precautions

8.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

8.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.