AOZ1050PI

EZBuck™ 2 A Synchronous Buck Regulator

Not Recommended For New Designs

General Description

The AOZ1050PI is a high efficiency, easy to use, 2 A synchronous buck regulator. The AOZ1050PI works from 4.5 V to 18 V input voltage range, and provides up to 2 A of continuous output current with an output voltage adjustable down to 0.8 V.

The AOZ1050PI comes in an exposed pad SO-8 package and is rated over a -40 °C to +85 °C operating ambient temperature range.

Replacement Parts:

AOZ6662DI

AOZ6682CI

Features

- 4.5 V to 18 V operating input voltage range
- Synchronous Buck: 80 mΩ internal high-side switch and 50 mΩ internal low-side switch (at 12 V)
- Up to 95 % efficiency
- External soft start
- Output voltage adjustable to 0.8 V
- 2 A continuous output current
- 500 kHz PWM operation
- Cycle-by-cycle current limit
- Pre-bias start-up
- Short-circuit protection
- Thermal shutdown
- Exposed pad SO-8 package

Applications

- Point of load DC/DC converters
- LCD TV
- Set top boxes
- DVD and Blu-ray players/recorders
- Cable modems

Green Product

Typical Application

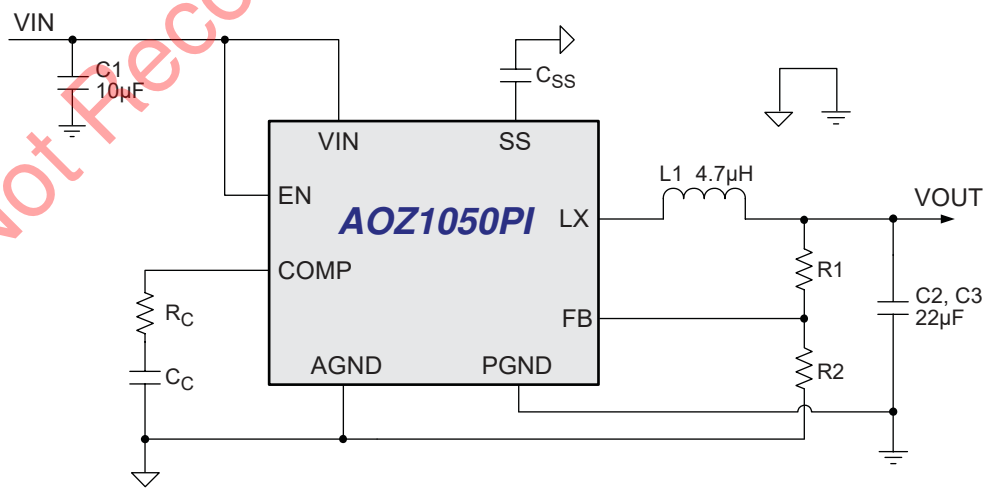


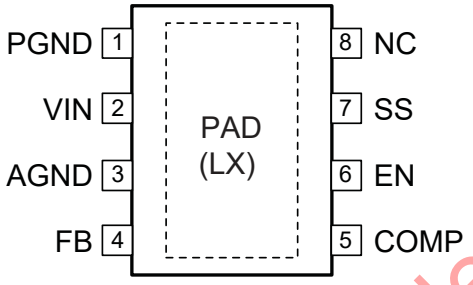
Figure 1. 3.3 V 2 A Synchronous Buck Regulator, Fs = 500 kHz

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ1050PI	-40 °C to +85 °C	EPAD SO-8	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration

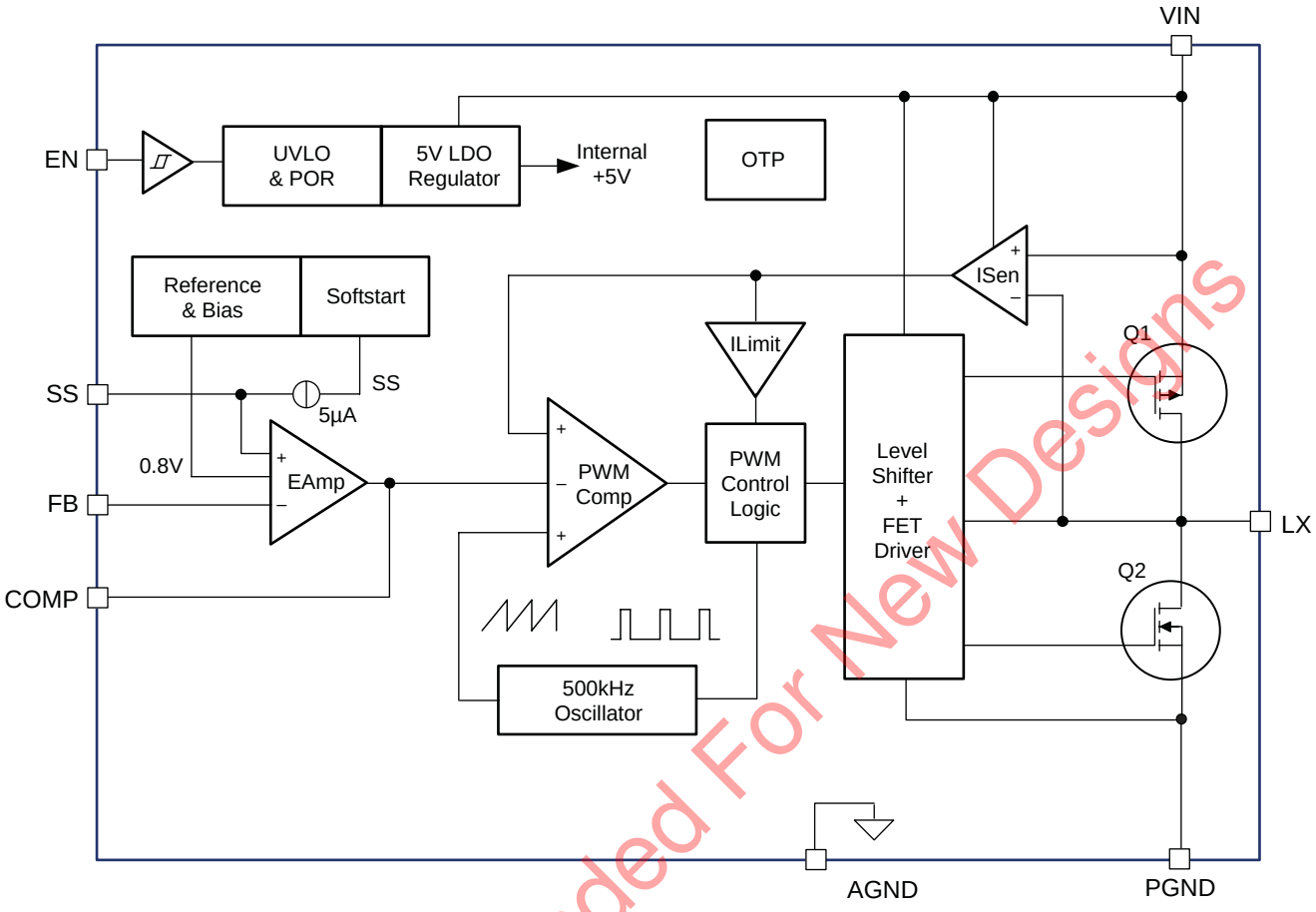


Exposed Pad SO-8
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PGND	Power ground. PGND needs to be electrically connected to AGND.
2	VIN	Supply voltage input. When VIN rises above the UVLO threshold and EN is logic high, the device starts up.
3	AGND	Analog ground. AGND is the reference point for controller section. AGND needs to be electrically connected to PGND.
4	FB	Feedback input. The FB pin is used to set the output voltage via a resistive voltage divider between the output and AGND.
5	COMP	External loop compensation pin. Connect a RC network between COMP and AGND to compensate the control loop.
6	EN	Enable pin. Pull EN to logic high to enable the device. Pull EN to logic low to disable the device. If on/off control in not needed, connect EN to VIN and do not leave it open.
7	SS	Soft-start pin. 5 µA current charging current.
8	NC	No Connect Pin. Pin 8 is not internally connected. Connect this pin externally to LX and use it for better thermal performance.
Exposed pad	LX	Switching node. LX is the drain of the internal PFET. LX is used as the thermal pad of the power stage.

Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
Supply Voltage (V_{IN})	20 V
LX to AGND	-0.7 V to V_{IN}+0.3 V
LX to AGND (20 ns)	-5 V to 22 V
EN to AGND	-0.3 V to V_{IN}+0.3 V
FB, SS, COMP to AGND	-0.3 V to 6.0 V
PGND to AGND	-0.3 V to +0.3 V
Junction Temperature (T_J)	+150 °C
Storage Temperature (T_S)	-65 °C to +150 °C
ESD Rating[1]	2.0 kV

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5 kΩ in series with 100 pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (V_{IN})	4.5 V to 18 V
Output Voltage Range	0.8 V to 0.85 • V_{IN}
Ambient Temperature (T_A)	-40 °C to +85 °C
Package Thermal Resistance Exposed Pad SO-8 (Θ_{JA})[2]	50 °C/W

Note:

2. The value of Θ_{JA} is measured with the device mounted on a 1-in^2 FR-4 board with 2 oz. Copper, in a still air environment with T_A = 25 °C. The value in any given application depends on the user's specific board design.

Electrical Characteristics

T_A = 25 °C, V_{IN} = V_{EN} = 12 V, V_{OUT} = 3.3 V unless otherwise specified[3]

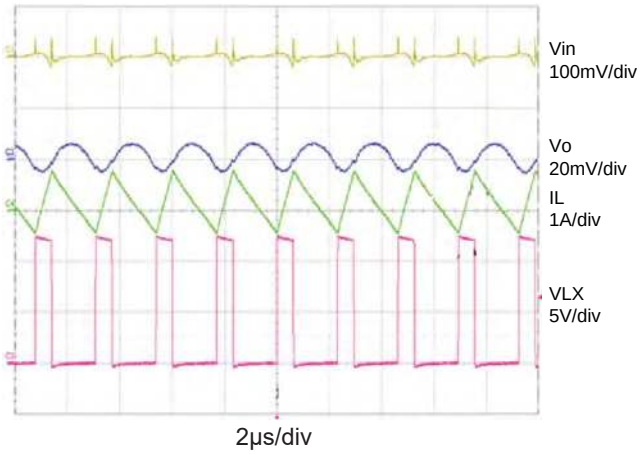
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN}	Supply Voltage		**4.5**		**18**	V
V_{UVLO}	Input Under-Voltage Lockout Threshold	V_{IN} Rising V_{IN} Falling		4.1 3.7		V
I_{IN}	Supply Current (Quiescent)	I_{OUT} = 0, VFB = 1.2 V, V_{EN} > 1.2 V		1.6	2.5	mA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0 V		**1**	**10**	µA
V_{FB}	Feedback Voltage	T_A = 25 °C	0.788	0.8	0.812	V
	Load Regulation			0.5		%
	Line Regulation			1		%
I_{FB}	Feedback Voltage Input Current				200	nA
V_{EN}	EN Input Threshold	Off Threshold On Threshold	 **2**		**0.6**	V
V_{HYS}	EN Input Hysteresis			100		mV
	EN Leakage Current				**1**	µA
	SS Time	C_{SS} = 16 nF		2		ms
MODULATOR						
f_O	Frequency		400	500	600	kHz
D_{MAX}	Maximum Duty Cycle		85			%
T_{MIN}	Controllable Minimum On Time				150	ns
	Current Sense Transconductance			7		A / V
	Error Amplifier Transconductance			200		µA / V
PROTECTION						
I_{LIM}	Current Limit		2.5	3.5		A
	Over-Temperature Shutdown Limit	T_J Rising T_J Falling		150 100		°C
OUTPUT STAGE						
	High-Side Switch On-Resistance	V_{IN} = 12 V V_{IN} = 5 V		80 120		mΩ
	Low-Side Switch On-Resistance	V_{IN} = 12 V V_{IN} = 5 V		50 60		mΩ

Note:
3. Specification in **BOLD** indicate an ambient temperature range of -40 °C to +85 °C. These specifications are guaranteed by design.

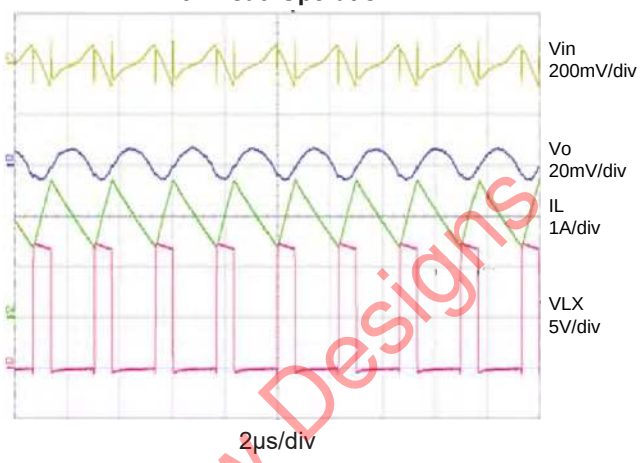
Typical Performance Characteristics

Circuit of Figure 1. T_A = 25 °C, V_{IN} = V_{EN} = 12 V, V_{OUT} = 3.3 V unless otherwise specified.

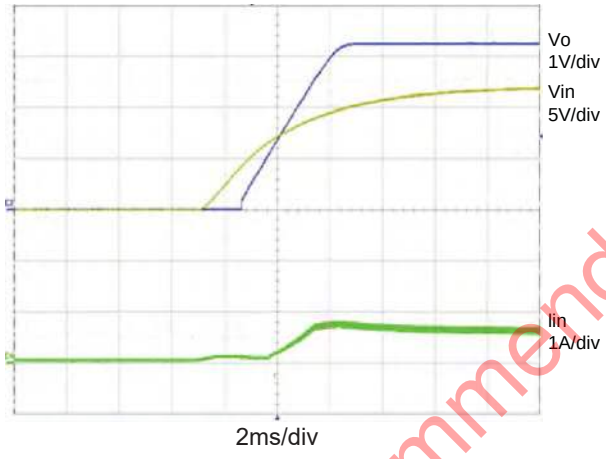
Light Load Operation



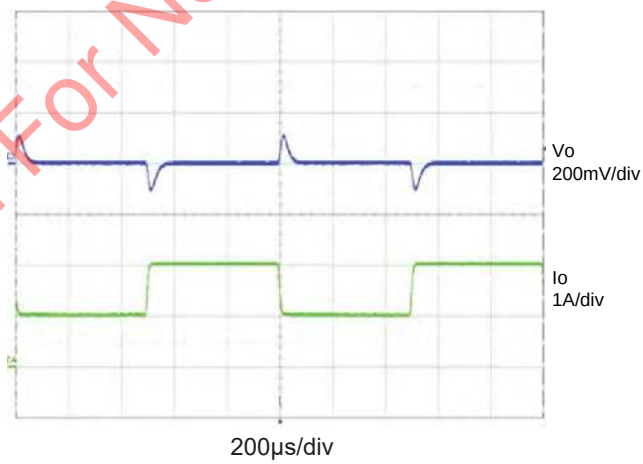
Full Load Operation



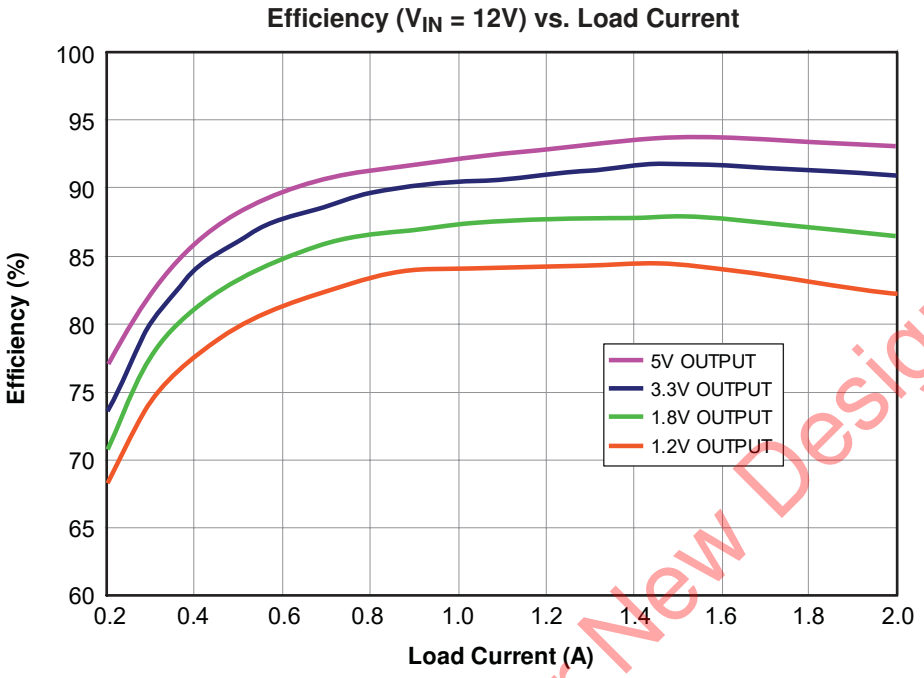
Start Up to Full Load



50% to 100% Load Transient



Efficiency



Detailed Description

The AOZ1050PI is a current-mode step down regulator with an integrated high-side PMOS switch and a low-side NMOS switch. The AOZ1050PI operates from a 4.5 V to 18 V input voltage range and supplies up to 2 A of load current. Features include enable control, power-on reset, input under voltage lockout, output over voltage protection, external soft-start and thermal shut down.

The AOZ1050PI is available in an exposed pad SO-8 package.

Enable and Soft Start

The AOZ1050PI has an external soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. The soft start process begins when the input voltage rises to 4.1 V and voltage on the EN pin is HIGH. In the soft start process, the FB voltage is ramped to follow the voltage of the soft start pin until it reaches 0.8 V. The voltage of the soft-start pin is charged by an internal 5 µA current.

The EN pin of the AOZ1050PI is active high. Connect the EN pin to VIN if the enable function is not used. Pulling EN to ground will disable the AOZ1050PI. Do not leave EN open. The voltage on the EN pin must be above 2 V to enable the AOZ1050PI. When the EN pin voltage falls below 0.6 V, the AOZ1050PI is disabled.

Steady-State Operation

Under heavy load steady-state conditions, the converter operates in fixed frequency and Continuous-Conduction Mode (CCM).

The AOZ1050PI integrates an internal P-MOSFET as the high-side switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the high side power MOSFET. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and reference voltage is amplified by the internal transconductance error amplifier. The error voltage, which shows on the COMP pin, is compared against the current signal, which is the sum of inductor current signal and ramp compensation signal, at the PWM comparator input. If the current signal is less than the error voltage, the internal high-side switch is on. The inductor current flows from the input through the inductor to the output. When the current signal exceeds the error voltage, the high-side switch is off. The inductor current is freewheeling through the internal low-side N-MOSFET switch to output. The internal adaptive FET driver guarantees no turn on overlap of both the high-side and the low-side switch.

Compared with regulators using freewheeling Schottky diodes, the AOZ1050PI uses a freewheeling NMOSFET to realize synchronous rectification. This greatly improves the converter efficiency and reduces power loss in the low-side switch.

The AOZ1050PI uses a P-Channel MOSFET as the high-side switch. This saves the bootstrap capacitor normally seen in a circuit using an NMOS switch. It also allows 100 % turn-on of the high-side switch to achieve linear regulation mode of operation. The minimum voltage drop from V_{IN} to V_O is the load current times DC resistance of the MOSFET plus DC resistance of the buck inductor. It can be calculated by equation below:

$$V_{O\_MAX} = V_{IN} - I_O \times R_{DS(ON)}$$

where;

V_{O_MAX} is the maximum output voltage,

V_{IN} is the input voltage from 4.5 V to 18 V,

I_O is the output current from 0 A to 2 A, and

$R_{DS(ON)}$ is the on resistance of the internal MOSFET.

Output Voltage Programming

Output voltage can be set by feeding back the output to the FB pin using a resistor divider network as shown in Figure 1. The resistor divider network includes R_1 and R_2. Usually, a design is started by picking a fixed R_2 value and calculating the required R_1 with the equation below:

$$V_O = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Some standard value of R_1 and R_2 for the most common output voltages are listed in Table 1.

Table 1.

V_O (V)	R_1 (kΩ)	R_2 (kΩ)
0.8	1.0	Open
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	31.1	10
5.0	52.3	10

The combination of R_1 and R_2 should be large enough to avoid drawing excessive current from the output, which will cause power loss.

Since the switch duty cycle can be as high as 100 %, the maximum output voltage can be set as high as the input voltage minus the voltage drop on the upper PMOS and the inductor.

Protection Features

The AOZ1050PI has multiple protection features to prevent system circuit damage under abnormal conditions.

Over Current Protection (OCP)

The sensed inductor current signal is also used for over current protection. Since the AOZ1050PI employs peak current mode control, the COMP pin voltage is proportional to the peak inductor current. The COMP pin voltage is limited to be between 0.4 V and 2.5 V internally. The peak inductor current is automatically limited cycle-by-cycle.

When the output is shorted to ground under fault conditions, the inductor current slowly decays during a switching cycle because the output voltage is 0 V. To prevent catastrophic failure, a secondary current limit is designed inside the AOZ1050PI. The measured inductor current is compared against a preset voltage which represents the current limit, between 3.5 A and 5.0 A. When the output current is greater than the current limit, the high side switch will be turned off. The converter will initiate a soft start once the over-current condition is resolved.

Power-On Reset (POR)

A power-on reset circuit monitors the input voltage. When the input voltage exceeds 4.1 V, the converter starts operation. When input voltage falls below 3.7 V, the converter will be shut down.

Thermal Protection

An internal temperature sensor monitors the junction temperature. The sensor shuts down the internal control circuit and high side PMOS if the junction temperature exceeds 150 ºC. The regulator will restart automatically under the control of the soft-start circuit when the junction temperature decreases to 100 ºC.

Application Information

The basic AOZ1050PI application circuit is show in Figure 1. Component selection is explained below.

Input Capacitor

The input capacitor must be connected to the V_{IN} pin and the PGND pin of AOZ1050PI to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}\left(1 - \frac{V_O}{V_{IN}}\right)}$$

if we let *m* equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relationship between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 2 below. It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is 0.5 x I_O.

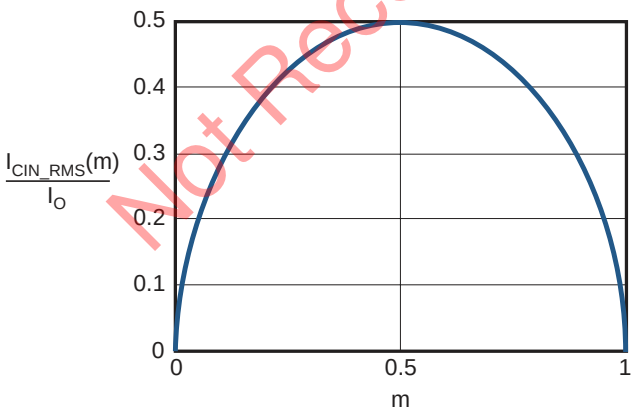


Figure 2. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have a current rating higher than I_{CIN_RMS} at the worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high current rating. Depending on the application circuits, other low ESR tantalum capacitors may be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors should be used for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures are based on a certain operating life time. Further de-rating may need to be considered for long term reliability.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For a given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on the inductor is designed to be 20 % to 40 % of output current.

When selecting the inductor, confirm it is able to handle the peak current without saturation at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on the inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. However, they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times \left(ESR_{CO} + \frac{1}{8 \times f \times C_O} \right)$$

where,

C_O is output capacitor value, and

ESR_{CO} is the equivalent series resistance of the output capacitor.

When a low ESR ceramic capacitor is used as the output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum capacitors are recommended as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, the output capacitor could be overstressed.

Loop Compensation

The AOZ1050PI employs peak current mode control for ease of use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It also greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole can be calculated by:

$$f_{P1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to the output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

where;

C_O is the output filter capacitor,

R_L is load resistor value, and

ESR_{CO} is the equivalent series resistance of output capacitor.

The compensation design shapes the converter control loop transfer function for the desired gain and phase. Several different types of compensation networks can be used with the AOZ1050PI. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ1050PI, FB and COMP are the inverting input and the output of the internal error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{P2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

where;

G_{EA} is the error amplifier transconductance, which is 200 x 10^{-6} A/V,

G_{VEA} is the error amplifier voltage gain, which is 500 V/V, and

C_C is the compensation capacitor in Figure 1.

The zero given by the external compensation network, capacitor C_C and resistor R_C, is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

To design the compensation circuit, a target crossover frequency f_C to close the loop must be selected. The system crossover frequency is where the control loop has unity gain. The crossover is the also called the converter bandwidth. Generally a higher bandwidth means faster response to load transients. However, the bandwidth should not be too high because of system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be equal or less than 1/10 of the switching frequency.

The strategy for choosing R_C and C_C is to set the cross over frequency with R_C and set the compensator zero with C_C. Using selected crossover frequency, f_C, to calculate R_C:

$$R_C = f_C \times \frac{V_O}{V_{FB}} \times \frac{2\pi \times C_C}{G_{EA} \times G_{CS}}$$

where;

f_C is the desired crossover frequency. For best performance, f_C is set to be about 1/10 of the switching frequency;

V_{FB} is 0.8V,

G_{EA} is the error amplifier transconductance, which is 200×10^{-6} A/V, and

G_{CS} is the current sense circuit transconductance, which is 8 A/V

The compensation capacitor C_C and resistor R_C together make a zero. This zero is put somewhere close to the dominate pole f_{p1} but lower than 1/5 of the selected crossover frequency. C_C can is selected by:

$$C_C = \frac{1.5}{2\pi \times R_C \times f_{P1}}$$

The above equation can be simplified to:

$$C_C = \frac{C_O \times R_L}{R_C}$$

An easy-to-use application software which helps to design and simulate the compensation loop can be found at www.aosmd.com.

Thermal Management and Layout Considerations

In the AOZ1050PI buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the VIN pin, to the LX pad, to the filter inductor, to the output capacitor and load, and then returns to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from the inductor, to the output capacitors and load, to the low side NMOSFET. Current flows in the second loop when the low side NMOSFET is on.

In PCB layout, minimizing the area of the two loops will reduce the noise of the circuit and improves efficiency. A ground plane is strongly recommended to connect the input capacitor, the output capacitor, and the PGND pin of the AOZ1050PI.

In the AOZ1050PI buck regulator circuit, the major power dissipating components are the AOZ1050PI and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power:

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of the inductor can be approximately calculated by the output current and DCR value of the inductor:

$$P_{inductor\_loss} = I_O^2 \times R_{inductor} \times 1.1$$

The actual junction temperature can be calculated by the power dissipation in the AOZ1050PI and the thermal impedance from junction to ambient:

$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss}) \times \Theta_{JA}$$

The maximum junction temperature of the AOZ1050PI is 150 ºC, which limits the maximum load current capability.

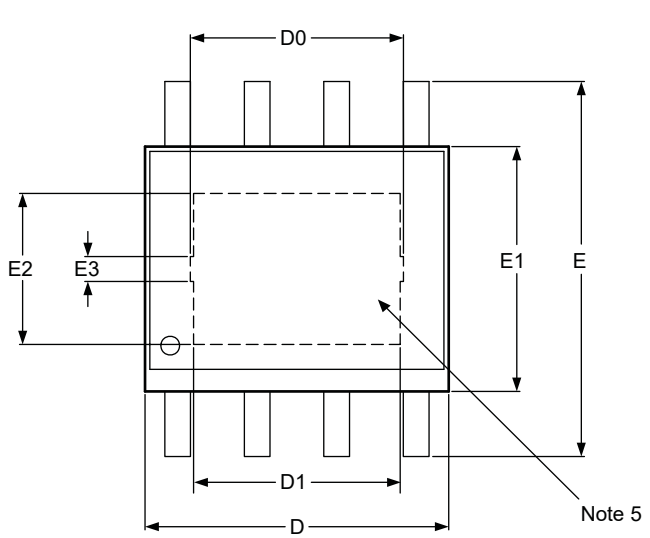
The thermal performance of the AOZ1050PI is strongly affected by the PCB layout. Care should be taken during the design process to ensure that the IC will operate under the recommended environmental conditions.

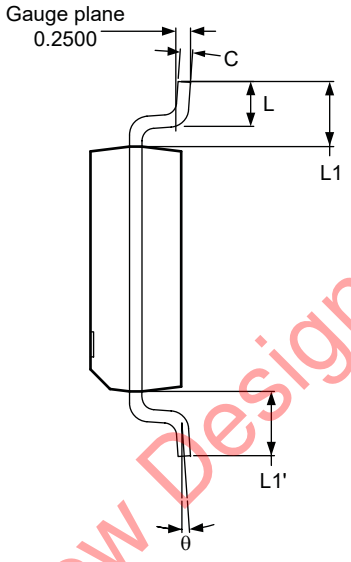
Layout Considerations

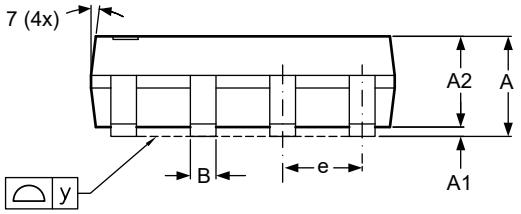
The AOZ1050PI is an exposed pad SO-8 package. Several layout tips are listed for the best electric and thermal performance.

1. The exposed pad (LX) is connected to the internal PFET and NFET drains. Connected a large copper plane to the LX pin to help thermal dissipation.
2. Do not use a thermal relief connection to the VIN pin or the PGND pin. Pour a maximized copper area to the PGND pin and the VIN pin to help thermal dissipation.
3. The input capacitor should be connected as close as possible to the VIN pin and the PGND pin.
4. A ground plane is preferred. If a ground plane is not used, separate PGND from AGND and only connect them at one point to avoid the PGND pin noise coupling to the AGND pin.
5. Make the current trace from the LX pad to L to Co to the PGND as short as possible.
6. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.
7. Keep sensitive signal trace away from the LX pad.

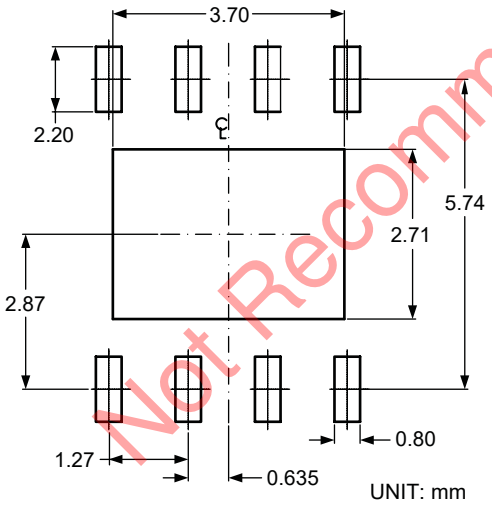
Package Dimensions, SO-8 EP1







RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.40	1.55	1.70
A1	0.00	0.05	0.10
A2	1.40	1.50	1.60
B	0.31	0.406	0.51
C	0.17	—	0.25
D	4.80	4.96	5.00
D0	3.20	3.40	3.60
D1	3.10	3.30	3.50
E	5.80	6.00	6.20
e	—	1.27	—
E1	3.80	3.90	4.00
E2	2.21	2.41	2.61
E3	0.40 REF		
L	0.40	0.95	1.27
y	—	—	0.10
θ	0°	3°	8°
| L1–L1' |	—	0.04	0.12
L1	1.04 REF		

Dimensions in inches

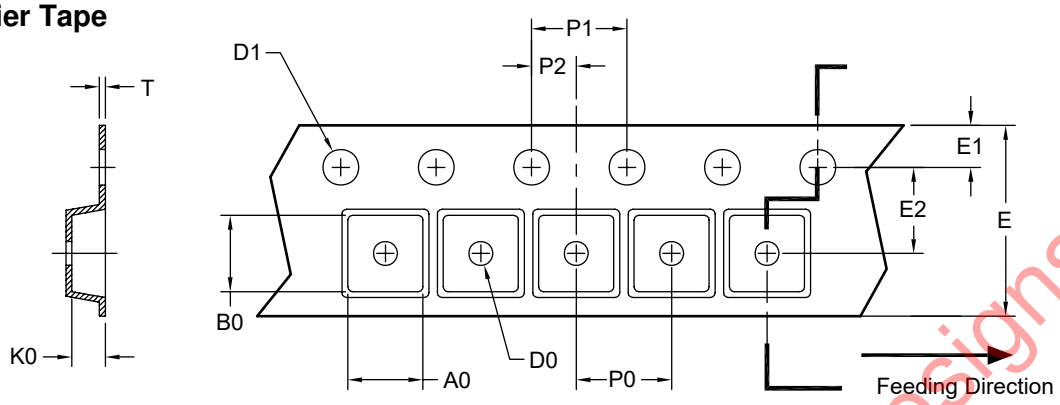
Symbols	Min.	Nom.	Max.
A	0.055	0.061	0.067
A1	0.000	0.002	0.004
A2	0.055	0.059	0.063
B	0.012	0.016	0.020
C	0.007	—	0.010
D	0.189	0.195	0.197
D0	0.126	0.134	0.142
D1	0.122	0.130	0.138
E	0.228	0.236	0.244
e	—	0.050	—
E1	0.150	0.153	0.157
E2	0.087	0.095	0.103
E3	0.016 REF		
L	0.016	0.037	0.050
y	—	—	0.004
θ	0°	3°	8°
| L1–L1' |	—	0.002	0.005
L1	0.041 REF		

Notes:

1. Package body sizes exclude mold flash and gate burrs.
2. Dimension L is measured in gauge plane.
3. Tolerance 0.10mm unless otherwise specified.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
5. Die pad exposure size is according to lead frame design.
6. Followed from JEDEC MS-012

Tape and Reel Dimensions, SO-8 EP1

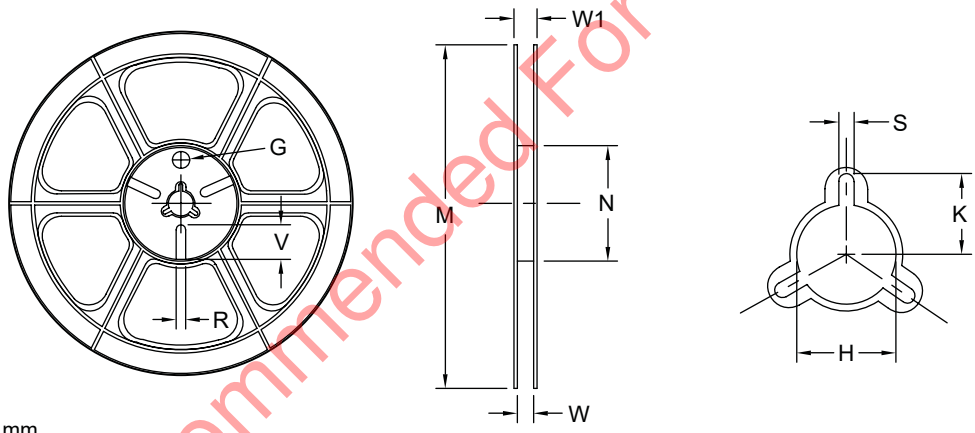
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SO-8 (12mm)	6.40 ±0.10	5.20 ±0.10	2.10 ±0.10	1.60 ±0.10	1.50 ±0.10	12.00 ±0.10	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.25 ±0.10

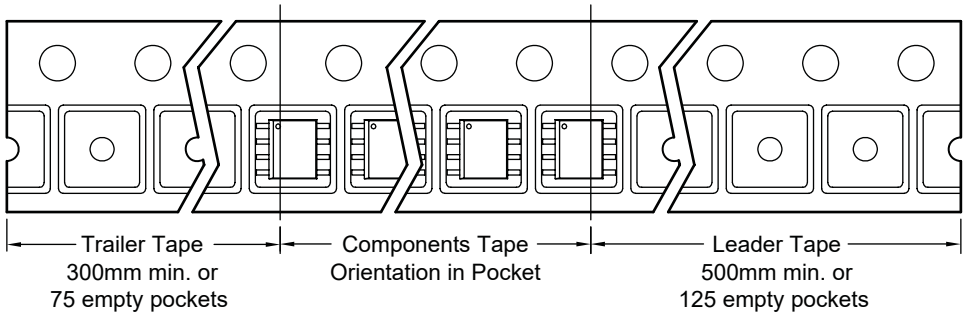
Reel



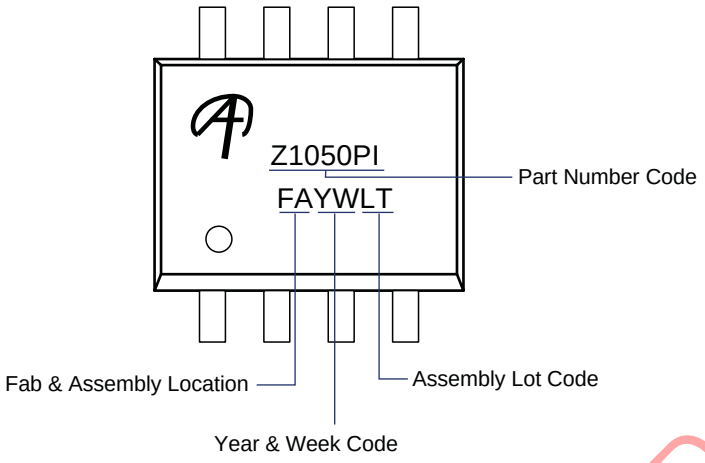
UNIT: mm

Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50/-0.20	10.60	2.00 ±0.50	—	—	—

Leader/Trailer and Orientation



Part Marking



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.