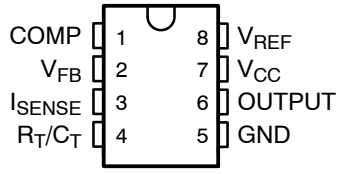
UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP
CURRENT-MODE PWM CONTROLLER

SGLS134D – SEPTEMBER 2002 – REVISED JANUARY 2013

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **Optimized for Off-line and DC-to-DC Converters**
- **Low Start Up Current (<0.5 mA)**
- **Trimmed Oscillator Discharge Current**
- **Automatic Feed Forward Compensation**
- **Pulse-by-Pulse Current Limiting**
- **Enhanced Load Response Characteristics**
- **Under-Voltage Lockout With Hysteresis**
- **Double Pulse Suppression**
- **High Current Totem Pole Output**
- **Internally Trimmed Bandgap Reference**
- **500 kHz Operation**
- **Low R_O Error Amp**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

D PACKAGE
(TOP VIEW)



description

The UC1842A/3A/4A/5A family of control ICs is a pin-for-pin compatible improved version of the UC3842/3/4/5 family. Providing the necessary features to control current mode switched mode power supplies, this family has the following improved features. Start up current is guaranteed to be less than 0.5 mA. Oscillator discharge is trimmed to 8.3 mA. During under voltage lockout, the output stage can sink at least 10 mA at less than 1.2 V for V_{CC} over 5 V.

The difference between members of this family are shown in the table below.

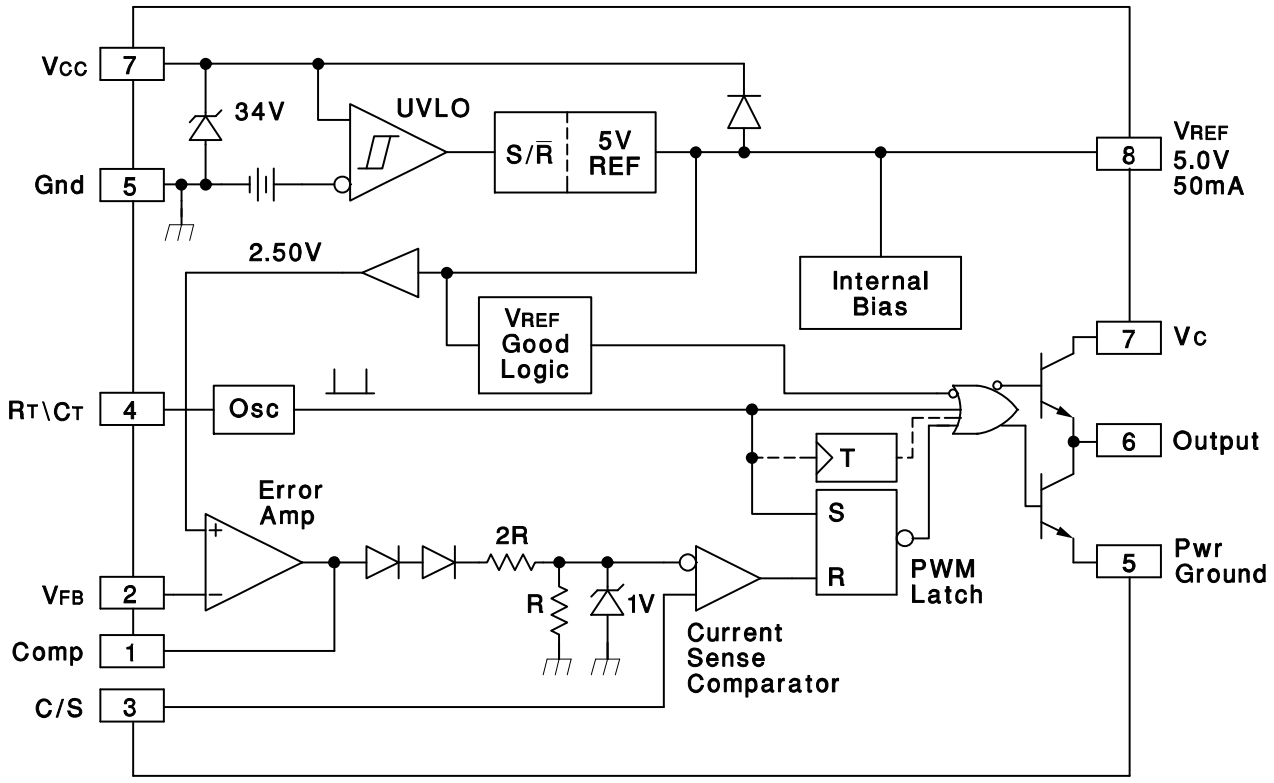
PART NUMBER	UVLO ON	UVLO OFF	MAXIMUM DUTY CYCLE
UC1842A	16 V	10 V	<100%
UC1843A	8.5 V	7.9 V	<100%
UC1844A	16 V	10 V	<50%
UC1845A	8.5 V	7.9 V	<50%

ORDERING INFORMATION‡

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOP – D	Tape and reel	UC1842AMDREP	1842AME
–55°C to 125°C	SOP – D	Tape and reel	UC1843AMDREP	1843AME
–55°C to 125°C	SOP – D	Tape and reel	UC1844AMDREP	1844AME
–55°C to 125°C	SOP – D	Tape and reel	UC1845AMDREP	1845AME

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

block diagram



NOTES: 1. Toggle flip flop used only in 1844A and 1845A.

Ordering Information

UC 184 4 A M D R EP

- EP — ENHANCED PLASTIC INDICATOR
- R — TAPE and REEL INDICATOR
- D — PACKAGE
  - D = Plastic SOIC
- M — MILITARY TEMPERATURE RANGE INDICATOR
- A — IMPROVED PERFORMANCE INDICATOR
- 4 — PRODUCT OPTION
  - 2 through 5

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†‡

V_{CC} voltage (low impedance source) . . . . . 30 V
V_{CC} voltage (I_{CC} mA) . . . . . self limiting
Output current, I_O . . . . . ±1 A
Output energy (capacitive load) . . . . . 5 μJ
Analog Inputs (pins 2, 3) . . . . . –0.3 V to 6.3 V
Error Amp Output Sink current . . . . . 10 mA
Power Dissipation at T_A < 25°C . . . . . 1 W
Package thermal impedance, θ_{JA} (see Note 1): . . . . . 97°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Maximum junction temperature, T_J . . . . . 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Unless otherwise indicated, voltages are reference to ground and currents are positive into and negative out of the specified terminals.

NOTE 1: Long term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

electrical characteristics, T_A = –55°C to 125°C for the UC184xAM-EP, V_{CC} = 15 V (see Note 1), R_T = 10 kΩ, C_T = 3.3 nF, and T_A = T_J (unless otherwise stated)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Reference Section						
Output voltage	T_J = 25°C, I_O = 1 mA		4.95	5	5.05	V
Line regulation voltage	V_{IN} = 12 V to 25 V			6	20	mV
Load regulation voltage	I_O = 1 mA to 20 mA			6	25	mV
Temperature stability	See Notes NO TAG and NO TAG			0.2	0.4	mV/°C
Total output variation voltage	Line, Load, Temp.		4.9		5.1	V
Output noise voltage	f = 10 Hz to 10 kHz, See Note NO TAG	T_J = 25°C		50		μV
Long term stability	1000 hours, See Note 2	T_A = 125°C		5	25	mV
Output short-circuit current			–30	–100	–180	mA
Oscillator Section						
Initial accuracy	See Note NO TAG	T_J = 25°C	47	52	57	kHz
Voltage stability	V_{CC} = 12 V to 25 V			0.2%	1%	
Temperature stability	T_A = MIN to MAX, See Note 2			5%		
Amplitude peak-to-peak	V pin 4, See Note 2			1.7		V
Discharge current	V pin 4 = 2 V, See Note 3	T_J = 25°C	7.8	8.3	8.8	mA
		T_J = Full range	7.5		8.8	

NOTES: 1. Adjust V_{CC} above the start threshold before setting at 15 V.
2. Not production tested.
3. This parameter is measured with R_T = 10 kΩ to V_{REF}. This contributes approximately 300 μA of current to the measurement. The total current flowing into the $R_{T/C}$ pin will be approximately 300 μA higher than the measured value.

electrical characteristics, T_A = –55°C to 125°C for the UC184xAM-EP, V_{CC} = 15 V (see Note 1), R_T = 10 kΩ, C_T = 3.3 nF, and $T_A = T_J$ (unless otherwise stated)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Error Amplifier Section						
Input voltage	COMP = 2.5 V		2.45	2.5	2.55	V
Input bias current				–0.3	–1	μA
Open loop voltage gain (A_{VOL})	V_O = 2 V to 4 V		65	90		dB
Unity gain bandwidth	See Note 2	T_J = 25°C	0.7	1		MHz
PSRR	V_{CC} = 12 V to 25 V		60	70		dB
Output sink current	FB = 2.7 V, COMP = 1.1 V		2	6		mA
Output source current	FB = 2.3 V, COMP = 5 V		–0.5	–0.8		mA
V_{OUT} high	FB = 2.3 V, R_L = 15 kΩ to GND		5	6		V
V_{OUT} low	FB = 2.7 V, R_L = 15 kΩ to V_{REF}			0.7	1.1	V
Current Sense Section						
Gain	See Note 3 and Note 4		2.85	3	3.15	V/V
Maximum input signal	COMP = 5 V, See Note 3		0.9	1	1.1	V
PSRR	V_{CC} = 12 V to 25 V, See Note 3			70		dB
Input bias current				–2	–10	μA
Delay to output	I_{SENSE} = 0 V to 2 V, See Note 2			150	300	ns
Output Section (OUT)						
Low-level output voltage	I_{OUT} = 20 mA			0.1	0.4	V
	I_{OUT} = 200 mA			15	2.2	
High-level output voltage	I_{OUT} = –20 mA		13	13.5		V
	I_{OUT} = –200 mA		12	13.5		
Rise time	C_L = 1 nF, See Note 2	T_J = 25°C		50	150	ns
Fall time	C_L = 1 nF, See Note 2	T_J = 25°C		50	150	ns
UVLO saturation	V_{CC} = 5 V, I_{OUT} = 10 mA			0.7	1.2	V
Undervoltage Lockout Section						
Start threshold		UC1842A, UC1844A	15	16	17	V
		UC1843A, UC1845A	7.8	8.4	9	
Minimum operation voltage after turn on		UC1842A, UC1844A	9	10	11	V
		UC1843A, UC1845A	7	7.6	8.2	

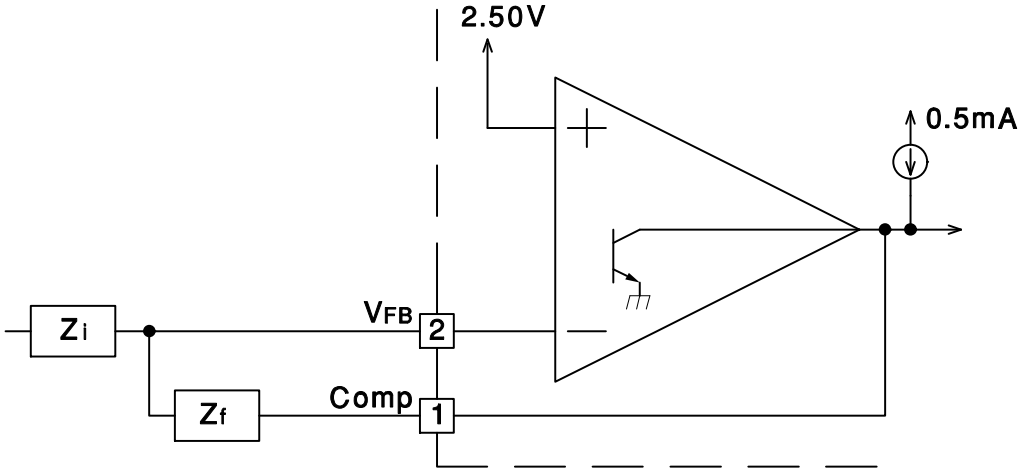
NOTES: 1. Adjust V_{CC} above the start threshold before setting at 15 V.
2. Not production tested.
3. Parameter measured at trip point of latch with V_{FB} at 0 V.
4. Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{SENSE}}$; $0 \le V_{SENSE} \le 0.8$ V.

electrical characteristics, T_A = –55°C to 125°C for the UC184xAM-EP, V_{CC} = 15 V (see Note 1), R_T = 10 kΩ, C_T = 3.3 nF, and T_A = T_J (unless otherwise stated)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
PWM Section						
Maximum duty cycle		UC1842A, UC1843A	94%	96%	100%	
		UC1844A, UC1845A	47%	48%	50%	
Minimum duty cycle					0%	
Total Standby Current						
Start-up current				0.3	0.5	mA
Operating supply current	FB = 0 V, SENSE = 0 V			11	17	mA
V_{CC} internal zener voltage	I_{CC} = 25 mA		30	34		V

NOTES: 1. Adjust V_{CC} above the start threshold before setting at 15 V.

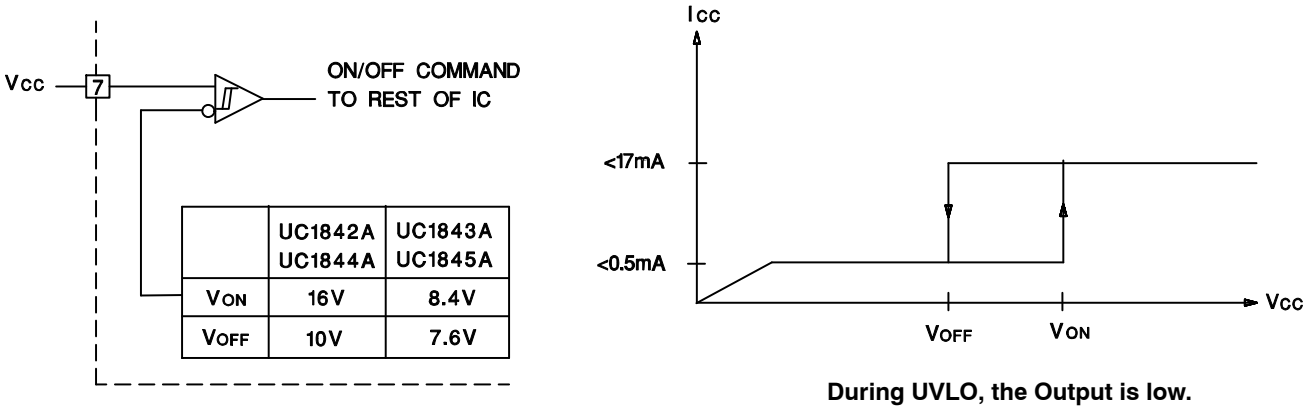
PARAMETER MEASUREMENT INFORMATION



Error Amp can source and sink up to 0.5 mA and sink up to 2 mA.

Figure 1. Error Amp Configuration

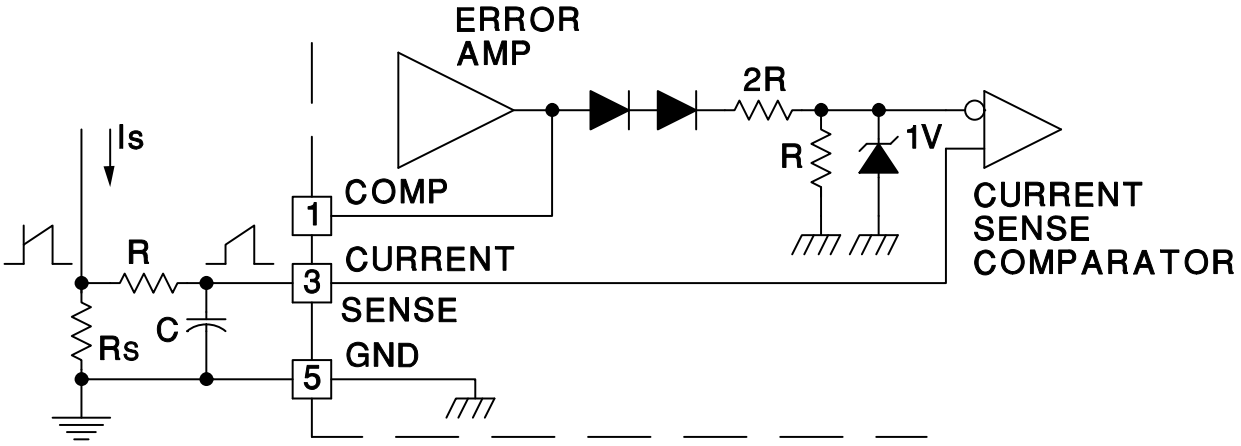
PARAMETER MEASUREMENT INFORMATION



	UC1842A UC1844A	UC1843A UC1845A
VON	16V	8.4V
VOFF	10V	7.6V

During UVLO, the Output is low.

Figure 2. Under Voltage Lockout



Peak Current (Is) is determined by the following formula:

$$Ismax' \frac{1V}{RS}$$

A small RC filter may be required to suppress switch transients.

Figure 3. Current Sense Circuit

PARAMETER MEASUREMENT INFORMATION

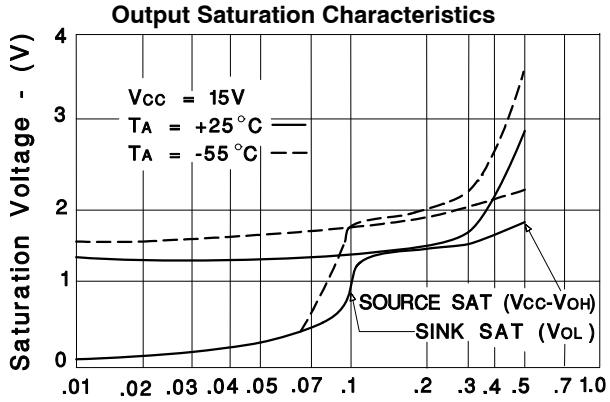


Figure 4

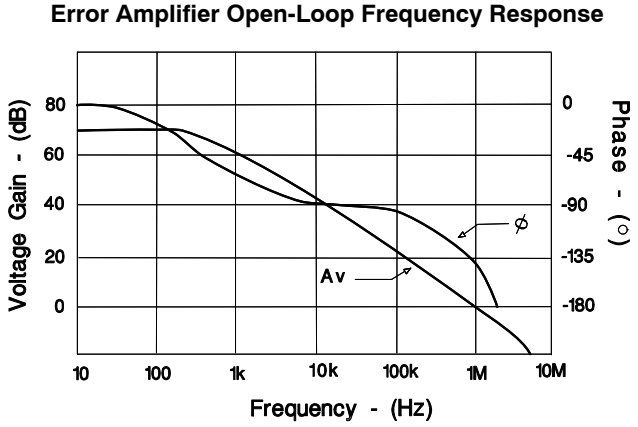
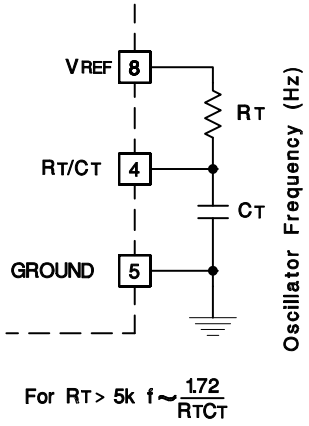
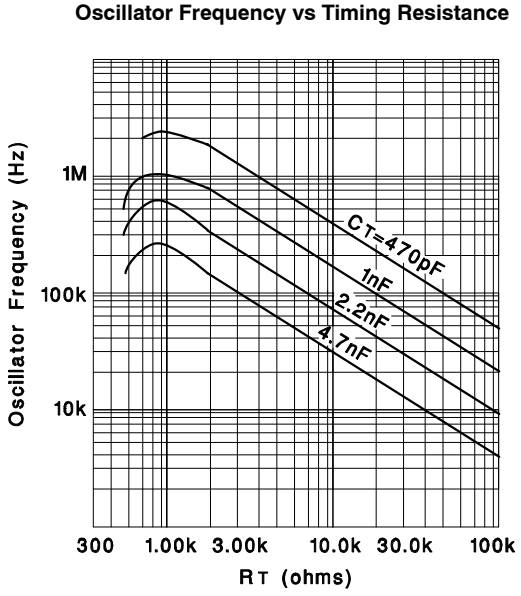


Figure 5

APPLICATION INFORMATION





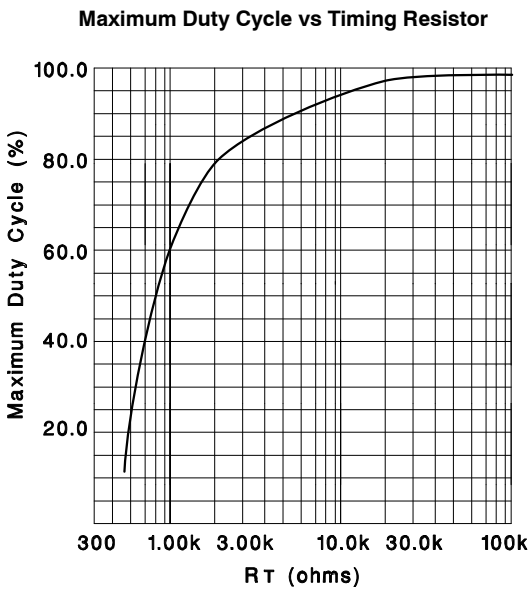
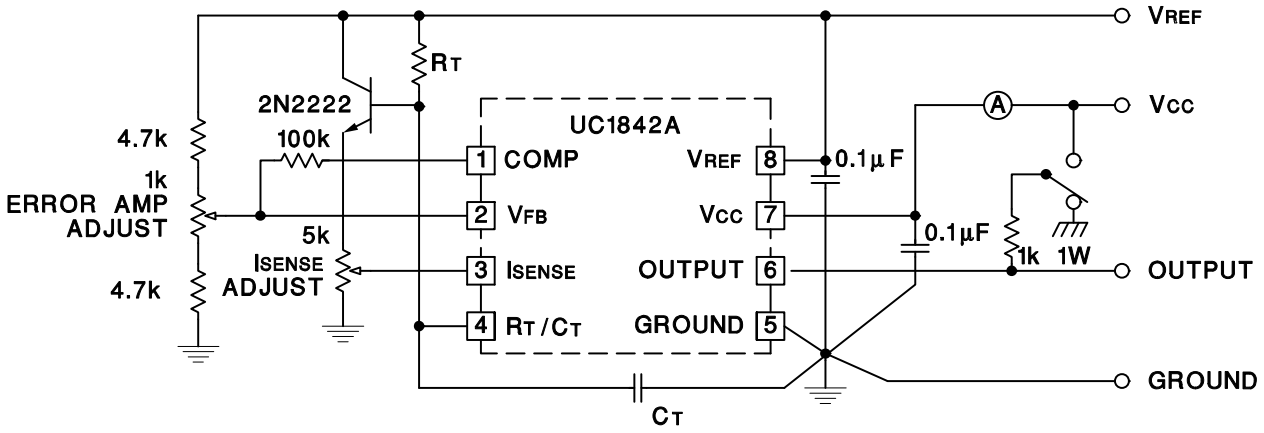


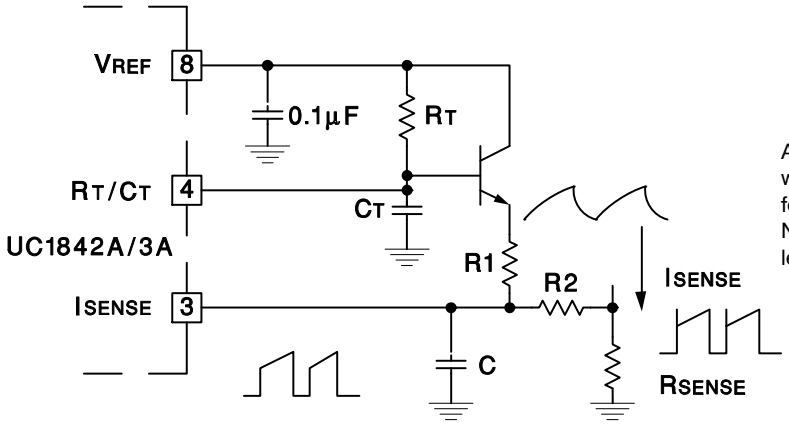
Figure 6. Oscillator

APPLICATION INFORMATION



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

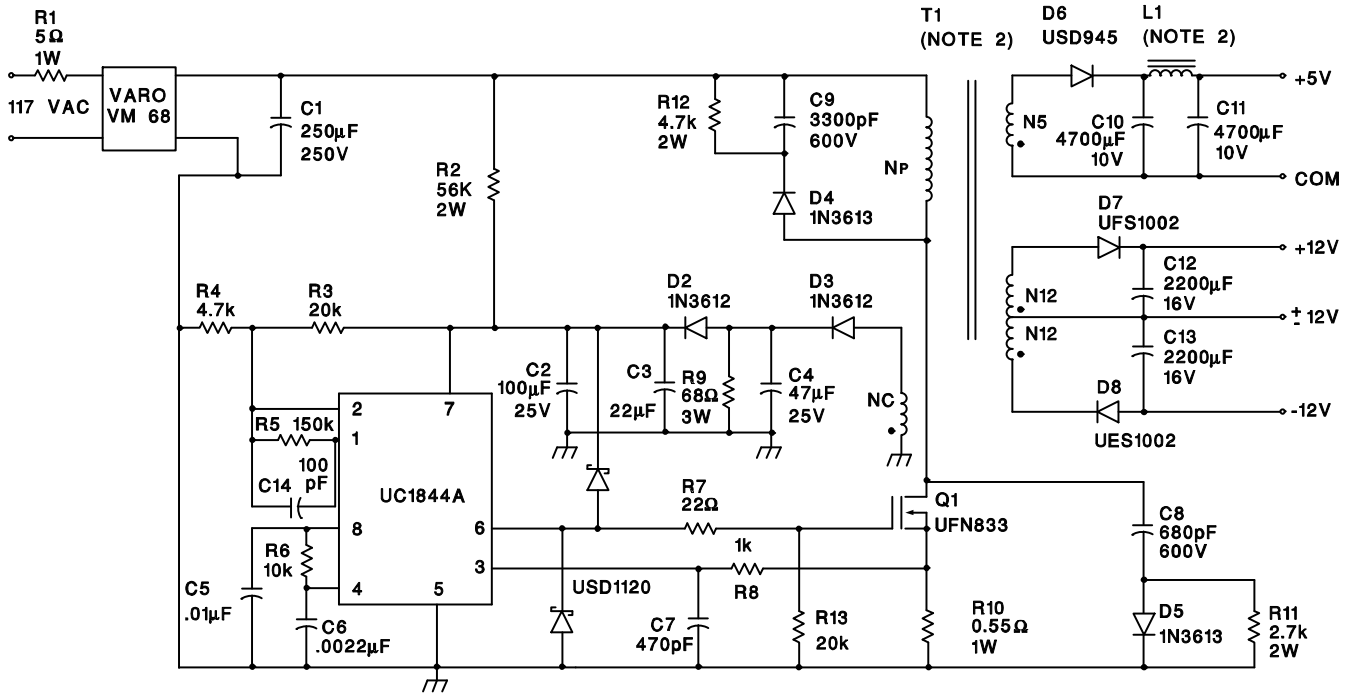
Figure 7. Open-Loop Laboratory Text Fixture



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.
Note that capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

Figure 8. Slope Compression

APPLICATION INFORMATION



Power Supply Specifications

1. Input Voltage 95VAC to 130VAC (50 Hz/60 Hz)
2. Line Isolation 3750 V
3. Switching Frequency 40 kHz
4. Efficiency, Full Load 70%
5. Output Voltage:
   A. +5V, ±5%; 1A to 4A Load
   B. +12V, ±3%; 0.1A to 0.3A Load Ripple voltage: 100 mV P-P Max
   C. −12V, ±3%; 0.1A to 0.3A Load Ripple voltage: 100 mV P-P Max

Figure 9. Off-Line Flyback Regulator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC1842AMDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1842AME	Samples
UC1843AMDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1843AME	Samples
UC1844AMDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1844AME	Samples
UC1845AMDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	(1845AE, 1845AME)	Samples
UC1845AMDREPG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	(1845AE, 1845AME)	Samples
V62/03625-01YE	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1842AME	Samples
V62/03625-02YE	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1843AME	Samples
V62/03625-03YE	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1844AME	Samples
V62/03625-04YE	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	(1845AE, 1845AME)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

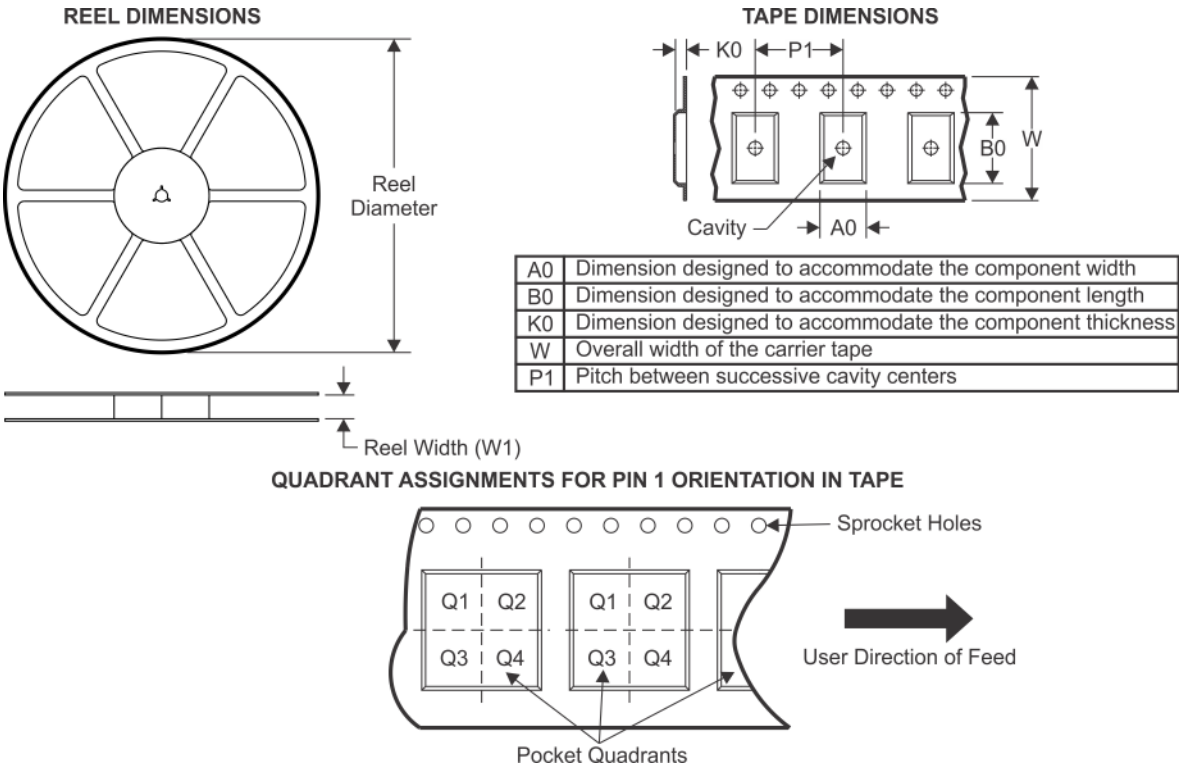
OTHER QUALIFIED VERSIONS OF UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP :

- Catalog: UC1842A, UC1843A, UC1844A, UC1845A
- Space: UC1842A-SP, UC1843A-SP, UC1844A-SP, UC1845A-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

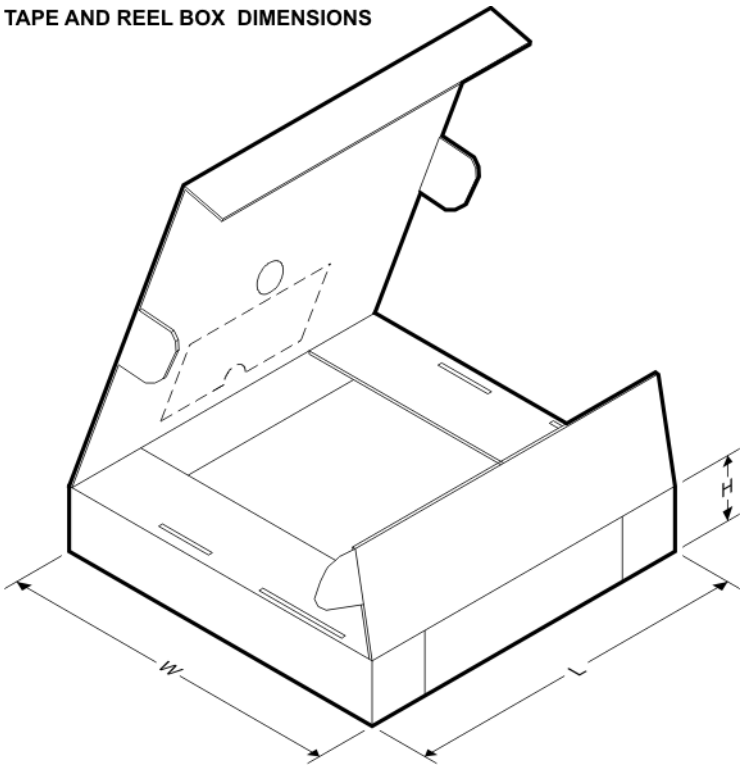


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

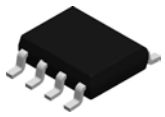
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC1842AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC1843AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC1844AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC1845AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC1842AMDREP	SOIC	D	8	2500	350.0	350.0	43.0
UC1843AMDREP	SOIC	D	8	2500	350.0	350.0	43.0
UC1844AMDREP	SOIC	D	8	2500	350.0	350.0	43.0
UC1845AMDREP	SOIC	D	8	2500	350.0	350.0	43.0

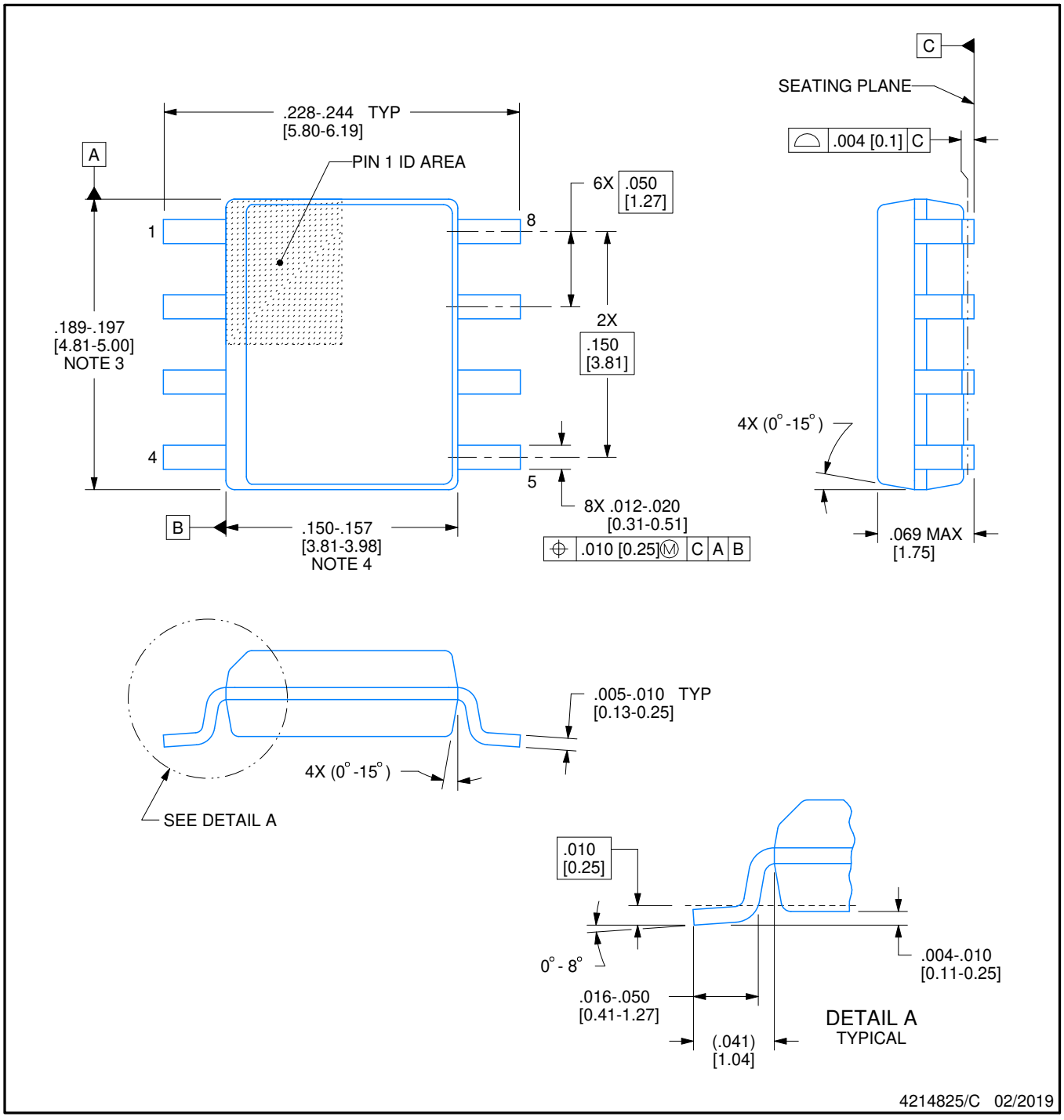


PACKAGE OUTLINE

D0008A

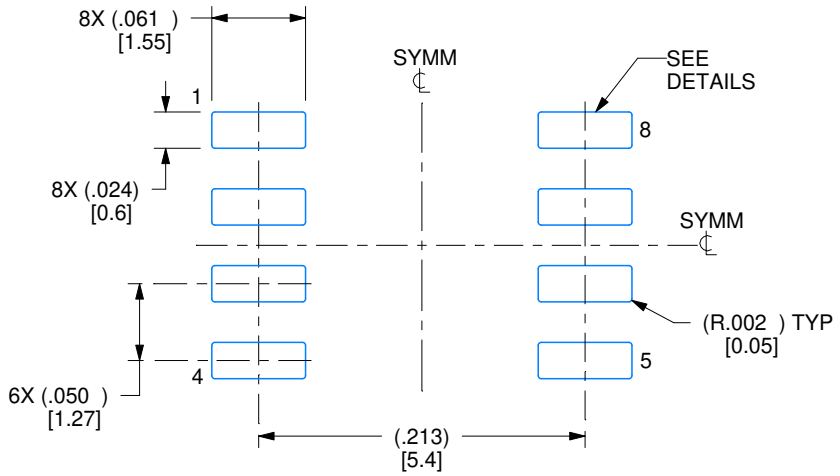
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

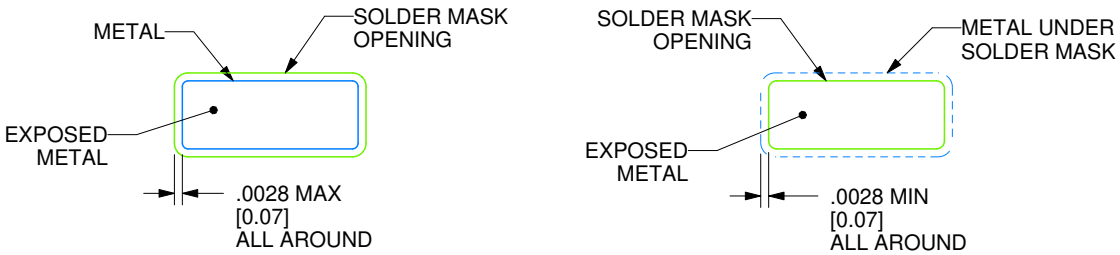


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

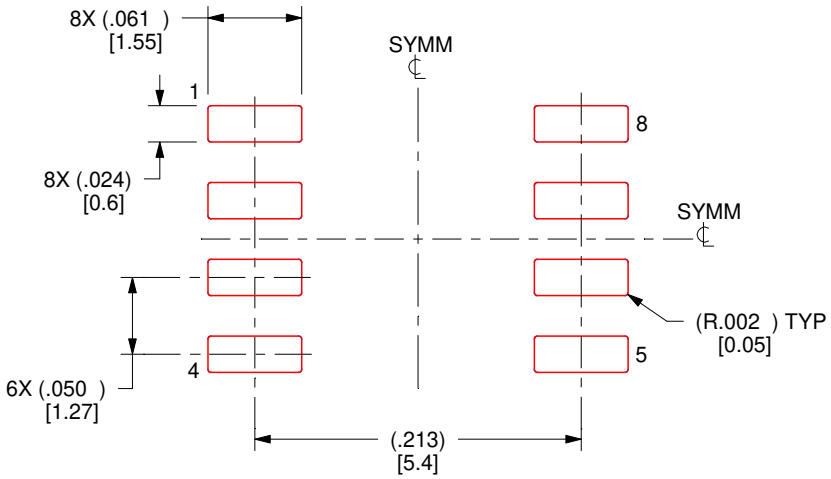
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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