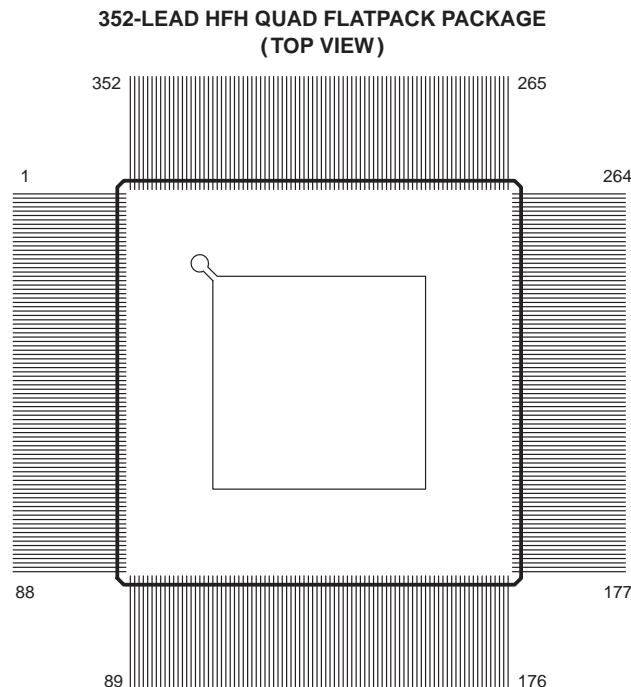


- **Performance**
  - 40 MFLOPS (Million Floating-Point Operations per Second) With 256-Megabyte/s Burst I/O Rate for 40-MHz Modules
  - 128K Word × 32 Bit Zero-Wait-State SRAM Connected to the 'C40 Local Bus
- **Compliant to MIL-PRF-38535 QML**
- **'C40 Performance With Local Memory Requiring Only 4.35 Square Inches of Board Space**
- **Enhanced Performance Offered By Multichip-Module Solution**
  - 46% Reduction In Number of Interconnects
  - 23% Reduction (Minimum) in Board Area
  - Estimated 20% Reduction in Power Dissipation Due to Reduced Parasitic Capacitance and Interconnect Lengths
- **Two Memory Ports for High Data Bandwidth**
  - Full 2-Gigaword External Bus
  - Internal Bus Mapped to 128K Word × 32 Bit Zero-Wait-State SRAM
- **Six External Communication Ports for Direct Processor-to-Processor Communication**
- **Supports IEEE-1149.1†-Compliant (JTAG) With Boundary-Scan Testing**
- **Operating Free-Air Temperature Ranges:**
  - Military: –55°C to 125°C
  - Commercial: 0°C to 70°C
- **Packaging:**  
352-Lead Ceramic Quad Flatpack (HFH Suffix)



ADVANCE INFORMATION

## description

The 'MCM41 single-SMJ320C40 multichip module‡ (MCM) contains one SMJ320C40 device with 128K word × 32 bit zero-wait-state SRAM mapped to the local memory bus. The MCM is footprint-compatible with the monolithic '320C40HFH package to allow easy upgradeability and design-in. The local memory bus is not routed to the device footprint. The 'MCM41 is available in both a commercial temperature range (0°C to 70°C) and a military temperature range (–55°C to 125°C) option.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

†IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port and Boundary-Scan Architecture

‡The 'MCM41 single-SMJ320C40 multichip module will be referred to as 'MCM41 throughout this data sheet.

# SMJ320MCM41D SINGLE-SMJ320C40 MULTICHIP MODULE

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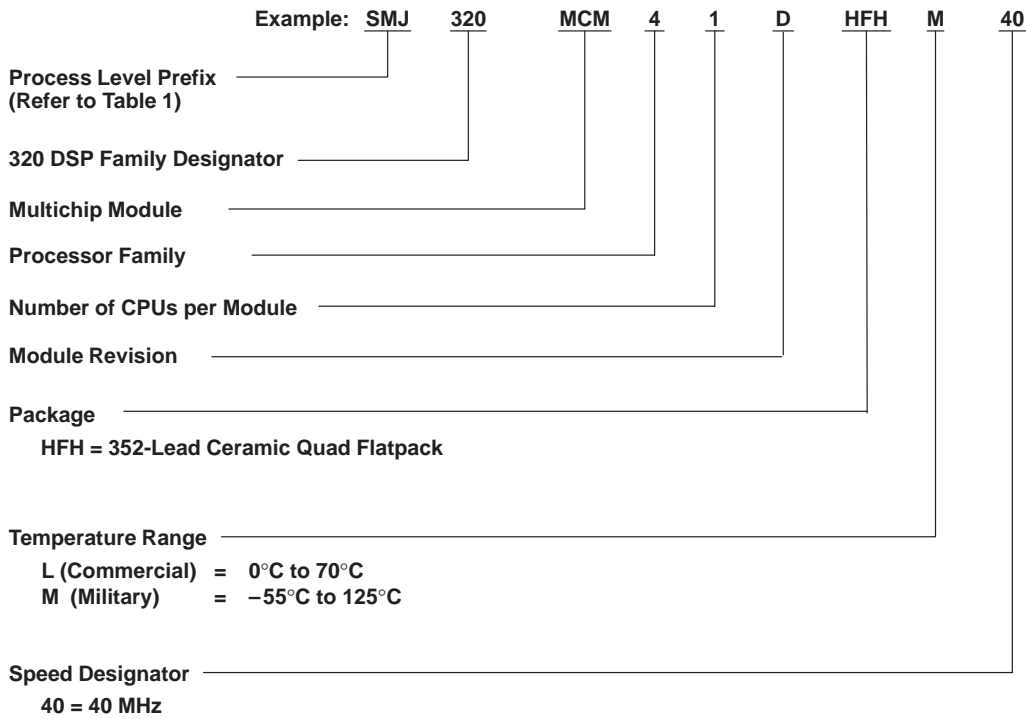
**Table 1. MCM Processing Matrix**

PROCESS LEVEL	TEMPERATURE RANGE		DIE	100% PROCESSED	SPEED TEST	TEST TEMPERATURE RANGE	QUALIFICATION TESTING
SM	L version	0°C to 70°C	Probed	No	No	25°C to 70°C	Package
	M version	-55°C to 125°C	Probed	No	Yes	-55°C to 125°C	Package
SMJ†	M version	-55°C to 125°C	KGD‡	Yes	Yes	-55°C to 125°C	MIL-H-38534

† SMJ-level product is fully MIL-PRF-38535 QML compliant.

‡ KGD stands for the known-good-die strategy as defined in the reference documentation and data sheet scope section.

## Multichip Module Naming Nomenclature and Ordering Information



For descriptions of the HFH package pin assignments, refer to the SMJ320C40 signals descriptions table in the SMJ320C40 data sheet (literature number SGUS017).

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**HFH package pin assignments — numerical listing**

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
01	D31	41	D0	81	CSTRB5	121	DVDD <sup>‡</sup>	161	C1D7
02	D30	42	CE1	82	CACK5	122	IVSS <sup>†</sup>	162	C1D6
03	D29	43	RDY1	83	CREQ5	123	IVSS <sup>†</sup>	163	C1D5
04	D28	44	DVSS <sup>§</sup>	84	CRDY4	124	C2D7	164	C1D4
05	D27	45	DVSS <sup>§</sup>	85	CSTRB4	125	C2D6	165	C1D3
06	D26	46	CVSS <sup>†</sup>	86	CACK4	126	C2D5	166	C1D2
07	GDDVDD <sup>‡</sup>	47	CVSS <sup>†</sup>	87	CREQ4	127	C2D4	167	C1D1
08	D25	48	LOCK	88	CVSS <sup>†</sup>	128	C2D3	168	C1D0
09	D24	49	VDDL <sup>¶</sup>	89	DVSS <sup>§</sup>	129	C2D2	169	DVDD <sup>‡</sup>
10	D23	50	VSSL <sup>#</sup>	90	DVSS <sup>§</sup>	130	C2D1	170	C0D7
11	D22	51	CE0	91	DVDD <sup>‡</sup>	131	C2D0	171	C0D6
12	D21	52	RDY0	92	C5D7	132	CVSS <sup>†</sup>	172	C0D5
13	D20	53	DE	93	C5D6	133	DVSS <sup>§</sup>	173	C0D4
14	D19	54	TCK	94	C5D5	134	DVSS <sup>§</sup>	174	C0D3
15	D18	55	TDO	95	C5D4	135	DVDD <sup>‡</sup>	175	C0D2
16	D17	56	TDI	96	C5D3	136	CRDY3	176	C0D1
17	D16	57	TMS	97	C5D2	137	CSTRB3	177	C0D0
18	CVSS <sup>†</sup>	58	TRST	98	C5D1	138	CACK3	178	CVSS <sup>†</sup>
19	CVSS <sup>†</sup>	59	EMU0	99	C5D0	139	CREQ3	179	DVDD <sup>‡</sup>
20	IVSS <sup>†</sup>	60	EMU1	100	DVDD <sup>‡</sup>	140	VDDL <sup>¶</sup>	180	ROMEN
21	GDDVDD <sup>‡</sup>	61	DVSS <sup>§</sup>	101	C4D7	141	VSSL <sup>#</sup>	181	IIOF0
22	GDDVDD <sup>‡</sup>	62	DVSS <sup>§</sup>	102	C4D6	142	CRDY2	182	DVSS <sup>§</sup>
23	DVSS <sup>§</sup>	63	DVDD <sup>‡</sup>	103	C4D5	143	CSTRB2	183	DVSS <sup>§</sup>
24	DVSS <sup>§</sup>	64	PAGE1	104	C4D4	144	CACK2	184	IIOF1
25	D15	65	R/W1	105	C4D3	145	CREQ2	185	IIOF2
26	D14	66	STRB1	106	C4D2	146	DVDD <sup>‡</sup>	186	IIOF3
27	D13	67	STAT0	107	C4D1	147	CRDY1	187	NMI
28	D12	68	STAT1	108	C4D0	148	CSTRB1	188	NC
29	D11	69	IVSS <sup>†</sup>	109	CVSS <sup>†</sup>	149	CACK1	189	NC
30	D10	70	STAT2	110	DVSS <sup>§</sup>	150	CREQ1	190	NC
31	D9	71	STAT3	111	DVSS <sup>§</sup>	151	CRDY0	191	NC
32	D8	72	PAGE0	112	DVDD <sup>‡</sup>	152	CSTRB0	192	NC
33	D7	73	R/W0	113	C3D7	153	CACK0	193	NC
34	D6	74	STRB0	114	C3D6	154	CREQ0	194	NC
35	D5	75	AE	115	C3D5	155	CVSS <sup>†</sup>	195	DVDD <sup>‡</sup>
36	GDDVDD <sup>‡</sup>	76	RESETLOC1	116	C3D4	156	CVSS <sup>†</sup>	196	CVSS <sup>†</sup>
37	D4	77	DVDD <sup>‡</sup>	117	C3D3	157	DVSS <sup>§</sup>	197	NC
38	D3	78	RESETLOC0	118	C3D2	158	DVSS <sup>§</sup>	198	NC
39	D2	79	RESET	119	C3D1	159	IVSS <sup>†</sup>	199	NC
40	D1	80	CRDY5	120	C3D0	160	DVDD <sup>‡</sup>	200	NC

† CVSS and IVSS pins are connected internally.

‡ DVDD, LADVDD, LDDVDD, GDDVDD, and GADVDD pins are connected internally.

§ DVSS pins are connected internally.

¶ VDDL pins are connected internally.

# VSSL pins are connected internally.

|| Pins marked NC should be left electrically unconnected.

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# SMJ320MCM41D SINGLE-SMJ320C40 MULTICHIP MODULE

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## HFH package pin assignments — numerical listing (continued)

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
201	TCLK0	241	CV <sub>SS</sub> <sup>†</sup>	281	LDDV <sub>DD</sub> <sup>‡</sup>	321	A20
202	TCLK1	242	DV <sub>SS</sub> <sup>§</sup>	282	CV <sub>SS</sub> <sup>†</sup>	322	A19
203	H3	243	DV <sub>SS</sub> <sup>§</sup>	283	DV <sub>SS</sub> <sup>§</sup>	323	A18
204	H1	244	NC	284	DV <sub>SS</sub> <sup>§</sup>	324	A17
205	NC	245	NC	285	IV <sub>SS</sub> <sup>†</sup>	325	GADV <sub>DD</sub> <sup>‡</sup>
206	IV <sub>SS</sub> <sup>†</sup>	246	NC	286	NC	326	GADV <sub>DD</sub> <sup>‡</sup>
207	NC	247	NC	287	NC	327	CV <sub>SS</sub> <sup>†</sup>
208	NC	248	NC	288	NC	328	CV <sub>SS</sub> <sup>†</sup>
209	NC	249	NC	289	NC	329	DV <sub>SS</sub> <sup>§</sup>
210	NC	250	NC	290	NC	330	DV <sub>SS</sub> <sup>§</sup>
211	NC	251	NC	291	NC	331	A16
212	$\overline{\text{IACK}}$	252	NC	292	NC	332	A15
213	V <sub>DDL</sub> <sup>¶</sup>	253	NC	293	NC	333	A14
214	V <sub>SSL</sub> <sup>#</sup>	254	NC	294	NC	334	A13
215	X1	255	NC	295	NC	335	A12
216	X2/CLKIN	256	LADV <sub>DD</sub> <sup>‡</sup>	296	NC	336	A11
217	CV <sub>SS</sub> <sup>†</sup>	257	NC	297	NC	337	A10
218	CV <sub>SS</sub> <sup>†</sup>	258	NC	298	LDDV <sub>DD</sub> <sup>‡</sup>	338	A9
219	DV <sub>DD</sub> <sup>‡</sup>	259	NC	299	NC	339	A8
220	DV <sub>SS</sub> <sup>§</sup>	260	NC	300	NC	340	A7
221	DV <sub>SS</sub> <sup>§</sup>	261	DV <sub>SS</sub> <sup>§</sup>	301	NC	341	A6
222	NC	262	DV <sub>SS</sub> <sup>§</sup>	302	NC	342	A5
223	NC	263	CV <sub>SS</sub> <sup>†</sup>	303	NC	343	A4
224	NC	264	NC	304	V <sub>DDL</sub> <sup>¶</sup>	344	GADV <sub>DD</sub> <sup>‡</sup>
225	NC	265	NC	305	V <sub>SSL</sub> <sup>#</sup>	345	A3
226	LADV <sub>DD</sub> <sup>‡</sup>	266	NC	306	CV <sub>SS</sub> <sup>†</sup>	346	A2
227	NC	267	NC	307	CV <sub>SS</sub> <sup>†</sup>	347	A1
228	NC	268	LDDV <sub>DD</sub> <sup>‡</sup>	308	DV <sub>SS</sub> <sup>§</sup>	348	A0
229	NC	269	NC	309	DV <sub>SS</sub> <sup>§</sup>	349	CV <sub>SS</sub> <sup>†</sup>
230	NC	270	NC	310	A30	350	DV <sub>SS</sub> <sup>§</sup>
231	NC	271	NC	311	A29	351	DV <sub>SS</sub> <sup>§</sup>
232	NC	272	NC	312	A28	352	SUBS
233	NC	273	NC	313	GADV <sub>DD</sub> <sup>‡</sup>		
234	NC	274	NC	314	A27		
235	NC	275	NC	315	A26		
236	NC	276	NC	316	A25		
237	NC	277	NC	317	A24		
238	LADV <sub>DD</sub> <sup>‡</sup>	278	NC	318	A23		
239	LADV <sub>DD</sub> <sup>‡</sup>	279	NC	319	A22		
240	CV <sub>SS</sub> <sup>†</sup>	280	LDDV <sub>DD</sub> <sup>‡</sup>	320	A21		

† CV<sub>SS</sub> and IV<sub>SS</sub> pins are connected internally.

‡ DV<sub>DD</sub>, LADV<sub>DD</sub>, LDDV<sub>DD</sub>, GADV<sub>DD</sub>, and GADV<sub>DD</sub> pins are connected internally.

§ DV<sub>SS</sub> pins are connected internally.

¶ V<sub>DDL</sub> pins are connected internally.

# V<sub>SSL</sub> pins are connected internally.

|| Pins marked NC should be left electrically unconnected.

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### functional block diagram

The following pins have 10-k $\Omega$  pullup resistors added within the module:

- $\overline{\text{CREQ}}_x$ ,  $\overline{\text{CACK}}_x$ ,  $\overline{\text{CSTRB}}_x$ ,  $\overline{\text{CRDY}}_x$ , where  $x = 0-5$
- $\overline{\text{LCE}}_1$  (internal connections)

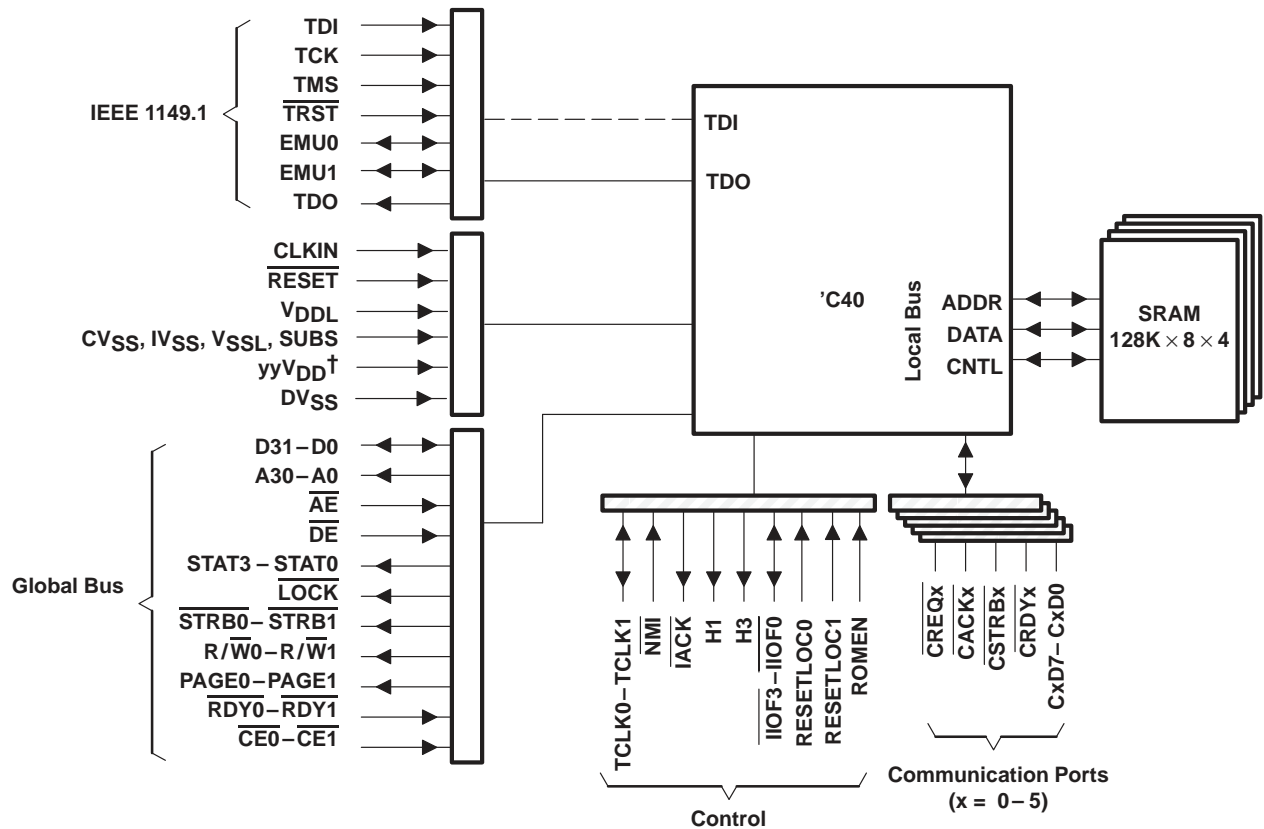
A total of eight decoupling capacitors have been connected within the module.

Between clean power and ground ( $V_{\text{DDL}}$  and  $CV_{\text{SS}}$ ), the following capacitors have been connected:

- One 0.1- $\mu\text{F}$  capacitor
- One 0.01- $\mu\text{F}$  capacitor

Between dirty power and ground ( $GDDV_{\text{DD}}$ ,  $GADV_{\text{DD}}$ ,  $LDDV_{\text{DD}}$ ,  $LADV_{\text{DD}}$ , and  $DV_{\text{SS}}$ ), the following capacitors have been connected:

- Three 0.1- $\mu\text{F}$  capacitors
- Three 0.01- $\mu\text{F}$  capacitors



†  $yyV_{\text{DD}}$  represents  $GDDV_{\text{DD}}$ ,  $GADV_{\text{DD}}$ ,  $LDDV_{\text{DD}}$ , and  $LADV_{\text{DD}}$ .

### operational overview

Treatment of the detailed operation of the 'C40 device is beyond the scope of this document. Refer to the *TMS320C4x User's Guide* (literature number SPRU063) for a detailed description of this DSP.

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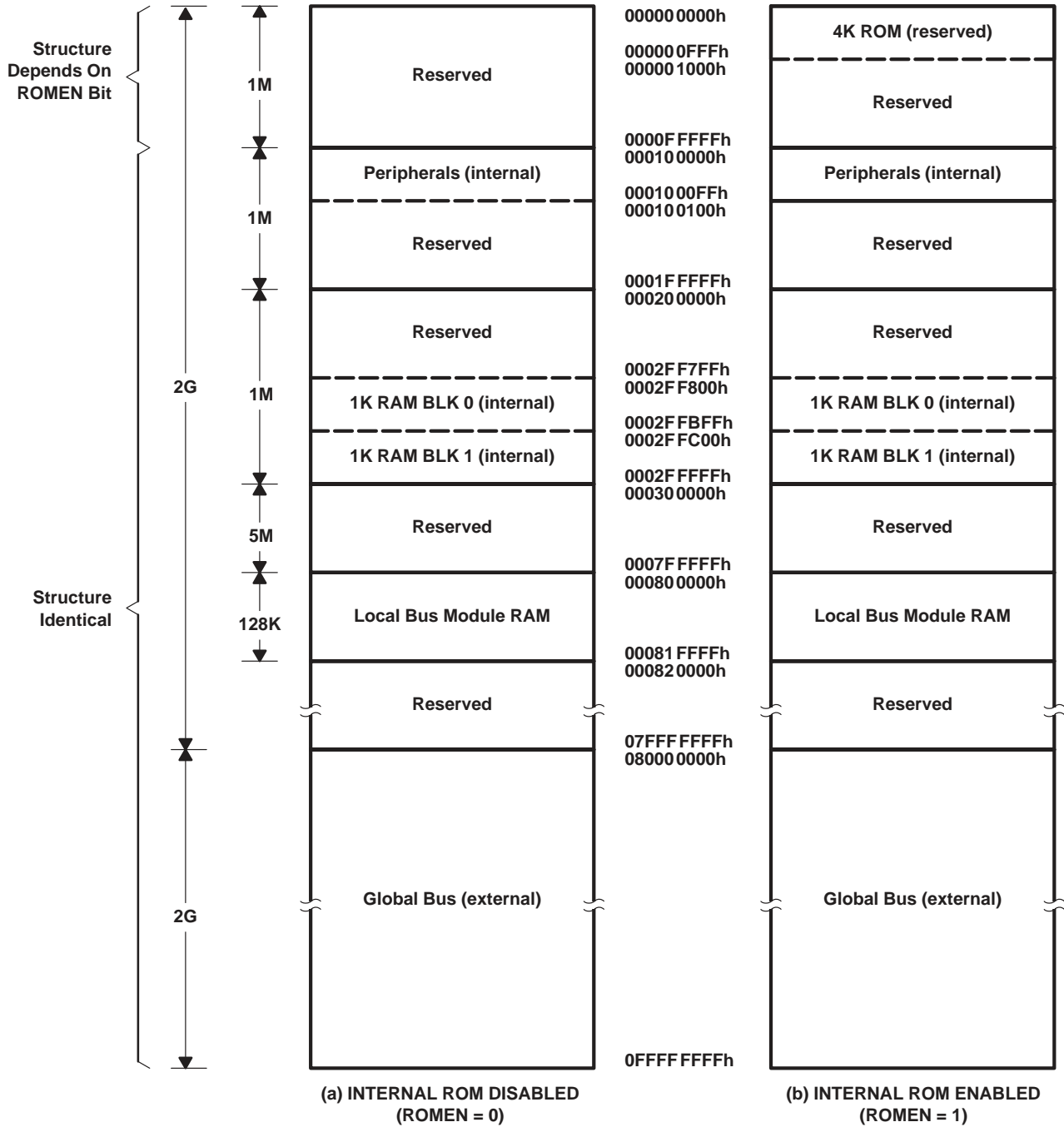


Figure 1. Memory Map for the 'C40 Within the Multichip Module

## reference documentation and data sheet scope

The SMJ320MCM41D is qualified to MIL-PRF-38535. Electrical continuity of the module is ensured through use of IEEE-1149.1-compatible boundary-scan testing and functional checkout of local SRAM space.

KGD refers to Texas Instruments (TI™) known-good-die strategy. TI KGDs are fully tested over the military temperature range per MIL-PRF-38535 QML. Electrical testing ensures compliance of the 'C40 KGD components to the SMJ320C40 data sheet (literature number SGUS017) over the operating temperature range. The SMJ320MCM41D module timings are virtually unchanged from the SMJ320C40 data sheet timings. A SMJ320C40 data sheet is provided for customer reference only and does not imply MCM compliance to published timings.

For a complete description of the 'C40 operation and application information, refer to the *TMS320C4x User's Guide* (literature number SPRU063).

## capacitance

Capacitance of a single 'C40 die is specified by design to be 15 pF maximum for both inputs and outputs. Module networks add up to 25 pF. Simulation of die or substrate capacitance is performed after any design change. Power measurements taken for the 'C40 die are made with an additional 80-pF load capacitance. Refer to the SMJ320C40 data sheet (literature number SGUS017) for the test load circuit.

## operational timings and module testing

TI processing ensures that operation is verified to the published data sheet specifications on the 'C40 in die form. All voltage, timing, speed, and temperature specifications are met before any die is placed into a multichip module. For this reason, it is unnecessary to verify all 'C40 voltage and timing parameters at the module level.

Characterization of the 'MCM41D substrate shows that the module performs as an equivalent system of discretely packaged 'C40 devices. This performance is ensured through a full-frequency functional checkout of the module that verifies selected worst-case timings. An additional propagation delay is introduced by the substrate. This value is assured by design to be less than 1 ns, but it is not tested. Refer to the SMJ320C40 data sheet (literature number SGUS017) for a complete listing of timing diagrams and limits.

## module test capability (future compatibility)

The 'C40 supports the IEEE-1149.1 testability standard, and all test-access port (TAP) pins are brought out to the module footprint. This configuration allows users to test the module using third-party JTAG testability tools or other boundary-scan control software. Proper software configuration allows users to debug or launch code on the module via the 'C40 emulator and XDS™ pod. Both of these tools are used as a part of outgoing module testing.

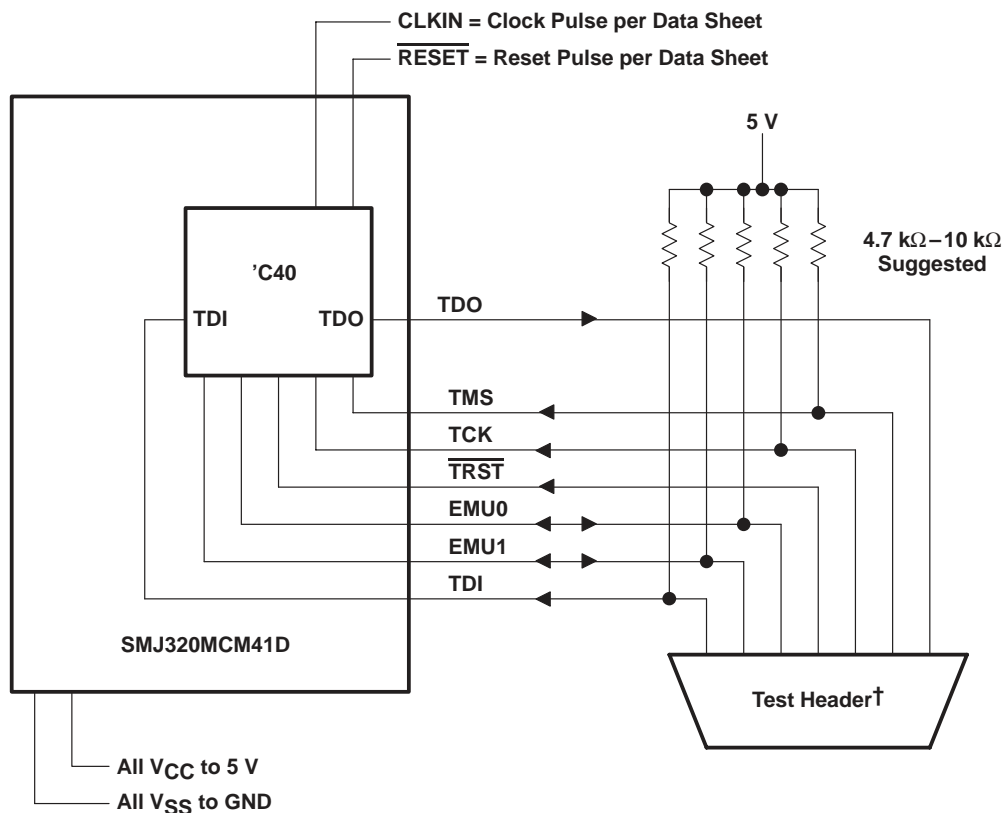
The 'MCM41 supports third-party JTAG diagnostic families of products for verification and debug of boundary-scan circuits, boards, and systems. For further information on JTAG testability tools, please contact your local TI sales representative or authorized TI distributor.





module test circuit

Figure 2 illustrates the basic circuits for the 'MCM41D. Refer to the *TMS320C4x User's Guide* (literature number SPRU063) for more detailed information.



† The test header normally consists of the XDS510™ for the 'C40 emulation or ASSET hardware for interconnect testing.

Figure 2. Sample Test Circuit

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XDS510 is a trademark of Texas Instruments Incorporated.

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## thermal analysis

Thermal conduction of components in the SMJ320MCM41D is dependent on the thermal resistance of the material under each die as well as the die area thermally connected to the heat-dissipating medium. Since these properties vary with layout and die size, 'C40 and SRAM components should be considered separately. The following table lists primary parameters required for thermal analysis of the module. The junction temperature,  $T_J$ , is not to be exceeded for the 'C40 or the SRAM die.

### primary parameters required for thermal analysis of the SMJ320MCM41D module

PARAMETER	ALTERNATE SYMBOL	MIN	TYP	MAX	UNIT
$T_J$ Junction temperature under operating condition	$T_J$			150	°C
PMCM Single MCM power dissipation	PMCM		2.0	5.2	W
$Z_{0JC}$ Thermal impedance (junction-to-case) of package	$T_{jc}$		1.3		°C/W
$Z_{0JA}$ Thermal impedance (junction-to-ambient air, 0 cfm) of package	$T_{ja}$		28.0		°C/W
TSOL Maximum solder temperature (10 s duration)	TSOL			260	°C

## power estimation

The power requirements of the '320MCM41 have been characterized over the operating temperature range. See the application report *Calculation of TMS320C40 Power Dissipation* (literature number SPRA032) as reference for power estimation of the 'C40 components.

Typical power dissipation has been measured with the 'C40s executing a 64-point Fast Fourier Transform (FFT) algorithm. Input and output data arrays resided in module SRAM, and output data was written out to the global-address space. The global databus was loaded with 80-pF test loads, and both local and global writes were configured for zero-wait-state memory. Under typical conditions of 25°C, 5-V  $V_{CC}$ , and 40-MHz CLKIN frequency, the power dissipation was measured to be 1.75 W.

Maximum power dissipation has been measured under worst-case conditions. The global databus was loaded with 80-pF test loads, and simultaneous zero-wait-state writes have been performed to both local and global buses. Under worst-case conditions of -55°C, 5.25-V  $V_{CC}$ , and 40-MHz CLKIN frequency, the power dissipation was determined to be 3 W. The algorithm executed during these tests consists of parallel writes of alternating 0xAAs and 0x55s to both local SRAM and global-address spaces. This algorithm is not considered to be a practical use of the 'C40's resources; therefore, the associated power measurement should be considered absolute maximum only.

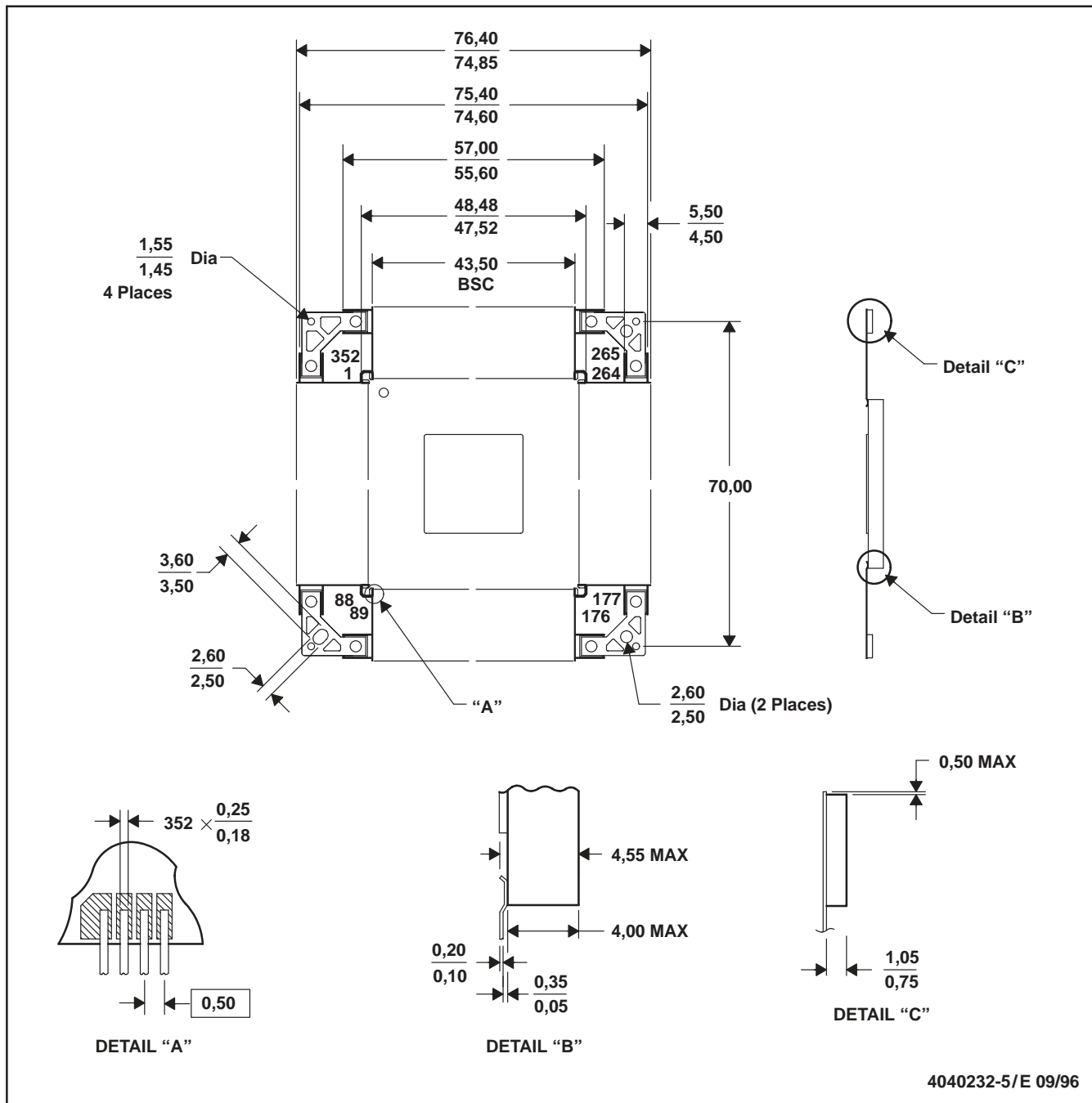
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MECHANICAL DATA

HFH (S-CQFP-F352)

CERAMIC QUAD FLATPACK WITH NCTB



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- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a metal lid.  
 D. The terminals are gold plated.  
 E. Falls within JEDEC MO-134 AE

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