

3.0V, SOTinyTM Single-Supply 0.4 Ω SPST (NO) CMOS Analog Switch

Features

• Low On-Resistance: 0.4Ω Max (+2.7V Supply)

• 0.1Ω Max. On-Resistance Flatness at +25°C

• Fast Switching: 10ns Max.

• +1.5V to +3.6V Single-Supply Operation

• TTL/CMOS-Logic Compatible

• -25dB Off-Isolation at 100kHz

• 1nA Max. Off-Leakage at +25°C

• Packaging (Pb-free & Green available):

- 5-pin Small Compact SOT23 (T)

Applications

- · Cellular Phones
- Communications Circuits
- · Battery-Operated Equipment
- · DSL Modems
- · Audio and Video Signal Routing
- · PCMCIA Cards

Description

PI3A4626 is a single-pole/single-throw (SPST) normally open (NO) analog switch that operates from a single +1.5V to +3.6V supply.

The switch has 0.4Ω Max On-Resistance (R_{ON}), with 0.1Ω Max R_{ON} flatness over the analog signal range when powered from a +3.0V supply. Leakage currents are less than 2nA and fast switching times are less than 10ns.

To minimize PC board area use, the device is available in a small compact SOT23 package.

Pin Description

SOT23	Name	Function	
1	COM	Analog Switch, Common	
2	NO	Analog Switch, Normally Open	
3	GND	Ground	
4	IN	Digital Control Input	
5	V_{DD}	Positive Supply Voltage	
-	N.C.	No Internal Connection	

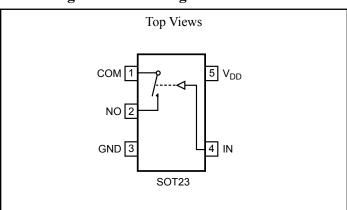
Note:

 NO and COM pins are identical and interchangeable. Any pin may be considered as an input or an output; signals pass.

Truth Table

Input	Switch State
LOW	OFF
HIGH	ON

Block Diagrams/Pin Configurations





Absolute Maximum Ratings

Voltages Referenced to GND	
V _{DD}	0.5V to +3.6V
$V_{IN}, V_{COM}, V_{NC}, V_{NO}$ $^{(1)}$ or 30mA, whichever occurs first	
Current (any terminal)	±200mA
Peak Current, COM, NO, NC (Pulsed at 1ms 10% duty cycle)	±400mA

Thermal Information

0.5W
.–65°C to +150°C
+300°C

Note:

Caution: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Electrical Specifications - Single +3.3V Supply

 $(V_{DD} = +3.3V \pm 10\%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.5V)$

Description	Parameters	Test Conditions	Package	Temp.(°C)	Min.(1)	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Analog Switch								
Analog Signal Range ⁽³⁾	V _{ANALOG}			Full	0		V _{DD}	V
On Pagistanaa	Day	$V_{DD} = 2.7V,$		25			0.4	
On Resistance	R _{ON}		SOT23	Full			0.5	
On-Resistance Match	I A D			25			0.05	
Between Channels ⁽⁴⁾ ΔR_{ON}	+1.5V		Full			0.06	Ω	
		V _{DD} =2.7V		25			0.1	
On-Resistance Flatness ⁽⁵⁾	R _{FLAT(ON)}	$I_{COM} = 100 \text{mA},$ $V_{NO} \text{ or } V_{NC} = 0.8 \text{V},$ 2.0 V		Full			0.1	
NO or NC Off Leakage	I _{COM(OFF)} or	$V_{DD} = 3.3V$,		25	-1		1	
Current ⁽⁶⁾	I _{NC(OFF)}	$V_{COM} = 0V, V_{NO} \text{ or}$ $V_{NC} = +2.0V$		Full	-20		10	
COM On Leakage Current ⁽⁶⁾		$V_{DD} = 3.3V$,		25	-2		2	nA
	I _{COM(ON)}	$V_{COM} = +2.0V,$ V_{NO} or $V_{NC} = +2.0V$		Full	-20		20	

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^{1.} Signals on NC, NO, COM, or IN exceeding V_{DD} or GND are clamped by internal diodes. Limit forward diode current to 30mA.



Electrical Specifications - Single +3.3V Supply (continued)

 $(V_{DD} = +3.3V \pm 10\%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.5V)$

Description	Parameters	Test Conditions	Temp (°C)	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Logic Input							
Input High Voltage	V _{IH}	Guaranteed logic High Level	Full	1.4			V
Input Low Voltage	$V_{\rm IL}$	Guaranteed logic Low Level				0.5	ľ
Input Current with Voltage High	I _{INH}	$V_{IN} = 1.4V$, all others = $0.5V$		-1		1	
Input Current with Voltage Low	I _{INL}	$V_{IN} = 0.5V$, all other = 1.4V		-1		1	μA
Dynamic	-						
Turn-On Time	t _{ON}	$V_{DD} = 3.3V$, V_{NO} or $V_{NC} = 2.0V$, Figure 1	25			10	
			Full			10	ns
Turn-Off Time	t _{OFF}		25			10	
			Full			10	
Charge Injection ⁽³⁾	Q	$C_L = 1$ nF, $V_{GEN} = 0$ V, $R_{GEN} = 0$ Ω, Figure 2	25		50		pC
Off Isolation ⁽⁷⁾	O _{IRR}	$R_L = 50\Omega$, $f = 100$ kHz, Figure 3			-25		dB
NC or NO Capacitance	C _(OFF)	f = 1 MHz, Figure 4	'		130		
COM Off Capacitance	C _{COM(OFF)}	1 – 1 Minz, rigule 4			130		pF
COM On Capacitance	C _{COM(ON)}	f = 1 MHz, Figure 4			270		
Supply							
Power Supply Range	V_{DD}		Full	1.5		3.6	V
Positve Supply Current	I_{CC}	$V_{DD} = 3.6V, V_{IN} = 0V \text{ or } V_{DD}$				100	nA

Notes:

- 1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
- 2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
- 3. Guaranteed by design.
- 4. $\Delta R_{ON} = R_{ON} Max. R_{ON} Min.$
- 5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
- 6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.
- 7. Off Isolation = $20\log_{10} [V_{COM} / (V_{NO} \text{ or } V_{NC})]$. See Figure 3.

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Electrical Specifications - Single +2.5V Supply

 $(V_{DD} = +2.5V \pm 10\%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.5V)$

Description	Parameters	Test Conditions	Temp.(°C)	Min.(1)	Typ.(2)	Max. ⁽¹⁾	Units
Analog Switch							
Analog Signal Range ⁽³⁾	V _{ANALOG}			0		V_{DD}	V
On-Resistance	R _{ON}	$V_{\rm DD} = 2.5 \text{V}, I_{\rm COM} = -8 \text{mA},$	25			0.4	
On-resistance	KON	V_{NO} or $V_{NC} = 1.8V$	Full			0.4	
On-Resistance Match	$\Delta R_{ m ON}$	l -	25			0.05	$ _{\Omega}$
Between Channels ⁽⁴⁾	ARON		Full			0.06	
On-Resistance Flatness ⁽⁵⁾	Dry ATKOND	V_{NO} or $V_{NC} = 0.8V$, 1.8V	25			0.1	
On-Resistance Matness	R _{FLAT(ON)}		Full			0.1	
Dynamic							
Turn-On Time	4		25			10	
Turn-On Time	t _{ON}	$V_{DD} = 2.5V$	Full			15]
Turn-Off Time	4	V_{NO} or $V_{NC} = 1.8V$, Figure 1	25			10	ns
Turn-On Time	t _{OFF}		Full			10	
Charge Injection ⁽³⁾	Q	$C_L = 1$ nF, $V_{GEN} = 0$ V, $R_{GEN} = 0$ V, Figure 2	25		42		рC
Logic Input							
Input HIGH Voltage	V_{IH}	Guaranteed logic high level	Full	1.4		17	V
Input LOW Voltage	V_{IL}	Guaranteed logic Low level	Full			0.5	<u> </u>
Input HIGH Current	I _{INH}	$V_{IN} = 1.4V$, all others = $0.5V$	Full	-1		1	
Input HIGH Current	I _{INL}	$V_{IN} = 0.5V$, all others = 1.4V	Full	-1		1	μΑ

Notes:

- 1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
- 2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
- 3. Guaranteed by design.
- 4. $\Delta R_{ON} = R_{ON} \text{ max.} R_{ON} \text{ min.}$
- 5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.

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Electrical Specifications - Single +1.8V Supply

 $(V_{DD} = +1.8V \pm 10\%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.5V)$

Description	Parameters	Test Conditions	Temp.(°C)	Min.(1)	Typ.(2)	Max. ⁽¹⁾	Units
Analog Switch							
Analog Signal Range ⁽³⁾	V _{ANALOG}			0		V_{DD}	V
On-Resistance	D	$V_{DD} = 1.8V, I_{COM} = -4mA,$	25			0.4	
On-Resistance	R _{ON}	V_{NO} or $V_{NC} = 1.5V$	Full			0.8	
On-Resistance Match	AD	$V_{DD} = 1.8V, I_{COM} = -4mA,$	25			0.05	
Between Channels ⁽⁴⁾	$\Delta R_{ m ON}$	V_{NO} or $V_{NC} = 0.8V, 1.5V$	Full			0.06	Ω
On-Resistance Flatness ⁽⁵⁾	D		25			0.4	1
On-Resistance Flatness	R _{FLAT(ON)}		Full			0.6	
Dynamic							
T. O. T.	1.		25			15	
Turn-On Time	t _{ON}	$V_{DD} = 1.8V$, V_{NO} or $V_{NC} =$	Full			15	1
Turn-Off Time	1,	1.5V, Figure 1	25			10	ns
	t _{OFF}		Full			15	
Charge Injection ⁽³⁾	Q	$CL = 1nF, V_{GEN} = 0V,$ $R_{GEN} = 0V, Figure 2$	25		29		pC
Logic Input							
Input HIGH Voltage	V _{IH}	Guaranteed logic high level	Full	1.4			* 7
Input LOW Voltage	$V_{\rm IL}$	Guaranteed logic Low level	Full			0.5	V
Input HIGH Current	I _{INH}	$V_{IN} = 1.4V$, all others = 0.5V	Full	-1		1	
Input HIGH Current	I _{INL}	$V_{IN} = 0.5V$, all others = 1.4V	Full	-1		1	μΑ

Notes:

- 1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
- 2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
- 3. Guaranteed by design.
- 4. $\Delta R_{ON} = R_{ON} \text{ max.} R_{ON} \text{ min.}$
- 5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.

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Test Circuits/Timing Diagrams

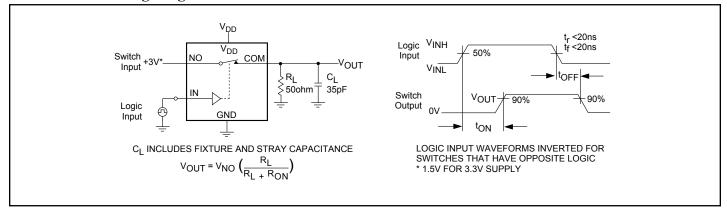


Figure 1. Switching Time

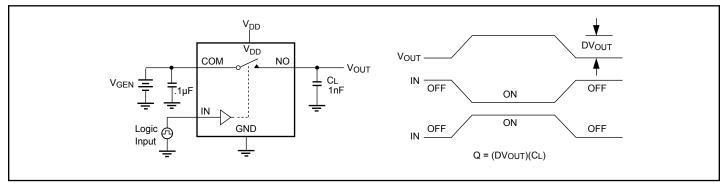


Figure 2. Charge Injection

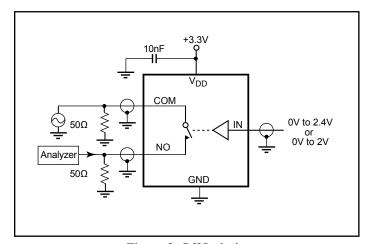


Figure 3. Off Isolation

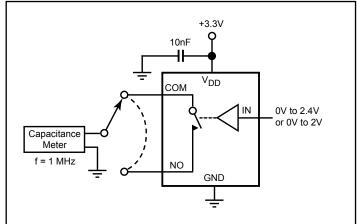
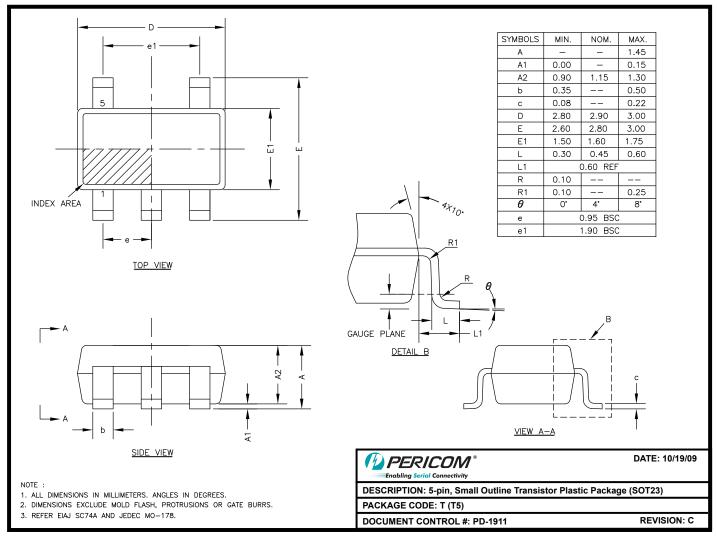


Figure 4. Channel On/Off Capacitance

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Packaging Mechanical: 5-Pin SOT23 (T)



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Note:

• For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Packaging Code	Package Description	Top Mark
PI3A4626TEX	T	Pb-free & Green, 5-pin Small Compact SOT23	ZD

Notes:

- 1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- 2. X = Tape/Reel
- 3. Number of transistors = TBD

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